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(54) Title: MULTI-CHIP PACKAGE WITH HIGH THERMAL CONDUCTIVITY DIE ATTACH

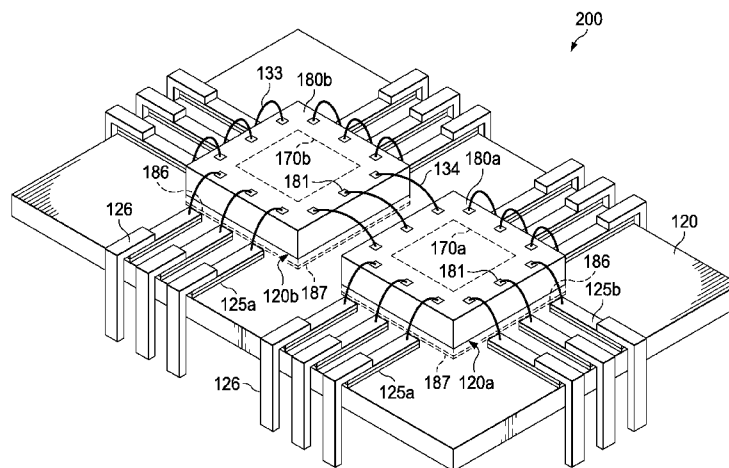


FIG. 2A

(57) Abstract: A packaged semiconductor device (200) includes a metal substrate (120) having a first and second through-hole aperture (120a, 120b) having an outer ring, and metal pads (125b) around the apertures on dielectric pads (125a). A first and second semiconductor die (180a, 180b) have a back side metal (BSM) layer (186) on its bottom side are mounted top side up on a top portion of the apertures. A metal die attach layer (187) is directly between the BSM layer and walls of the metal substrate bounding the apertures to provide a die attachment for the first and the second semiconductor die that fills a bottom portion of the apertures. Leads (126) contact the metal pads, wherein the leads include a distal portion that extends beyond the metal substrate. Bondwires (133) are between the metal pads and bond pads on the first and second semiconductor die, and a mold compound provides encapsulation for the packaged semiconductor device.

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Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

- *with international search report (Art. 21(3))*

MULTI-CHIP PACKAGE WITH HIGH THERMAL CONDUCTIVITY DIE ATTACH

[0001] This Disclosure relates to semiconductor device assembly, more specifically to metal die attachment to a substrate.

BACKGROUND

[0002] Packaged semiconductor devices generally comprise an integrated circuit (IC) die which is conventionally a silicon die that is mounted on a die pad of a workpiece such as a lead frame using a die attach adhesive. Other workpieces include an interposer, printed circuit board (PCB), and another IC die. For IC die assembled top (active) side up and back side down, the die attach adhesive provides a mechanical attachment, and generally also provides an electrical and/or thermal pathway to the die pad. The die attach adhesive generally comprises a polymer such as a polyimide or an epoxy-based adhesive. Silver is often added in particle flake form as a filler to raise both the electrical conductivity and the thermal conductivity of the polymer material.

SUMMARY

[0003] This Summary is provided to introduce a brief selection of disclosed concepts in a simplified form that are further described below in the Detailed Description including the drawings provided. This Summary is not intended to limit the claimed subject matter's scope.

[0004] Disclosed aspects recognize conventional die attach solutions comprising metal particle filled polymers have significant thermal and electrical resistance. Since thermal management is becoming more important with the trend for more compact and more highly integrated electronic systems having smaller features and running at higher operating currents, higher thermal conductivity die attach arrangements are needed that also provide a low electrical resistance when back side electrical contact to the semiconductor die is used. It is recognized that although solder die attach, such as eutectic gold and tin (AuSn), can provide back side electrical contact to the semiconductor die with relatively good thermal and electrical resistance performance as compared to metal particle filled polymers, solder die attach is relatively expensive, and is limited to solderable die surfaces. Moreover, the solder die attach process involves an inert reflow process at temperatures that can cause temperature induced stresses to the semiconductor

die's metal interconnect.

[0005] Disclosed aspects include a packaged semiconductor device including a metal substrate having a first and second through-hole aperture each having an outer ring, and metal pads around the apertures on dielectric pads on the metal substrate. A first and second semiconductor die having a BSM layer on its bottom side are mounted top side up on a top portion of the apertures. A metal die attach layer is between the BSM layer and walls of the metal substrate bounding the apertures to provide a die attachment for the first and the second semiconductor die that fills a bottom portion of the apertures. Leads contact the metal pads, wherein the leads include a distal portion that extends beyond the metal substrate. Bondwires are between the metal pads and bond pads on the first and second semiconductor die, and a mold compound generally provides device encapsulation for the packaged semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Reference will now be made to the accompanying drawings, which are not necessarily drawn to scale, wherein:

[0007] FIGS. 1A-F show components utilized and assembly process progression process for an assembly process for forming a disclosed multi-chip packaged semiconductor device having a first and a second semiconductor die on a metal substrate having raised metal pads comprising metal pads on dielectric pads on the surface of a metal substrate, where each semiconductor die having a BSM layer is directly attached onto the metal substrate by a disclosed electroplated (plated) metal die attach layer, according to an example aspect.

[0008] FIGS. 2A shows an example leaded multi-chip semiconductor device having a first and a second semiconductor die on a metal substrate after singulation then wirebonding bond pads on the respective semiconductor die to raised metal pads that are connected to leads, and bond pads between the respective semiconductor die.

[0009] FIG. 2B shows the leaded multi-chip packaged semiconductor device shown in FIG. 2A after molding to form a mold compound to provide a molded leaded multi-chip packaged semiconductor device.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[00010] Example aspects are described with reference to the drawings, wherein like reference numerals are used to designate similar or equivalent elements. Illustrated ordering of acts or events should not be considered as limiting, as some acts or events may occur in different order

and/or concurrently with other acts or events. Furthermore, some illustrated acts or events may not be required to implement a methodology in accordance with this Disclosure.

[00011] Disclosed aspects include a multi-chip semiconductor package where the die attachment for the first and at least a second semiconductor die is established through a plated metal layer such as comprising copper, Ni, Co, or alloys thereof, as opposed to conventional solder. Therefore, voiding issues for solder die attached processes related to Sn-Cu intermetallic formation are eliminated in disclosed multi-chip packages.

[00012] FIG. 1A shows an example dielectric cover 130 for covering a metal substrate (see the metal substrate 120 in FIG. 1B) for forming a covered substrate stack, where the dielectric cover 130 has a repeating pattern each including a recess pair 130a, 130b comprising a first recess 130a and a second recess 130b. The covered substrate stack is configured for immersing in a plating container described below relative to FIG. 1E shown as 150 that provides an electroplating bath.

[00013] The dielectric cover 130 can comprise a plastic. The first recess 130a is for covering a first semiconductor die and the second recess 130b is for covering a second semiconductor die, that are both shown for example as being rectangular shaped and sized to match the dimensions of the respective semiconductor die to be covered. The recesses 130a, 130b are slightly larger in area as compared to the first and second semiconductor die to enable receiving the respective semiconductor die. Although shown as the same size and shape, the first and the second recesses 130a and 130b can be sized and shaped differently relative to one another to match the respective dimensions of the first and second semiconductor die.

[00014] Alternatively, a UV curable electroplating solution resistant tape can be used as the dielectric cover 130. In the case of a tape instead of the dielectric cover, there will be no need for recesses. A dielectric cover on the top side of the first and second semiconductor die prevents the die from falling off when inside the plating solution.

[00015] FIG. 1B shows an example metal substrate 120 with an inset expanding a portion thereof to show respective components of the raised pads 125 each comprising a metal pad 125b on a dielectric pad 125a (e.g., a polyimide) on the surface of the metal substrate 120. The metal substrate 120 is generally in the form of a substrate sheet/panel having a plurality of dual-die position through-hole apertures comprising a first aperture 120a, and a second aperture 120b configured for a first and a second semiconductor die 180a, 180b shown in FIG. 1C to be positioned top side up within the apertures 120a, 120b. The metal substrate sheet/panel may

have about 50 to 1,000 dual-die positions. The metal substrate 120 is generally about 0.1 mm (3.94 mils) to 0.3 mm (11.81 mils) thick.

[00016] The metal substrate 120 can comprise copper, such as a copper alloy. Other example metals for the metal substrate 120 can also include Ni, Co, Sn, or their alloys. The first and second apertures 120a, 120b are in a repeating pattern having positions matching the size(s) and repeating pattern of the recess pairs 130a, 130b of the dielectric cover 130 shown in FIG. 1A. The apertures 120a and 120b each have an outer ring 120a1 and 120b1 for the first and second semiconductor die to sit on, where the raised pads 125 are on sides generally around the through-hole apertures 120a and 120b. The metal pads 125b may be printed on the dielectric pads 125a. The printing is generally registered by alignment marks on the metal substrate 120.

[00017] FIG. 1C shows a first and a second semiconductor die 180a and 180b sitting top (active) side up with their back side down on the outer rings 120a1 and 120b1 (shown in FIG. 1B) within the apertures 120a and 120b of the metal substrate 120. Bond pads 181 that are coupled to nodes in the circuitry 170a, 170b are shown on the active top side of the semiconductor die 180a and 180b. The circuitry 170a, 170b comprises circuit elements (including transistors, and generally diodes, resistors, capacitors, etc.) formed in a semiconductor layer (an epitaxial layer on a bulk substrate) configured together for generally realizing at least circuit function. Example circuit functions include analog (e.g., amplifier or power converter), radio frequency (RF), digital, or non-volatile memory functions.

[00018] The first and second semiconductor die 180a and 180b have a BSM layer 186, such as comprising copper. Although not shown, there can be an optional refractory metal barrier layer (e.g., TiW TaN, or Cr) underneath the BSM layer 186. The bond pads 181 can include Cu pillars or solder bumps thereon.

[00019] FIG. 1D shows the dielectric cover 130 after being placing on the metal substrate 120 over the semiconductor die 180a, 180b with the view inverted to look down at the bottom of the metal substrate 120 that reveals the portion of the apertures 120a and 120b not occupied by the semiconductor die 180a, 180b. The BSM layer 186 is shown on the back side of the semiconductor die 180a, 180b.

[00020] FIG. 1E shows immersing a disclosed covered substrate stack comprising a dielectric cover 130 on a metal substrate 120 having first and second semiconductor die (not shown) therein within a plating container 150 that provides an electroplating bath. These components

are immersed in a plating solution 145 including an electrolyte containing one or more dissolved metal salts including the metal of interest to electroplate, as well as other ions in the solution that permit the flow of electricity.

[00021] In the case of a dielectric cover there is also generally a sealant, such as electroplating solution resistant tape between the dielectric cover 130 and the metal substrate 120 to avoid plating the plated metal die attach layer on the top side of the semiconductor die 180a, 180b. For electroplating, the metal substrate 120 is connected to a negative terminal (cathode) of a power supply 190, and an electrically conductive structure spaced apart from the metal substrate 120 such as a metal block shown as an anode 135 spaced apart from the metal substrate 120 is connected to a positive terminal (anode) of the power supply 190.

[00022] The electroplating is generally performed at a temperature from 15 °C to 30 °C to avoid introduction of temperature induced stresses, such as to the interconnect on the semiconductor die. At the cathode, the dissolved metal ions (e.g., Cu^{+2}) in the plating solution 145 are reduced at the interface between the solution and the cathode, such that they plate out to a zero valence state metal (e.g., Cu metal) onto the cathode. The electroplating is generally performed using direct current (DC), but can also be performed as pulsed electroplating.

[00023] The electroplating deposits a plated metal die attach layer shown herein as 187 including in FIG. 1F, as a single layer, such as comprising copper, to fill a volume between the BSM layer 186 on the bottom side of the semiconductor die 180a and 180b and the walls of the metal substrate 120 bounding the apertures 120a, 120b to provide a die attachment. The time for the electroplating process can be calculated by dividing the desired metal die attach layer 187 thickness by the deposition rate. The plated metal die attach layer 187 thickness is designed to fill the apertures 120a, 120b, such as being 10 to 250 μm thick, for example being 40 to 250 μm thick.

[00024] FIG. 1F shows the portion of the apertures 120a, 120b not occupied by the semiconductor die 180 (under the die) now filled with a plated metal die attach layer 187 that is deposited as a sheet on the entire bottom side of the metal substrate 120. Although the plated metal die attach layer 187 is shown being planar, there is generally a slight depression when over the respective apertures 120a, 120b.

[00025] The plated metal die attach layer 187 being a plated metal layer is a distinctive layer even as compared to other layers of the same metal material deposited by other methods, such as

sputtered metal layers. Electrodeposited layers are known to fill regions that are not line of sight, unlike sputtered layers. Electrodeposited layers are also known to have a unique microstructure that includes an initially deposited Nernst diffusion layer that has a density and microstructure distinct from that of the bulk portion of the electrodeposited layer.

[00026] FIG. 2A shows a single leaded multi-chip semiconductor device 200 after removing the covered substrate stack from the plating solution 145, removing the dielectric cover 130, singulating the metal substrate 120 and adding leads 126 onto the metal pads 125b of the raised pads 125, such as by soldering. The leaded multi-chip semiconductor device 200 can be seen to be an 18 lead package. The leads 126 comprise strips of metal (e.g., the same metal as for lead frames) such as being copper, copper alloy or tin coated leads 126 that can be acquired commercially or generated in-house. For example, a metal sheet can be cut into strips of metal for the leads 126.

[00027] The leads 126 have at least one bend and include a distal portion that extends beyond the metal substrate 120. Although not shown, the leads 126 can be in a gull wing arrangement. The leads 126 are generally soldered to the metal pads 125b but can also be attached via welding or by an electrically conductive adhesive material. The bondwires 133 and 134 shown are added before singulation, including bondwires 133 connecting between the metal pads 125b of the raised pads 125 and the bond pads 181 on the semiconductor die 180a, 180b. There are also optional bondwires 134 shown connecting between bond pads 181 on the respective semiconductor die 180a, 180b. FIG. 2B shows the disclosed leaded multi-chip packaged semiconductor device now shown as 250 after forming a mold compound 290 that provides encapsulation for the packaged semiconductor device.

[00028] Disclosed aspects can be integrated into a variety of assembly flows to form a variety of different multi-chip semiconductor packaged devices and related products. The semiconductor die may include various elements therein and/or layers thereon, including barrier layers, dielectric layers, device structures, active elements and passive elements including source regions, drain regions, bit lines, bases, emitters, collectors, conductive lines, conductive vias, etc. Moreover, the semiconductor die can be formed from a variety of processes including bipolar, insulated-gate bipolar transistor (IGBT), CMOS, BiCMOS and MEMS.

[00029] Those skilled in the art to which this Disclosure relates will appreciate that many variations of disclosed aspects are possible within the scope of the claimed invention, and further

additions, deletions, substitutions and modifications may be made to the above-described aspects without departing from the scope of this Disclosure.

CLAIMS

What is claimed is:

1. A packaged semiconductor device, comprising:
 - a metal substrate having a first through-hole aperture and a second through-hole aperture each having an outer ring, and a plurality of metal pads around the first and the second through-hole apertures on dielectric pads;
 - a first and a second semiconductor die that each have a back side metal (BSM) layer on its bottom side mounted top side up on a top portion of the apertures;
 - a metal die attach layer directly between the BSM layer and walls of the metal substrate bounding the apertures to provide a die attachment for the first and the second semiconductor die that fills a bottom portion of the apertures;
 - leads that contact the plurality of metal pads, wherein the leads include a distal portion that extends beyond the metal substrate;
 - bondwires between the plurality of metal pads and bond pads on the first and the second semiconductor die, and
 - a mold compound providing encapsulation for the packaged semiconductor device.
2. The packaged semiconductor device of claim 1, wherein the dielectric pads comprise a polymer.
3. The packaged semiconductor device of claim 1, wherein the metal die attach layer consists of a single layer.
4. The packaged semiconductor device of claim 1, wherein the BSM layer, the metal substrate, and the metal die attach layer all comprise copper.
5. The packaged semiconductor device of claim 1, wherein the metal die attach layer is an electroplated metal layer.
6. The packaged semiconductor device of claim 1, further comprising other bondwires between other bond pads on the first semiconductor die and other bond pads on the second semiconductor die.
7. The packaged semiconductor device of claim 1, wherein the metal die attach layer is 40 to 250 μm thick.
8. The packaged semiconductor device of claim 1, wherein the metal substrate is 0.1 mm to 0.3 mm thick.

9. A packaged semiconductor device, comprising:

a metal substrate having a first through-hole aperture and a second through-hole aperture each having an outer ring, and a plurality of metal pads around the first and the second apertures on dielectric pads;

a first and a second semiconductor die that each have a back side metal (BSM) layer on its bottom side mounted top side up on a top portion of the apertures;

a metal die attach layer directly between the BSM layer and walls of the metal substrate bounding the apertures to provide a die attachment for the first and the second semiconductor die that fills a bottom portion of the apertures;

leads that contact the plurality of metal pads, wherein the leads include a distal portion that extends beyond the metal substrate;

bondwires between the plurality of metal pads and bond pads on the first and the second semiconductor die; and

a mold compound providing encapsulation for the packaged semiconductor device;

wherein the metal die attach layer consists of a single layer, and

wherein the BSM layer, the metal substrate, and the metal die attach layer all comprise copper.

10. The packaged semiconductor device of claim 9 further comprising other bondwires between other bond pads on the first semiconductor die and on the second semiconductor die.

11. The packaged semiconductor device of claim 9, wherein the metal die attach layer is 40 to 250 μm thick.

12. A method of semiconductor assembly for multichip packages, comprising:

providing a metal substrate including a repeating pattern of a first through-hole aperture and a second through-hole aperture each having an outer ring, and a plurality of metal pads around the apertures on dielectric pads, the outer rings position matching a first and a second semiconductor die that each have a back side metal (BSM) layer thereon;

inserting the first semiconductor die and the second semiconductor die each having bond pads top side up into respective ones of the plurality of apertures to sit on the outer rings;

sealing a top side of the first semiconductor die and the second semiconductor die to secure the first and the second semiconductor die in the apertures to provide a plurality of covered substrate stacks;

immersing the plurality of covered substrate stacks in a metal electroplating solution within a solution container, with the metal substrate connected to a negative terminal of a power supply and an electrically conductive structure spaced apart from the metal substrate connected to a positive terminal of the power supply, and

electroplating to deposit an electroplated metal die attach layer to fill a volume between the BSM layer and walls of the metal substrate bounding the apertures to provide a die attachment for the first semiconductor die and the second semiconductor die.

13. The method of claim 12, wherein a dielectric cover is used for the sealing, further comprising removing the dielectric cover after the electroplating and then performing wirebonding between the plurality of metal pads and the bond pads on the first semiconductor die and the second semiconductor die.

14. The method of claim 12, wherein an ultraviolet (UV) light curable tape is used for the sealing.

15. The method of claim 12, further comprising printing on the metal substrate dielectric pads then printing the metal pads on the dielectric pads.

16. The method of claim 12, wherein the metal electroplating solution comprises a copper electroplating solution, and wherein the BSM layer, the metal substrate, and the metal die attach layer all comprise copper.

17. The method of claim 12, wherein the dielectric pads comprise a polymer.

18. The method of claim 16, wherein the wirebonding further comprises placing bondwires between other bond pads on the first semiconductor die and other bond pads on the second semiconductor die.

19. The method of claim 12, further comprising forming a mold compound for encapsulation of the packaged semiconductor device.

1/5

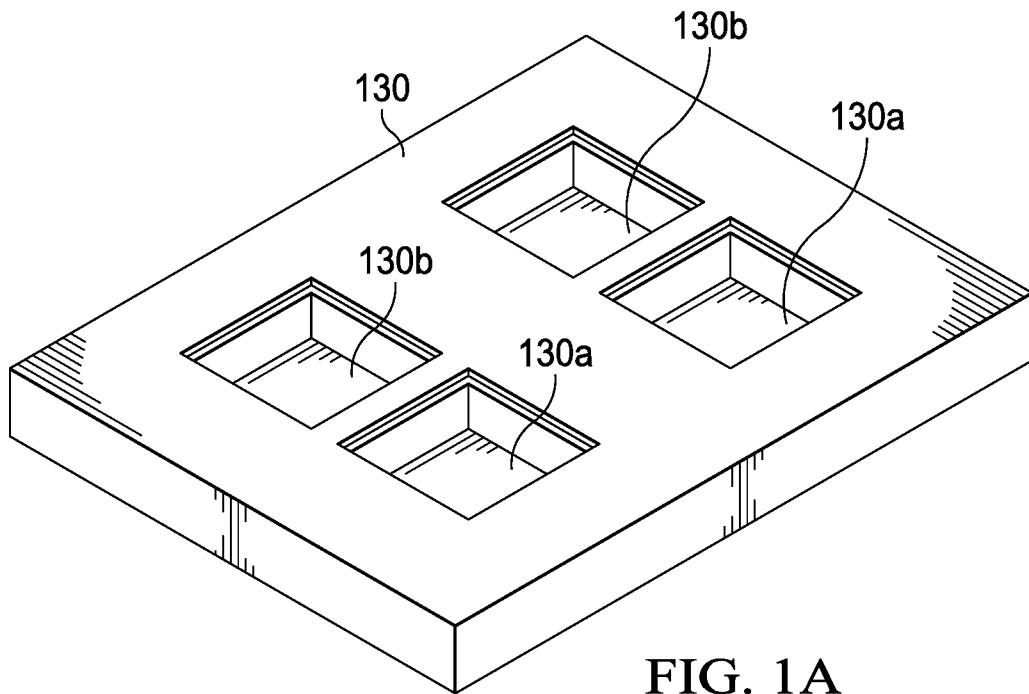


FIG. 1A

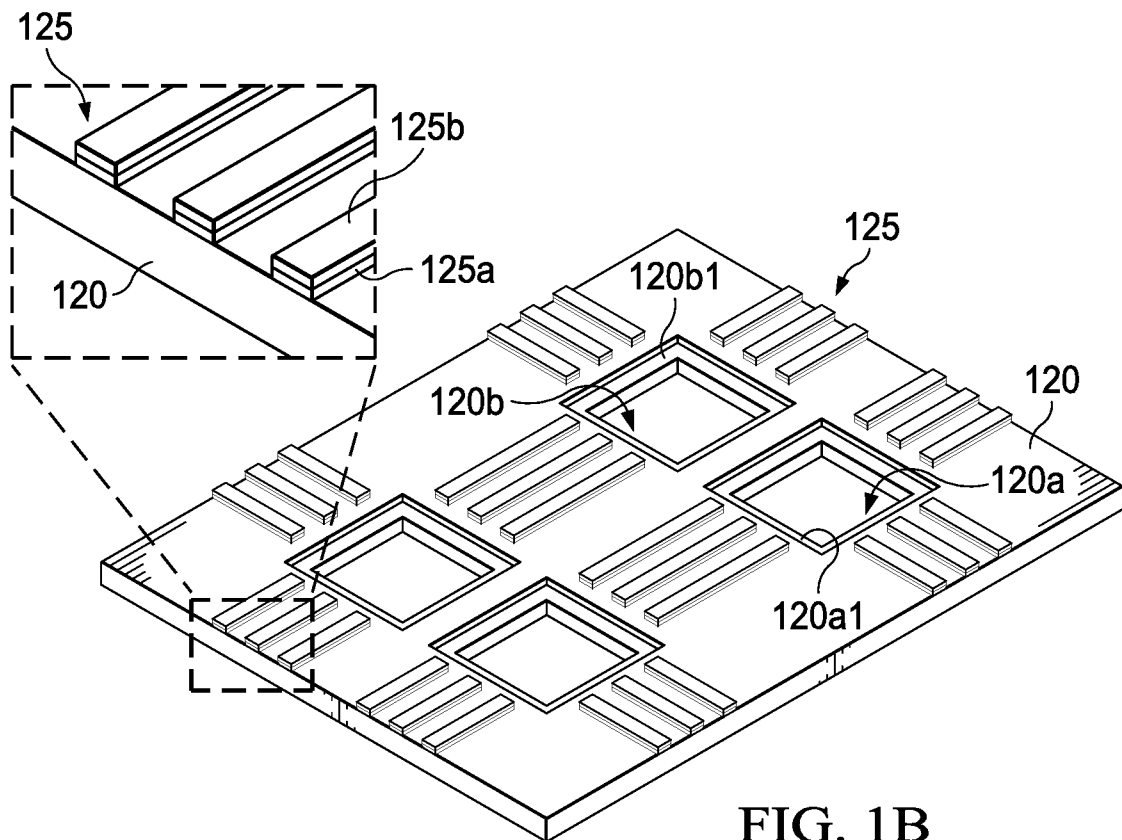


FIG. 1B

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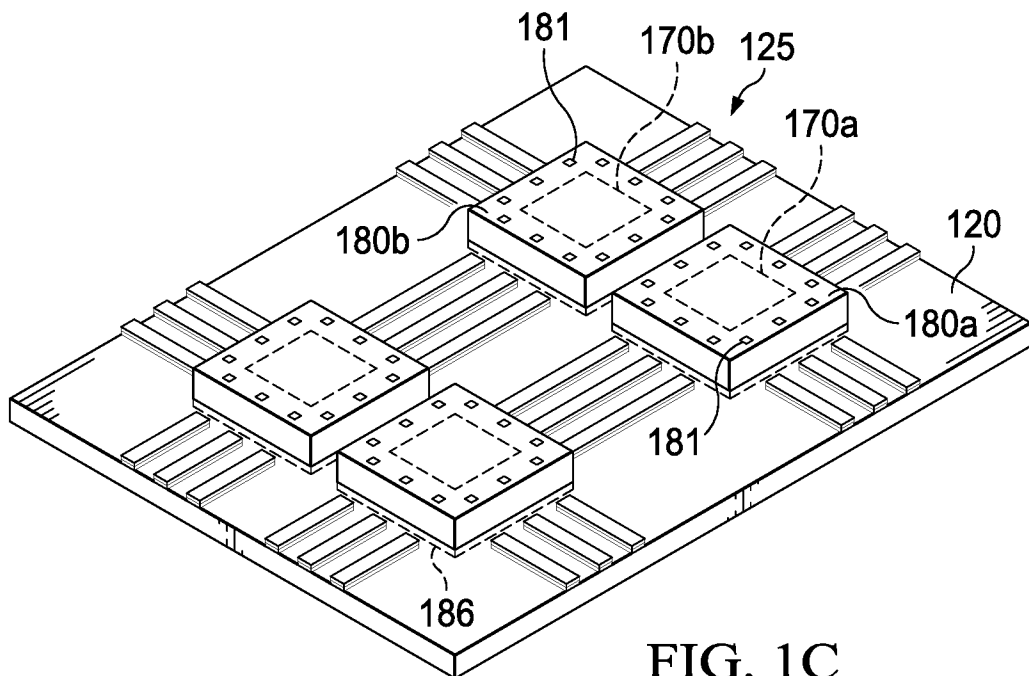


FIG. 1C

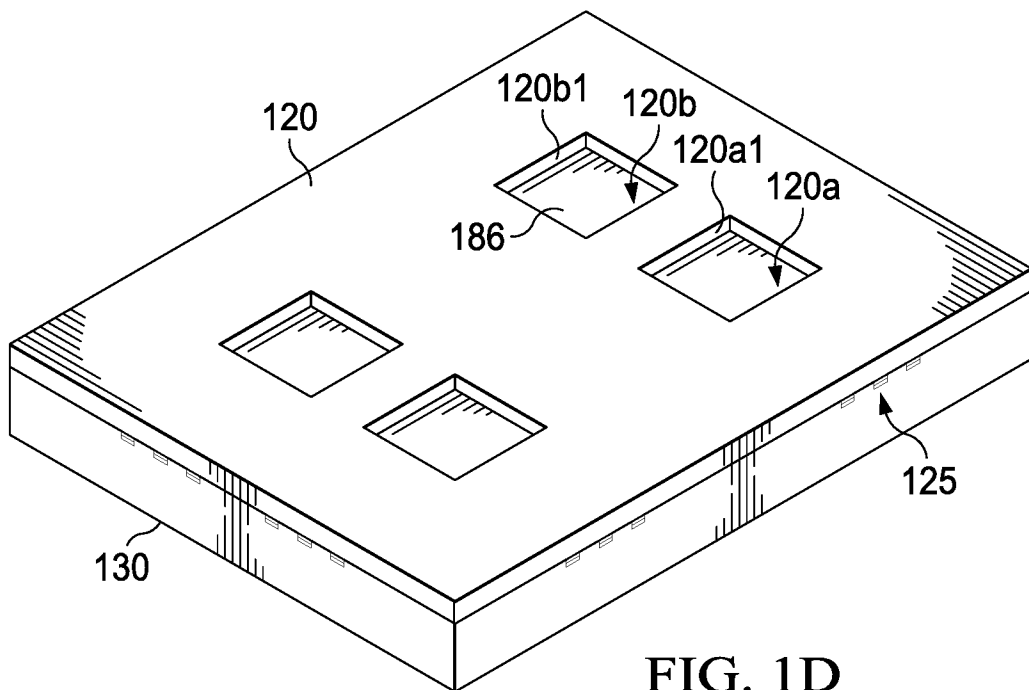


FIG. 1D

3/5

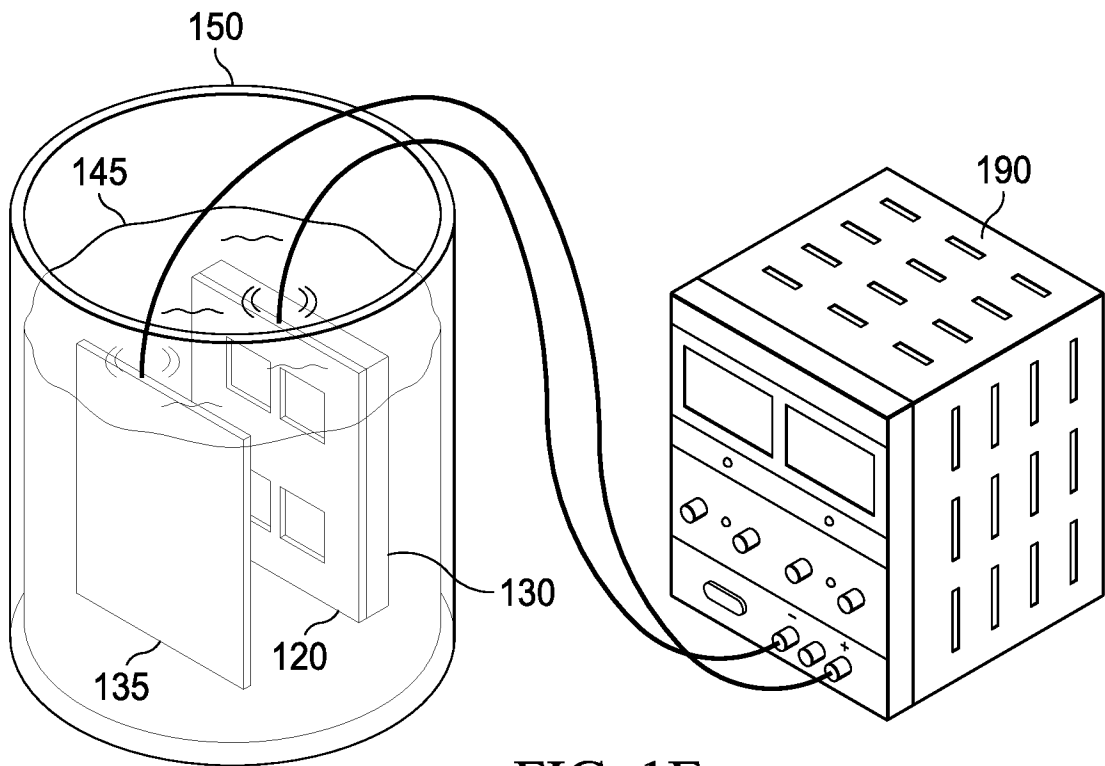


FIG. 1E

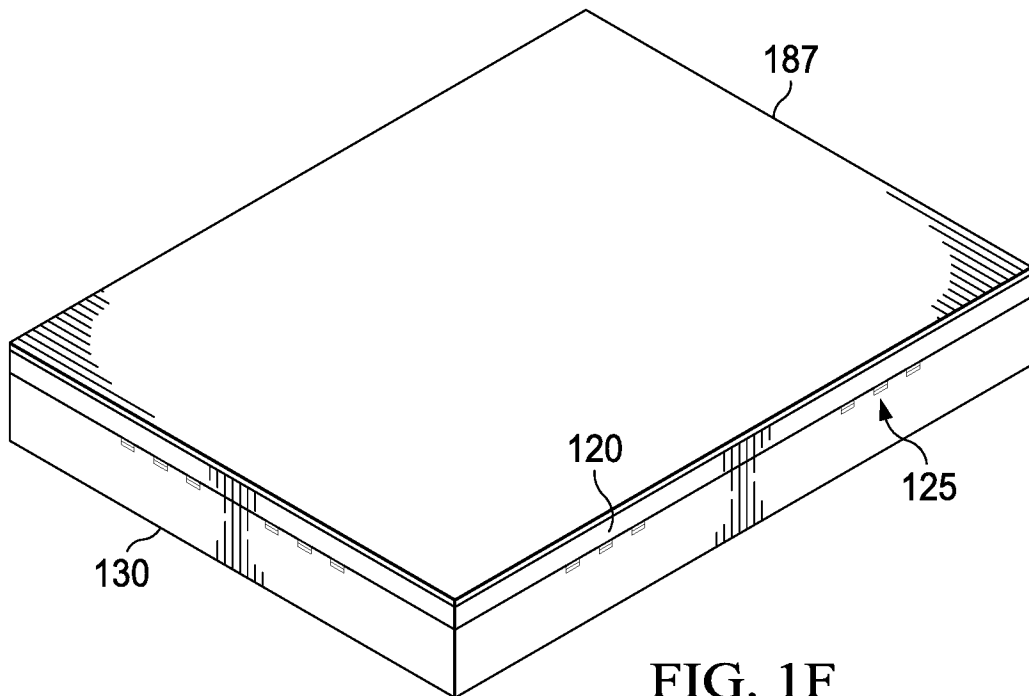


FIG. 1F

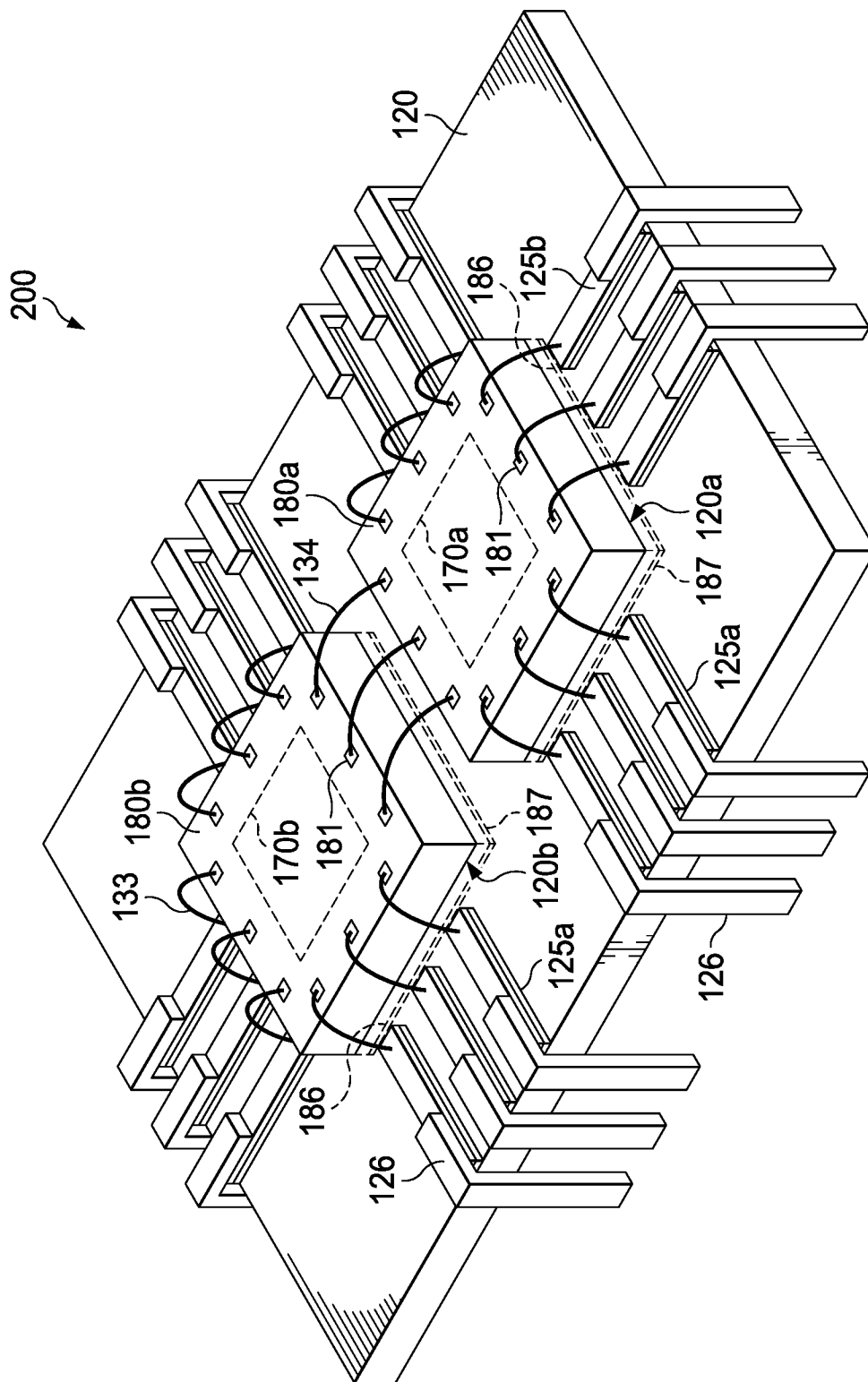


FIG. 2A

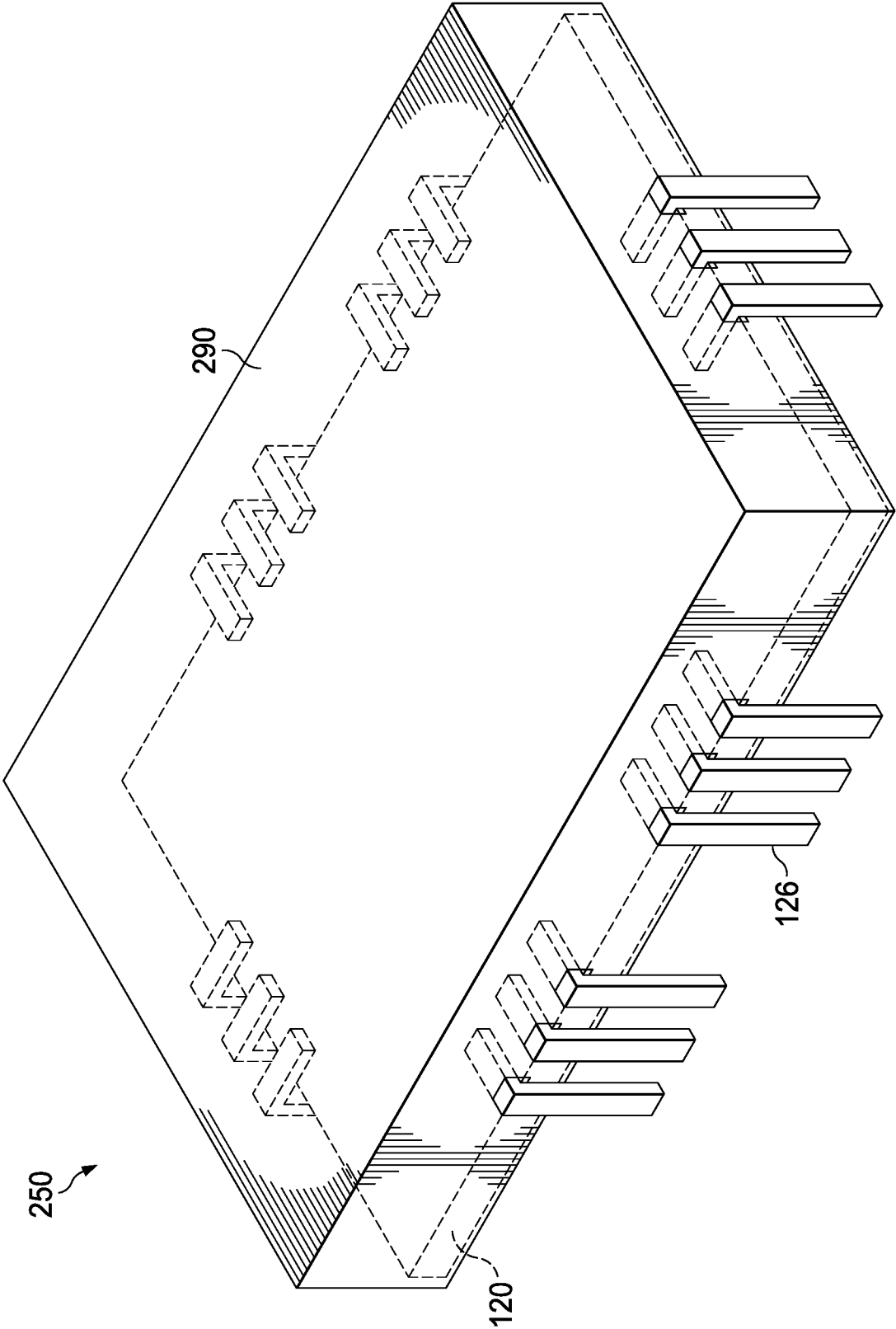


FIG. 2B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2020/022553

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/50 (2006.01)**H01L 27/02 (2006.01)**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/56, 27/04, 23/28

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO Internal), USPTO, PAJ, Espacenet, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6277672 B1 (THIN FILM MODULE, INC.) 21.08.2001, fig. 1, abstract, col. 5, line 1 –col. 7, lines 55	1-19
A	US 2012/0199960 A1 (TEXAS INSTRUMENTS INCORPORATED) 09.08.2012	1-19
A	US 2004/0063249 A1 (MEGIC CORPORATION) 01.04.2004	1-19
A	KR 20130015484 A (DOOSUNG ADVANCED TECHNOLOGY CO. LTD.) 14.02.2013	1-19



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

“A”	document defining the general state of the art which is not considered to be of particular relevance	“T”	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
“E”	earlier document but published on or after the international filing date	“X”	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
“L”	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	“Y”	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
“O”	document referring to an oral disclosure, use, exhibition or other means	“&”	document member of the same patent family
“P”	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

01 June 2020 (01.06.2020)

Date of mailing of the international search report

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