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(54) **METHOD FOR MAKING INTERNALLY OVERLAPPED CONDITIONERS**

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(21) Appl. No.: **13/175,918**

(22) Filed: **Jul. 4, 2011**

Related U.S. Application Data

(63) Continuation of application No. 12/861,811, filed on Aug. 23, 2010, now Pat. No. 7,974,062, which is a continuation of application No. 11/817,634, filed on Aug. 31, 2007, now Pat. No. 7,782,587, filed as application No. PCT/US06/06607 on Feb. 27, 2006.

(60) Provisional application No. 60/656,910, filed on Mar. 1, 2005, provisional application No. 60/661,002, filed on Mar. 14, 2005, provisional application No. 60/668,992, filed on Apr. 7, 2005, provisional application No. 60/671,107, filed on Apr. 14, 2005, provisional application No. 60/671,532, filed on Apr. 15, 2005, provisional application No. 60/674,284, filed on Apr. 25, 2005, provisional application No. 60/751,273, filed on Dec. 19, 2005.

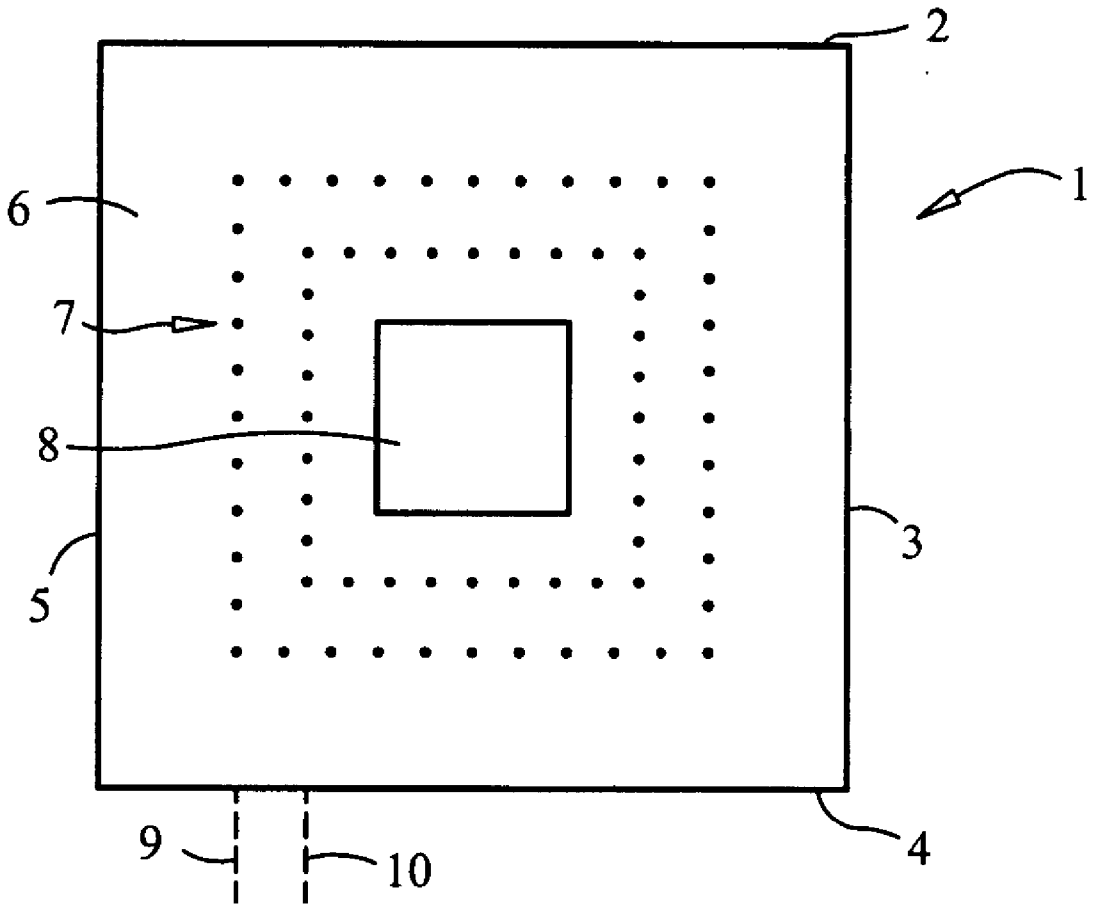
Publication Classification

(51) **Int. Cl.**
H01G 7/00 (2006.01)

(52) **U.S. Cl.** **29/25.41**

(57) **ABSTRACT**

The application discloses novel internal structures of energy conditioners, assemblies of external structures of energy conditioners and mounting structure, and novel circuits including energy conditioners having A, B, and G master electrodes.



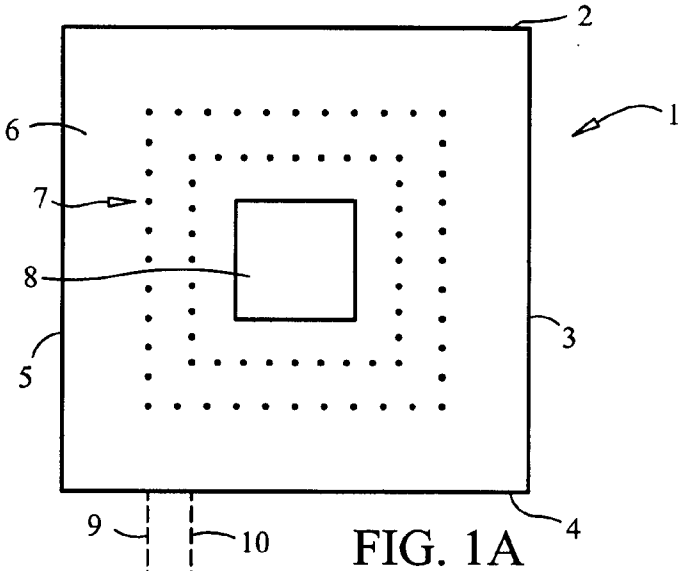


FIG. 1A

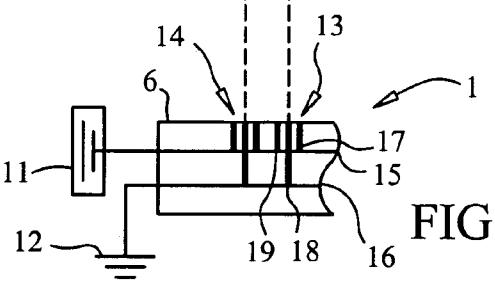


FIG. 1B

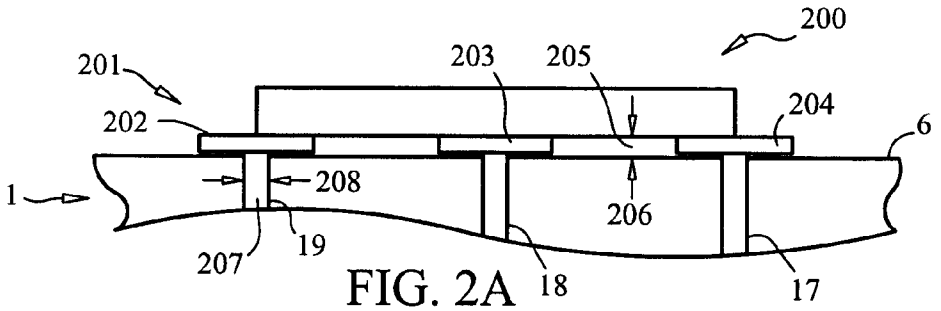


FIG. 2A

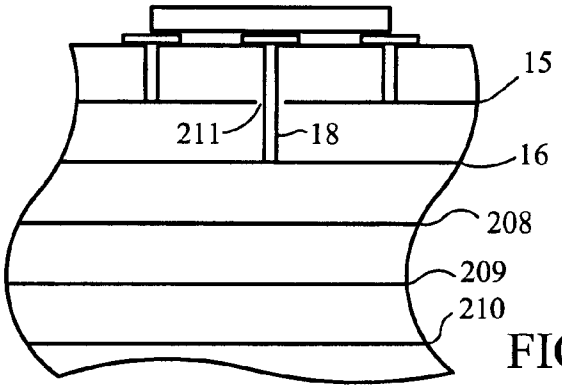


FIG. 2B

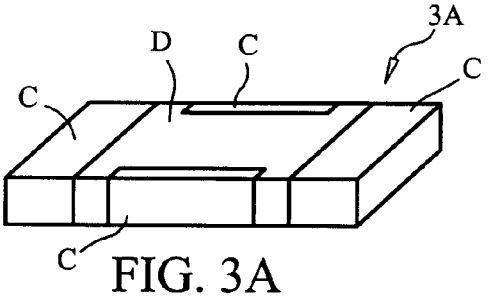


FIG. 3A

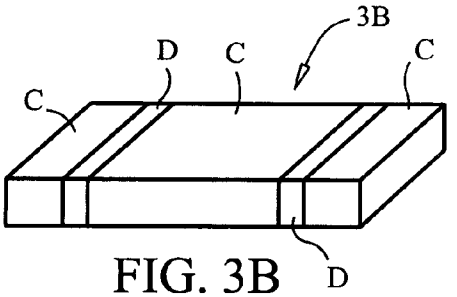


FIG. 3B

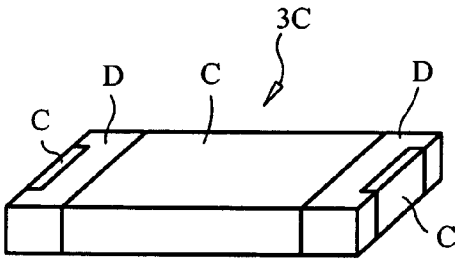


FIG. 3C

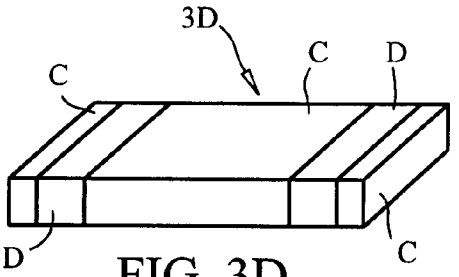


FIG. 3D

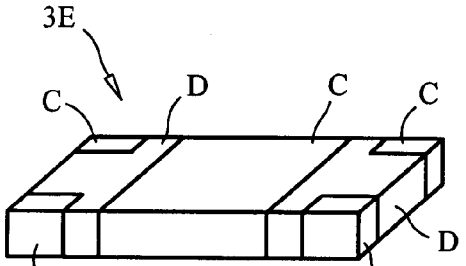


FIG. 3E

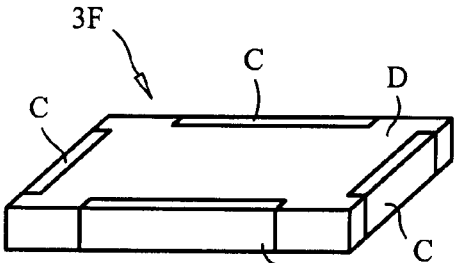


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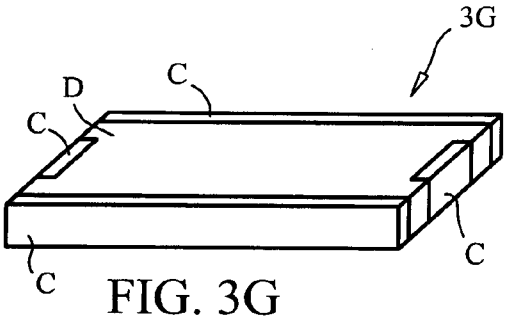


FIG. 3G

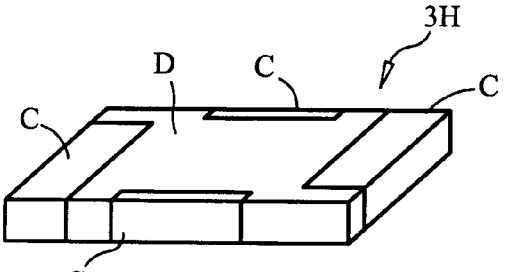


FIG. 3H

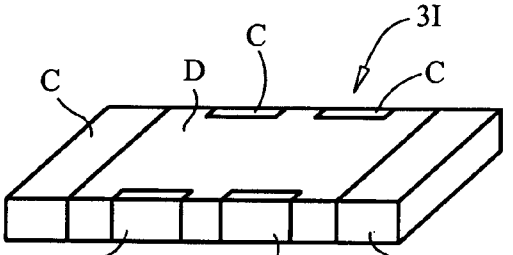


FIG. 3I

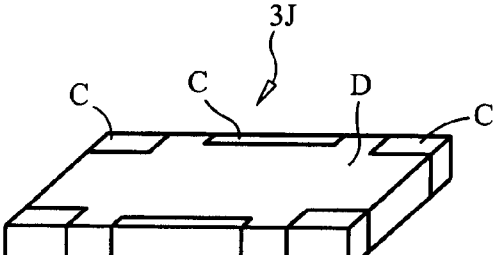


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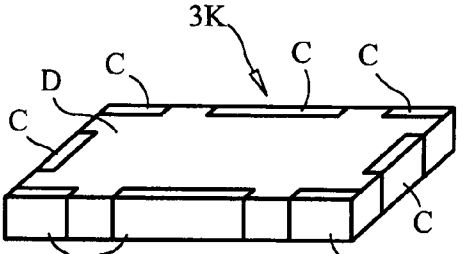


FIG. 3K

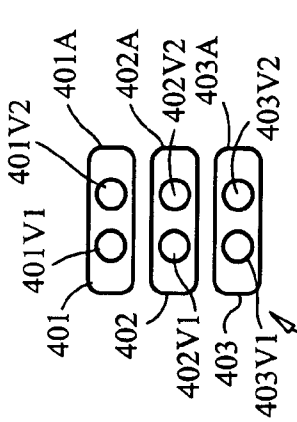


FIG. 4A

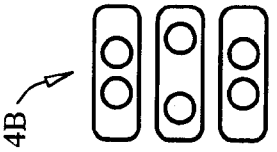


FIG. 4B

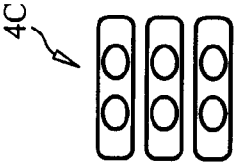


FIG. 4C

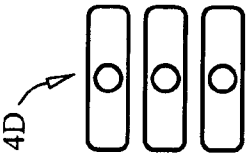


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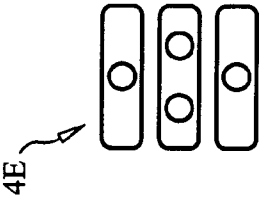


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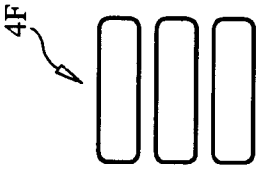


FIG. 4F

FIG. 4G

FIG. 4H

FIG. 4I

FIG. 4J

FIG. 4K

FIG. 4L

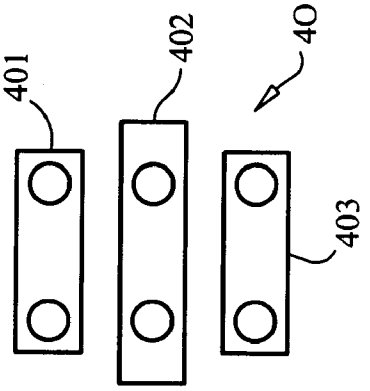


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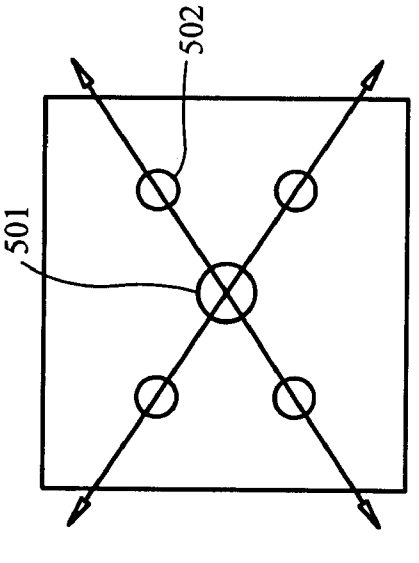


FIG. 4N

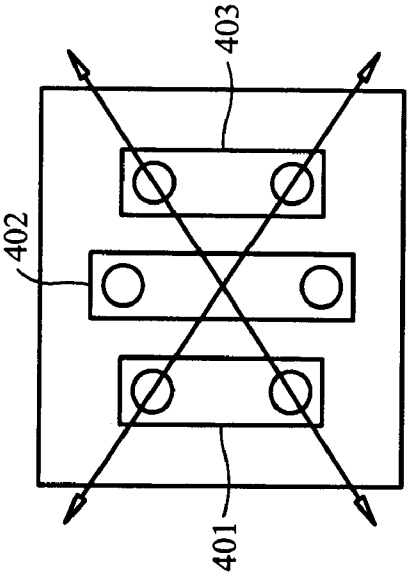


FIG. 4M

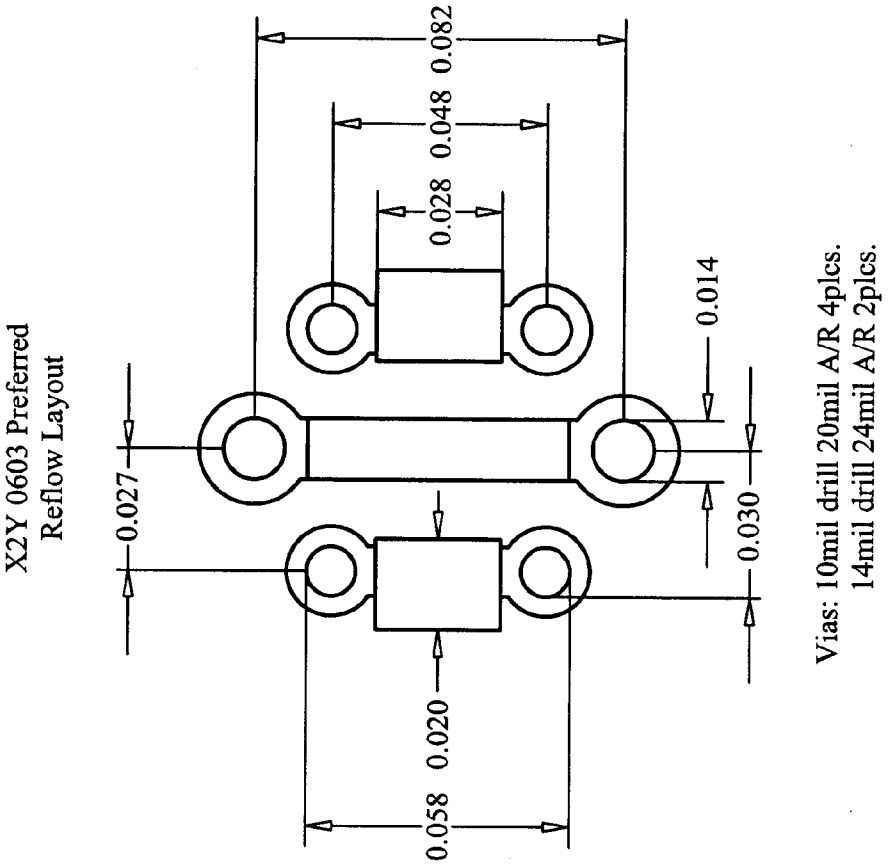

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Reflow Layout
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0.048
0.028
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0.027
0.030
0.020
0.058
Vias: 10mil drill 20mil A/R 4plcs.
14mil drill 24mil A/R 2plcs.

FIG. 5A

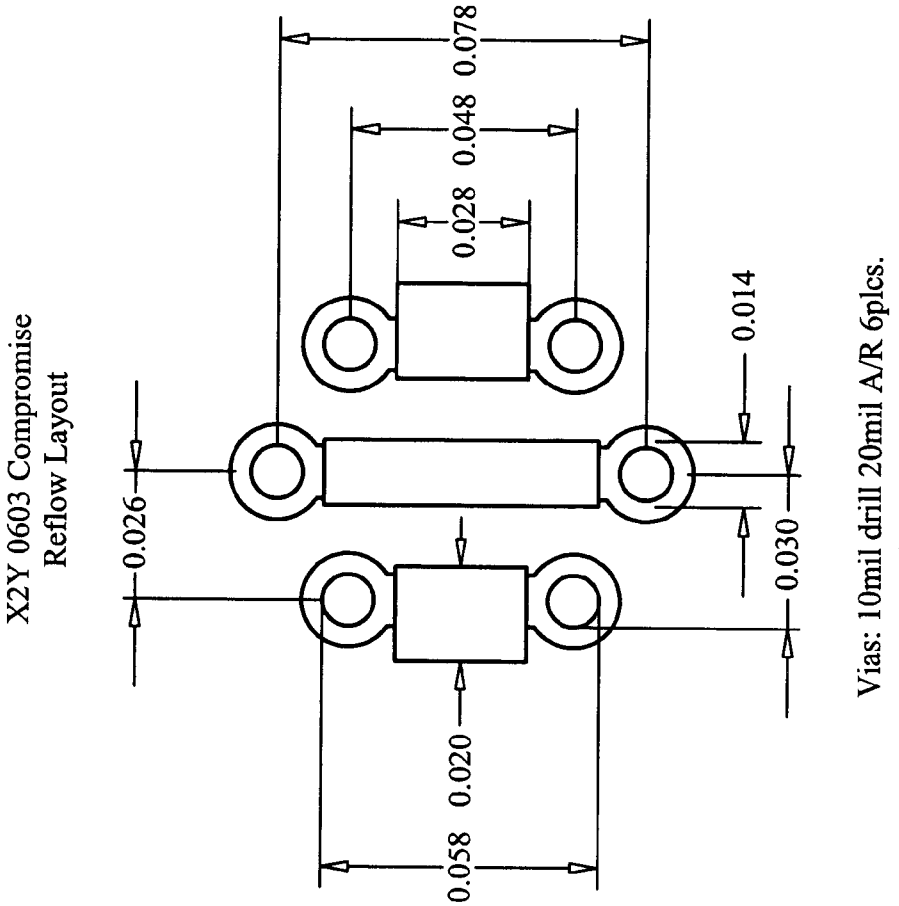

X2Y 0603 Compromise
Reflow Layout
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FIG. 5B

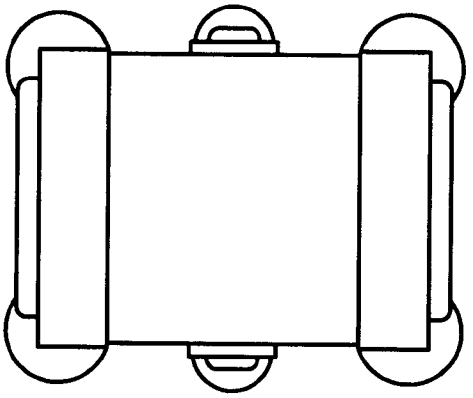


FIG. 6C

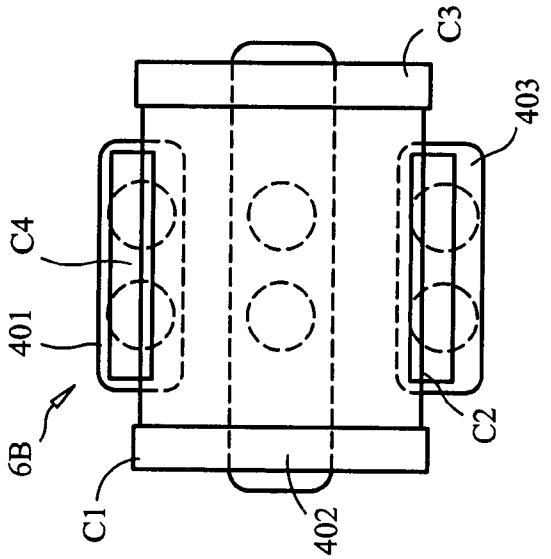


FIG. 6B

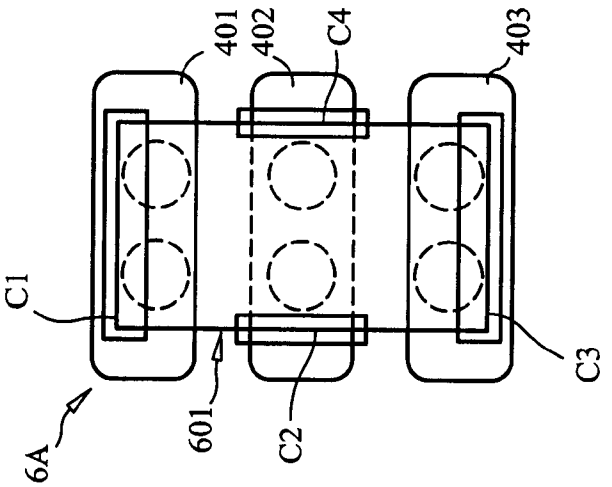


FIG. 6A

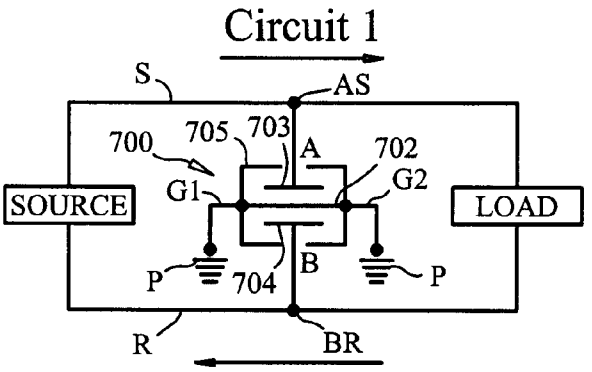


FIG. 7

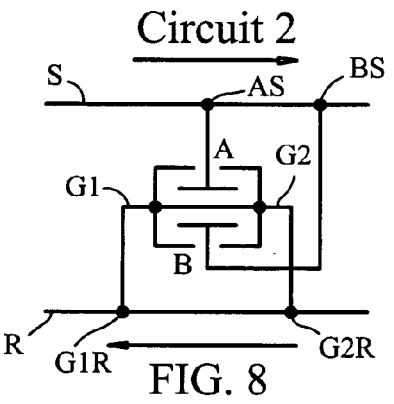


FIG. 8

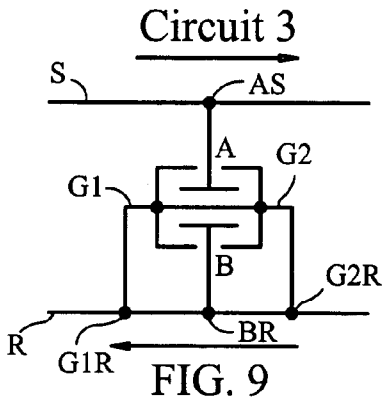


FIG. 9

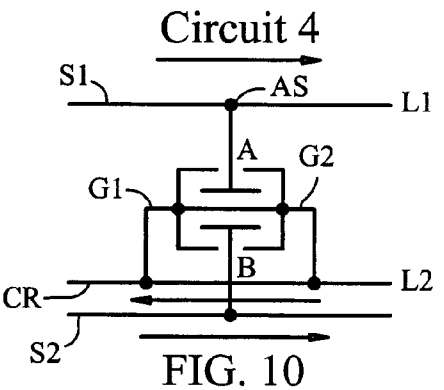


FIG. 10

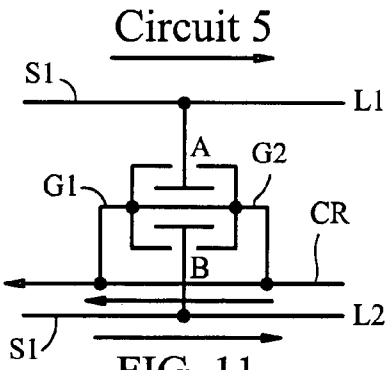


FIG. 11

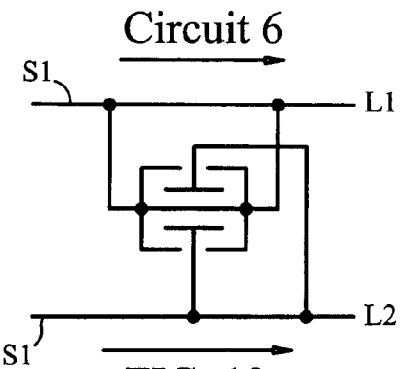


FIG. 12

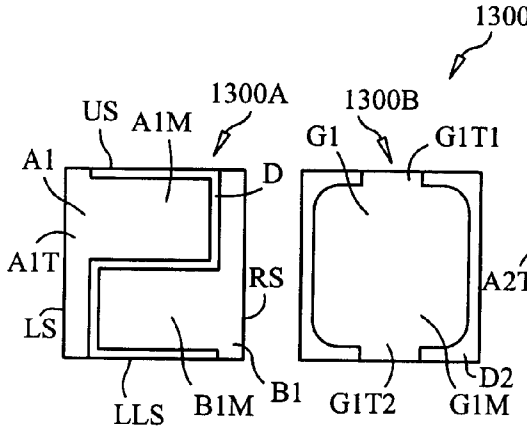


FIG. 13

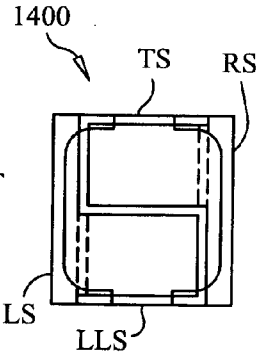


FIG. 14

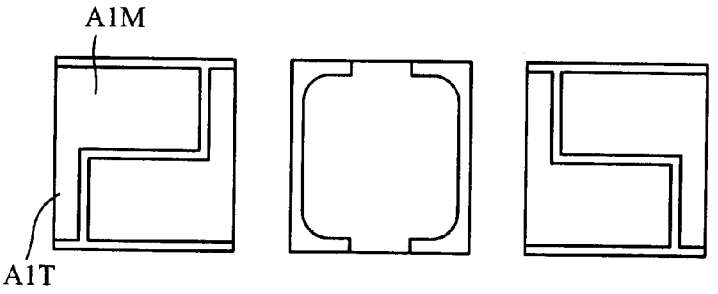


FIG. 15

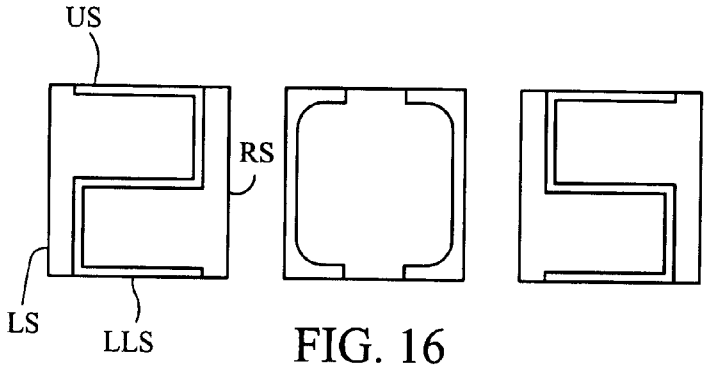


FIG. 16

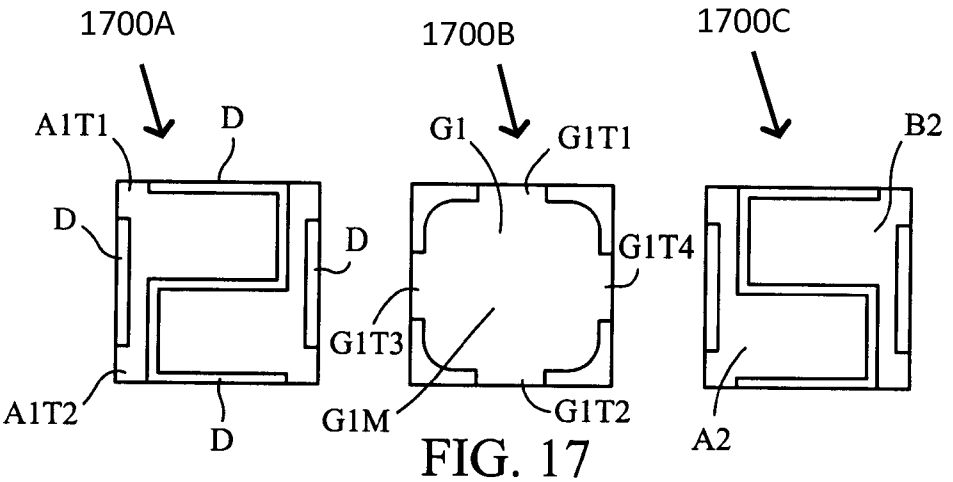


FIG. 17

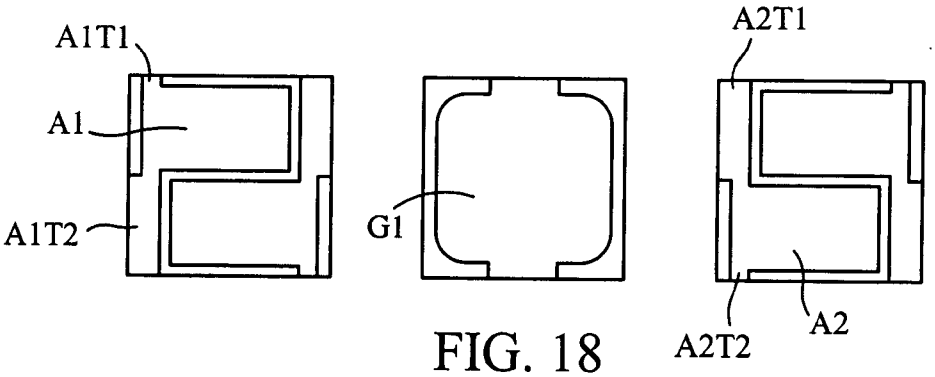


FIG. 18

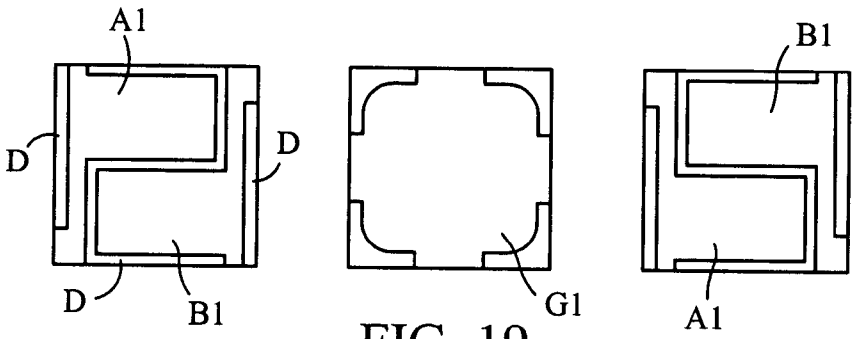


FIG. 19

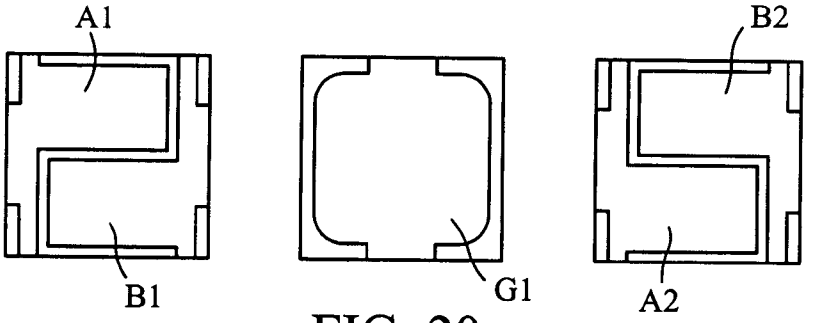


FIG. 20

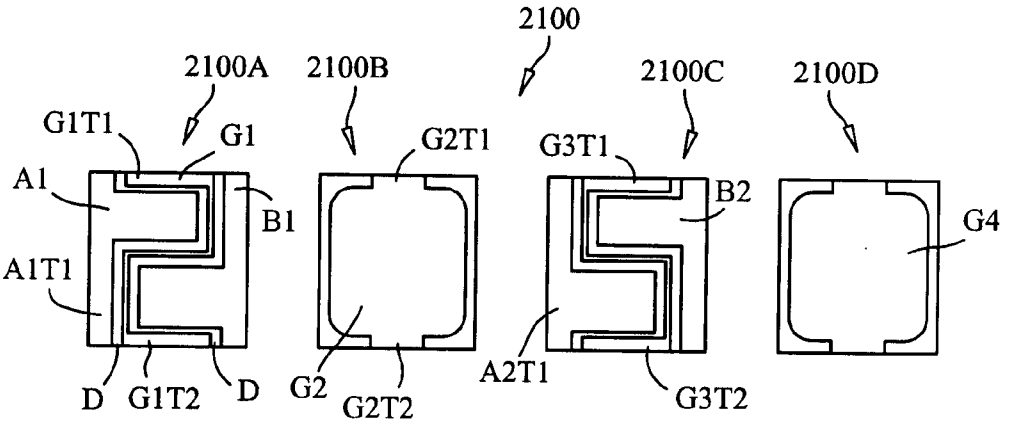

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2100B
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G2T1
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FIG. 21

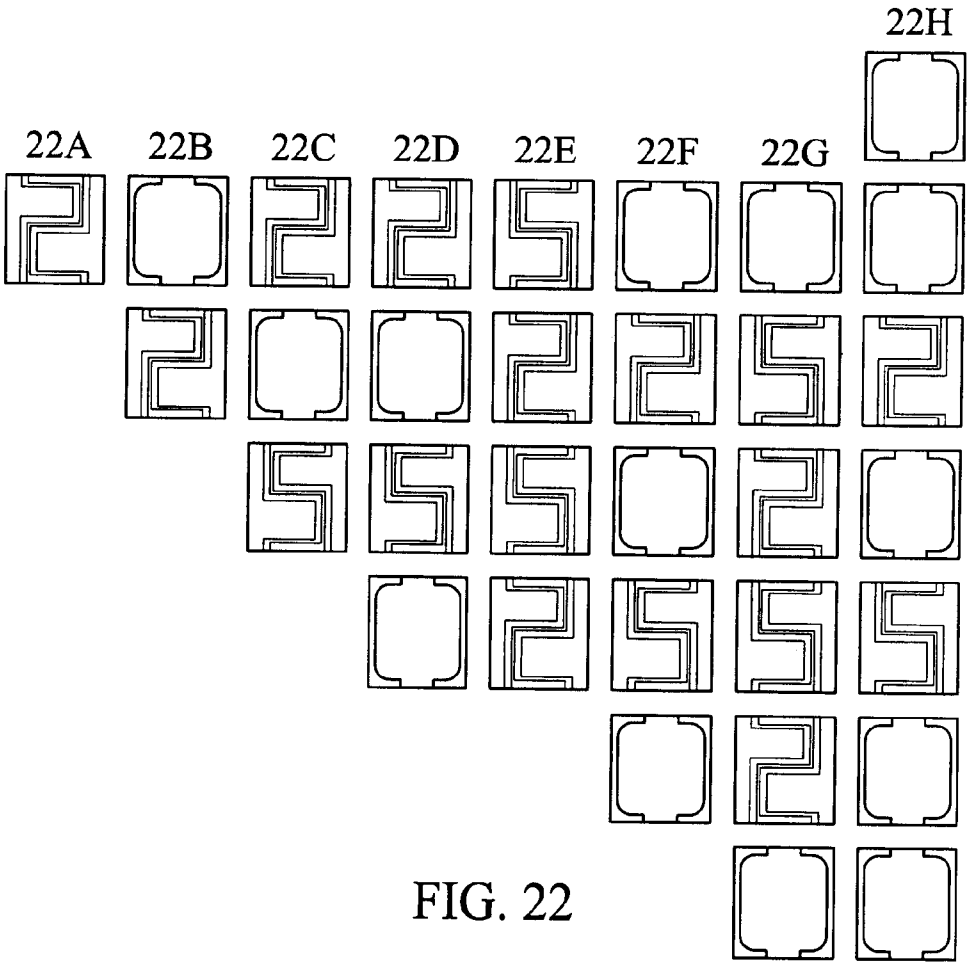

22H
22A
22B
22C
22D
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22F
22G

FIG. 22

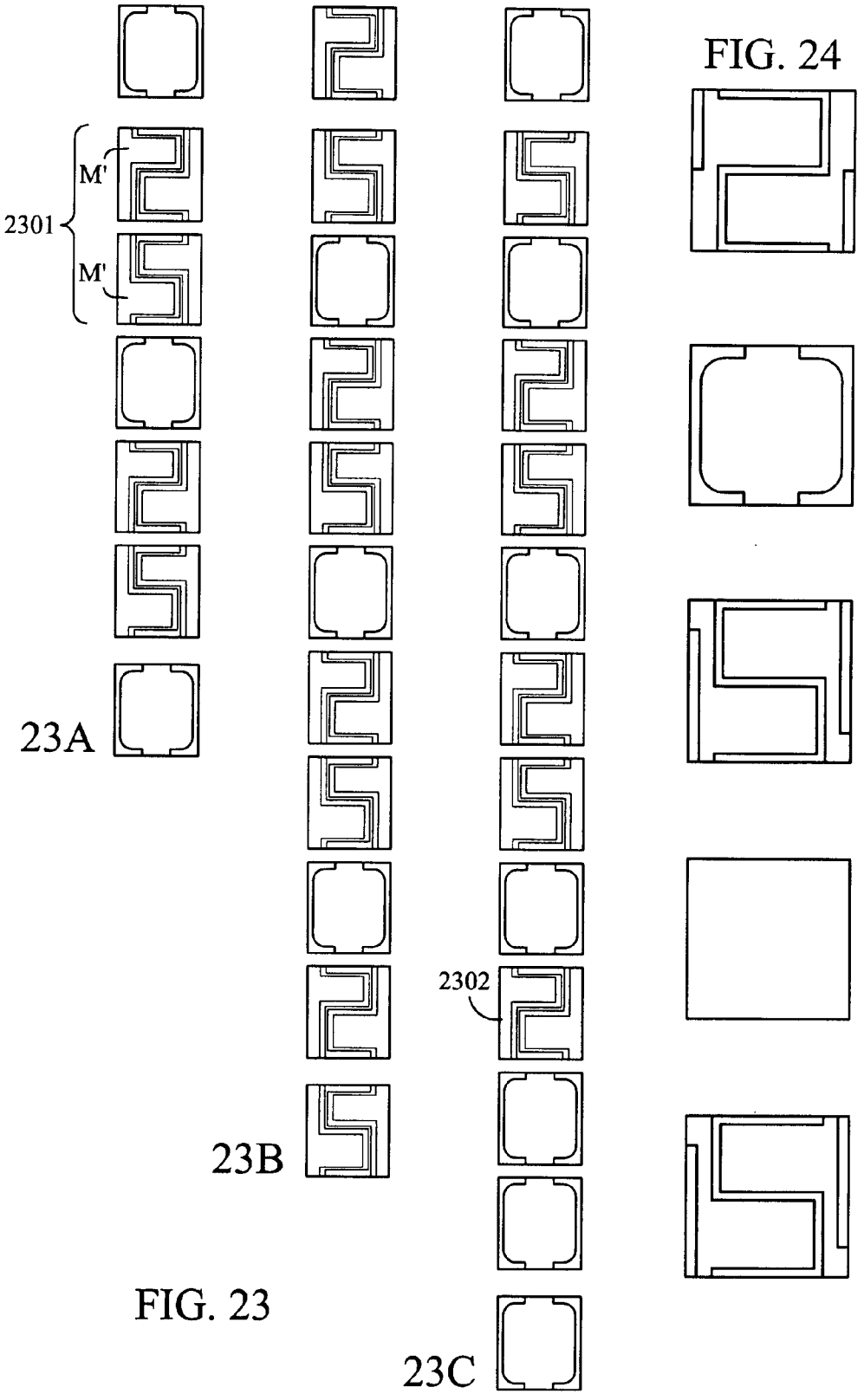


FIG. 23

FIG. 24

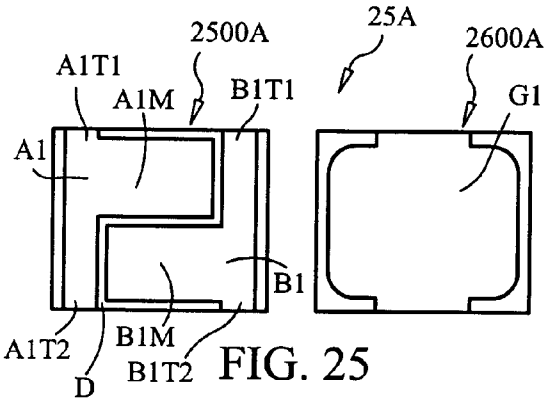


FIG. 25

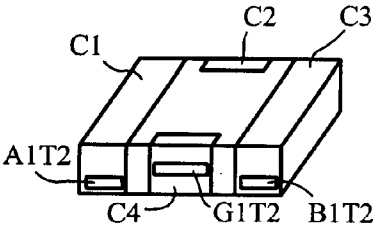


FIG. 26

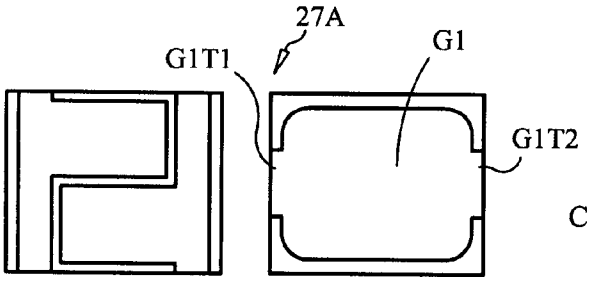


FIG. 27

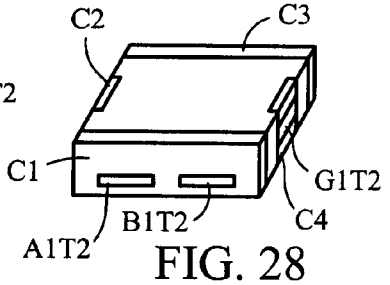


FIG. 28

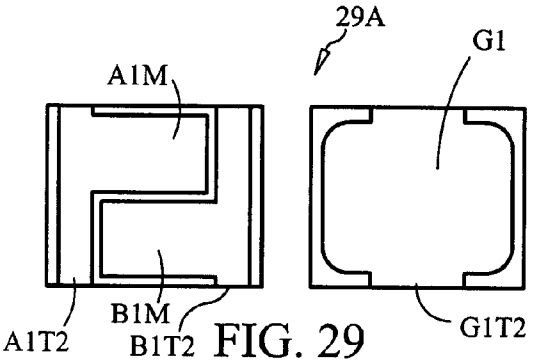


FIG. 29

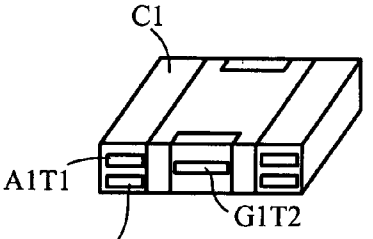


FIG. 30

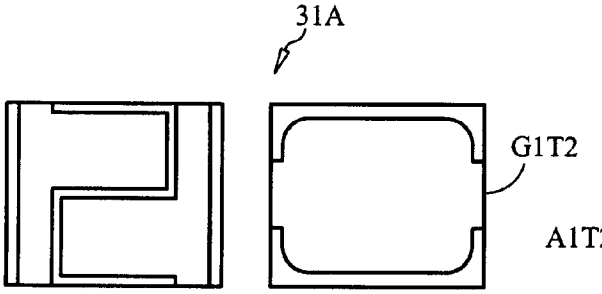


FIG. 31

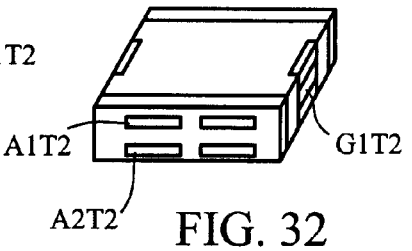


FIG. 32

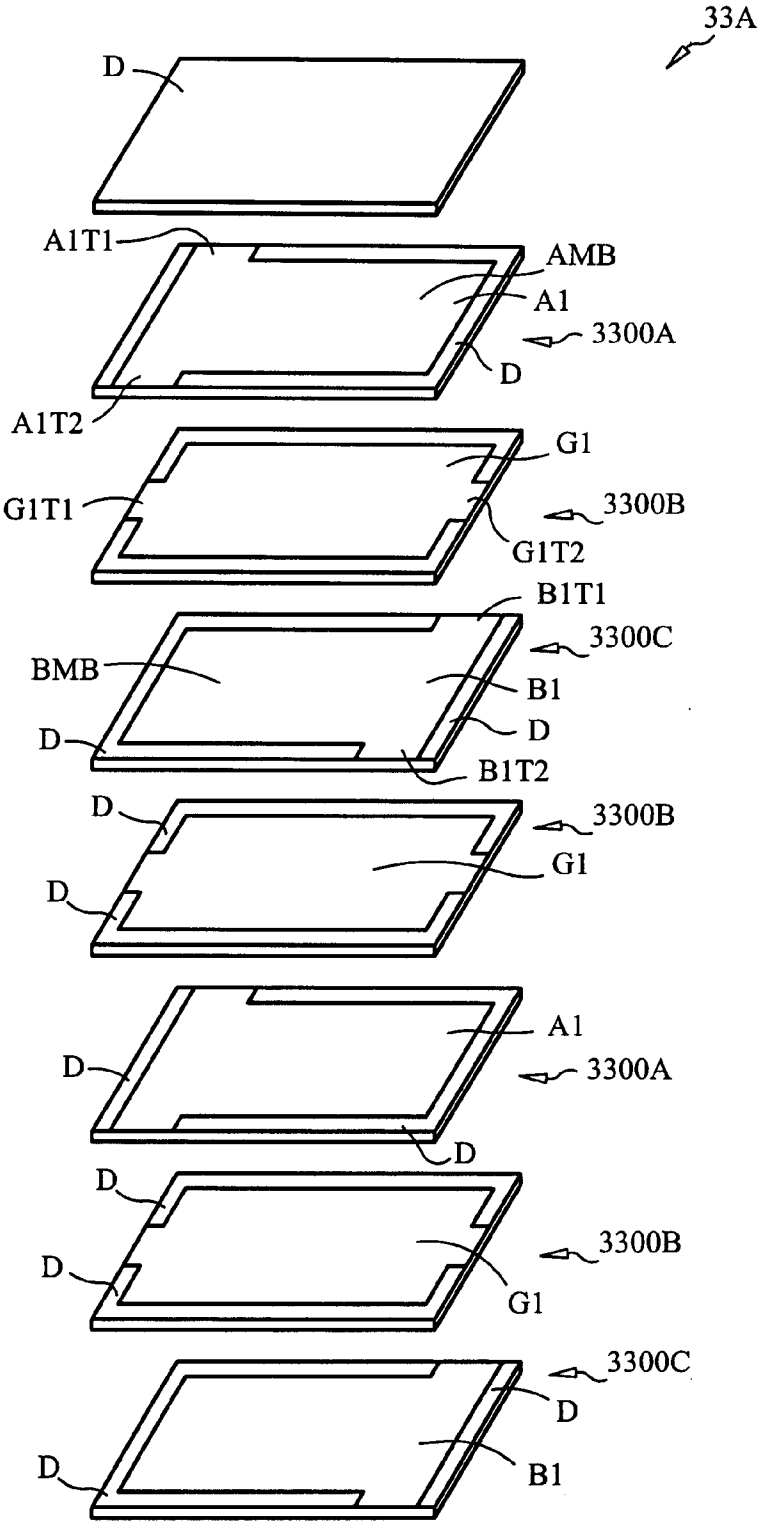

33A
D
A1T1
AMB
A1
3300A
D
A1T2
G1
G1T1
3300B
G1T2
B1T1
3300C
BMB
B1
D
D
B1T2
D
3300B
G1
D
A1
D
3300A
D
D
3300B
G1
3300C
D
D
B1

FIG. 33

METHOD FOR MAKING INTERNALLY OVERLAPPED CONDITIONERS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of application Ser. No. 12/861,811, filed Aug. 23, 2010, which is a continuation of application Ser. No. 11/817,634, filed Aug. 31, 2007, now issued as U.S. Pat. No. 7,782,587, which is a U.S. National Stage Application of International Application PCT/US06/06607, filed Feb. 27, 2006, which claims the benefit of provisional Application No. 60/656,910, filed Mar. 1, 2005, provisional Application No. 60/661,002, filed Mar. 14, 2005, provisional Application No. 60/668,992, filed Apr. 7, 2005, provisional Application No. 60/671,107, filed Apr. 14, 2005, provisional Application No. 60/671,532, filed Apr. 15, 2005, provisional Application No. 60/674,284, filed Apr. 25, 2005, and provisional Application No. 60/751,273, filed December 19, 2005.

[0002] The following applications are each incorporated by reference herein: application Ser. No. 12/861,811, filed Aug. 23, 2010, application Ser. No. 11/817,634, filed Aug. 31, 2007, International Application PCT/US06/06607, filed Feb. 27, 2006, provisional Application No. 60/656,910, filed Mar. 1, 2005, provisional Application No. 60/661,002, filed Mar. 14, 2005, provisional Application No. 60/668,992, filed Apr. 7, 2005, provisional Application No. 60/671,107, filed Apr. 14, 2005, provisional Application No. 60/671,532, filed Apr. 15, 2005, provisional Application No. 60/674,284, filed Apr. 25, 2005, and provisional Application No. 60/751,273, filed Dec. 19, 2005.

FIELD OF THE INVENTION

[0003] This invention relates to energy conditioning.

BACKGROUND OF THE INVENTION

[0004] Electrical circuits using low frequency electrical power generate noise that is coupled through the power distribution system. That noise is generally detrimental. In the past, capacitors have been used to condition the electrical power propagating to and from devices. One type of device in which capacitors have been used to condition electrical power is an active circuitry. Capacitors have been used to in active circuitry to decouple noise from the power lines. Typically, in applications involving Large or Very Large

[0005] Scale Integration (LSI or VLSI) Integrated Circuits (ICs), multiple rows of capacitors are arrayed on a PC board as close as feasible to the location of the IC in the PC board, given design constraints. This arrangement provides sufficient decoupling of the power and ground from the IC's active circuitry. The terms "bypass" and "decoupling" are used interchangeable herein.

SUMMARY OF THE INVENTION

[0006] This application discloses novel energy conditioner structures and novel combinations of the connections of the energy conditioners on other structures, such as PC board structures, and novel circuit arrangements of the energy conditioners with structures, such as PC boards, described herein, generally provide improved decoupling, per conditioner, and require less conditioners and related structure, such as vias, to provide sufficient decoupling. Similarly to PC boards, the structures to which the novel conditioners and the novel combination of the connections of the energy conditioners may be applied include first level interconnects and semiconductor chips, including for example ASIC, FPGA, CPU, memory, transceiver, computer on a chip, and the like.

[0007] More particularly, this application discloses and claims energy conditioner internal structures and external structures, connection structure, and circuits including energy conditioners having A, B, and G master electrodes.

[0008] In one aspect, the claims define an internal structure of an energy conditioner: wherein said internal structure has a left side surface, a right side surface, an upper side surface, a lower side surface, a top side surface, and a bottom side surface;

[0009] wherein said internal structure comprises a dielectric material and a conductive material;

[0010] wherein surfaces of said dielectric material and surfaces of said conductive material define said left side surface, said right side surface, said upper side surface, said lower side surface, said top side surface, and said bottom side surface;

[0011] wherein said conductive material comprises a first A conductive layer and a first B conductive layer in a first plane;

[0012] wherein said first A conductive layer and said first B conductive layer are electrically isolated from one another in said structure;

[0013] wherein said first A conductive layer comprises at least one first A conductive layer first tab and a first A conductive layer main body portion;

[0014] wherein said first B conductive comprises at least one first B conductive layer first tab and a first B conductive layer main body portion;

[0015] wherein said first A conductive layer main body portion does not extend to any one of said left side, right side, upper side, and lower side;

[0016] wherein said first B conductive layer main body portion does not extend to any one of said left side, right side, upper side, and lower side;

[0017] wherein said at least one first A conductive layer first tab extends to said left side surface, said upper side surface, and said lower side surface; and

[0018] wherein said at least one first B conductive layer first tab extends to at least portions of said right side surface, said upper side surface, and said lower side surface.

[0019] In aspects dependent upon the foregoing, the claims define wherein said first A conductive layer main body portion extends to a region closer to said right side surface than said left side surface and closer to said upper side surface than said lower side surface, and wherein said first B conductive layer main body portion extends to a region closer to said left side surface than said right side surface and closer to said lower side surface than said upper side surface; wherein said at least one first A conductive layer first tab comprises a single tab extending across all of said left side, extending to a left side end of said upper side surface, and extending to a left side end of said lower side surface; wherein said at least one first A conductive layer first tab comprises at least two tabs; wherein said conductive material further comprises a first G conductive layer; wherein conductive material further comprises a first G conductive layer between said first A conductive layer and said first B conductive layer; wherein conductive material further comprises a first G conductive layer in a second plane parallel to said first plane, and said G conductive layer has a G conductive layer main body portion having a region opposing at least a portion of said first A conductive

layer A main body portion and a portion of said first B conductive layer main body portion;

[0020] wherein said conductive material comprises a second A conductive layer in a second plane and a second B conductive layer in said second plane;

[0021] wherein said second A conductive layer and said second B conductive layer are electrically isolated from one another in said structure;

[0022] wherein said second A conductive layer comprises at least one second A conductive layer first tab and a second A conductive layer main body portion;

[0023] wherein said second B conductive layer comprises at least one second B conductive layer first tab and a second B conductive layer main body portion;

[0024] wherein said second A conductive layer main body portion does not extend to any one of said left side surface, said right side surface, said upper side surface, and said lower side surface;

[0025] wherein said second B conductive layer main body portion does not extend to any one of said left side surface, said right side surface, said upper side surface, and said lower side surface;

[0026] wherein said at least one second A conductive layer first tab extends to at least portions of said left side surface, said upper side surface, and said lower side surface;

[0027] wherein said at least one second B conductive layer first tab extends to at least portions of said right side surface, said upper side surface, and said lower side surface;

[0028] wherein said second A conductive layer main body portion extends to a region closer to said right side surface than said left side surface and closer to said lower side surface than said upper side surface, and wherein said second B conductive layer main body portion extends to a region closer to said left side surface than said right side surface and closer to said upper side surface than said lower side surface;

[0029] whereby said first A conductive layer main body portion and said second B conductive layer main body portion have a first region of substantial overlap and said second A conductive layer main body portion and said first B conductive layer main body portion have a second region of substantial overlap; wherein said conductive material further comprises a first G conductive layer, and wherein said first G conductive layer comprises a main body portion having a substantial overlap with both said first region and said second region; wherein said first G conductive layer is in a third plane between said first plane and said second plane; wherein said conductive material further comprises:

[0030] a first G conductive layer in said first plane between said first A conductive layer and said first B conductive layer and electrically isolated in said structure from said first A conductive layer and said first B conductive layer; and

[0031] a second G conductive layer in said second plane between said second A conductive layer and said second B conductive layer and electrically isolated in said structure from said second A conductive layer and said second B conductive layer; wherein said conductive material further comprises a second G conductive layer, and wherein said second G conductive layer comprises a main body portion having a substantial overlap with both said first region and said second region; and wherein said first G conductive layer is in a third plane between said first plane and said second plane.

[0032] In a second aspect the claims define an assembly comprising said internal structure and an external structure of an energy conditioner, wherein said external structure comprises: a first conductive integration region that extends along at least one of said left side surface, said upper side surface, and said lower side surface and contacts there at, at least one of said at least one first A conductive layer first tab; and a second conductive integration region that extends along at least one of said right side surface, said upper side surface, and said lower side surface and contacts thereat at least one of said at least one first B conductive layer first tab.

[0033] Dependent upon the second aspect, the claims define wherein said internal structure further comprises a G conductive layer including a G conductive layer main body portion, a G conductive layer first tab, and a G conductive layer second tab, and wherein said external structure further comprises a third conductive integration region that extends along at least one side surface of said internal structure and contacts thereat said G conductive layer first tab; wherein said external structure further comprises a fourth conductive integration region that extends along at least one side surface of said internal structure opposite the one side surface of said internal structure along which said third conductive integration region extends where at said fourth conductive integration region contacts said G conductive layer second tab; wherein at least one of said first conductive integration region, said second conductive integration region, said third conductive integration region, and said fourth conductive integration region are formed from solder; wherein at least one of said first conductive integration region, said second conductive integration region, said third conductive integration region, and said fourth conductive integration region comprise a conductive band; further comprising a mounting structure to which said external structure is mounted, wherein said mounting structure consists of only a first conductive regions, a second conductive region, and a third conductive region; wherein said first conductive region comprises conductive material in a first via, said second conductive region comprises conductive material in a second via, and said third conductive region comprises conductive material in a third via.

[0034] In a third aspect the claims define a circuit comprising an internal structure of an energy conditioner having A and B layers in the same plane and tabs extending to at least three side surfaces; a source, and a load, wherein said internal structure is connected in said circuit in a circuit **1** configuration; a circuit comprising an internal structure of an energy conditioner having A and B layers in the same plane and tabs extending to at least three side surfaces, a source, and a load, wherein said internal structure is connected in said circuit in a circuit **2** configuration; a circuit comprising an internal structure of an energy conditioner having A, B, and G master electrode components, a source, and a load, wherein said internal structure is connected in said circuit in a circuit **3** configuration; a circuit comprising an internal structure of an energy conditioner having A, B, and G master electrode components, a first source, a second source, a first load, and a second load, wherein said internal structure is connected in said circuit in a circuit **4** configuration; a circuit comprising an internal structure of an energy conditioner having A, B, and G master electrode components, a first source, a first load, and a second load, wherein said internal structure is connected in said circuit in a circuit **5** configuration; a circuit comprising said internal structure of an energy conditioner having A, B, and G master electrode components, a first source, a first load, and a second load, wherein said internal structure is connected in said circuit in a circuit **6** configuration.

[0035] In additional aspects, the invention comprises an assembly having an energy conditioner having an internal structure, a mounting structure; and wherein said internal structure is mounted on said mounting structure; wherein said mounting structure comprises no more than three separate conductive elements; an assembly comprising: an energy conditioner having an internal structure including components of A, B, and G master electrodes, and an external structure comprising conductive regions that conductively connect components of the A master electrode to one another, components of the B master electrode to one another, and components of the G master electrode to one another; a mounting structure; wherein said internal structure is mounted on said mounting structure; wherein said mounting structure consists of only a first conductive region, a second conductive region, and a third conductive region; and wherein said A master electrode contacts said first conductive region, said B master electrode contacts said second conductive region, and said G master electrode contacts said third conductive region.

[0036] In additional aspects, the claims define that said G master electrode includes a first G conductive integration region that and a second G conductive integration region spatially separated and not contacting said first G conductive integration region, wherein both said a first G conductive integration region and said second G conductive integration region contact said third conductive region.

[0037] In another aspect, the claims define an internal structure of an energy conditioner: wherein said internal structure has a left side surface, a right side surface, an upper side surface, a lower side surface, a top side surface, and a bottom side surface; wherein said internal structure comprises a dielectric material and a conductive material; wherein surfaces of said dielectric material and surfaces of said conductive material define said left side surface, said right side surface, said upper side surface, said lower side surface, said top side surface, and said bottom side surface; wherein said conductive material comprises a stack of at least seven conductive layers in the following order from top to bottom: A**1**; G**1**; B**1**; G**1**; A**1**; G**1**; and B**1** wherein each A**1** conductive layer has an A**1** first tab that extends to said upper side surface near said left side surface and an A**2** tab that extends to said lower side surface near said left side surface; wherein each G**1** conductive layer has a G**1** first tab that extends to said left side surface and a G**2** tab that extends to said right side surface near; and wherein each B**1** conductive layer has a B**1** first tab that extends to said upper side surface near said right side surface and a B**2** tab that extends to said lower side surface near said right side surface. In dependent aspects, each tab of the same type has a vertical overlap with all other tabs of the same type, and conductive integration regions conductively connect layers of the same type only to one another; and wherein additional conductive layers exist within the seven layer sequence.

BRIEF DESCRIPTION OF THE DRAWINGS

[0038] The figures show elements of embodiments of the inventions. The same reference number in different figures refers to identical elements or elements with similar structure or function.

[0039] FIG. **1**A is a plan view of a conventional digital circuit board, also called a PC board, for a conventional high speed VLSI IC (Very Large Scale Integration Integrated Circuit) chip;

[0040] FIG. **1**B is schematic partial edge side sectional view of the conventional board of FIG. **1**A;

[0041] FIG. **2**A is a partial side sectional view of a structure including a more than two terminal energy conditioner mounted via pads to a board, showing vias connecting the conditioner and conductive planes in the board;

[0042] FIG. **2**B is another side sectional view showing power and ground planes and connection of the multi terminal conditioner to the power and ground planes;

[0043] FIGS. **3**A to **3**K are perspective views of exterior surfaces of novel energy conditioners disclosed herein, particularly showing surfaces of conductive band structures, C, and surfaces of dielectric material, D;

[0044] FIGS. **4**A-O are plan views each showing arrangements of conductive elements of mounting surface structure, including conductive pad and/or via structure to which novel discrete component energy conditioners disclosed herein may be mounted;

[0045] FIGS. **5**A and **5**B are plan views showing geometric relationships of vias;

[0046] FIG. **6**A is a schematic view showing a novel combination of a novel energy conditioner on an arrangement of mounting surface structure elements including conductive pads and vias, with two vias per pad;

[0047] FIG. **6**B is a schematic view showing a novel combination of a novel energy conditioner on an arrangement of mounting surface structure elements including conductive pads and vias, with two vias per pad, and a central pad that extends further than the outer two pads such that the central pad contacts conductive terminals, caps, or bands on left and right hand sides of the energy conditioner;

[0048] FIG. **6**C is a top plan view showing a novel combination of a novel energy conditioner on an arrangement of mounting surface structure elements including conductive pads and vias showing overlap of terminals of the conditioner with vias;

[0049] FIG. **7** is a partial schematic of circuit one for use with an energy conditioner having A, B, and G master electrodes;

[0050] FIG. **8** is a partial schematic of circuit two for use with an energy conditioner having A, B, and G master electrodes;

[0051] FIG. **9** is a partial schematic of circuit three for use with an energy conditioner having A, B, and G master electrodes;

[0052] FIG. **10** is a partial schematic of a circuit four for use with an energy conditioner having A, B, and G master electrodes;

[0053] FIG. **11** is a partial schematic of a circuit five for use with an energy conditioner having A, B, and G master electrodes;

[0054] FIG. **12** is a partial schematic of a circuit six for use with an energy conditioner having A, B, and G master electrodes;

[0055] FIG. **13** is an exploded view of a stack of four plates internal to a novel energy conditioner in which the plate elements have been displaced laterally in the page;

[0056] FIG. **14** is a schematic plan view of an assembly of the plates of FIG. **13**;

[0057] FIG. **15** is an exploded view of a stack of three plates internal to a novel energy conditioner in which the plate elements have been displaced laterally in the page;

[0058] FIG. **16** is an exploded view of a stack of three plates internal to a novel energy conditioner in which the plate elements have been displaced laterally in the page;

[0059] FIG. **17** is an exploded view of a stack of three plates internal to a novel energy conditioner in which the plate elements have been displaced laterally in the page;

[0060] FIG. **18** is an exploded view of a stack of three plates internal to a novel energy conditioner in which the plate elements have been displaced laterally in the page;

[0061] FIG. **19** is an exploded view of a stack of three plates internal to a novel energy conditioner in which the plate elements have been displaced laterally in the page;

[0062] FIG. **20** is an exploded view of a stack of three plates internal to a novel energy conditioner in which the plate elements have been displaced laterally in the page;

[0063] FIG. **21** is an exploded view of a stack of four plates internal to a novel energy conditioner in which the plate elements have been displaced laterally in the page;

[0064] FIG. **22** is a set of exploded views of stacks **22**A-**22**H of plates of novel energy conditioners in which the plates of each stack have been displaced vertically in the page;

[0065] FIG. **23** is a set of exploded views of stacks **23**A-**23**C of plates of novel energy conditioners in which the plates of each stack have been displaced vertically in the page;

[0066] FIG. **24** is an exploded view of a stack of plates of a novel energy conditioner in which the plates have been displaced vertically in the page;

[0067] FIG. **25** is an exploded view of a set of two plates of a novel energy conditioner in which the plates have been displaced vertically in the page;

[0068] FIG. **26** is a perspective view of an exterior surface of a novel energy conditioner including the stack of two plates shown in FIG. **25**;

[0069] FIG. **27** is an exploded view of a set of two plates of a novel energy conditioner in which the plates have been displaced vertically in the page;

[0070] FIG. **28** is a perspective view of an exterior surface of a novel energy conditioner including the stack of two plates shown in FIG. **27**;

[0071] FIG. **29** is an exploded view of a set of two plates of a novel energy conditioner in which the plates have been displaced vertically in the page;

[0072] FIG. **30** is a perspective view of an exterior surface of a novel energy conditioner including the stack of two plates shown in FIG. **29**;

[0073] FIG. **31** is an exploded view of a set of two plates of a novel energy conditioner in which the plates have been displaced vertically in the page;

[0074] FIG. **32** is a perspective view of an exterior surface of a novel energy conditioner including the stack of two plates shown in FIG. **31**; and

[0075] FIG. **33** is an exploded view of a stack of 8 plates of a novel energy conditioner in which the plates have been displaced vertically in the page.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0076] FIG. **1**A shows PC board **1** having sides **2**, **3**, **4**, and **5**, top surface **6**, array **7** of structure for mounting discrete capacitors, and region **8** for mounting an IC. Each side of array **7** defines plural rows, such as rows **9** and **10**. Each element of array **7** represents mounting structure for mounting a discrete capacitor. Conventional PC boards often have an array including at least two rows of structure for mounting capacitors. Each row may have several to tens of array elements for mounting capacitors. The board is designed so that capacitors mounted to the elements of array **7** sufficiently decouple the power to the IC from active circuitry so that the IC and any other coupled circuit elements functions as intended.

[0077] Conventional capacitors are two terminal discrete devices.

[0078] FIG. **1**B shows a portion of board **1**, a source of electrical power **11**, a ground **12**, mounting structure **13** corresponding to one element of array **7**, mounting structure **14** corresponding to another element of array **7**, power plane **15**, and ground plane **16**. In addition, FIG. **1**B shows three vias extend down from each mounting structure element, such as vias **17**, **18**, **19** below mounting structure **13**. Use of more than two vias enables mounting unconventional devices, such as **3** terminal energy conditioners.

[0079] In operation, power source **11** distributes electrical power to circuit elements mounted to board **1** via conductive connection of power source **11** to power plane **15**. Ground plane **16** conductively connects to ground **12**. Vias **17** and **19** conductively connect to power plane **15**. Via **18** does not conductively connect to power plane **15** and instead passes through an aperture in power plane **15** to ground plane **16**. Power plane **15** is above ground plane **16**.

[0080] FIG. **2**A shows assembly **200** including energy conditioner **201** mounted on board **1**. Board **1** includes pads **202**, **203**, **204** that separate conditioner **201** from board surface **6** by a distance **205** as indicated by the distance between facing arrows **206**. Vias **17**, **18**, **19**, have a width **207** as indicated by the distance between facing arrows **209**.

[0081] FIG. **2**B shows additional structure underneath conditioner **201** including additional power, ground, and/or signal planes **208**, **209**, **210**, and aperture **211** through which the conductive path in via **18** passes without shorting to power plane **15**. Additional power, ground and/or signal planes may exist in any particular board.

[0082] In operation, power feed from source **11** through one or more power planes provides power for active circuitry in the IC mounted in region **8** to operate. Conditioners mounted to the elements of array **7**, one conditioner per array element, decouple transients otherwise induced in power due to switching and the like in the active circuitry of the IC.

[0083] FIGS. **3**A to **3**K are perspective views of exterior surfaces **3**A to **3**K of certain novel energy conditioners disclosed herein. In FIGS. **3**A to **3**K, "C" denotes electrically conductive material and "D" denotes dielectric material (electrically insulating). The electrically conductive portions, C, may be referred to herein as bands or outer terminals.

[0084] FIG. **3**A shows conductive bands C, and FIG. **3**G shows conductive bands C, for purpose of discussion with energy conditioner internal structure disclosed herein below.

[0085] FIG. **4**A-**4**O each show one arrangement of conductive elements of mounting structure for mounting a single one of the novel discrete energy conditioners. These arrangements are also referred to as land patterns. The mounting surface may be a surface of a PC board, first level interconnect, or semiconductor chip.

[0086] FIG. **4**A shows an arrangement **4**A of mounting surface structure including a set of three generally rectangularly shaped conductive pads **401**, **402**, **403**. Conductive pads **401**, **402**, **403**, have relatively long sides (unnumbered) and relatively short sides. The relatively short sides are labeled **401**A, **402**A, **403**A. Relatively short sides **401**A, **402**A, **403**A

are aligned with one another such that a straight line segment could contact substantially all of short sides **401**A, **402**A, **403**A. Conductive pad **401** contains vias **401**V**1**, **401**V**2**. Conductive pad **402** contains vias **402**V**1**, **402**V**2**. Conductive pad **403** contains vias **403** V**1**, **403**V**2**. Vias **401** V**1**, **402**V**1**, and **403** V**1** are aligned such that a single line segment could intersect them. Vias **401**V**2**, **402**V**2**, and **403**V**2** are aligned such that a single line segment could intersect them.

[0087] In alternatives to arrangement **4**A, pads may have different sizes, lengths, or widths from one another. For example, pad **402** may be shorter than pads **401**, **403**.

[0088] In another alternative to arrangement **4**A, outer pads **401**, **403** may have a different shape than central pad **402**. For example, outer pads **401**, **403** may include convex central regions and/or flared end regions. For example, outer pads **401**, **403** may be the same length as one another but shorter or longer than central pad **402**.

[0089] In another alternative to arrangement **4**A, certain vias may have a diameter larger than the width or length of the pad to which they are attached such that the via is not entirely contained within the footprint of a conductive pad. For example, a via diameter may be equal to a width of a conductive pad, 1.5, 2, or 3 times a width of the conductive pad.

[0090] In another alternative to arrangement **4**A, certain vias may have different cross-sectional diameters from one. For example, cross-section diameters of vias connecting to the central pad **402** may be ⅓, ½, 1, 1.5, 2, or 3 times the cross-sectional diameter of vias connecting to outer pads **401**, **403**.

[0091] In another alternative to arrangement **4**A, vias **402**V**1**, **402**V**2** may be spaced from one another by more than or less than the spacing between vias **401**V**1**, **401**V**2** and the spacing between **403**V**1**, **403**V**2**.

[0092] In another alternative to arrangement **4**A, each conductive pad may contain one, two, three, or more vias. For example, each conductive pad **401**, **402**, **403** may contain a single via. For example, pads **401** and **403** may contain 2 or 3 vias and pad **402** may contain one via. For example, pads **401** and **403** may contain 1 via and pad **402** may contain 2 or 3 vias.

[0093] In another alternative to arrangement **4**A, the pads may not exist in which case just conductive vias exist in one of the foregoing arrangements. For example, two parallel rows of three vias.

[0094] In another alternative to arrangement **4**A, some pads may have connected vias and some may not. For example, central pad **402** may contain 1, 2, 3, or more vias and outer pads **401**, **403** may contain no vias. For example, central pad **402** may contain no vias and each outer pad **401**, **403**, may contain 1, 2, 3, or more vias.

[0095] In another alternative to arrangement **4**A, the cross-sections of vias may not be circular, such as elliptical, elongated, or irregular.

[0096] FIGS. **4**B-**4**L show various arrangements of the alternatives discussed above.

[0097] FIG. **4**B shows arrangement **4**B of mounting structure having vias of pad **402** more widely spaced from one another than the spacing between vias of either pad **401** or pad **403**.

[0098] FIG. **4**C shows arrangement **4**C of mounting structure having vias having elongated elliptical cross-sections.

[0099] FIG. **4**D shows arrangement **4**D of mounting structure having a single via in each one of pads **401**, **402**, **403**.

[0100] FIG. **4**E shows arrangement **4**E of mounting structure having outer pads **401**, **403** having one centrally located via.

[0101] FIG. **4**F shows arrangement **4**F of mounting structure having pads **401**, **402**, **403** having no vias. In this alternative, conductive lines may radiate along the surface of the structure from each pad.

[0102] FIG. **4**G shows arrangement **4**G of mounting structure having pads **401**, **402**, **403** each having three vias, each via in each pad aligned with one via in each one of the other two pads.

[0103] FIG. **4**H shows arrangement **4**H of mounting structure having a single via in each pad, and in which the central pad **402** is short than the outer pads **401**, **403**.

[0104] FIG. **41** shows arrangement **41** of mounting surface structure having equal length pads **401**, **402**, **403**, and in which the central pad **402** connects to only one via whereas the outer pads **401**, **402** connect to 2 vias.

[0105] FIG. **4**J shows arrangement **4**J of mounting structure having three pairs of vias, and no pads.

[0106] FIG. **4**K shows arrangement **4**K of mounting structure having outer pads **401**, **403** connecting to two vias and central pad **402** connecting to three vias.

[0107] FIG. **4**L shows arrangement **4**L of mounting structure having central pad **402** connecting to one via and outer pads **401**, **403** having no vias.

[0108] FIG. **4**M shows mounting structure **4**M having central pad **402** extending further than pads **401**, **403**, and vias in central pad **402**.

[0109] FIG. **4**N shows mounting structure **4**N having via **501** having a larger diameter than via **502**. Moreover, larger via **501** is more centrally located than the other smaller diameter vias. That is, FIG. **5**N contemplates benefits from conductively filled or lined vias of different dimensions from one another, and in which the larger vias are more centrally located relative to the energy conditioner to which they connect.

[0110] FIG. **4**O shows mounting structure **40** having central pad **402** extending symmetrically further than pads **401**, **403**.

[0111] Preferably, vias in each pad are spaced symmetrically on either side of the center of the pad. Preferably, the arrangement of vias is symmetric about the center point of central pad **402**.

[0112] The inventors contemplate all variations of arrangements of mounting structures (pads and vias combinations, sizes, and shapes) and energy conditioners mounted therein that provide conductive connection between the conductive elements of the mounting structure and A, B, and G master electrodes (defined herein below) internal to the energy conditioner. The A, B, and G master electrodes either have regions forming part of the surface of the energy conditioner or internally physically contact conductive bands (outer electrodes) forming part of the surface of the energy conditioner. Thus, all variations of the conductive band structures and mounting structure that provide suitable connection to the A, B, and G master electrodes are contemplated. In addition, the inventors contemplate all variations of energy conditioners lacking conductive band (outer electrodes) that can be mounted on and soldered (or conductively pasted) to the board thereby conductively connecting the A, B, and G master electrodes to the conductive regions of the mounting structure.

[0113] Herein, conductive integration region, means either a conductive band or equivalent solder providing the contact to tabs of layers of a master electrode thereby conductively integrating those conductive layers to one master electrode. Tabs mean those portions of conductive layers of an internal structure of an energy conditioner that extend to the upper, lower, left or right side surfaces of the internal structure. Main body portions of conductive layers of an internal structure means those portions of the conductive layers that do not extend to the upper, lower, left or right side surfaces of the internal structure.

[0114] Thus, the inventors contemplate all combinations of the mounting structure configurations for mounting a conditioner to a surface and (1) either conductive band configurations or exposed A, B, and G master electrodes surfaces of energy conditioners that provide suitable connections for the A, B, and G master electrodes.

[0115] Some combinations of novel energy conditioner and surface mounting structure provide (1) a first conductive and mechanical contact, such as a solder connection, to at least one and more preferably all conductive bands connected to one side of the A and B master electrodes, (2) a second conductive and mechanical contact, such as a solder contact, to at least one and preferably all conductive bands connected to the opposite side of the A and B master electrodes, and (3) a third conductive contact to at least one and preferably all bands connected to both of the opposite ends of the G master electrode. The foregoing reference to electrical contact includes situations where DC current is blocked, such as where a dielectric cap or layer exists somewhere along a via.

[0116] FIG. **5**A shows geometric values and dimensions for one currently preferred mounting structure.

[0117] FIG. **5**B shows geometric values and dimensions for another currently preferred mounting structure.

[0118] It has been determined by numerical calculations that the values shown in FIGS. **5**A and **5**B provided superior decoupling when 0603 X2Y type energy conditioners are mounted thereto. 0603 X2Y type capacitors have a capacitance of 1 to 100 nano farads, and nominal length, width, and thickness and height of 0.8, 0.6, 0.6, and 0.4 millimeters, respectively, as indicated for example by the URL: http://www.yageo.com/pdf/X2Y_series_10.pdf?5423212=EE8DCCAFD2263EBA74A6443AF7A8BC75&4620207=.

[0119] FIGS. **6**A-**6**B each schematically show a combination of a novel energy conditioner having a certain exterior surface structure in operable location on mounting structure.

[0120] FIG. **6**A shows an arrangement **6**A of energy conditioner **601** on mounting structure **4**A. Conditioner **601** had exterior surface structure **3**A. Conductive band C**1** is on top of conductive pad **401**. Part of conductive band C**2** is on top (since its ends extend beyond) of a first end of conductive pad **402**. Conductive band C**3** is on top of pad **403**. Conductive band C**4** is on top of a second end of conductive pad **402**. The first and second ends of conductive pad **402** are on opposite sides of energy conditioner **601** from one another. Vias and portions of pads hidden from view are shown in dashed lines.

[0121] FIG. **6**B shows arrangement **6**B of energy conditioner **602** mounted on arrangement **4**O of FIG. **4**O. Conditioner **602** also has exterior surface structure **3**A. Conductive band C**1**, C**3** contact near opposite ends of conductive pad **402**. Conductive bands C**4**, C**2** contact respectively to conductive pads **401**, **403**.

[0122] FIG. **6**C shows arrangement **6**C of energy conditioner **603** mounted on mounting structure **4**J showing alignment of conductive bands of conditioner **603**, and also solder, on vias of mounting structure **4**J.

[0123] FIGS. **7-12** show circuits including an energy conditioner having A, B, and G master electrodes, which relate to the special properties of such conditioners. The inventors have determined that connection of the G master electrode at at least two points, preferably at two points on opposite sides from one another, provides significant advantages. This is in spite of the fact that the G master electrode is a single conductive structure wherein location of connection would not be relevant in a lumped circuit representation. Circuit diagrams rely upon a lumped circuit model for accuracy of representation. In order to represent this geometric requirement relating to distributed circuit design in lumped circuit figures, the inventors schematically represent the energy conditioners as devices having at least **3** terminal device, with A, B, G terminals. More terminals may exist for each master electrode, and additional master electrodes may be integrated into the same component. The inventors have also determined that relative locations of A, B, and G electrode terminals relative to the A, B, and G master electrode structures, may affect performance of the energy conditioners. FIG. **7-12** therefore show circuits peculiar to this type of energy conditioner.

[0124] In FIGS. **7-12**, external terminal A conductively connects to the A master electrode, external terminal B conductively connects to the B master electrode, external terminal G**1** conductively connects to the G master electrode. More specifically as used in FIGS. **7-12**, embodiments having at least **2** G external terminals, such as a G**1** and G**2**, a first side of the G master electrode, and external terminal G**2** conductively connects to a different side of the G master electrode.

[0125] FIGS. **7-12** each show conditioner **700**, and external terminals A, B, G**1**, and G**2**. The G master electrodes is represented by portions **702**, **705**, and the A and B master electrodes are represented respective by flat plate elements **703**, **704**. Internal to conditioner **700**, the G master electrode is spaced between or acts to shield the effects of charge buildup on the A master electrode from the B master electrode. This is schematically represented by the portion **702** of the G master electrode extending between the flat plate elements **703**, **704** of the A and B master electrodes. G master electrode portion **705** schematically represents shielding by the G master electrode of the A and B master electrodes relative to space outside conditioner **700**.

[0126] FIG. **7** show a circuit **1** configuration for a conditioner **700** having A, B, and G master electrodes. In circuit one, external terminal A conductively connects to node AS of conductive path S between a source of electrical power, SOURCE, and a load, LOAD. In addition, external terminal B conductively connects to node BR of a return conductive path R between LOAD and SOURCE. In addition, external G**1** and G**2** terminals both conductively connect to a source of ground/constant potential P. Arrows above and below conductive paths between SOURCE and LOAD indicate that current flows in a loop.

[0127] FIG. **8** shows a circuit **2** configuration wherein external terminal A is tied to node AS on path S, external terminal B is tied to node BS also on path S, external terminal G**1** is tied to node G**1**R on path R, and external terminal G**2** is tied to node G**2**R also on path R.

[0128] FIG. **9** shows a circuit **3** configuration wherein external terminal A is tied to node AS on path S, external

terminal B is tied to node BR on path R, external terminal G1 is tied to node G1R on path R, and external terminal G2 is tied to node G2R on path R.

[0129] FIG. **10** shows a circuit **4** configuration wherein external terminal A is tied to a node on path S, and external terminals G1, B, and G2 are tied to nodes on path R.

[0130] FIG. **11** shows a circuit **5** configuration wherein external terminal A is tied to a node on source path Si from a source to a first load, L1, external terminal B is tied to a node S2 on a path from a source to a second load L2, and external terminals G1 and G2 are tied to a common return path CR.

[0131] FIG. **12** shows a circuit **6** configuration wherein external terminal A is tied to a node on path R (see element R in FIG. **7**), external terminal B is tied to a node on path R, and external terminals G1 and G2 are tied to nodes on path S (see element S in FIG. **7**).

Relation of Internal Structure to External Structure of Energy Conditioners

[0132] FIGS. **13-33** generally show structure internal to the external surface **3**A to **3**K of FIGS. **3**A-**3**K. The configuration of conductive layers of FIGS. **13-33** can be arranged relative to the external surfaces **3**A to **3**K so that the conductive layers of the A master electrode contact the same conductive band or bands as one, the conductive layers of the B master electrode contact the same conductive band or bands as one, and the conductive layers of the G master electrode contact the same conductive band or bands as one. Alternatively, instead of conductive bands, solder applied to the sides of the conditioners may conductively contact the conductive layers of the A master electrode to one another, the conductive layers of the B master electrode to one another, and the conductive layers of the G master electrode to one another. The same solder contacts may also contact corresponding conductive regions of the mounting structures shown in FIGS. **4**A to **40**.

[0133] Meaning of "Plate", and Interconnector and IC Alternative Embodiments

[0134] The term "plate" herein generally is used to simplify explanation by defining a combination of a dielectric under layer with none, one, or more than one distinct conductive over layers. However, the relevant structure is the sequence of conductive layers separated by dielectric material. The hidden surface of the structures referred as plates in the following figures represents a dielectric surface; that is, dielectric material vertically separating the defined conductive layers from one another. In discrete energy conditioner component embodiments, the structure are often formed by layering dielectric precursor material (green material) with conductive layer precursor material (conductive paste or the like), firing that layered structure at temperatures sufficient to convert the dielectric precursor to a desired structurally rigid dielectric material and to convert the conductive precursor layer to a high relatively conductivity (low resistivity) conductive layer. However, embodiments formed in interconnects and semiconductor structures would use different techniques, including conventional lithographic techniques, to fabricate equivalent or corresponding structures to those shown in FIGS. **13-25**, **27**, **29**, **31**, and **33**. Importantly, the conductive bands and solder connections for stacked layers discussed herein below would in many cases be replaced by an array of conductively filled or lined vias selectively connecting conductive layers of the same master electrode to one another. Preferably, those vias would be spaced to selectively contact the tab regions of the A, B, and G layers discussed herein.

[0135] Regardless of the mechanism of formation, it is the existence of the master electrodes' morphologies, assembly with external conductive structure, assembly with mounting structure, and integration into circuits **1-6** that are functionally important for decoupling.

[0136] Common Features of Internal Structure of Energy Conditioners

[0137] A master electrode refers to the conductive layers or regions internal to an energy conditioner and the structure internal to the energy conditioner physically contacting those conductive layers or regions so that they form one integral conductive structure.

[0138] Internal structure of energy conditioners includes conductive layers or regions spaces by dielectric material from other conductive layers or regions. The conductive layers or regions each have tab regions that extend to an edge or periphery of the dielectric material. An edge of each tab region of each conductive layer is contacted to external surface conductive structure. The external surface conductive structure may be either conductive bands integral to the discrete energy conditioner or by solder employed also to mount the energy conditioner internal structure to mounting structure. In energy conditioner internal structures having a plurality of conductive layers or regions designed to form a single master electrode, tabs of those conductive layers or regions are vertically aligned in the stack of layers so that a single conductive tab may conductively connect those conductive layers or regions to thereby form a master electrode.

[0139] Alternatively, or in addition to conductive bands or solder connecting to externally exposed edges of conductive layers or regions of a master electrode, conductively filled or lined vias may selectively connect to the same conductive layers or regions.

[0140] Relationship Between Internal Structures of Energy Conditioners and External Structure of Energy Conditioners

[0141] Each one of the internal structures of energy conditioners shown in FIGS. **13-25**, **27**, **29**, **31**, and **33** may reside in each one of external surface **3**A to **3**K of FIGS. **3**A-**3**K in two distinct configurations. In one configuration, a first set of tabs of a G conductive layer of the G master electrode are on the left and right sides (as shown in FIGS. **3**A to **3**K) of the external surfaces **3**A to **3**K. In the other configuration, the same first set of tabs of that same G conductive layer of the G master electrode are on the upper and lower sides (as shown in FIGS. **3**A to **3**K) of the external surfaces **3**A to **3**K. In each configuration of the internal structures of energy conditioners shown in FIGS. **13-25**, **27**, **29**, **31**, and **33** and external surfaces **3**A to **3**K, the conductive layers of the A and B master electrodes each have a region that extends into contact with at least one conductive band (or solder, when solder is applied) of the corresponding one of external surfaces **3**A to **3**K.

[0142] Relationship Between Internal Structures of Energy Conditioners, External Structure of Energy Conditioners, and Circuits **1-6**

[0143] At least in circuits wherein the A and B master electrode are not tied to the same conductive path of the circuit (circuits **1**, **3**, **4**, and **5**; see FIGS. **7-12**), the conductive layer or layers of the A master electrode do not contact the same conductive band on external surfaces **3**A to **3**K as the conductive layer or layers of the B master electrode.

[0144] At least in circuits wherein the A master electrode is not tied to the same conductive path of the circuit as the G master electrode (circuits **1-6**; see FIGS. **7-12**), the conductive layer or layers of the A master electrode do not contact the

same conductive band on external surfaces **3**A to **3**K as the conductive layer or layers of the G master electrode.

[0145] At least in circuits wherein the B master electrode is not tied to the same conductive path of the circuit as the G master electrode (circuits **1**,**2** and **6**; see FIGS. **7**- **12**), the conductive layer or layers of the B master electrode do not contact the same conductive band on external surfaces **3**A to **3**K as the conductive layer or layers of the G master electrode.

[0146] Features Common to Various Internal Structures Shown in FIGS. **13**-**33**.

[0147] FIGS. **13**-**33** all show structures wherein a G master electrode has at least two distinct tabs. As used herein, tab does not require a narrowing or necking compared to a body. Instead, it requires only extension to an edge of a dielectric structure. However, many of the conductive layers of G master electrodes shown in FIGS. **13**-**33** include tab regions that are narrowed or necked compared to the region of the same conductive layer not adjacent the edge of dielectric structure.

[0148] FIGS. **13**-**16**, **21**, **22**, **23** show conductive layers of an A master electrode and conductive layers of a B master electrode that each have only have one distinct tab.

[0149] FIGS. **17**, **18**, **19**, **24**, **25**, **27**, **29**, **31**, and **33** show conductive layers of an A master electrode and conductive layers of a B master electrode that each have two distinct tabs.

[0150] FIGS. **20** shows conductive layers of an A master electrode and conductive layers of a B master electrode that each have three distinct tabs.

[0151] FIGS. **13**, **16**, **17**, **18**, **19**, **20**, **21**, **22**, **23**, and **24** show plates having conductive layers of A and B master electrodes that extend to portions of at least three edges of their plate.

[0152] FIGS. **13**-**25**, **27**, **29**, **31**, and **33** show internal structure of novel energy conditioners.

[0153] FIGS. **28**, **30**, and **32** show external structure of novel energy conditioner embodiments of FIGS. **27**, **29**, and **31**, respectively;

[0154] FIGS. **13**-**25**, **27**, **29**, and **31** show plates that each have a conductive layer of an A master electrode and a conductive layer of a B master electrode in the same plate.

[0155] FIGS. **13**-**24** show stacks of plates that each have a conductive layer of an A master electrode and a conductive layer of a B master electrode in the same plate, and wherein two such plates are mirror images of one another about a line of symmetry extending vertically or horizontally in the plane of the paper of each figure.

[0156] FIGS. **13**-**24** show both (1) structures that each have a conductive layer of an A master electrode and a conductive layer of a B master electrode in the same plate and (2) stacks of plates wherein a conductive layer of an A master electrode on one plate has a region of substantial overlap with a conductive layer of a B master electrode on another plate.

[0157] FIGS. **13**-**24** show structures that include stacks of plates wherein (1) a first plate has a surface including a conductive layer of an A master electrode and a conductive layer of a B master electrode, (2) a second plate also has a surface including a conductive layer of an A master electrode and a conductive layer of a B master electrode, the conductive layer of the A master electrode in the first plate and the conductive layer of the B master electrode in the second plate have a region of substantial overlap, and (3) a third plate resides between the first two plates and has a conductive layer of a G master electrode extending throughout the region of substantial overlap.

[0158] FIGS. **25**, **27**, and stacks **22**A and **22**B of FIG. **22** show structures including only a single plate having a surface including a conductive layer of an A master electrode and a conductive layer of a B master electrode, and a single plate having a surface including a conductive layer of a G master electrode.

[0159] FIGS. **29** and **31** show structures including only a two plate each having a surface including a conductive layer of an A master electrode and a conductive layer of a B master electrode, and a single plate there between having a surface including a conductive layer of a G master electrode.

[0160] FIGS. **21**, **22**, and **23** show structures including at least one plate having a surface including a conductive layer of an A master electrode, a conductive layer of a B master electrode and a conductive layer of a G master electrode between the aforementioned conductive layers of the A and B master electrodes.

[0161] FIGS. **22** stacks **22**E and **22**G, and FIG. **23** stacks **23**A, **23**B, and **23**C each show structures including plates having a substantial region of a conductive layer of an A master electrode opposing a corresponding region of a conductive layer of a B master electrode on another plate having no intervening conductive layer of a G master electrode there between.

[0162] FIGS. **22** stack **22**H and FIG. **23** stack **23**C show structures in which the outermost conductive layers on one or both ends of the stack have a sequence of two or three conductive layers.

[0163] FIG. **33** shows a structure including a stack of plates wherein: (1) each plate has a surface including a conductive layer of only one master electrode, the sequence of conductive layers follows the pattern A, G, B, G, A, G, B; (2) conductive layers of the A and B master electrodes substantially overlap; (3) conductive layers of the G master electrode extend substantially throughout the area of overlap; (4) each conductive layer of the A master electrode has A tabs extends to front and back edges of the corresponding plate; (5) each conductive layer of the B master electrode has B tabs extends to front and back edges of the corresponding plate without overlapping any of the A tabs; and (6) each conductive layer of the G master electrode extends to left and right side edges of the corresponding plate.

[0164] Detailed Description of FIGS. **13**-**33**

[0165] In the following figures, plates of a stack shown displaced horizontally or vertically in the page exist in the stack in the sequence as expanded horizontally or vertically in the page. Each stack includes a top and a bottom spaced from one another in a direction perpendicular to the face of the paper of the figures. In addition, each plate of each stack is shown in the figures as having in the plane of the paper a left side LS, right side RS, upper side US, and lower side LLS.

[0166] FIG. **13** shows stack **1300** of plates **1300**A, **1300**B, and **1300**C. Plate **1300**A includes dielectric material uniformly extending to the LS, RS, US, and LLS of stack **1300**. Conductive layer A**1** designed to be part of the A master electrode and conductive layer B**1** designed to be part of the B master electrode reside on the surface of dielectric material of plate **1300**A. Conductive layers A**1** and B**1** are separated from one another by exposed dielectric surface D. Conductive layer A**1** has a tab A**1** T extending to the entire LS, and also the far left sides of the US and LLS. Conductive layer B**1** has a tab B**1**T extending to the entire RS, and also to the far right sides of the US and LLS. Conductive layer A**1** has a main body portion A**1**M extending the majority of the distance from the LS to the RS on the upper half of plate **1300**A. Conductive

layer B1 has a main body portion B1M extending the majority of the distance from the RS to the LS on the lower half of plate **1300**A.

[0167] Plate **1300**B includes dielectric material on which resides conductive layer G1. Conductive layer G1 has tab G1T1 extending to a central region of the US. Conductive layer G1 has tab G1T2 extending to a central region of the LS. Conductive layer G1 has a main body portion B1M between tabs G1T1 and G1T2.

[0168] Plate **1300**C includes conductive layer A2 for the A master electrode, conductive layer B2 for the B master electrode. Conductive layers A2 and B2 are separated from one another by exposed dielectric surface D. Conductive layer A2 has a tab A2T extending to the entire LS, and also the far left sides of the US and LLS. Conductive layer B2 has a tab B2T extending to the entire RS, and also to the far right sides of the US and LLS. Conductive layer A2 has a main body portion A2M extending the majority of the distance from the LS to the RS on the lower half of plate **1300**A. Conductive layer B2 has a main body portion B2M extending the majority of the distance from the RS to the LS on the upper half of plate **1300**A.

[0169] FIG. **14** schematically shows the stack of layers **1300**C, **1300**B, **1300**A wherein main bodies A1M and B2M have a region of substantial overlap, and main bodies A2 and B1M have a region of substantial overlap, and conductive layer G1M extends over a substantial portion of the regions of overlap. Preferably, the regions of overlap occupy at least 20, more preferably at least 40 and more preferably at least 60 percent of the area of the A1M conductive layer. Preferably, the G1M layer extends over lat least 40, and more preferably at least 60 percent of the areas of overlap.

[0170] The stack of FIGS. **13** and **14**, once formed, may be mounted to mounting structure on a PC board or interconnect, and soldered in place to complete the connections of the A, B, and G master electrodes. Alternatively, the structure of FIGS. **13** and **14** may be fabricated with conductive bands forming a portion of the external structure thereby completing formation of the A, B, and G master electrodes.

[0171] FIGS. **13** and **14** are only exemplary of a sequence of layers forming an energy conditioner using the plates **1300**A, **1300**B, **1300**C. Alternatively to the FIGS. **13** and **14** stack embodiment, a stack may have an integral number of repeats of the sequence **1300**A, **1300**B, **1300**C. Alternatively, a stack may have the sequence **1300**A, **1300**B, **1300**C followed by any integral number of repeats of either the sequence **1300**B, **1300**C or the sequence **1300**A, **1300**B. Alternatively, one, two, or more than two **1300**B plates may reside at either or both of the top and the bottom of a stack.

[0172] FIGS. **15-20** show alternative shapes for conductive layers of A, B, and G master electrodes wherein each plate having an conductive layer for an A master electrode also has a conductive layer for a B master electrode. The same alternatives and methods of assembly just noted for the FIGS. **13** and **14** embodiment apply to the FIGS. **15-20** stack embodiments.

[0173] FIG. **15** shows conductive layer A1M having tab A1T extending over only a portion of LS and over no other side.

[0174] FIG. **16** is identical to FIG. **13**. FIG. **17** shows a stack of plates including plates **1700**A, **1700**B, and **1700**C. Plate **1700**A having conductive layer A1M having tabs A1T1 and A1T2 separated by exposed dielectric D at the center of the LS. Plate **1700**B includes conductive layer of a G master electrode include main body portion G1M, and tab portions G1T1, G1T2, G1T3, and

[0175] G1T4 in each side edge. Plate **1700**C includes conductive layers A2 and B2 for the A and B master electrodes respectively. Tabs of the A1 and A2 plated, the B1 and B2 plates in the stack are vertically aligned. Dielectric surface is exposed at the center of each side of plate **1700**A and **1700**C. The existence of exposed dielectric surfaces vertically aligned in the stack of plates, and existing on each side of the plates having conductive layers for the A and B electrodes, enables the existence of G tabs aligned on each side of the stack to be contacted by a conductive connecting material (conductive band or solder) without shorting the G tabs to the A or B tabs. In one alternative to FIG. **17**, the G1 layer has only two tabs that extend to either the US and LLS or the LS and RS.

[0176] FIG. **18** shows a stack of plates wherein the conductive layers for the A master electrode each have two tabs, and those tabs are not completely aligned with one another. FIG. **18** shows layer A1 and A2 having tabs A1T1 and A2T1 that only partially align at the left side of the US. Similarly the remaining tabs for the A and B layers have partial overlap.

[0177] FIG. **19** shows a stack similar to that shown in FIG. **18** except that extent of the tabs of the A1, B1, A2, and B2 layers is reduced so that the exposed dielectric D extends over the center of the LS and RS, and the G1 layer has four tabs two of which extend to the center of the LS and RS. In one alternative to FIG. **19**, the G1 layer has only two tabs that extend to either the US and LLS or the LS and RS.

[0178] FIG. **20** shows a stack wherein the A1 layer has tabs that extend to portions of the LS, US, and LLS, but not to any corner, and not to the center of the LS. This configuration enables up to three separate conductive connections on the side of the stack to the A layer, and likewise to the B layer, for example with the external structure **3**K's left side and right side conductive bands connecting to the A and B layers.

[0179] FIG. **21** shows a stack **2100** including plates **2100**A, **2100**B, **2100**C, and **2100**D. Each one of plates **2100**A and **2100**C contain conductive layers for the A, B, and G master electrodes separated by dielectric D. Plate **2100**A includes conductive layer A1 that includes tab A1T1 extending over the entire LS and portions of the left end of the US and LLS. Plate **2100**A also includes conductive layer B1 that includes tab B1 extending over the entire RS and portions of the right end of the US and LLS. Between A1 and B1 resides conductive layer G1 that winds between the main body portions of A1 and B1 to tabs G1T1 and G1T2 in the center of the US and LLS. Plate **2100**B includes layer G2 having tabs G2T1 and G2T2 in the center of the US and LLS. Plate **2100**C includes layers A2, B2, and G3, and it is a mirror image of plate **2100**A. Plate **2100**D is identical to plate **2100**B. The stack **2100** has all tabs for the G layers aligned in the center of the US and LLS so that the G layers between A and B layers as well as the G layers above or below A and B layers are integrated into the G master electrode. Alternatively, stack sequences are feasible, including the plate sequence **2100**A, **2100**B, **2100**C, and **2100**D followed or preceded by any number of repetitions of either **2100**C, **2100**D or **2100**A, **2100**B; by including 2 or more of plates of the form of **2100**B/**2100**D instead of single plates, and not including the central G conductive layer in one, or alternating ones of the plates of the form **2100**A/**2100**C, and including one, two, or more plates of the form of **2100**B/**2100**D at one or both ends of the stack.

[0180] FIG. **22** shows stacks, **22**A to **22**H each including additional alternative stacks of the plates **2100**A to **2100**D. Note in particular that stacks **22**A, **22**B, and **22**C have less than 4 plates; one, two, and three plates or layers, respectively.

[0181] FIG. **23** shows stacks **23**A, **23**B, and **23**C which employ the same plates **2100**A, **2100**B, **2100**C, **2100**D as the stack of FIG. **21**. However, FIG. **23**'s sequence differs from the sequences in FIGS. **21** and **22** in that there are adjacent pair **2301** of mirror image layers M, M' where overlap regions of conductive surfaces for A**1** and B**1** layers oppose one another without an intervening conductive layer for the G master electrode, like layers G**2** and G**4** of FIG. **21**. There are also plates where G conductive layers like layers G**2** and G**4** do bracket a layer in which A, B, and G conductive layers reside, like plate **2302**. FIG. **23** shows paired layers M, M'. Alternatively, stack sequences may include any number of repeats of the pair of M, M' adjacent to one another with or without any of the layers having a single G layer, like layers G**2** and G**4** of FIG. **21**. Preferably, there is an odd total number of layers in which conductive layers exist, and an odd total number of layers in which only layers forming part of the G master electrode exist.

[0182] FIG. **24** shows a stack containing plates having various shapes from the preceding embodiments (a top plate having the same conductive pattern as the left side plate in FIG. **18**, a second from top plate having the conductive pattern of G**1** in FIG. **13**, a third plate having the conductive pattern of a plate from FIG. **19**, a fourth plate representing a dielectric spacer region, and a fifth plate like the third plate) showing the plates of different shapes and sizes and of non-uniform spacings may exist in stacks contemplated by the inventors. All such modifications and variations of layers are within the scope contemplated.

[0183] FIGS. **25-28** are views of energy conditioners including conductive layers on only two planes and various external structures.

[0184] FIG. **25** shows stack **25**A containing plate **2500**A and **2500**B. An upper surface of plate **2500**A is formed from surfaces of conductive layer A**1**, conductive layer B**1**, and exposed dielectric material D. An upper surface of plate **2500**B is formed from conductive layer G**1** and exposed dielectric material D. A**1** has tabs A**1**T**1** near the left hand end of the US and A**1**T**2** at near lower left hand end of the LLS. G**1** has tabs G**1**T**1** in the middle of the US and G**1**T**2** in the middle of the LLS. A**1** does not extent to the RS, and B**1** does not extend to the LS. A**1** has main body portion A**1**M. B**1** has main body portion B**1**M. A**1**M extends to a location closer to the US and RS than the LLS and LS. B**1**M extends to a location closer to the LS and LLS than the US and RS.

[0185] FIG. **26** schematically shows an energy conditioner defined by one arrangement of (1) stack **25**A and (2) external structure **3**A of FIG. **3**A. In this arrangement, tabs A**1**T**1** and A**2**T**2** contact internal surfaces of conductive band C**1**, tabs G**1**T**1** and G**1**T**2** respectively contact internal surfaces of bands C**2** and C**4**, and tabs B**1**T**1** and B**1**T**2** contact internal surfaces of conductive band C**3**.

[0186] In one alternative external structure, the third conductive integration structure and the fourth conductive integration structure form a single conductive band around the outer surface of said energy conditioner. The same alternative applies to FIGS. **28**, **30**, and **32**.

[0187] FIG. **27** shows stack **27**A including plates **2500**A and **2700**B. Plate **2700**B differs from plate **2500**B in that the tabs G**1**T**1** and G**1**T**2** of layer G**1** are in the LS and RS as opposed to the US and LLS.

[0188] FIG. **28** schematically shows an energy conditioner defined by one arrangement of (1) stack **27**A and (2) external structure **3**A of FIG. **3**A. Tabs A**1**T**1** and B**1**T**1** contact the internal surface of conductive band C**3**, tabs A**1**T**2** and B**1**T**2** contact the internal surface of conductive band C**1**, tab G**1**T**1** contacts the internal surface of conductive band C**2**, and tab G**1**T**2** contacts the internal surface of conductive band C**4**. In this energy conditioner, the A and B master electrodes are conductively tied together at the edges of the tabs by conductive bands C**1**, C**3**.

[0189] FIGS. **29-32** are views of energy conditioners including conductive layers on three planes and various external structures.

[0190] FIG. **29** shows stack **29**A including plates **2500**A and **2500**B. Stack **29**A also includes another plate **2500**C (not shown) having the same layered pattern as plate **2500**A and on an opposite side of plate **2500**A relative to plate **2500**B. Plate **2500**C has elements A**2**T**1**, A**2**T**2**, B**2**T**1**, B**2**T**2**, A**2**M, and B**2**M aligned with corresponding elements of plate **2500**A. Plate **2500**C has conductive layers A**2** and B**2** having tabs aligned with corresponding tabs of plate **2500**A, including tab A**2**T**1**, A**2**T**2**, B**2**T**1**, and B**2**T**2**. In addition, plate **2500**C has A**1**M and B**1**M as shown in FIG. **25**.

[0191] Alternatively, for FIG. **29**, and stack **29**A, plate **2500**C may be replaced by a plate having a conductive pattern that is a mirror image of the conductive pattern on plate **2500**A, the mirror defined by a vertical line passing through the center of conductive plate **2500**A. In this alternative, conductive tabs A**1**T**1** and A**2**T**2**, for example, are still vertically aligned and conductively connected by contacts to the inner surface of conductive band C**1**. However, in this alternative, A**1**M has a substantial overlap with B**2**M, and A**2**M has a substantial overlap with B**1**M.

[0192] FIG. **30** schematically shows an energy conditioner defined by one arrangement of (1) stack **29**A and (2) external structure **3**A of FIG. **3**A. In this structure, tabs for conductive layers of the same master electrode are aligned in the stack and contact conductive band structure. For example, tabs A**1**T**1** and A**2**T**1** are aligned and contact the internal surface of conductive band C**1**. In an alternative to stack **29**A, discussed above, A**1**M has a substantial overlap with B**2**M, and A**2**M has a substantial overlap with B**1**M. As with other embodiments, additional alternatives stacks include a repeating sequences of the three plates of layers of stack **29**A, and irregular sequences of **2500**A, **2500**B, and **2500**C, and the alternative to **2500**C noted above.

[0193] FIG. **31** shows stack **31**A including plates **2500**A and **2500**B. Stack **31**A also includes a second plate **2500**C having the same layered pattern as plate **2500**A and on an opposite side of plate **2500**A relative to plate **2500**B. Plate **2500**C has conductive layers A**2** and B**2** having tabs aligned with corresponding tabs of plate **2500**A, including tab A**2**T**1**, A**2**T**2**, B**2**T**1**, and B**2**T**2**.

[0194] FIG. **32** schematically shows an energy conditioner defined by one arrangement of (1) stack **31**A and (2) external structure **3**A of FIG. **3**A. In this structure, tabs for conductive layers of the same master electrode are aligned in the stack and contact conductive band structure. For example, tabs A**1**T**1** and A**2**T**1** are aligned and contact the internal surface of conductive band C**1**.

[0195] Alternatively, for FIG. **31**, plate **2500**C may be replaced by a plate having a conductive pattern that is a mirror image of the conductive pattern on plate **2500**A, the mirror defined by a vertical line passing through the center of conductive plate **2500**A. In this alternative, conductive tabs A**1**T**1** and A**2**T**2**, for example, are still vertically aligned and conductively connected by contacts to the inner surface of conductive band C**1**. As with other embodiments, additional alternatives stacks include a repeating sequences of the three plates of layers of stack **29**A, and irregular sequences of **2500**A, **2500**B, and **2500**C, and the alternative to **2500**C noted above.

[0196] FIG. **33** shows stack **33**A including a sequence of plates **3300**A, **3300**B, **3300**C, **3300**B, **3300**A, **3300**B, **3300**C.

[0197] Plates **3300**A each have an upper surface that consists of a surface of conductive layer A**1** and exposed dielectric surface D. Conductive layer A**1** consists of tabs A**1**T**1**, A**1**T**2**, and main body portion AMB. Conductive layer A**1** is part of an A master electrode. Tab A**1**T**1** extends to the US near the LS. Tab A**1**T**2** extends to the LLS near the LS. AMB extends from tabs A**1**T**1** and A**1**T**2** towards the LS. Plates **3300**B each have an upper surface that consists of a surface of conductive layer G**1** and exposed dielectric surface D. Conductive layer G**1** consists of tabs G**1**T**1**, G**1**T**2**, and main body portion GMB. Tab G**1**T**1** extends to the middle of the LS. Tab G**1**T**2** extends to the middle of the RS.

[0198] Plates **3300**C each have an upper surface that consists of a surface of conductive layer B**1** and exposed dielectric surface D. Conductive layer B**1** consists of tabs B**1**T**1**, B**1**T**2**, and main body portion BMB. Conductive layer B**1** is part of a B master electrode. Tab B**1**T**1** extends to the US near the LS. Tab A**1**T**2** extends to the LLS near the LS. AMB extends from both tabs A**1**T**1** and A**1**T**2** towards the center.

[0199] Stack **33**A also shows a dielectric plate having no conductive layers thereon at the top of the stack. The dielectric cover represents the condition that the conductive layers not be shorted to external conductive material, as might happen if they were otherwise uncovered.

[0200] Alternatives to stack **33**A include one or more repetitions of the sequence of plates **3300**A, **3300**B, **3300**C, **3300**B, **3300**A, **3300**B, **3300**C, and one or more repetitions of the sequence of plates **3300**A, **3300**B, **3300**C added to the top or the bottom of the sequence of plates **3300**A, **3300**B, **3300**C, **3300**B, **3300**A, **3300**B, **3300**C.

[0201] Stack **33**A may be assembled in a variety of external structures to provide various connections. In one assembly of stack **33**A and external structure **31** of FIG. **31** results in tabs A**1**T**2** of the A**1** conductive layers in contact with the internal surface of band C**4**, tabs A**1**T**1** in contact with the internal surface of band C**2**, tabs B**1**T**2** in contact with the internal surface of band C**6**, tabs B**1**T**1** in contact with the internal surface of band C**5**, tabs G**1**T**1** in contact with the internal surface of the LS of band C**1**, and tabs G**1**T**2** in contact with the internal surface of the RS of band C**3**.

[0202] In alternatives assemblies, stack **33**A is assembled with either external structure **3**A or **3**G wherein the tabs of the G conductive layer contact internal surfaces of bands C**2** and C**4**. In these alternatives, band C**1** contacts to tabs at opposite ends of contact A conductive layer thereby forming two parallel conductive paths from tab A**1**T**1** to tab A**1**T**2**; one directly between the tabs and the other through the connecting structure of band C**1**. Similarly, two parallel conductive paths are formed from B tabs of the same B layer by band C**3**.

[0203] The foregoing describe embodiments and alternatives within the scope of the novel concepts disclosed herein. The following claims define the scope of protection sought.

We claim:

1. A method for making an energy conditioning structure with stacked, overlapping conductive layers, said method comprising:

providing a plurality of dielectric layers;

providing a plurality of conductive material layers;

placing a first conductive material layer of said plurality of conductive material layers upon a first dielectric layer of said plurality of dielectric layers;

positioning a first electrode of said first conductive material layer in a first position upon said first dielectric layer such that a first electrode main body portion of said first conductive material layer does not extend to any one of a left side surface edge, a right side surface edge, an upper side surface edge, and a lower side surface edge of a first dielectric surface of said first dielectric layer and also that a first electrode tab of said first conductive material layer extends to at least a portion of said left side surface edge of said first dielectric layer but does not extend to said right side surface edge of said first dielectric layer;

positioning a second electrode of said first conductive material layer in a second position upon said first dielectric layer such that a second electrode main body portion of said first conductive material layer does not extend to any one of said left side surface edge, said right side surface edge, said upper side surface edge, and said lower side surface edge of said first dielectric surface of said first dielectric layer and also that a second electrode tab of said first conductive material layer extends to at least a portion of said right side surface edge of said first dielectric layer but does not extend to said left side surface edge of said first dielectric layer;

electrically isolating said first electrode of said first conductive material layer from said second electrode of said first conductive material layer;

placing a second conductive material layer of said plurality of conductive material layers upon a second dielectric layer of said plurality of dielectric layers;

positioning upon said second dielectric layer a single electrode that is contained in said second conductive material layer and contains at least two electrode tabs;

placing a third conductive material layer of said plurality of conductive material layers upon a third dielectric layer of said plurality of dielectric layers;

positioning a first electrode of said third conductive material layer in a first position upon said third dielectric layers such that a first electrode main body portion of said third conductive material layer does not extend to any one of a left side surface edge, a right side surface edge, a upper side surface edge, and a lower side surface edge of a first dielectric surface of said third dielectric layer and also that a first electrode tab of said third conductive material layer extends to at least a portion of said left side surface edge of said third dielectric layer but does not extend to said right side surface edge of said third dielectric layer;

positioning a second electrode of said third conductive material layer in a second position upon said third dielectric layer such that a second electrode main body portion of said third conductive material layer does not

extend to any one of said left side surface edge, said right side surface edge, said upper side surface edge, and said lower side surface edge of said first dielectric surface of said third dielectric layer and also that a second electrode tab of said third conductive material layers extends to at least a portion of said right side surface edge of said third dielectric layer but does not extend to said left side surface edge of said third dielectric layer;

positioning a second electrode of said third conductive material layer in a second position upon said dielectric layer;

electrically isolating said first electrode of said third conductive material layer from said second electrode of said third conductive material layer;

electrically isolating said single electrode of said second conductive material layer from said first and second electrodes of said first conductive material layer;

electrically isolating said single electrode of said second conductive material layer from said first and second electrodes of said third conductive material layer;

stacking said second dielectric layer upon said first conductive material layer of said plurality of conductive material layers and a portion of said first surface of said first dielectric layer;

stacking said third dielectric layer upon said second conductive material layer of said plurality of conductive material layers and a portion of said first surface of said second dielectric layer;

stacking a fourth dielectric layer of said plurality of dielectric layers upon said third conductive material layer of said plurality of conductive material layers and a portion of said first surface of said third dielectric layer;

stacking said second dielectric layer upon said first dielectric layer, stacking said third dielectric layer upon said second dielectric layer, and stacking said fourth dielectric layer upon said third dielectric layer;

positioning a main body portion of said second electrode to completely shield said first electrode main body portion and said second electrode main body portion of said first conductive material layer from said first electrode main body potion and said second electrode main body portion of said third conductive material layer;

positioning said first electrode tab of said first conductive material layer to overlap said first electrode tab of said third conductive material layer;

positioning said second electrode tab of said first conductive material layer to overlap said second electrode tab of said third conductive material layer;

conductively coupling said first electrode tab of said first conductive material layer to said first electrode tab of said third conductive material layer;

conductively coupling said second electrode tab of said first conductive material layer to said second electrode tab of said third conductive material layer;

aligning said first electrode main body portion of said first conductive material layer to overlap said second electrode main body portion of said third conductive material layer; and

aligning said second electrode main body portion of said first conductive material layer to overlap said first electrode main body portion of said third conductive material layer.

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