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(71) Applicant: **NANYANG TECHNOLOGICAL UNIVERSITY** [SG/SG]; 50 Nanyang Avenue, Singapore 639798 (SG).

(72) Inventors: **CHANG, Joseph Sylvester**; c/o Nanyang Technological University, 50 Nanyang Avenue, Singapore 639798 (SG). **GE, Tong**; c/o Nanyang Technological University, 50 Nanyang Avenue, Singapore 639798 (SG). **GUO, Linfei**; c/o Nanyang Technological University, 50 Nanyang Avenue, Singapore 639798 (SG).

(74) Agent: **FOO, Chee Hiong, Ricky**; Marks & Clerk Singapore LLP, Tanjong Pagar, P O Box 636, Singapore 910816 (SG).

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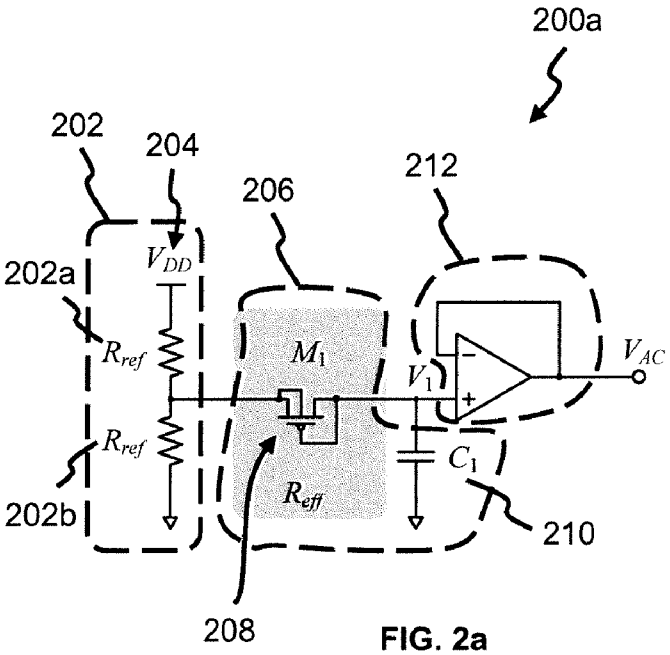

FIG. 2a

(57) Abstract: A voltage reference (200a) is disclosed, which comprises a voltage divider (202) arranged to be coupled to a voltage supply (204); and a filter circuit (206) arranged to be coupled to output of the voltage divider, the filter circuit includes at least one transistor (208) and a capacitive element (210). When in use, the transistor is configured to operate in cut-off mode to enable the filter circuit to function as an RC low-pass filter to attenuate supply noise of the voltage supply, and to enable the filter circuit to generate a reference voltage based on the voltage supply, the reference voltage substantially free of the supply noise.

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Voltage Reference and Self-Oscillating Amplifier Circuit

Field

The present invention relates to a voltage reference, and a self-oscillating amplifier circuit.

Background

- ***Problem 1***

Class D amplifiers (CDAs) are becoming ubiquitous, largely due to their higher power efficiencies compared to their linear counterparts. FIG. 1 shows the schematics 100 of a typical CDA. However, a potential drawback of CDAs is their susceptibility to supply noise, which can be qualified and quantified as Power Supply Rejection Ratio (PSRR) and Power Supply Induced Intermodulation Distortion (PS-IMD). Poor PSRR and PS-IMD may result in undesirable audible noise generated at the output stage and is of particular pertinence when the CDAs are integrated in a system-on-chip (SoC), where the power supply used tends to be fairly noisy. To achieve high quality device performance by the SoC, it is thus imperative that both the PSRR and PS-IMD are high, preferably greater than 100 dB.

To achieve a high PSRR and PS-IMD, particularly for PSRR to be about 100 dB, it is imperative that the AC ground (V_{AC}) used is reasonably clean, i.e. the supply noise is highly attenuated in the AC ground. It is also imperative that V_{AC} is approximately half of the supply voltage, V_{DD}. This is because similar to many other designs (e.g. linear amplifiers), the range of V_{DD} for CDAs is usually high. For instance, low power CDAs (i.e. 2 W rating) are normally designed to operate at a V_{DD} of between 2.5 V to 5.5 V. Any deviation of V_{AC} from $0.5V_{DD}$ will result in reduced dynamic range of the CDA.

Preferably, V_{AC} is to have high supply noise attenuation, and be approximately half V_{DD}. This can be easily achieved if the V_{AC} is generated externally (i.e. off-chip), since a capacitor with large capacitance (e.g. a 1 µF capacitor) can be employed. However, this is not the case when V_{AC} is generated internally (i.e. on-chip). Instead, a bandgap voltage reference (or its variations) has to be used. Although the bandgap voltage reference is virtually supply-noise-free, it is

however largely a fixed voltage (independent of V_{DD}). An alternative is to adopt a voltage divider, which is used to provide an approximately half V_{DD}, but noise attenuation performance of the voltage divider is poor (particularly when the supply noise frequency is low, e.g. 217 Hz).

Other reported methods also include solutions based on a switched capacitor, or a mid-resolution (8-bit) DAC with a counter. Drawbacks of the former method include generating a large voltage droop at the output of the switched capacitor, due to the very low clock rate and presence of leakage current in the switched capacitor (i.e. it is to be noted that this is common in switched capacitor circuits but is usually inconsequential, if the clock rate is reasonably high). The voltage droop can be greater than 100 mV, which may result in degraded Total Harmonic Distortion plus Noise (THD+N) or affect the dynamic range of the CDA. On the other hand, drawbacks of the latter method include observing a situation where $V_{AC} = 0.5V_{DD}$ being true only when V_{DD} increases, but not when V_{DD} reduces. Specifically, when V_{DD} increases from 0 V to 5 V (and the circuit operates at V_{DD} = 5 V thereafter), a V_{AC} = 2.5 V (i.e. half V_{DD}) is generated. However, when V_{DD} reduces from 5 V to 2.5 V (and the circuit operates at V_{DD} = 2.5 V thereafter), V_{AC} cannot be adjusted to the desired 1.25 V (i.e. $0.5V_{DD}$), unless the counter undergoes a reset, hence requiring further hardware to detect V_{DD} changes, and etc. Other drawbacks of both methods also include relatively complex hardware, and high power consumption – these problems are due to embodying the voltage reference generator and switched capacitor circuits in the former method, and then embodying the bandgap voltage reference and DAC in the latter method.

- ***Problem 2***

Modulation techniques commonly used in CDAs include Pulse-Width-Modulation (PWM), Sigma-Delta Modulation, Bang-Bang control modulation, and etc. Amongst said modulation techniques, CDAs based on Bang-Bang control modulation (i.e. Bang-Bang control CDAs) are arguably the most advantageous for low-power power-critical applications. This is because Bang-Bang control CDAs have significantly higher power-efficiency (in part due to hardware simplicity), comparable fidelity (as qualified by THD) and higher noise immunity (as qualified by PSRR). Specifically, it was reported in literature that for certain micro-power applications, the power-efficiency of the Bang-Bang control CDAs is

a high 53%, whilst that of competing and conventional PWM CDAs is substantially lower at 35%, at the nominal operating condition of Modulation Index, M = 0.15 (i.e. 15dB below the maximum due to the crest factor of audio/speech signal). Furthermore, in said reported design, the THD and PSRR of Bang-Bang Control CDAs are respectively 0.08% and 70 dB, whilst the THD and PSRR of the competing PWM CDAs are respectively 0.09% and 45 dB. In short, Bang-Bang control CDAs are arguably the most power-efficient architecture for low-power power-critical applications, and yet featuring comparable or better fidelity than PWM CDAs.

At this juncture, it is to be highlighted that the reported Bang-Bang control CDAs were configured to use the single-ended, or the 2-state Bridge-Tide-Load (BTL) architecture/topology. A major drawback of the single-ended and 2-state BTL Bang-Bang control CDAs however is that an output low-pass filter is required to filter out high frequency carrier components. Using the output low-pass filter is highly undesirable in this case, as the low-pass filter typically occupies more than 70% of the PCB area and adds 30% further costs, thus consequently undesirably substantially increasing the overall form factor and associated costs of the Bang-Bang control CDAs.

In relation, the schematics 500, 520 of the single-ended and 2-state BTL Bang-Bang control CDAs and their output waveforms 510, 530 are respectively depicted in FIGs. 5a to 5d. Briefly, the single-ended and 2-state BTL Bang-Bang control CDAs each comprises a Bang-Bang controller (realized using a hysteresis comparator), an output stage, an *RC* feedback network, a low-pass filter and a (resistive) loudspeaker load.

The operation of the single-ended and 2-state BTL Bang-Bang control CDAs is similar: the *RC* feedback network feeds back the output signal to the Bang-Bang controller. The Bang-Bang controller then controls an error signal (V_{err}) between the input signal and output signal (ideally a replica of the input signal for Gain = 1), and generates digital-like switching signal(s) by comparing V_{err} with the hysteresis band. The output stage provides current to drive the loudspeaker load. The low-pass filter is configured to filter the high frequency switching components and to recover the desired output signal at the loudspeaker load.

Further, it can be seen from FIGs. 5d and 5d that the respective output switching signals of the single-ended and 2-state BTL Bang-Bang control CDAs are effectively 2-state. Specifically, for the single-ended CDA, the output switching signal, V_{SE}, alternates between the two supply rails (i.e. V_{DD} and 0), regardless of the magnitude of the input signal. For the 2-state BTL CDA, the resultant output switching signal, V_{2State_p}-V_{2State_n}, alternates between V_{DD} and -V_{DD}, since two output signals (i.e. V_{2State_p} and V_{2State_n}) are always 180° out-of-phase. It is well-established that in 2-state output signals, the carrier components are large, and hence an output low-pass *LC* filter is thus required to filter these carrier components.

One object of the present invention is therefore to address at least one of the problems of the prior art and/or to provide a choice that is useful in the art.

Summary

According to a 1st aspect, there is provided a voltage reference comprising: a voltage divider arranged to be coupled to a voltage supply; and a filter circuit arranged to be coupled to output of the voltage divider, the filter circuit includes at least one transistor and a capacitive element, wherein in use, the transistor is configured to operate in cut-off mode to enable the filter circuit to function as an RC low-pass filter to attenuate supply noise of the voltage supply, and to enable the filter circuit to generate a reference voltage based on the voltage supply, the reference voltage substantially free of the supply noise.

Advantageously, the disclosed voltage reference employs at least one transistor operating in the cut-off mode to realize a resistor with very high resistance (i.e. greater than 10 GΩ). Consequently, a large *RC* constant can be realized to enable the filter circuit to act as an *RC* low-pass filter, without requiring a large IC/PCB area or incurring high power dissipation.

Preferably, the transistor may be an n-type transistor or a p-type transistor.

Preferably, the capacitive element may include being in a series circuit arrangement with the transistor.

Preferably, the voltage reference may further include a buffer circuit coupled to the filter circuit to receive and store the reference voltage from the filter circuit.

Preferably, the buffer circuit may be an amplifier configured in negative feedback arrangement.

Preferably, the at least one transistor may include at least first and second transistors in a parallel circuit arrangement.

Alternatively, the at least first transistor may include a plurality of transistors in a series circuit arrangement.

Similarly, the at least second transistor may preferably include a plurality of transistors in a series circuit arrangement.

According to a 2nd aspect, there is provided a method of generating a reference voltage using a voltage reference, which includes a voltage divider arranged to be coupled to a voltage supply, and a filter circuit arranged to be coupled to output of the voltage divider, the filter circuit includes at least one transistor and a capacitive element. The method comprises: operating the transistor in cut-off mode to enable the filter circuit to function as an RC low-pass filter to attenuate supply noise of the voltage supply; and generating the reference voltage by the filter circuit based on the voltage supply, the reference voltage substantially free of the supply noise.

According to a 3rd aspect, there is provided a self-oscillating amplifier circuit comprising: a hysteresis controller for receiving a pair of input signals, the controller includes first and second hysteresis comparators to generate first and second output signals; a synchronization module configured to synchronize high frequency carrier components of the first and second hysteresis comparators by providing the first and second output signals as feedbacks to the second and first hysteresis comparators respectively; and first and second output stages respectively coupled to the first and second hysteresis comparators, and configured to generate third and fourth output signals based on the first and second output signals to provide a resultant switching signal for driving a load,

wherein the resultant switching signal alternates between 3-states in dependence of the input signals.

Beneficially, the proposed amplifier circuit does not require usage of an output low-pass filter, because ability to generate the 3-state switching signal means the signal itself has significantly reduced carrier components, thereby eliminating need to include the output low-pass filter.

Preferably, the first and second hysteresis comparators may be configured in a parallel arrangement.

Preferably, the amplifier circuit may further comprise first and second feedback modules arranged to respectively feedback the third and fourth output signals.

Specifically, each feedback module may be in an *RC* network configuration.

Preferably, the third and fourth output signals may include in-phase high frequency components, and out-of-phase low frequency components.

Preferably, the synchronization module may comprise a pair of resistors in parallel circuit arrangement.

Preferably, each output stage may include a driver module coupled to an output module, which includes a pair of transistors.

Preferably, the 3-states may include V_{DD}, 0 V, and $-V_{DD}$.

According to a 4th aspect, there is provided a method of generating a resultant switching signal that alternates between 3-states using a self-oscillating amplifier circuit, which includes a hysteresis controller having first and second hysteresis comparators, a synchronization module, and first and second output stages respectively coupled to the first and second hysteresis comparators. The method comprises: receiving a pair of input signals by the hysteresis controller to enable the first and second hysteresis comparators to generate first and second output signals; providing the first and second output signals as

feedbacks by the synchronization module to the second and first hysteresis comparators respectively to synchronize high frequency carrier components of the first and second hysteresis comparators; and generating third and fourth output signals by the first and second output stages based on the first and second output signals to provide the resultant switching signal for driving a load, wherein the resultant switching signal alternates between the 3-states in dependence of the input signals.

It should be apparent that features relating to one aspect of the invention may also be applicable to the other aspects of the invention.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

Brief Description of the Drawings

Embodiments of the invention are disclosed hereinafter with reference to the accompanying drawings, in which:

FIG. 1 shows the schematics of a typical Class D amplifier (CDA), according to prior art;

FIG. 2a shows the schematics of a voltage reference, according to a first embodiment;

FIGs. 2b to 2f show the respective schematics of voltage references, according to variant embodiments;

FIGs. 3a to 3b show the respective schematics of voltage references, according to further variant embodiments;

FIG. 4 depicts a method of generating a reference voltage using the voltage reference of any of FIGs. 2a-2f, or FIGs. 3a to 3b;

FIG. 5a shows the schematics of a single-ended Bang-Bang control CDA, according to prior art, and FIG. 5b shows output waveforms generated by the single-ended Bang-Bang control CDA;

FIG. 5c is a schematic diagram of a 2-state Bridge-Tied-Load (BTL) Bang-Bang control CDA, according to prior art, and FIG. 5d shows output waveforms generated by the 2-state BTL Bang-Bang control CDA;

FIG. 6 is a block diagram of a self-oscillating amplifier circuit, according to a different embodiment;

FIG. 7a shows the schematics of the amplifier circuit of FIG. 6, and FIG. 7b shows output waveforms generated by the said amplifier circuit;

FIG. 8 shows waveforms generated in the upper branch of a hysteresis controller used in the amplifier circuit of FIG. 6;

FIG. 9 depicts a method of generating a resultant switching signal that alternates between 3-states using the amplifier circuit of FIG. 6;

FIG. 10 is a table showing different sets of circuit parameters adoptable for components in the self-oscillating amplifier circuit of FIG. 6 for purpose of conducting evaluations;

FIG. 11 shows output signal waveform (V_{out_p}-V_{out_n}) corresponding to the resultant switching signal generated; and

FIG. 12 shows results of Total Harmonic Distortion (THD) versus modulation index, M, based upon evaluation of the amplifier circuit of FIG. 6 using the different circuit parameters set out in the table of FIG. 10.

Detailed Description of Preferred Embodiments

- ***A Voltage Reference***

FIG. 2a is a schematic diagram of a first voltage reference 200a, according to a first embodiment. The first voltage reference 200a comprises a voltage divider 202 arranged to be coupled to a voltage supply 204; and a filter circuit 206 arranged to be coupled to output of the voltage divider 202, the filter circuit 206 includes at least one transistor (M_1 or M_2) 208 and a capacitive element (C_1) (e.g. a capacitor, and referred to as such hereinafter) 210. When in use, the transistor 208 is configured to operate in cut-off mode to enable the filter circuit 206 to function as an *RC* low-pass filter to attenuate supply noise of the voltage supply 204, and to enable the filter circuit 206 to generate a reference voltage based on the voltage supply 204, in which the reference voltage is consequently substantially free of the supply noise. The voltage divider 202 comprises two resistors 202a, 202b (R_{ref}) arranged in circuit series, and the transistor 208 is a *p*-type transistor. Then, the capacitor 210 is in a series circuit arrangement with the transistor 208. Also, the first voltage reference 200a optionally includes a buffer circuit 212 coupled to the filter circuit 206 to receive and store the reference voltage from the filter circuit 206. In this case, the buffer circuit 212 is an amplifier configured in negative feedback arrangement. Also, output voltage generated by the buffer circuit 212 is labelled as V_{AC}.

To explain, the transistor 208 is switched on (i.e. in active mode) when a supply voltage (V_{DD}) from the voltage supply 204 increases, e.g. from 0 V to 5 V. The transistor 208 then charges the capacitor 210, and so V_1 (i.e. the voltage across the capacitor 210) and V_{AC} are also increased correspondingly. When V_1 reaches about $0.5V_{DD}$, the transistor 208 turns off (i.e. in cut-off mode) and then functions as a resistor with an effective large resistance (R_{eff}) greater than 10 GΩ. Hence, the transistor 208 and capacitor 210 work in tandem to function as an *RC* low-pass filter to attenuate the supply noise. Depending on configured values of the transistor 208, voltage supply 204 and capacitor 210, the supply noise attenuation at 217 Hz may be greater than 40 dB.

When the supply voltage is reduced from 5 V to 2.5 V (where the first voltage reference 200a operates at 2.5 V thereafter), the transistor 208 remains in the cut-off mode, and the capacitor 210 then discharges at a very low current (e.g. tens of pA or even lower). Hence the first voltage reference 200a takes a longer time (i.e. about 1 s) to reach steady state operation (whose output V_{AC} is about 1.25 V).

FIG. 2b shows schematics of a second voltage reference 200b, according to a second embodiment, and it is to be appreciated that the second voltage reference 200b is entirely similar in configuration to the first voltage reference 200a, except that an *n*-type transistor is now used as the transistor 208.

FIGs. 2c and 2d show respective schematics of third and fourth voltage references 200c, 200d, according to third and fourth embodiments. The third voltage reference 200c is based on the first voltage reference 200a, except that the *p*-type transistor is now configured differently as opposed to that in FIG. 2a. Specifically, in FIG. 2a, the source terminal of the *p*-type transistor M_1 is connected to the voltage divider 204, and the gate and drain terminals are connected to the capacitor 210. But in FIG. 2c, the gate and drain terminals of *p*-type transistor M_2 are connected to the voltage divider 204, whereas the source terminal of M_2 is connected to the capacitor 210. Then, the fourth voltage reference 200d is based on the second voltage reference 200b of FIG. 2b, except that the *n*-type transistor is now configured differently as opposed to that in FIG. 2b. More specifically, in FIG. 2b, the gate and drain terminals of *n*-

type transistor M_1 are connected to the voltage divider 204, while the source terminal of M_1 is connected to the capacitor 210. On the other hand, in FIG. 2d, the source terminal of the *n*-type transistor M_2 is connected to the voltage divider 204, whereas the gate and drain terminals are connected to the capacitor 210. The operations of the third and fourth voltage references 200c, 200d are largely similar to the first and second voltage references 200a, 200b, except that the transistor 208 is in the cut-off region when the supply voltage increases (e.g. from V_{DD} = 0 V to V_{DD} = 5 V and the third and fourth voltage references 200c, 200d respectively operates at V_{DD} = 5 V thereafter) and the transistor 208 is in the above-threshold region when the supply voltage decreases (e.g. from V_{DD} = 5 V to V_{DD} = 2.5 V and the third and fourth voltage references 200c, 200d respectively operates at V_{DD} = 2.5 V thereafter). As a result, the third and fourth voltage references 200c, 200d respectively take a longer time to charge the capacitor 210 for V_1 to reach about $0.5V_{DD}$, but takes a shorter time (e.g. a few µs) to reach steady state operation when the supply voltage decreases. It is to be appreciated that when the third or fourth voltage reference 200c, 200d approaches steady state (i.e. when the voltage from the voltage divider 204 is $0.5V_{DD}$ and the capacitor 210 is $0.5V_{DD} \pm$ the threshold voltage of the transistor 208), the transistor 208 electrically switches to then operate in the cut-off region, hence functioning as a large resistor.

FIGs. 2e and 2f show respective schematics of fifth and sixth voltage references 200e, 200f, according to fifth and sixth embodiments. The fifth voltage reference 200e is based on the first voltage reference 200a and the third voltage reference 200c, except that two *p*-type transistors in parallel circuit arrangement now replace the single *p*-type transistor used in FIG. 2a and FIG. 2c. This configuration ensures that the fifth voltage reference 200e takes a shorter time to reach steady state operation, when the supply voltage increases and decreases. Similarly, the sixth voltage reference 200f is based on the second voltage reference 200b and the fourth voltage reference 200d, except that two *n*-type transistors in parallel circuit arrangement now replace the single *n*-type transistor used as shown in FIG. 2b and FIG.2d.

Separately, it is to be highlighted that one potential drawback of the voltage references 200a-200f in FIGs. 2a to 2f is that the disclosed voltage references

200a-200f are able to provide high supply noise attenuation, only when the supply noise on the supply voltage is smaller than 2x of the threshold voltage of the transistor(s) 208. When the supply noise is larger than 2x of the threshold voltage, the transistor(s) 208 will then turn on, and hence the supply noise will undesirably appear at V_{AC}. This is usually inconsequential for designs intended for low power applications, as the supply noise is usually smaller than 200 mV and is substantially lower than 2x of the threshold voltage (e.g. 0.5 V) of the transistor(s) 208. But in cases when the supply noise on the supply voltage is potentially higher than 2x of the threshold voltage, two or more transistors can beneficially be connected in circuit series to provide increased supply variation tolerance, as depicted in seventh and eighth voltage references 300, 350, based on seventh and eighth embodiments (see FIGs. 3a and 3b). Simply, the seventh voltage reference 300 only differs from the first voltage reference 200a, in that the two separate rows of *p*-type transistors, each row in series circuit arrangement, are adopted as a configuration for the transistor 208, and more specifically, the two rows of *p*-type transistors are in parallel circuit arrangement to each other. Then, the eighth voltage reference 350 is largely similar to the seventh voltage reference 300, except that *n*-type transistors replace all the *p*-type transistors. In this fashion, the supply noise can be tolerated up to $2n$x of the threshold voltage, where n is the number of (*p*-type/*n*-type) transistors within the series circuit arrangement of each row.

Referring to FIG. 4, there is disclosed a method 400 of generating the reference voltage, using the voltage reference 200a-200f, 300, 350, in which the method 400 comprises: at step 402, operating the transistor(s) 208 in cut-off mode to enable the filter circuit 206 to function as an *RC* low-pass filter to attenuate supply noise of the voltage supply 204; and at step 404, generating the reference voltage by the filter circuit 206 based on the voltage supply, in which the reference voltage is substantially free of the supply noise.

Hence, the proposed voltage references 200a-200f, 300, 350 address drawbacks of conventional voltage references, and have the following advantages: (i). simple hardware, (ii). negligible power dissipation, (iii). no voltage droop, and (iv). ability to track the supply voltage, when the supply voltage increases or decreases.

In summary, the proposed voltage references 200a-200f, 300, 350 employ at least one transistor 208 (or a plurality of transistors) operating in the cut-off mode to realize a resistor with very high resistance (i.e. greater than 10 GΩ). As a result, a large *RC* constant (and hence a low cut-off frequency of smaller than 10 Hz, with high noise attenuation (e.g. at 217Hz)) is realized, without requiring a large IC/PCB area or incurring high power dissipation. The proposed voltage references 200a-200f, 300, 350 may usefully find usage in Class D amplifiers, or other suitable applications.

- ***A Self-Oscillating Amplifier Circuit***

With reference to FIG. 6, a block diagram of a self-oscillating amplifier circuit 600 (also known as a 3-state Filter-less Bang-Bang Control CDA) is depicted, according to a different embodiment. In relation, FIG. 7a shows schematics of the amplifier circuit 600 and FIG. 7b shows output waveforms 700 generated by the amplifier circuit 600. Broadly, the amplifier circuit 600 comprises a hysteresis controller 602 (also known as a Bang-Bang controller) for receiving a pair of input signals (provided by first and second input modules 604a, 604b as V_{in}, V_{ip} respectively – see FIG. 7a), the controller 602 includes first and second hysteresis comparators 606a, 606b to generate first and second output signals; a synchronization module 608 configured to synchronize high frequency carrier components of the first and second hysteresis comparators 606a, 606b by providing the first and second output signals as feedbacks to the second and first hysteresis comparators 606a, 606b respectively; and first and second output stages 610a, 610b respectively coupled to the first and second hysteresis comparators 606a, 606b, and configured to generate third and fourth output signals based on the first and second output signals to provide a resultant switching signal for driving a load 612 (e.g. a loudspeaker). The third and fourth output signals (i.e. V_{out_p}, V_{out_n}) share in-phase high frequency components, and out-of-phase low frequency components. It is to be appreciated that synchronizing the high frequency carrier components of the first and second hysteresis comparators 606a, 606b by the synchronization module 608 specifically means synchronizing the high frequency carrier components in the first and second output signals generated by the first and second hysteresis comparators 606a, 606b.

The resultant switching signal alternates between 3-states (i.e. V_{DD}, 0 V, and $-V_{DD}$) in dependence of the input signals. That is, when the resultant input signal, V_{ip}-V_{in}, is positive, the generated switching signal, V_{out_p}-V_{out_n}, alternates between V_{DD} and 0. But when the resultant input signal, V_{ip}-V_{in}, is negative, the generated switching signal, V_{out_p}-V_{out_n}, then alternates between 0 and -V_{DD}. An advantage of the 3-state switching signal is having significantly reduced carrier components, thereby eliminating need to include an output low-pass filter in the proposed amplifier circuit 600.

Moreover, it is to be appreciated that the third and fourth output signals are further arranged to be feedback to the first and second hysteresis comparators 606a, 606b respectively, via first and second feedback modules 614a, 614b respectively. Each feedback module 614a, 614b is arranged in an *RC* network configuration. More specifically, the first feedback module 614a, which is coupled to the negative input terminal of the first hysteresis comparator 606a, comprises a feedback resistor R_{fb1} arranged in parallel with another feedback resistor R_{in1} and a capacitor C_{fb1}. Similarly, the second feedback module 614b, which is coupled to the negative input terminal of the second hysteresis comparator 606b, comprises a feedback resistor R_{fb2} arranged in parallel with another feedback resistor R_{in2} and a capacitor C_{fb2}.

Further, it is to be appreciated that the first and second hysteresis comparators 606a, 606b are configured in a parallel arrangement, and also that the controller 602 also includes four feedback resistors (i.e. labelled as R_{h11}, R_{h21}, R_{h12} and R_{h22} in FIG. 7a), where R_{h11}, R_{h21} are arranged at the first hysteresis comparator 606a, and R_{h12} and R_{h22} are arranged at the second hysteresis comparator 606b. Particularly, R_{h11}, R_{h21} and the first hysteresis comparator 606a forms the upper branch of the controller 602, whereas R_{h12} and R_{h22} and the second hysteresis comparator 606b then forms the lower branch of the controller 602. The synchronization module 608 includes a pair of resistors (i.e. labelled as R_{h31} and R_{h32} in FIG. 7a) in parallel circuit arrangement. Then, each output stage 610a, 610b includes a driver module 614a, 616a coupled to an output module 614b, 616b (which is in the form of a pair of transistors in parallel circuit arrangement).

For the amplifier circuit 600, the hysteresis (V_h) of the controller 602 is generated by the feedback resistors, R_{h11}, R_{h21}, R_{h12} and R_{h22}, and the synchronization module 608. The synchronization module 608 feeds back the output signal of the opposing branch of the controller 602 as inputs to the controller 602, and synchronizes the high frequency carrier components of the two branches of the controller 602, thereby generating the 3-state switching signal by comparing the error signal (V_{err1} and V_{err2}) with the hysteresis band (V_{h1}^-, V_{h1}^+, V_{h2}^-, V_{h2}^+) of the first and second hysteresis comparators 606a, 606b. The nomenclatures V_{h1}^- and V_{h1}^+ are the hysteresis bands of the first hysteresis comparator 606a; V_{h1}^- is the lower limit and V_{h1}^+ is the upper limit; and V_{h2}^- and V_{h2}^+ are the hysteresis bands of the second hysteresis comparator 606b. FIG. 8 shows waveforms 800 generated in the upper branch of the controller 602. For completeness, it is worth noting that in the reported single-ended and 2-state BTL Bang-Bang control CDAs, the synchronization module 608 is absent.

Consequent to the function of the synchronization module 608, the high frequency carrier components of the third and fourth output signals, V_{out_p} and V_{out_n}, are in-phase, whereas the low frequency audio components are out-of-phase. Put simply, the resultant switching signal is 3-state (i.e. see FIG. 7b).

On the basis of FIG. 7a and adopting a derived analytical methodology disclosed in a journal paper: "T. Ge and J. S. Chang, "Bang-Bang Control Class-D Amplifiers: Power-Supply Noise," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 55, pp. 723-727, 2008", the 'on' and 'off' period, t_{on} and t_{off}, can be derived as follows: t_{on} is the period when $V_M = V_{DD}$, and t_{off} is the period when $V_M = -V_{DD}$. By straightforward analysis, it can be shown that t_{on1} and t_{off1} respectively (as shown in FIG. 8), which are the 'on' and 'off' periods for the upper branch of the controller 602 can be derived as follows:

By application of Kirchhoff's Current Law,

$$\frac{V_{in} - V_{err1}}{R_{in1}} + \frac{V_{out\_p} - V_{err1}}{R_{fb1}} = C_{fb1}\frac{dV_{err1}}{dt} \qquad (1)$$

By re-arranging and integration,

$$\int \frac{dt}{R_{e1}C_{fb1}} = \int \frac{dV_{err1}}{\frac{R_{in1}}{R_{in1}+R_{fb1}}V_{out\_p} + \frac{R_{fb1}}{R_{in1}+R_{fb1}}V_{in} - V_{err1}} \quad (2)$$

wherein $R_{e1} = R_{in1}//R_{fb1}$ is the equivalent resistance of R_{in1} and R_{fb1} in parallel.

Hence,

$$e^{-\frac{t}{R_{e1}C_{fb1}}} * const = mV_{out\_p} + (1-m)V_{in} - V_{err1} \quad (3)$$

wherein $m = \frac{R_{in1}}{R_{in1}+R_{fb1}}$ is the resistance ratio.

During $t_1 \rightarrow t_2$, which is the 'on' period t_{on1} based on the waveform 800 depicted in FIG. 8, the error signal V_{err1} can be derived as follows:

At $t = t_1$,

$$V_{err1} = V_{h1}^-$$

At $t = t_2$,

$$V_{err1} = V_{h1}^+$$

Hence, *const* in equation (3) and t_{on1} and t_{off1} can be derived as:

$$const = mV_{DD} + (1-m)V_{in} - V_{h1}^- \quad (4)$$

$$t_{on1} = R_{e1}C_{fb1}\ln\left[\frac{mV_{DD} + (1-m)V_{in} - V_{h1}^-}{mV_{DD} + (1-m)V_{in} - V_{h1}^+}\right] \quad (5)$$

$$t_{off1} = R_{e1}C_{fb1}\ln\left[\frac{mV_{DD} - (1-m)V_{in} + V_{h1}^+}{mV_{DD} - (1-m)V_{in} + V_{h1}^-}\right] \quad (6)$$

Similarly, t_{on2} and t_{off2}, the 'on' and 'off' period of the lower branch of the controller 602, can be derived as:

$$t_{on2} = R_{s2}C_{fb2}\ln\left[\frac{mV_{DD} + (1-m)V_{ip} - V_{h2}^{-}}{mV_{DD} + (1-m)V_{ip} - V_{h2}^{+}}\right] \quad (7)$$

$$t_{off2} = R_{s2}C_{fb2}\ln\left[\frac{mV_{DD} - (1-m)V_{ip} + V_{h2}^{+}}{mV_{DD} - (1-m)V_{ip} + V_{h2}^{-}}\right] \quad (8)$$

wherein,

$$V_{h1}^{+} = \frac{R_{h11}}{R_{h11} + R_{h21}}V_{DD} + \frac{R_{h11}}{R_{h11} + R_{h31}}V_{M2} \quad (9)$$

$$V_{h1}^{-} = -\frac{R_{h11}}{R_{h11} + R_{h21}}V_{DD} + \frac{R_{h11}}{R_{h11} + R_{h31}}V_{M2} \quad (10)$$

$$V_{h2}^{+} = \frac{R_{h12}}{R_{h12} + R_{h22}}V_{DD} + \frac{R_{h12}}{R_{h12} + R_{h32}}V_{M1} \quad (11)$$

$$V_{h2}^{-} = -\frac{R_{h12}}{R_{h12} + R_{h22}}V_{DD} + \frac{R_{h12}}{R_{h12} + R_{h32}}V_{M1} \quad (12)$$

From equations (9) to (12), it can be noted that the hysteresis band of the controller 602 is determined by the feedback resistors, R_{h11}, R_{h21}, R_{h12} and R_{h22}, and the synchronization module 608. As mentioned, the synchronization module 608 synchronizes the high frequency carrier components by feeding the output signal of the opposing branch back to the controller 602. Hence, this feedback mechanism forces the synchronization of the signals at the two branches of the controller 602.

Based on the equations (5) to (8) and by using Taylor Series, when the input signal is 0, the idle switching frequency, f_{sw} can be easily derived as:

$$f_{sw} = \frac{mV_{DD}}{2R_sC_{fb}V_h} \quad (13)$$

wherein R_e and C_{fb} are the designed values of R_{e1} (or R_{e2}), C_{fb1} (or C_{fb2}), respectively. V_h is the average value of V_{h1}^+ and V_{h2}^+ (or $-V_{h1}^-$ and $-V_{h2}^-$).

So, with reference to FIG. 9, a method 900 of generating the resultant switching signal using the proposed amplifier circuit 600, comprises: at step 902, receiving the pair of input signals by the hysteresis controller 602 to enable the first and second hysteresis comparators 606a, 606b to generate the first and second output signals; at step 904, providing the first and second output signals as feedbacks by the synchronization module 608 to the second and first hysteresis comparators 606a, 606b respectively to synchronize high frequency carrier components of the first and second hysteresis comparators 606a, 606b; and generating third and fourth output signals by the first and second output stages 610a, 610b based on the first and second output signals to provide the resultant switching signal for driving a load, and feedback the third and fourth output signals to the first and second hysteresis comparators 606a, 606b respectively, wherein the resultant switching signal alternates between the 3-states in dependence of the input signals.

- ***Results and Verification***

The proposed amplifier circuit 600 is evaluated by simulations using software from Cadence™ based on a commercial 65 nm CMOS process. Different sets of circuit parameters for simulating four cases (i.e. Cases 1, 2, 3 and 4) of feedback and synchronization module block 608 designs of the amplifier circuit 600 are set out in a table 1000 depicted in FIG. 10 – the intention is to ascertain the important parameters thereto. Also, the input frequency f_{in} used is 2 kHz and supply voltage V_{DD} is 3.6 V.

FIG. 11 shows output signal waveform 1100 (V_{out_p}-V_{out_n}) corresponding to the resultant switching signal generated (based on Case 1 in the table 1000 of FIG. 10, M = 0.7), and as expected, the output obtained indeed is that of a filter-less 3-state Bang-Bang control CDA.

FIG. 12 shows evaluation results 1200 of Total Harmonic Distortion (THD) versus modulation index, M, of the amplifier circuit 600 for the four cases of circuit parameters provided in the table 1000 of FIG. 10. It can be seen from

FIG. 12 that unlike conventional PWM and Sigma-Delta CDAs, the THD of the proposed amplifier circuit 600 increases with decreasing *M*. The comparison between Case 1 and Case 2 (or Case 3 and Case 4) shows that a lower hysteresis band results in a lower THD. The comparison between Case 1 and Case 3 (or Case 2 and Case 4) shows that a smaller value of C_{fb1} and C_{fb2} results in reduced THD. This is somewhat expected, because with a lower hysteresis band and a smaller value of C_{fb1} and C_{fb2}, the proposed amplifier circuit 600 switches at a higher frequency (i.e. refer to equation (13)), but at the cost of higher switching power loss at the output stages 610a, 610b.

Although the THD performance is somewhat compromised in all four cases – the best being Case 1, the THD obtained is usually sufficient for a number of low-power power-critical applications. For example, as the signal-to-noise ratio/dynamic range of a sub-miniature loudspeaker in many wearable devices is smaller or equal to 40 dB, a THD of about 1 % is usually acceptable – particularly in view of the requirement of much desired hardware simplicity (with accompanying high power-efficiency).

In summary, the proposed amplifier circuit 600 is the first-ever filter-less 3-state Bang-Bang control CDA where an output low-pass filter (typically bulky in terms of PCB area needed, and also costly to make) is not required. Compared to the the single-ended and 2-state counterpart Bang-Bang control CDAs, the proposed amplifier circuit 600 features the simplest hardware (and highest power-efficiency), but with somewhat compromised fidelity. Nevertheless, the reduced fidelity is deemed sufficient for most ultra-low-power or power-critical applications such as in low-to-mid performance wearable devices, hearing aid devices, and the like.

While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary, and not restrictive; the invention is not limited to the disclosed embodiments. Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practising the claimed invention.

For example, with reference to FIG. 6, the first and second feedback modules 614a, 614b can be optional in certain variant embodiments, and so there is therefore no feedback of the third and fourth output signals back to the first and second hysteresis comparators 606a, 606b for those cases.

Claims

1. A voltage reference comprising:

a voltage divider arranged to be coupled to a voltage supply; and

a filter circuit arranged to be coupled to output of the voltage divider, the filter circuit includes at least one transistor and a capacitive element,

wherein in use, the transistor is configured to operate in cut-off mode to enable the filter circuit to function as an RC low-pass filter to attenuate supply noise of the voltage supply, and to enable the filter circuit to generate a reference voltage based on the voltage supply, the reference voltage substantially free of the supply noise.

2. The voltage reference of claim 1, wherein the transistor is an n-type transistor or a p-type transistor.

3. The voltage reference of any preceding claims, wherein the capacitive element includes being in a series circuit arrangement with the transistor.

4. The voltage reference of any preceding claims, further includes a buffer circuit coupled to the filter circuit to receive and store the reference voltage from the filter circuit.

5. The voltage reference of claim 4, wherein the buffer circuit is an amplifier configured in negative feedback arrangement.

6. The voltage reference of any preceding claims, wherein the at least one transistor includes at least first and second transistors in a parallel circuit arrangement.

7. The voltage reference of claim 6, wherein the at least first transistor includes a plurality of transistors in a series circuit arrangement.

8. The voltage reference of claim 6, wherein the at least second transistor includes a plurality of transistors in a series circuit arrangement.

9. A method of generating a reference voltage using a voltage reference, which includes a voltage divider arranged to be coupled to a voltage supply, and a filter circuit arranged to be coupled to output of the voltage divider, the filter circuit includes at least one transistor and a capacitive element, the method comprises:

operating the transistor in cut-off mode to enable the filter circuit to function as an RC low-pass filter to attenuate supply noise of the voltage supply; and

generating the reference voltage by the filter circuit based on the voltage supply, the reference voltage substantially free of the supply noise.

10. A self-oscillating amplifier circuit comprising:

a hysteresis controller for receiving a pair of input signals, the controller includes first and second hysteresis comparators to generate first and second output signals;

a synchronization module configured to synchronize high frequency carrier components of the first and second hysteresis comparators by providing the first and second output signals as feedbacks to the second and first hysteresis comparators respectively; and

first and second output stages respectively coupled to the first and second hysteresis comparators, and configured to generate third and fourth output signals based on the first and second output signals to provide a resultant switching signal for driving a load,

wherein the resultant switching signal alternates between 3-states in dependence of the input signals.

11. The amplifier circuit of claim 10, wherein the first and second hysteresis comparators are configured in a parallel arrangement.

12. The amplifier circuit of any of claims 10-11, further comprising first and second feedback modules arranged to respectively feedback the third and fourth output signals.

13. The amplifier circuit of claim 12, wherein each feedback module is in an *RC* network configuration.

14. The amplifier circuit of any of claims 10-13, wherein the third and fourth output signals include in-phase high frequency components, and out-of-phase low frequency components.

15. The amplifier circuit of any of claims 10-14, wherein the synchronization module comprises a pair of resistors in parallel circuit arrangement.

16. The amplifier circuit of any of claims 10-15, wherein each output stage includes a driver module coupled to an output module, which includes a pair of transistors.

17. The amplifier circuit of any of claims 10-16, wherein the 3-states include V_{DD}, 0 V, and $-V_{DD}$.

18. A method of generating a resultant switching signal that alternates between 3-states using a self-oscillating amplifier circuit, which includes a hysteresis controller having first and second hysteresis comparators, a synchronization module, and first and second output stages respectively coupled to the first and second hysteresis comparators, the method comprises:

receiving a pair of input signals by the hysteresis controller to enable the first and second hysteresis comparators to generate first and second output signals;

providing the first and second output signals as feedbacks by the synchronization module to the second and first hysteresis comparators respectively to synchronize high frequency carrier components of the first and second hysteresis comparators; and

generating third and fourth output signals by the first and second output stages based on the first and second output signals to provide the resultant switching signal for driving a load,

wherein the resultant switching signal alternates between the 3-states in dependence of the input signals.

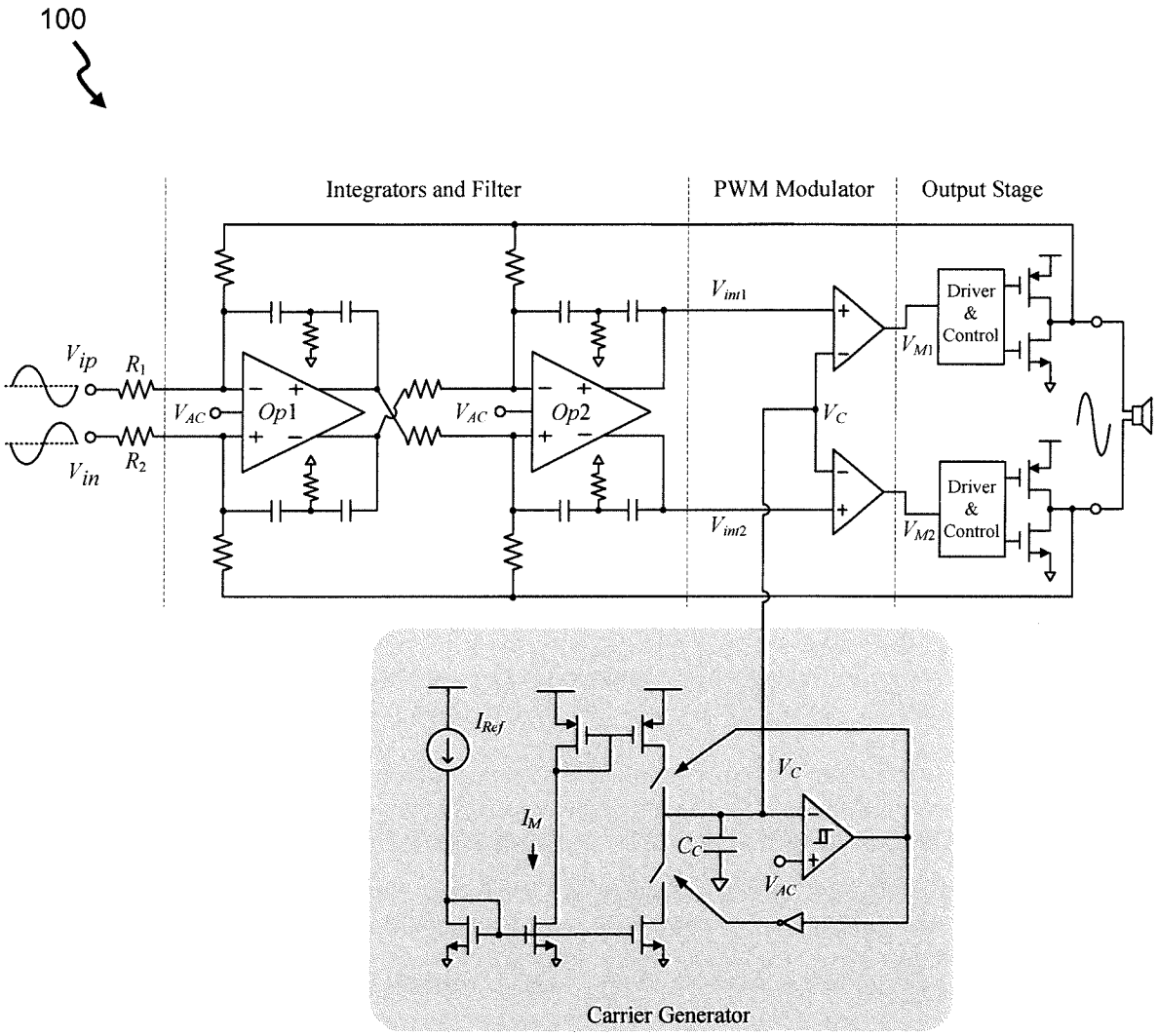

FIG. 1 (Prior Art)

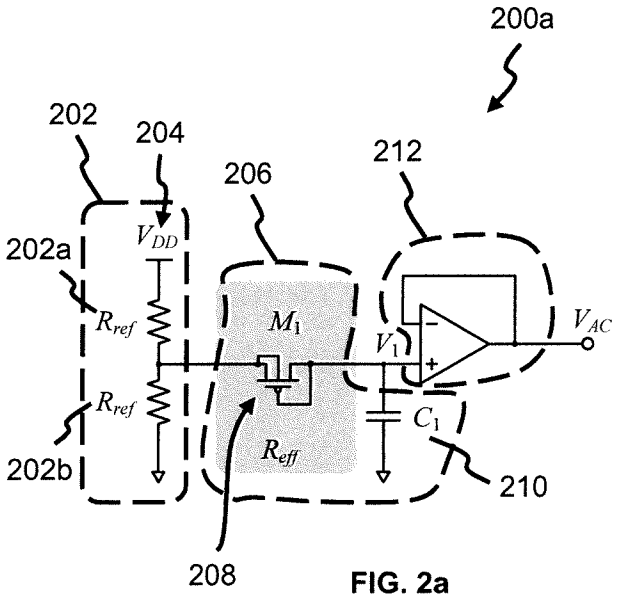

FIG. 2a

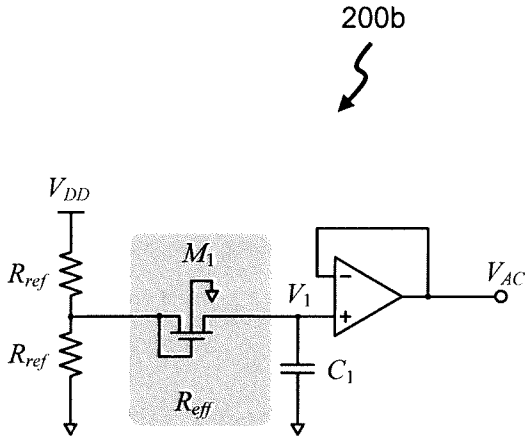

FIG. 2b

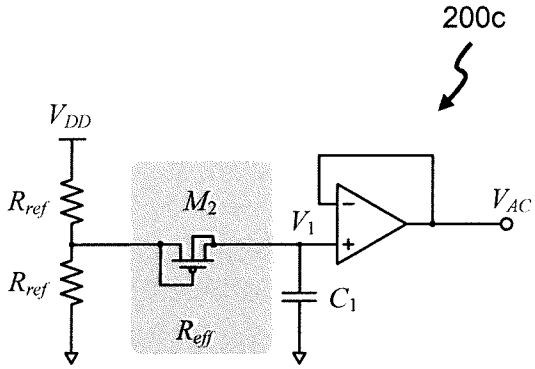

FIG. 2c

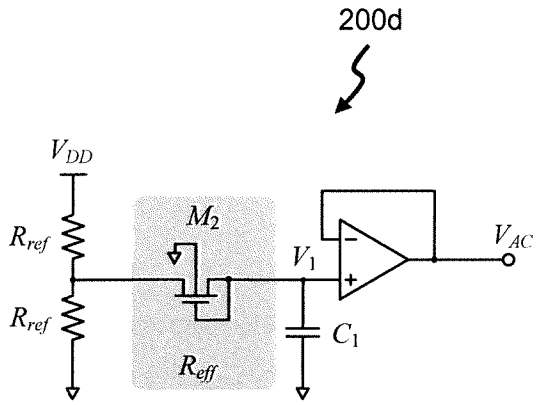

FIG. 2d

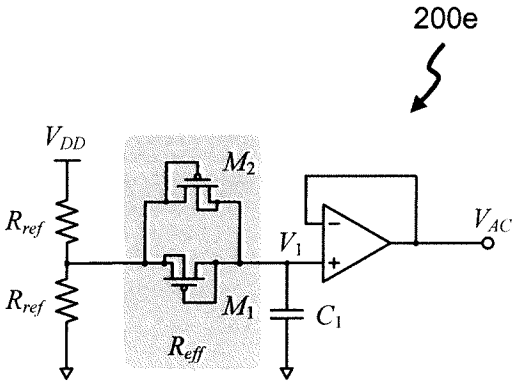

FIG. 2e

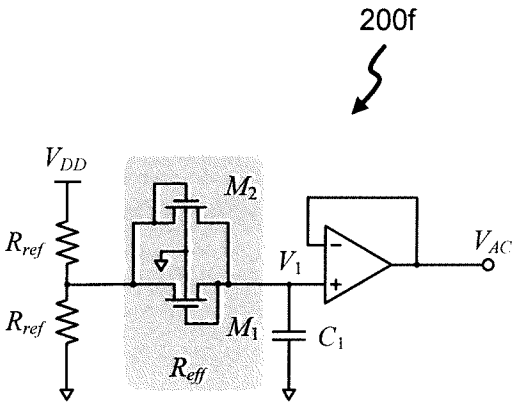

FIG. 2f

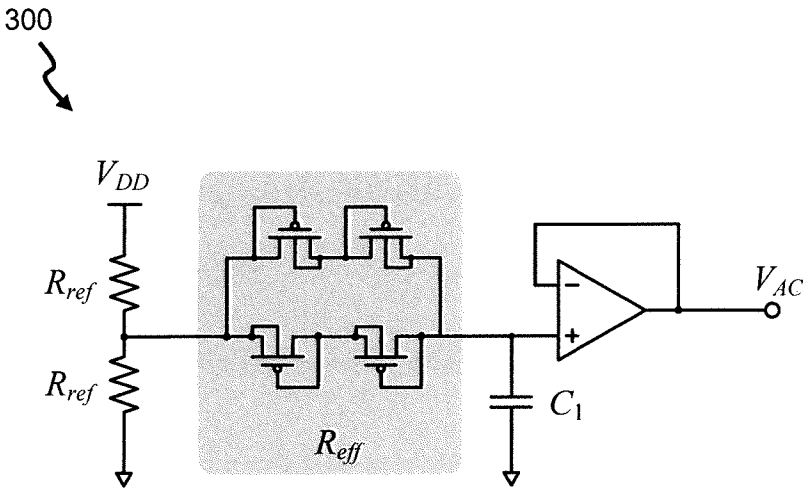

FIG. 3a

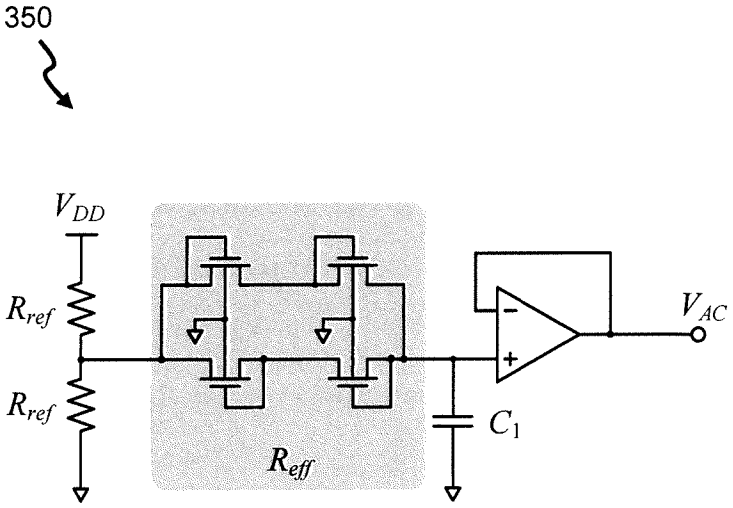

FIG. 3b

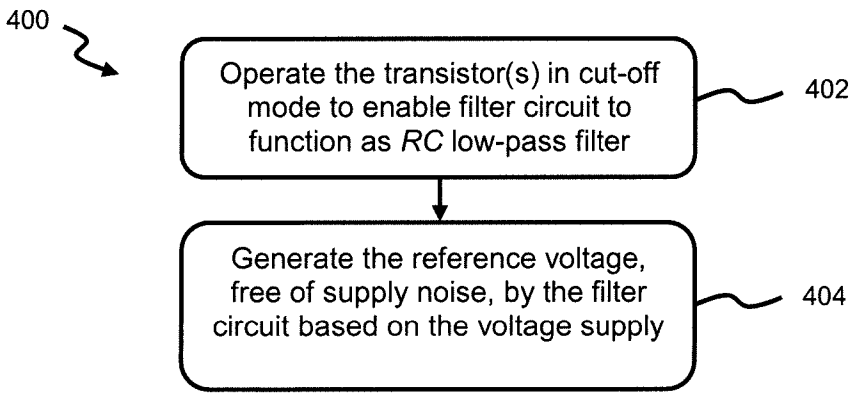
400
Operate the transistor(s) in cut-off mode to enable filter circuit to function as *RC* low-pass filter
402
Generate the reference voltage, free of supply noise, by the filter circuit based on the voltage supply
404

FIG. 4

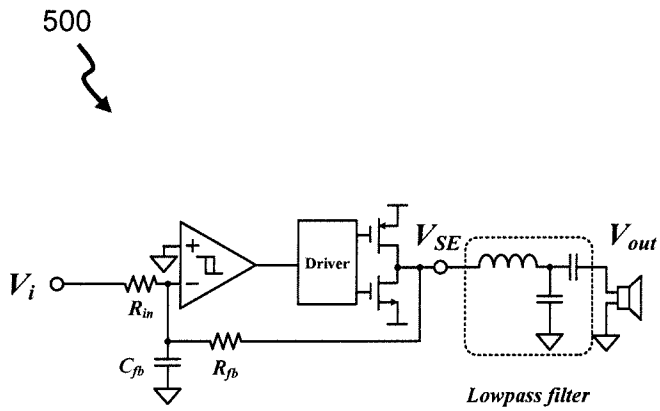

FIG. 5a (Prior Art)

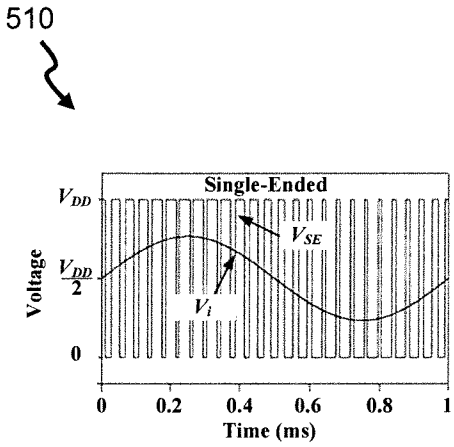

FIG. 5b (Prior Art)

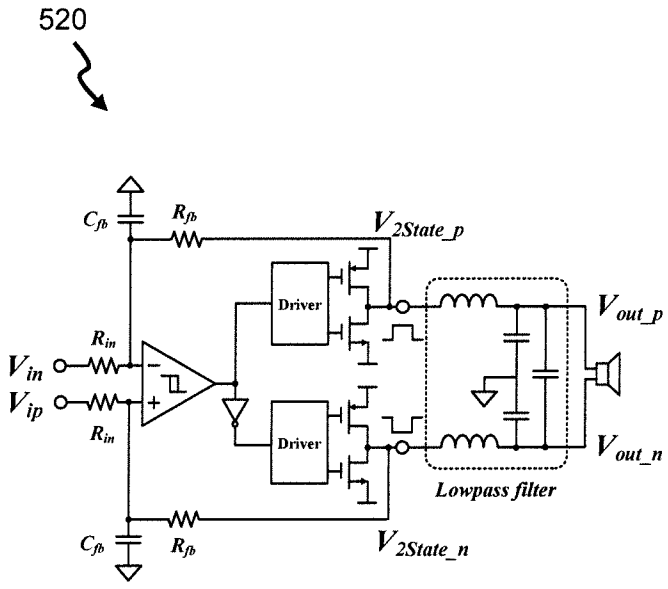

FIG. 5c (Prior Art)

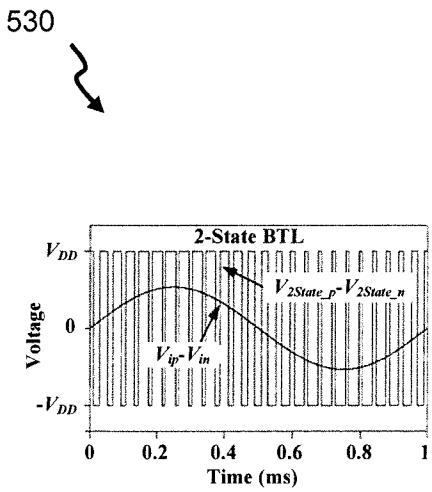

FIG. 5d (Prior Art)

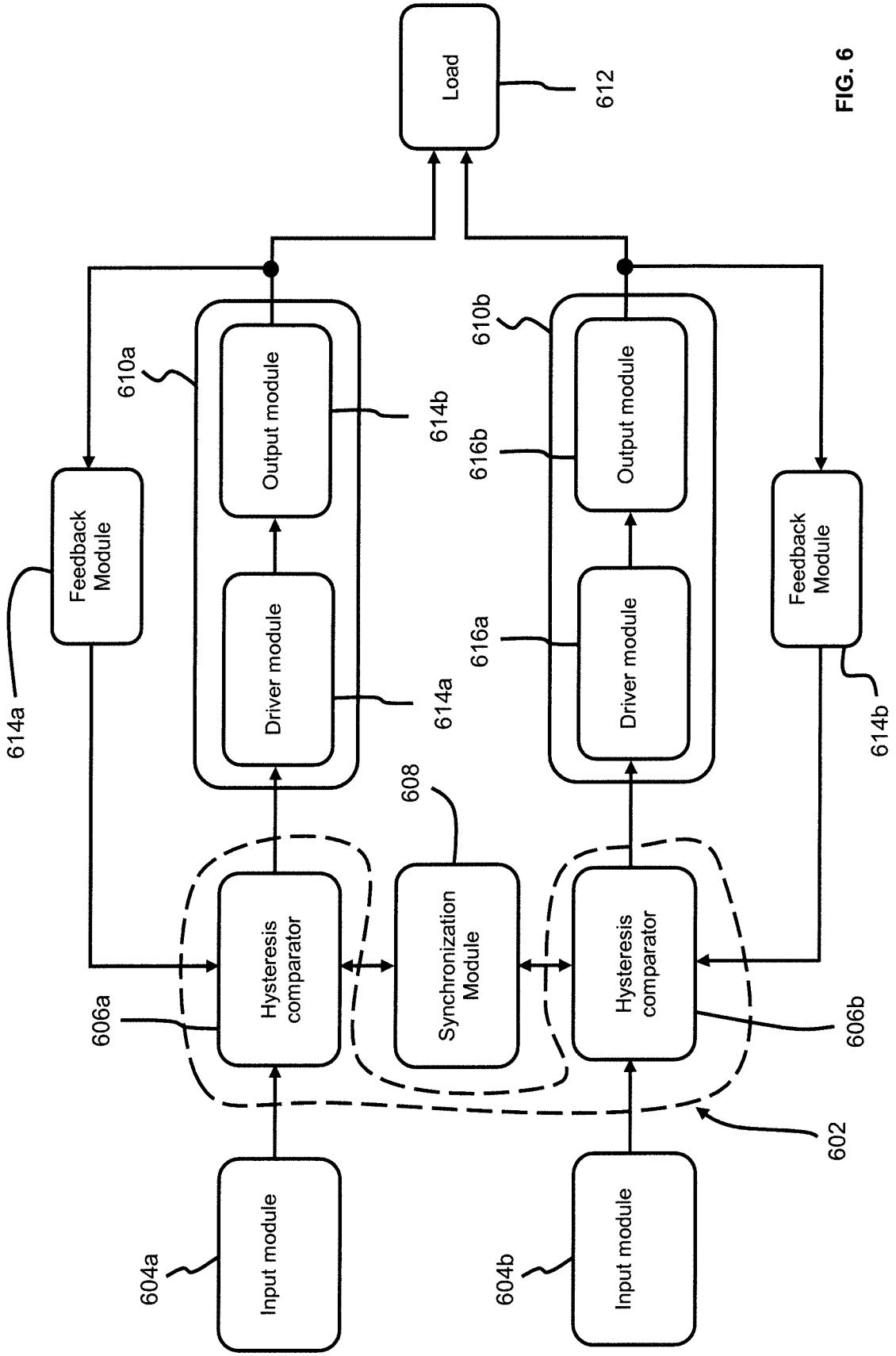
Load
612
610a
610b
Output module
Output module
614b
616b
Feedback Module
Feedback Module
614a
Driver module
Driver module
616a
614a
614b
608
Hysteresis comparator
Synchronization Module
Hysteresis comparator
606a
606b
602
Input module
Input module
604a
604b

FIG. 6

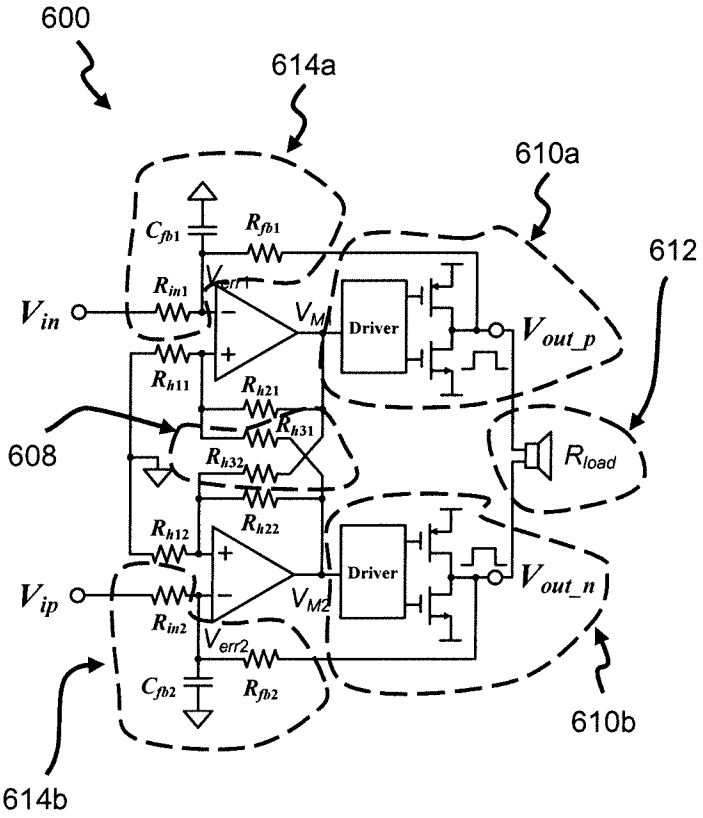

FIG. 7a

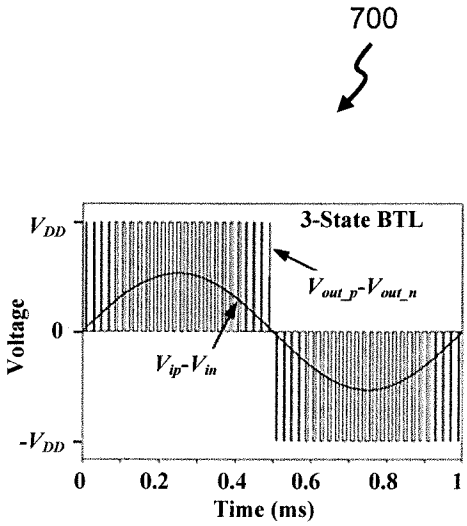

FIG. 7b

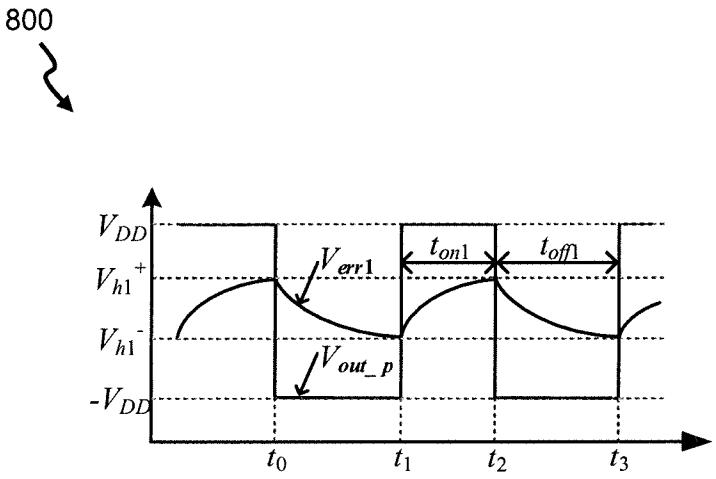

FIG. 8

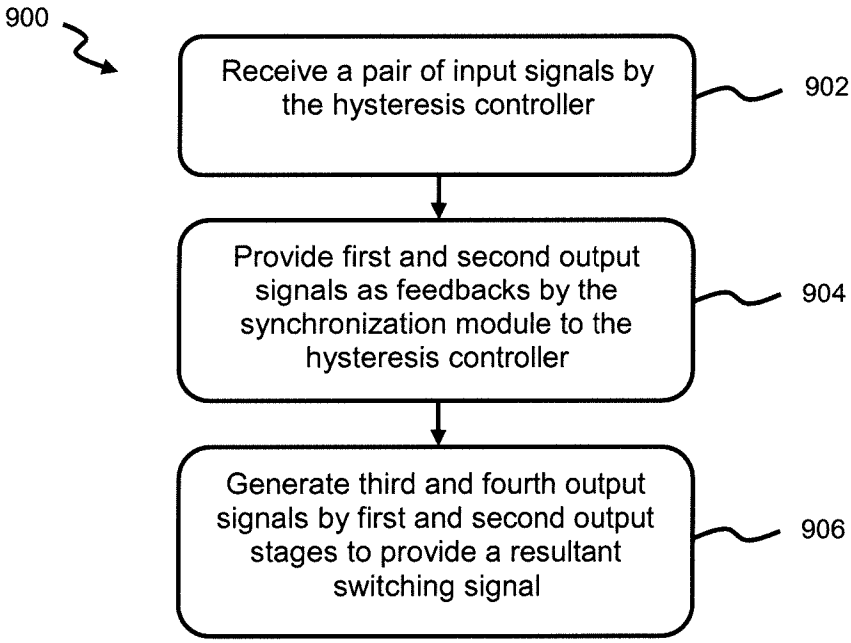
900
Receive a pair of input signals by the hysteresis controller
902
Provide first and second output signals as feedbacks by the synchronization module to the hysteresis controller
904
Generate third and fourth output signals by first and second output stages to provide a resultant switching signal
906

FIG. 9

1000

Parameter	Value			
	Case 1	Case 2	Case3	Case4
R_{h11}, R_{h12}	500 Ω	1 kΩ	500 Ω	1 kΩ
R_{h21}, R_{h22}	100 kΩ	100 kΩ	100 kΩ	100 kΩ
R_{h31}, R_{h32}	300 kΩ	300 kΩ	300 kΩ	300 kΩ
R_{in1}, R_{in2}, R_{fb1}, R_{fb2}	120 kΩ	120 kΩ	120 kΩ	120 kΩ
C_{fb1}, C_{fb2}	100 pF	100 pF	300 pF	300 pF
R_{load}	8 Ω (for all cases)			

FIG. 10

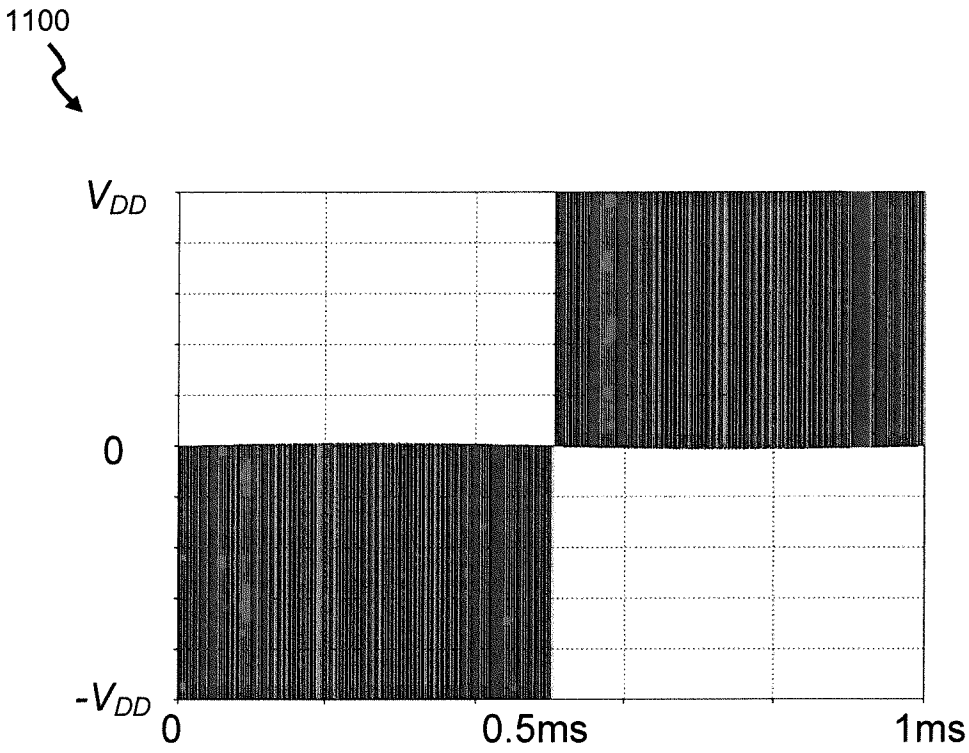

FIG. 11

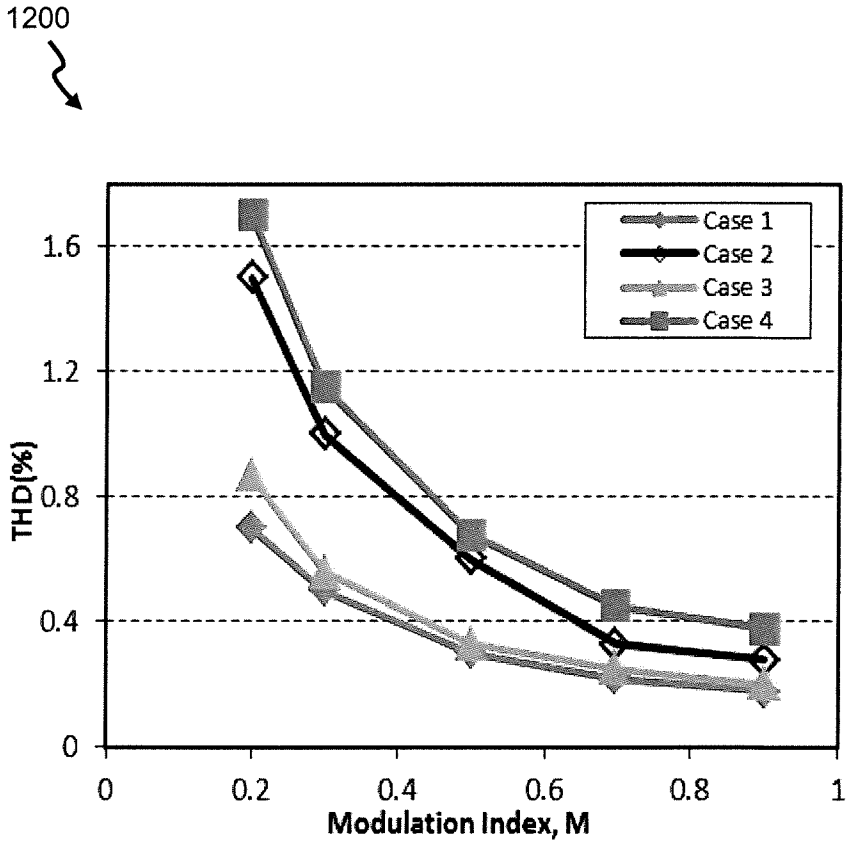
1200
Case 1
Case 2
Case 3
Case 4
THD(%)
1.6
1.2
0.8
0.4
0
0
0.2
0.4
0.6
0.8
1
Modulation Index, M

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2016/050585

A. CLASSIFICATION OF SUBJECT MATTER

H02M 1/12 (2006.01) H03K 17/16 (2006.01) G05F 1/46 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases: EPODOC, WPIAP, Espacenet, Google Scholat, Google Patents.

H02M1/-, H03K17/-, H03H1/-, G05F1/-, G05F3/-, G05F5/-, cut-off, attenuate, transient, filter, transistor, buffer circuit, voltage follower, unity gain, class D amplifier and other similar terms.

Applicant(s)/ Inventor(s) name searches performed on Espacenet, Auspat and internal IP Australia databases.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 February 2017	20 February 2017

Name and mailing address of the ISA/AU

AUSTRALIAN PATENT OFFICE
PO BOX 200, WODEN ACT 2606, AUSTRALIA
Email address: pct@ipaustralia.gov.au

Authorised officer

Aurobindo Ghosh
AUSTRALIAN PATENT OFFICE
(ISO 9001 Quality Certified Service)
Telephone No. 0262832301

INTERNATIONAL SEARCH REPORT C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		International application No. **PCT/SG2016/050585**
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6437639 B2 (NGUYEN et al.) 20 August 2002 Column 5 lines 1-7, 35-37, Column 6 lines1-2 and Figure 7	1-9
X	US 3257631 A (A. D. EVANS) 21 June 1966 Column 3 lines 72-74, Column 4 lines 20-25, 53-58, 62-64, 73-75 and Figures 1, 3, 4	1-9
X	US 3475623 A (R. A. MOOG) 28 October 1969 Column 1 lines 39-44, Column 5 lines 14-21, 24-26, Figure 1	1-9
X	Ge T. et al., 'Bang-Bang Control Class D Amplifiers: Total Harmonic Distortion and Supply Noise', IEEE Transactions on Circuits and Systems—I: Regular Papers, Vol. 56, No. 10, October 2009, Pages 2352 to 2361 [retrieved online 15 February 2017] <URL: http://ieeexplore.ieee.org/abstract/document/4738412/> [Published 06/01/2009] See whole document	1-9
X	Shu, W. et al., 'THD of Closed-Loop Analog PWM Class-D Amplifiers', IEEE Transactions on Circuits and Systems—I: Regular Papers, Vol. 55, No. 6, July 2008, Pages 1769 to 1777 [retrieved online 15 February 2017] <URL: http://ieeexplore.ieee.org/abstract/document/4447006/> [Published 07/02/2008] See whole document	1-9
X	US 8531237 B2 (AISU) 10 September 2013 See whole document	1-9
A	Lacanette, K., 'A basic introduction to filters- Active, Passive and Switched-Capacitor', National Semiconductor, Application Note 779, April 1991, pages 1 to 22 [retrieved online 13 February 2017] <URL: http://www.swarthmore.edu/NatSci/echeeve1/Ref/DataSheet/IntroToFilters.pdf> See whole document	1-9
A	Poole, I., 'Transistor capacitance multiplier circuit', [retrieved online 13 February 2017] <URL: http://www.radio-electronics.com/info/circuits/transistor/capacitance-multiplier-circuit.php> See whole document	1-9

Supplemental Box

Continuation of: **Box III**

This International Application does not comply with the requirements of unity of invention because it does not relate to one invention or to a group of inventions so linked as to form a single general inventive concept.

This Authority has found that there are different inventions based on the following features that separate the claims into distinct groups:

- Claims 1 to 9 are directed to a voltage reference comprising a voltage divider and a low pass filter. The feature of outputting a reference voltage substantially free of supply noise is specific to this group of claims.
- Claims 10 to 18 are directed to a self-oscillating amplifier circuit comprising hysteresis controllers and synchronisation modules. The feature of outputting a resultant switching signal which alternates between 3 states in dependence of the input signals is specific to this group of claims.

PCT Rule 13.2, first sentence, states that unity of invention is only fulfilled when there is a technical relationship among the claimed inventions involving one or more of the same or corresponding special technical features. PCT Rule 13.2, second sentence, defines a special technical feature as a feature which makes a contribution over the prior art.

When there is no special technical feature common to all the claimed inventions there is no unity of invention.

In the above groups of claims, the identified features may have the potential to make a contribution over the prior art but are not common to all the claimed inventions and therefore cannot provide the required technical relationship. Therefore there is no special technical feature common to all the claimed inventions and the requirements for unity of invention are consequently not satisfied *a priori*.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2016/050585

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
the subject matter listed in Rule 39 on which, under Article 17(2)(a)(i), an international search is not required to be carried out, including

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See Supplemental Box for Details

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-9

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT Information on patent family members	International application No. **PCT/SG2016/050585**

This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document/s Cited in Search Report		**Patent Family Member/s**	
Publication Number	**Publication Date**	**Publication Number**	**Publication Date**
US 6437639 B2	20 August 2002	None	
US 3257631 A	21 June 1966	US 3257631 A	21 Jun 1966
US 3475623 A	28 October 1969	US 3475623 A	28 Oct 1969
US 8531237 B2	10 September 2013	US 2011012582 A1	20 Jan 2011
		US 8531237 B2	10 Sep 2013
		JP 2011022689 A	03 Feb 2011
		JP 5446529 B2	19 Mar 2014

End of Annex

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.