

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization

International Bureau



(10) International Publication Number

WO 2014/105372 A1

(43) International Publication Date

3 July 2014 (03.07.2014)

WIPO | PCT

(51) International Patent Classification:

H01L 29/78 (2006.01) *H01L 21/336* (2006.01)
H01L 29/739 (2006.01) *H01L 21/331* (2006.01)
H01L 29/749 (2006.01) *H01L 21/332* (2006.01)
H01L 29/06 (2006.01) *H01L 29/16* (2006.01)

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(21) International Application Number:

PCT/US2013/073093

(22) International Filing Date:

4 December 2013 (04.12.2013)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

13/730,133 28 December 2012 (28.12.2012) US

(71) Applicant: CREE, INC. [US/US]; 4600 Silicon Drive, Durham, North Carolina 27703 (US).

(72) Inventors: ZHANG, Qingchun; 108 Hickorywood Blvd, Cary, North Carolina 27519 (US). HULL, Brett; 2101 Katesbridge Lane, Raleigh, North Carolina 27614 (US).

(74) Agent: WITHROW, Benjamin, S.; Withrow & Terranova, PLLC, 100 Regency Forest Drive, Suite 160, Cary, North Carolina 27518 (US).

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: SEMICONDUCTOR DEVICES HAVING REDUCED ELECTRIC FIELD AT A GATE OXIDE LAYER

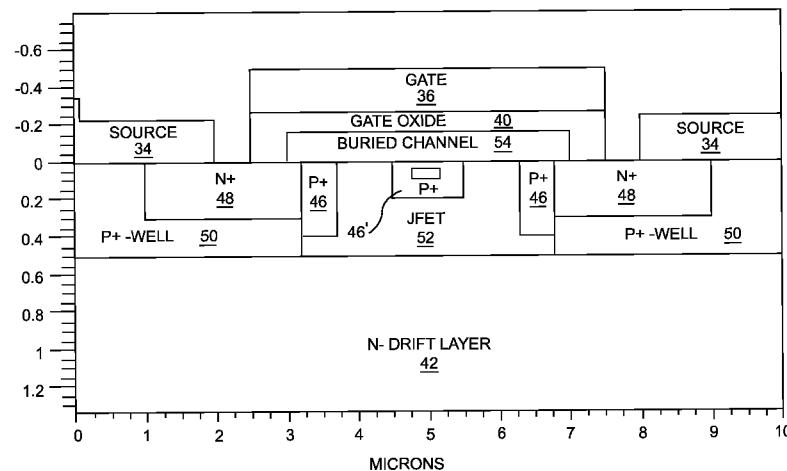


FIG. 3A

(57) Abstract: A semiconductor device such as a power MOSFET, an IGBT or a MOS-thyristor, eg. made of SiC, having reduced electrical field at a gate oxide layer interface. In one embodiment, the device comprises a gate (36), a source (34), and a drain, wherein the gate is at least partially in contact with a gate oxide layer (40). In order to reduce an electrical field on the gate oxide layer, the device has a highly doped region (46') of a first conductivity type, eg. a P⁺-type region, within a JFET region (52) of a second, opposite conductivity type, eg. an N-type JFET region, being a portion of a drift region (42) of said second conductivity type, eg. an N-type drift region, located between highly doped wells (50) of said first conductivity type, eg. P⁺-type wells.

WO 2014/105372 A1

TRANSISTOR STRUCTURES HAVING REDUCED ELECTRICAL FIELD AT THE GATE OXIDE AND METHODS FOR MAKING SAME

Field of the Disclosure

5 **[0001]** The present disclosure relates to transistor structures, and in particular, transistor structures such as metal–oxide–semiconductor field-effect transistors (MOSFETs) having a reduced electrical field at the gate oxide, and methods for making such transistor structures.

10 **Background**

15 **[0002]** Metal–oxide–semiconductor field-effect transistors (MOSFETs) are well-known. In particular, power MOSFETs have been commercialized and are expected to be widely used in power systems. For traditional MOSFET structures, such as power MOSFETs on Silicon Carbide (SiC), one potential issue is the presence of a high electrical field at the gate oxide in the center of the junction field effect (JFET) region of the device. A JFET region generally is an active portion of an N-type drift layer which may include an N-type dopant and is located between two P-type wells. The JFET region may refer to a region in contact with channel regions coming up to the surfaces of the P-type wells by applying a gate voltage. The JFET region makes up a conduction path for electrons with the N+ source region, the channel region, the N-type drift region, the substrate, and the drain electrode. Under operation conditions at which a high bias is applied to the drain (close to the operational maximum) and in which the gate is held near ground potential, a high electrical field is created in the gate oxide that sits just above the JFET region. Imperfections in the interface material and gate oxide could result in a gate oxide failure during long-term blocking operation, in which the drain is placed under a high positive bias. Second, traditional MOSFETs also may suffer from possible hot carrier injection during long-term blocking operation, in which the drain is placed under a high positive bias.

20

25

30

Summary

[0003] The present disclosure relates to a transistor device having reduced electrical field at the gate oxide interface, thus resulting in improved device reliability during long-term blocking operation, in which the drain is placed under

5 a high positive bias, due to a lower gate oxide field, and resulting in a reduction of the possibility of hot carriers injecting into the gate oxide during long-term blocking operation, in which the drain is placed under a high positive bias. In one preferred embodiment, the transistor device is a MOSFET device and even more preferably a Silicon Carbide (SiC) MOSFET device. However, the transistor
10 device may more generally be any type of device having a transistor (e.g., a power MOSFET; a double implanted field effect transistor (DIMOSFET); an insulated gate bipolar transistor (IGBT); and the like).

[0004] In one embodiment, a transistor device having a reduced electrical field at the gate oxide is disclosed. The transistor device comprises a gate, a source, and a drain, wherein the gate is at least partially atop a gate oxide layer. The transistor device has a P+ region within a JFET region of the transistor device in order to reduce an electrical field on the gate oxide. The transistor device may reduce the electrical field at the gate oxide interface and significantly reduce or eliminate reliability issues or failures that may occur during long-term
20 blocking operation, in which the drain is placed under a high positive bias.

[0005] In another embodiment, the transistor device has a gate, a source, and a drain and comprises a first epitaxial layer of a first conductivity type, a second epitaxial layer of a second conductivity type on the first epitaxial layer, and a buried channel layer adjacent a first surface of the transistor device. The buried
25 channel layer extends across a portion of the second epitaxial layer and is at least partially covered with a gate oxide. The transistor device also includes a well region of the first conductivity type extending from the first epitaxial layer down into the body of the transistor device to a depth, a JFET region adjacent the well region, and a drift layer below the well region.

30 **[0006]** A separate region of the first conductivity type, which may be a P+ region in one embodiment, is introduced within the JFET region of the transistor

device. In one embodiment, the P+ region is introduced substantially in the middle of the JFET region and is connected to a source, which effectively shields the electrical field from the drain side of the transistor device. The P+ region introduced within the JFET region may also be shallower than the P+ well

5 regions, which also mitigates the current spreading resistance.

[0007] In another embodiment, a MOSFET is disclosed having a reduced electrical field at the gate oxide. The MOSFET has a gate, a source, and a drain, wherein the gate is at least partially in contact with a gate oxide layer. The MOSFET comprises a P+-epitaxial layer and an N+-type region on the P+-type 10 epitaxial layer. The MOSFET also comprises a buried channel layer adjacent a first surface of the MOSFET, the buried channel layer extending across a portion of the N+-type region. The MOSFET also includes a P+-type well extending from the P+-type epitaxial layer down into the body of the MOSFET to a depth and a JFET region adjacent the P+ well. The MOSFET also comprises a P+ region

15 within the JFET region in order to reduce an electrical field on the gate oxide.

[0008] Methods for forming devices having a reduced electrical field at the gate oxide are also disclosed. In one embodiment, a method of forming a transistor device is disclosed. The method comprises providing a source and a gate, wherein the gate is at least partially in contact with a gate oxide layer. The 20 method also discloses providing a P+ region within a JFET region adjacent the P+-type well region in order to reduce an electrical field on the gate oxide.

[0009] In another embodiment, a method of forming a transistor is disclosed that includes providing a drift layer on a substrate and implanting a well region on the drift layer. The method also comprises providing a first epitaxial layer such 25 that the first epitaxial layer covers at least a portion of the well region, providing a second epitaxial layer on the first epitaxial layer, and providing a buried channel layer over a portion of the second epitaxial layer. A source and a gate are provided, wherein the gate is at least partially in contact with a gate oxide layer. The method also includes introducing a P+ region within a JFET region adjacent 30 the well region.

[0010] In yet another embodiment, a method of forming a MOSFET is disclosed. The method comprises providing a P+-type epitaxial layer on a drift layer and providing an N+-type region on the P+-type epitaxial layer. A buried channel layer is provided adjacent a first surface of the MOSFET, the buried 5 channel layer extending across a portion of the N+-type region. A P+-type well is formed that extends from the P+-type epitaxial layer down into the body of the MOSFET to a depth. A source and a gate are provided, wherein the gate is at least partially in contact with a gate oxide layer. The method also includes providing a P+ region within a JFET region adjacent the P+-type well region in 10 order to reduce an electrical field on the gate oxide.

[0011] Those skilled in the art will appreciate the scope of the present disclosure and realize additional aspects thereof after reading the following detailed description of the preferred embodiments in association with the accompanying drawing figures.

15

Brief Description of the Drawing Figures

[0012] The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the disclosure, and together with the description serve to explain the principles of the disclosure.

20 [0013] Figure 1 is a double implanted field effect transistor (DIMOSFET) having a buried channel;

[0014] Figure 2 is another embodiment of a standard MOSFET cell that does not have reduced electrical field at the gate oxide interface;

25 [0015] Figure 3A illustrates a transistor device having a new structure that includes a P+ region introduced within the JFET region of the transistor device according to one embodiment;

[0016] Figure 3B illustrates an alternate transistor device having a new structure that includes a plurality of P+ regions introduced within the JFET region of the transistor device according to one embodiment;

30 [0017] Figure 4A illustrates a forward current conduction distribution for a conventional MOSFET having a standard JFET gap of 2.6 microns;

[0018] Figure 4B illustrates a forward current conduction distribution for a conventional MOSFET having a narrowed JFET gap of 0.8 microns;

[0019] Figure 4C illustrates a forward current conduction distribution for a MOSFET having a P+ region introduced within the JFET region of the transistor

5 device according to one embodiment and having a standard JFET gap of 2.6 microns;

[0020] Figure 5 is a graphical representation of the forward IV curves for the various MOSFETs shown in Figures 4A-4C, which illustrates that the proposed transistor structure having a P+ region introduced within the JFET region of the 10 transistor device exhibits the same on-resistance as the conventional MOSFET with a standard JFET gap;

[0021] Figure 6A is a graphic illustrating an electrical field distribution for a conventional MOSFET having a standard JFET gap of 2.6 microns at a blocking voltage of 960 Volts;

15 **[0022]** Figure 6B is a graphic illustrating an electrical field distribution for a conventional MOSFET having a narrowed JFET gap of 0.8 microns at a blocking voltage of 960 Volts;

[0023] Figure 6C is a graphic illustrating an electrical field distribution for a MOSFET having a P+ region introduced within the JFET region of the transistor 20 device according to one embodiment and having a standard JFET gap of 2.6 microns at a blocking voltage of 960 Volts; and

[0024] Figure 7 is a graphic of the electric field distributions on top of the gate oxide at the center of the gate oxide for the various MOSFETs shown in Figures 4A-4C, which illustrates a significant electrical field reduction has been achieved 25 by the transistor structure having a P+ region introduced within the JFET region of the transistor device without sacrificing on-state resistance.

Detailed Description

[0025] The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the embodiments and illustrate the best mode of practicing the embodiments. Upon reading the following

5 description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

10 **[0026]** It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing 15 from the scope of the present disclosure. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

15 **[0027]** It will be understood that when an element such as a layer, region, or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements 20 may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. Likewise, it will be understood that when an element such as a layer, region, or substrate is referred to as being "over" or extending "over" another element, it can be directly over or extend directly over 25 the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly over" or extending "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other 30 element or intervening elements may be present. In contrast, when an element

is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

[0028] Relative terms such as "below" or "above" or "upper" or "lower" or "horizontal" or "vertical" may be used herein to describe a relationship of one

5 element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.

[0029] The terminology used herein is for the purpose of describing particular

10 embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes," and/or

"including" when used herein specify the presence of stated features, integers,

15 steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0030] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of

20 ordinary skill in the art to which this disclosure belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

25 **[0031]** There is a need for a MOSFET structure that has reduced electrical field at the gate oxide interface, thus resulting in improved device reliability. One approach at addressing this issue is to narrow the JFET gap. However, it has been recognized by the inventors of the present invention that narrowing down the JFET gap (without sacrificing forward voltage drop) on a conventional

30 MOSFET device could improve the device reliability under high electrical field stressing, but it may not eliminate failure.

[0032] The disclosure relates to a transistor device that has a new structure in order to reduce an electrical field at a gate oxide interface and significantly reduce or eliminate failure or reliability issues under long-term blocking operation,

5 in which the drain is placed under a high positive bias. In one preferred embodiment, the transistor device is a MOSFET device and even more preferably a Silicon Carbide (SiC) MOSFET device. However, the transistor device may more generally be any type of device having a transistor (e.g., a power MOSFET; a double differentiated field effect transistor (DMOSFET); a
10 trench gated metal oxide semiconductor field effect transistor (UMOSFET); an insulated gate bipolar transistor (IGBT); and the like).

[0033] In one embodiment, a transistor device having a reduced electrical field at the gate oxide is disclosed. The transistor device comprises a gate, a source, and a drain, wherein the gate is at least partially atop a gate oxide layer.

15 The transistor device has at least one P+ region within a JFET region of the transistor device in order to reduce an electrical field on the gate oxide. Due to the presence of material defects that may occur in the transistor device, a high electrical field in the gate oxide may be enhanced at or around the defective points. Reducing the electrical field can significantly reduce the role of the
20 defects on the reliability of the transistor device, particularly during long-term blocking operation, in which the drain is placed under a high positive bias. In silicon carbide MOSFETs, it may be desirable to reduce the gate field to less than one (1) MV/cm at a rated voltage to ensure reliability.

[0034] In another embodiment, the transistor device has a gate, a source, and

25 a drain and comprises a first epitaxial layer of a first conductivity type, a second epitaxial layer of a second conductivity type on the first epitaxial layer, and a buried channel layer adjacent a first surface of the transistor device. The buried channel layer extends across a portion of the second epitaxial layer and is at least partially covered with a gate oxide layer. The transistor device also
30 includes a well region of the first conductivity type extending from the first

epitaxial layer down into the body of the transistor device to a depth, a JFET region adjacent the well region, and a drift layer below the well region.

[0035] A separate region of the first conductivity type, which may be a P+ region in one embodiment, is introduced within the JFET region of the device. In

5 one embodiment, the P+ region is introduced substantially in the middle of the JFET region and is connected to a source, which effectively shields the electrical field from the drain side of the device. The P+ region introduced within the JFET region may also be shallower than the P+ well regions, which also mitigates the current spreading resistance.

10 **[0036]** Before specifically describing various embodiments of the present disclosure, a discussion is provided of research conducted by the inventors that will enable better understanding of the transistor devices disclosed herein.

[0037] Figure 1 illustrates a MOSFET device 10 that does not have reduced electrical field at the gate oxide interface. In Figure 1, the MOSFET device 10 is 15 a traditional DMOSFET. The traditional DMOSFET 10 includes a source 12, a gate 14, and a drain 16 positioned on a semiconductor body 20 with the gate 14 atop an oxide layer 18 insulating the gate region. The DMOSFET 10 includes a P+-type well 22 implanted into the semiconductor body 20 to a depth of about 0.5 microns and doped to an appropriate level, such as between about $5 \times 10^{18} \text{ cm}^{-3}$ 20 and $5 \times 10^{20} \text{ cm}^{-3}$ in one embodiment, although other dopant levels could be used. An N+ source region 24 doped to an appropriate level, such as approximately $5 \times 10^{19} \text{ cm}^{-3}$ in one embodiment, although other dopant levels could be used. The N+ source region 24 is adjacent the P+-type well 22 and positioned between the P+-type well 22 and a buried channel 26. The buried 25 channel 26 extends across portions of the source region 24, the P+-type well 22 and the semiconductor body 20 between active regions, i.e., a JFET region 28.

[0038] A JFET region 28 generally is an active portion of an N-type drift layer which may include an N-type dopant and is located between two P-type wells, such as P+-type well 22. The JFET region in general may refer to a region in 30 contact with channel regions coming up to the surfaces of the P-type wells by applying a gate voltage. The JFET region 28 makes up a conduction path for

electrons with the N+ source region 24, the channel region 26, an N-type drift region 30, a substrate, and the drain electrode 16. The JFET region 28 may be provided by epitaxial growth or by implantation. In certain embodiments, the JFET region 28 may have a thickness ranging from about 0.5 microns to about 5 1.5 microns. The buried channel 26, the JFET region 28, and a supporting drift region 30 of the DMOSFET 10 may be doped to appropriate levels. In one embodiment, the buried channel 26 may be doped between about $1 \times 10^{16} \text{ cm}^{-3}$ and $1 \times 10^{17} \text{ cm}^{-3}$, the JFET region 28 may be doped between about $2 \times 10^{16} \text{ cm}^{-3}$ and $5 \times 10^{16} \text{ cm}^{-3}$, and the supporting drift region 30 may be doped between 10 about $2 \times 10^{14} \text{ cm}^{-3}$ and $5 \times 10^{16} \text{ cm}^{-3}$, although other dopant levels could be used.

[0039] In a typical DMOSFET, the fabrication process controls the channel surface by using ion implantation instead of doping during layer growth. Ion implantation is difficult to achieve accurately in DMOSFETs, and the resulting 15 devices are limited in channel mobility. In addition, the traditional DMOSFET 10 shown in Figure 1 may have a high electrical field at the gate oxide in the center of JFET region 28 of the device.

[0040] The high electrical field combined with any imperfections in the 20 interface material and gate oxide could result in a gate oxide failure under long-term blocking operation, in which the drain is placed under a high positive bias. Also, the traditional DMOSFET 10 shown in Figure 1 may suffer from possible hot carrier injection during long-term blocking operation, in which the drain is placed under a high positive bias.

[0041] Figure 2 shows another embodiment of a standard DMOSFET cell that 25 does not have reduced electrical field at the gate oxide interface. In Figure 2, a DMOSFET 32 includes a source 34, a gate contact 36, and a drain 38 positioned on a body of the DMOSFET with the gate contact 36 atop an oxide layer 40 insulating the gate region. The DMOSFET 32 may have a supporting N-drift 30 layer 42 and a N+-substrate 44, which in one embodiment may be a silicon carbide substrate. The DMOSFET 32 may also include at least one P+ region(s) 46 and at least one N+ region(s) 48. The DMOSFET also includes at least one

P+-type well region 50 implanted into the body of the DMOSFET 32 having at least one P+ region 46. The at least one N+ source region 48 may be doped to an appropriate level (such as approximately $5 \times 10^{19} \text{ cm}^{-3}$ in one embodiment) and is adjacent the at least one P+ region 46. A JFET region 52 is located

5 underneath the oxide layer 40 and is doped to appropriate levels, such as between about $2 \times 10^{16} \text{ cm}^{-3}$ and $5 \times 10^{16} \text{ cm}^{-3}$ in one embodiment. The supporting drift region 52 of the DMOSFET 32 may also be doped to appropriate levels (such as between about $2 \times 10^{14} \text{ cm}^{-3}$ and $5 \times 10^{16} \text{ cm}^{-3}$ in one embodiment) and is supported by a substrate 44 (which may be any made of any

10 material, but may be a N+ silicon carbide substrate in one embodiment) down to the drain 38.

[0042] In a typical related art DMOSFET, the fabrication process controls the channel surface by using ion implantation instead of doping during layer growth. Ion implantation is difficult to achieve accurately in DMOSFETs, and the resulting 15 devices are limited in channel mobility. In addition, the DMOSFET 32 shown in Figure 2 also may have a high electrical field at the gate oxide in the center of the JFET region 52 of the device. The high electrical field combined with any imperfections in the interface material and gate oxide could result in a gate oxide failure under long-term blocking operation, in which the drain is placed under a 20 high positive bias. Also, the DMOSFET 32 shown in Figure 2 may suffer from possible hot carrier injection during long-term blocking operation, in which the drain is placed under a high positive bias.

[0043] The related art MOSFET devices in Figures 1 and 2 illustrate the common need for modifications to transistor design that reduces the electrical 25 field at the gate oxide interface and increases maximum current flow in the on state with the ability to block incident voltages in reverse biased operation. For illustrative purposes, assume that the substrate and the drift layer of the devices shown in Figures 1-3 are each formed of Silicon Carbide (SiC). However, other semiconductor materials may be used.

30 **[0044]** One approach at addressing high electrical field at the gate oxide interface is to narrow the JFET gap. However, it has been recognized by the

inventors of the present invention that narrowing down the JFET gap (without sacrificing forward voltage drop) on a conventional MOSFET device could improve the device reliability during long-term blocking operation, in which the drain is placed under a high positive bias, but it may not eliminate failure.

5 **[0045]** In order to reduce the electrical field at the gate oxide interface and eliminate failure during long-term blocking operation, in which the drain is placed under a high positive bias, a new transistor structure is proposed. At least one separate P+ region is introduced within the JFET region. In one embodiment, the at least one P+ region is introduced substantially in the middle of the JFET region
10 and is connected to the source, which effectively shields the electrical field from the drain side of the device. The at least one P+ region introduced within the JFET region may also be shallower than the P+ well regions, which also mitigates the current spreading resistance.

[0046] Referring now to Figure 3A, a proposed new structure is shown.
15 Figure 3A illustrates a device that has reduced electrical field at the gate oxide interface due to the introduction of at least one P+ region in the JFET region. Although shown in Figure 3A as having a square or rectangular shape, the at least one P+ region introduced in the JFET region may be any shape. In addition, the P+ region(s) introduced in the JFET region may be flush with the
20 surface of the JFET region or the P+ region(s) may be below a top surface of the JFET region.

[0047] In Figure 3A, the device is a DMOSFET, but the device could be any type of device having a source, a gate, a gate oxide layer, a P+ well, and a JFET region, including but not limited to MOSFETs, UMOSFETs, IGBTs, and the like.
25 Like the traditional DMOSFET shown in Figure 1, the new structure includes a source 34 and a gate contact 36 with the gate contact 36 atop an oxide layer 40 insulating the gate region. The device includes a P+-type well 50 implanted into the device to a depth of about 0.5 microns and doped to an appropriate level, such as between about $5 \times 10^{18} \text{ cm}^{-3}$ and $5 \times 10^{20} \text{ cm}^{-3}$ in one embodiment,
30 although other dopant levels could be used. An N+ source region 48 is doped to an appropriate level (such as approximately $5 \times 10^{19} \text{ cm}^{-3}$ in one embodiment,

although other dopant levels could be used) and is adjacent the P+ well 50 and positioned between the P+-type well 50 and a buried channel 54. The buried channel 54 may extend across portions of the device between active regions, i.e., a JFET region 52.

5 [0048] A JFET region like JFET region 52 generally is an active portion of an N-type drift layer which may include an N-type dopant and is located between two P-type wells or inside a P+-type well, such as P+-type well 50. The JFET region in general may refer to a region in contact with channel regions coming up to the surfaces of the P-type wells by applying a gate voltage. The JFET region 10 52 makes up a conduction path for electrons with the N+ source region 48, the channel region 54, an N-type drift region 42, a substrate, and the drain (not shown in Figure 3A). The JFET region 52 may be provided by epitaxial growth or by implantation. In certain embodiments, the JFET region 52 may have a thickness ranging from about 0.5 microns to about 1.5 microns.

15 [0049] The buried channel 54, the JFET region 52, and supporting drift region 42 of the device may be doped to appropriate levels. In one embodiment, the buried channel 54 may be doped between about $1 \times 10^{16} \text{ cm}^{-3}$ and $1 \times 10^{17} \text{ cm}^{-3}$, the JFET region 52 may be doped between about $1 \times 10^{16} \text{ cm}^{-3}$ and $5 \times 10^{17} \text{ cm}^{-3}$, and the supporting drift region 42 may be doped between about $1 \times 10^{14} \text{ cm}^{-3}$ 20 and $5 \times 10^{16} \text{ cm}^{-3}$, although other dopant levels could be used.

[0050] In the new proposed device, at least one separate P+ region 46', such as a separate P+ region 46', is introduced within the JFET region 52, as shown in Figure 3A. Although shown in Figure 3A as having a square or rectangular shape, the at least one separate P+ region 46' introduced in the JFET region 52 25 may be any shape. In addition, the at least one separate P+ region(s) 46' introduced in the JFET region 52 may be flush with the surface of the JFET region 52 or the at least one separate P+ region(s) 46' may be below a top surface of the JFET region 52. In one embodiment, the separate P+ region 46' may be formed by implanting aluminum with a doping equal to or greater than 30 approximately $1 \times 10^{18} \text{ cm}^{-3}$. In one embodiment, the separate P+ region 46' is introduced substantially in the middle of the JFET region 52 and is connected to

the source 34, which effectively shields the electrical field from the drain side of the device. The separate P+ region 46' introduced within the JFET region 52 may also be shallower than the P+-type well regions 50, which also mitigates the current spreading resistance.

5 [0051] In one embodiment, the separate P+ region 46' is approximately 0.2 microns deep into the device, though other depths may be used. In addition, in one embodiment, the separate P+ region 46' introduced within the JFET region 52 may be between 0.5 and 1.0 microns wide, though other widths are possible. As shown in Figure 3, the separate P+ region 46' may have a ohmic contact used 10 for simulation purposes only (shown by the box in the separate P+ region 46'). In operation, the separate P+ region 46' is shorted to the source 34.

15 [0052] Figure 3B illustrates an alternate transistor device having a new structure that includes a plurality of P+ regions 46' and 46" introduced within the JFET region 52. In Figure 3B, there are two P+ regions (46' and 46") introduced within the JFET region 52, although any number of P+ regions 46' and 46" may be introduced within the JFET region 52. In various embodiments, the P+ regions 46' and 46" can have various shapes and different implant profiles below a top surface of the JFET region 52. In the embodiment of Figure 3B, the P+ regions 46' and 46" are below a top surface of the JFET region 52. In particular, 20 in one embodiment, one or more of the P+ regions 46' and 46" can be retrograde to the top surface of the JFET region 52 to reduce the implant damage to the MOS interface, as long as the P+ region 46' or 46" is shorted to the source 34.

25 [0053] Figures 4A-4C show forward current conduction distributions of various devices. Figure 4A shows the forward current conduction distribution for a conventional control MOSFET having a typical JFET gap of approximately 2.6 microns. Figure 4B shows the forward current conduction distribution for a control MOSFET having a narrowed JFET gap of approximately 0.8 microns. As can be seen in Figure 4B, the MOSFET with the narrowed JFET gap significantly increases spreading resistance as compared to the conventional control 30 MOSFET. This indicates that the MOSFET with the narrowed JFET gap creates a bottleneck at a narrow JFET region. Figure 4C shows the forward current

conduction distribution for a MOSFET having the proposed structure with a P+ region introduced within the JFET gap and a standard JFET gap of about 2.6 microns. As can be seen in Figure 4C, the MOSFET having the proposed structure with a P+ region introduced within the JFET gap does not have the

5 increased spreading resistance associated with the MOSFET having the narrowed JFET gap and is more in line with the traditional MOSFET having the standard JFET gap.

[0054] Further, as can be seen in Figure 5, the proposed device having a P+ region introduced within the JFET gap also exhibits the same on-resistance as
10 the conventional MOSFET with the standard JFET gap. Figure 5 shows forward IV's as measured in drain voltage versus drain current density for each of the devices shown in Figures 4A-4C. As can be seen from Figure 5, the MOSFET having the narrowed JFET gap has a lower on-resistance as compared to the conventional MOSFET with the standard JFET gap, while the proposed device
15 having a P+ region introduced within the JFET gap also exhibits the same on-resistance as the conventional MOSFET with the standard JFET gap.

[0055] Figures 6A-6C illustrate the electrical field contours of the devices shown in Figures 4A-4C compared to G2 1200V control DMOSFETs. A drain voltage of 960 volts was used in these simulations. As seen in Figures 6A-6C,
20 the proposed device having a P+ region introduced within the JFET gap results in reduced electrical field at the gate oxide interface (Figure 6C) as compared to the conventional DMOSFET with a standard JFET gap.

[0056] This may also be seen in Figure 7, which shows the electrical field distributions at the top of the gate oxide and at the center of the gate oxide. As
25 seen in Figure 7, significant electrical field reduction has been achieved on the proposed structure having a P+ region introduced within the JFET gap, all without sacrificing the on-resistance.

[0057] The proposed structure of Figure 3 may be fabricated according to any of various standard techniques. Likewise, the P+ region 46' introduced within the
30 JFET region 52 may be formed according to any of various standard techniques one embodiment of the present disclosure. Through the process, exemplary

materials, doping types, doping levels, structure dimensions, and the selected alternatives are outlined, these aspects are merely illustrative, and the concepts disclosed herein and the claims that follow are not limited to these aspects.

[0058] The method of forming the improved transistor structure described

5 herein enhances technology that has been advantageously used for DMOSFETs of the related art. The traditional methods, however, are modified to account for the fact that the transistor device includes a P+ region introduced within the JFET region of the transistor device. As noted above, MOSFETs according to this invention optionally include a silicon carbide substrate formed by known means.

10 Referring back to Figures 2 and 3, a drift region layer 42 of 4H-SiC is epitaxially grown on a substrate 44. The method includes forming at least one doped well region 50 of a first conductivity type, preferably P+. The well region 50 can be formed by any common technique but is preferably formed by implanting dopants into the device from the top of the device down to a depth that is greater than one 15 micron. A second layer 48 of a second conductivity type (such as N+ in one embodiment) is formed on the first layer 50. The body of the transistor device at this point includes semiconductor layers, preferably of silicon carbide, for controlling electrical conduction from top to bottom.

[0059] Structures 46, 48, 50, and 52 are formed primarily by ion implantation, 20 and layer 54 is then grown on top by epitaxy. A buried channel layer 54 is formed by epitaxy, and the buried channel layer 54 is etched through selectively in areas that sit above the P+-type well 50 and the N+ source region 48 in order to make contact to those layers. Afterwards, the channel 54 is covered with a 25 layer of gate insulation (gate oxide 40), such as silicon dioxide, on which the gate contact 36 is formed. A region of the first conductivity type is then introduced into the JFET region according to any known methods. In one embodiment, the region of the first conductivity type is a P+ region. Source and drain contacts 34 and 38, common in these types of transistors, complete the transistor device.

[0060] The method described herein can also be used to form other 30 transistors that include a P+ region introduced into the JFET region to reduce the electrical field at the gate oxide interface. Accordingly, this invention is not

limited to various MOSFETs, but is equally applicable to insulated gate bipolar transistors and metal-oxide-semiconductor controlled thyristors. The semiconductor material used for forming all of these devices is preferably silicon carbide, but the invention is not limited to such.

5 **[0061]** Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

10 **[0062]** Examples of methods that may be used to form the structures disclosed herein include, but are not limited to the following: A method of forming a transistor device comprising providing a source and a gate, wherein the gate is at least partially in contact with a gate oxide; and providing at least one P+ region within a junction field effect (JFET) region adjacent a P+-type well region, in order to reduce an electrical field on the gate oxide, wherein the at least one 15 P+ region introduced within the JFET region reduces an electrical field at the gate oxide. In addition, in one embodiment, a body of the transistor device may comprise silicon carbide. In one embodiment, the method may comprise any of the above disclosed methods, wherein the at least one P+ region is provided substantially in the middle of the JFET region. In yet another embodiment, the 20 method may comprise any of the above disclosed methods, further comprising connecting the at least one P+ region to the source. In one embodiment, the depth of the at least one P+ region is between about approximately 0.1 and about approximately 0.3 microns in depth, and the width of the at least one P+ region is between approximately 0.5 microns and approximately 1.0 microns in 25 width. The disclosed methods may provide a width of the JFET region between about approximately 2.0 and about approximately 3.6 microns.

30 **[0063]** In addition to the above methods, a method of forming a transistor device may comprise providing a drift layer on a substrate; implanting a well region on the drift layer; providing a first epitaxial layer such that the first epitaxial layer covers at least a portion of the well region; providing a second epitaxial layer on the first epitaxial layer; providing a buried channel layer over a portion of

the second epitaxial layer; providing a source and a gate, wherein the gate is at least partially in contact with a gate oxide; and providing at least one P+ region within a junction field effect (JFET) region adjacent the well region.

[0064] In another embodiment, the at least one P+ region introduced within

- 5 the JFET region reduces an electrical field at the gate oxide. In another embodiment, a body of the transistor device may comprise silicon carbide. In one embodiment, the at least one P+ region is provided substantially in the middle of the JFET region. In another embodiment, the method may comprise any method disclosed above, the method further comprising connecting the at
- 10 least one P+ region to the source. In yet another embodiment, the method may comprise any of the disclosed methods, wherein the P+ region is shallower in depth than the well region. In one embodiment, the at least one P+ region is between about approximately 0.1 microns and about approximately 0.3 microns in depth. In another embodiment, the at least one P+ region is between
- 15 approximately 0.5 microns and approximately 1.0 microns in width. In yet another embodiment, the width of the JFET region is between about approximately 2.0 and about approximately 3.6 microns.

[0065] In addition to the above methods, the method of forming a MOSFET may comprise: providing a P+-type epitaxial layer on a drift layer; providing an

- 20 N+-type region on the P+-type epitaxial layer; providing a buried channel layer adjacent a first surface of the MOSFET, the buried channel layer extending across a portion of the N+-type region; forming a P+-type well extending from the P+-type epitaxial layer down into the body of the MOSFET to a depth; providing a source and a gate, wherein the gate is at least partially in contact with a gate
- 25 oxide; and providing a P+ region within a junction field effect (JFET) region adjacent the P+-type well region in order to reduce an electrical field on the gate oxide. In one embodiment, the at least one P+ region introduced within the JFET region reduces an electrical field at the gate oxide. In another embodiment, a body of the MOSFET may comprise silicon carbide. In yet another embodiment,
- 30 the at least one P+ region is provided substantially in the middle of the JFET region. The method of forming a MOSFET may comprise connecting the at least

one P+ region to the source. In one embodiment, the at least one P+ region is shallower in depth than the P+ well region. In another embodiment, the at least one P+ region is between about approximately 0.1 microns to about approximately 0.3 microns in depth. In yet another embodiment, the at least one

5 P+ region is between approximately 0.5 microns and about approximately 1.0 microns in width. In another embodiment, the width of the JFET region is between about approximately 2.0 and about approximately 3.6 microns.

Claims

What is claimed is:

1. A transistor device comprising a gate, a source, and a drain, wherein the gate is at least partially in contact with a gate oxide, and wherein at least one P+ region resides within a junction field effect (JFET) region in order to reduce an electrical field on the gate oxide.
2. A transistor device according to claim 1, wherein a body of the transistor device comprises silicon carbide.
3. A transistor device according to claim 1, wherein the at least one P+ region is substantially in the middle of the JFET region.
4. A transistor device according to claim 1, wherein the at least one P+ region is connected to the source, which effectively shields the electrical field from a side of the MOSFET having the drain.
5. A transistor device according to claim 1, wherein the at least one P+ region is between about approximately 0.1 microns and about approximately 0.3 microns in depth.
6. A transistor device according to claim 1, wherein the at least one P+ region is between about approximately 0.5 microns and about approximately 1.0 microns in width.
7. A transistor device according to claim 1, wherein a width of the JFET region is between about approximately 2.0 and about approximately 3.6 microns.
8. A transistor device having a gate that is at least partially in contact with a gate oxide, a source, and a drain, the transistor device comprising:

a first epitaxial layer of a first conductivity type;
a second epitaxial layer of a second conductivity type on the first epitaxial layer;

5 a buried channel layer adjacent a first surface of the transistor device, the buried channel layer extending across a portion of the second epitaxial layer and being at least partially covered by the gate oxide;

a well region of the first conductivity type extending from the first epitaxial layer down into the a body of the transistor device to a depth;

10 a junction field effect (JFET) region adjacent the well region;

a drift layer below the well region; and

a region of the first conductivity type introduced within the JFET region.

9. A transistor device according to claim 8, wherein the region of the first conductivity type introduced within the JFET region reduces an electrical field at 15 the gate oxide.

10. A transistor device according to claim 8, wherein the transistor device is an MOSFET.

20 11. A transistor device according to claim 8, wherein the transistor device is an insulated gate bipolar transistor.

12. A transistor device according to claim 8, wherein the transistor device is a metal-oxide-semiconductor controlled thyristor.

25 13. A transistor device according to claim 8, wherein the first conductivity type is P+, and the second conductivity type is N+.

14. A transistor device according to claim 8, wherein a body of the transistor 30 device comprises silicon carbide.

15. A transistor device according to claim 8, wherein the region of the first conductivity type introduced within the JFET region is a P+ region and is introduced substantially in the middle of the JFET region.

5 16. A transistor device according to claim 8, wherein the region of the first conductivity type introduced within the JFET region is a P+ region and is connected to the source, which effectively shields the electrical field from a side of the transistor device having the drain.

10 17. A transistor device according to claim 8, wherein the region of the first conductivity type introduced within the JFET region is a P+ region and is shallower in depth than the well region.

15 18. A transistor device according to claim 8, wherein the region of the first conductivity type introduced within the JFET region is a P+ region and is between about approximately 0.1 microns and about approximately 0.3 microns in depth.

19. A transistor device according to claim 8, wherein the region of the first conductivity type introduced within the JFET region is a P+ region and is between 20 about approximately 0.5 microns and about approximately 1.0 microns in width.

20. A transistor device according to claim 8, wherein a width of the JFET region is between about approximately 2.0 and about approximately 3.6 microns.

25 21. A MOSFET having a gate, a source, and a drain, wherein the gate is at least partially in contact with a gate oxide, the MOSFET comprising:

a P+-type epitaxial layer;

an N+-type region on the P+-type epitaxial layer;

a buried channel layer adjacent a first surface of the MOSFET, the buried

30 channel layer extending across a portion of the N+-type region;

a P+ type well extending from the P+ type epitaxial layer down into a body of the MOSFET to a depth;

5 a junction field effect (JFET) region adjacent the P+ well; and

a P+ region within the JFET region in order to reduce an electrical field on the gate oxide.

22. A MOSFET according to claim 21, wherein a body of the MOSFET comprises silicon carbide.

10 23. A MOSFET according to claim 21, wherein the P+ region is substantially in the middle of the JFET region.

24. A MOSFET according to claim 21, wherein the P+ region is connected to the source, which effectively shields the electrical field from a side of the

15 MOSFET having the drain.

25. A MOSFET according to claim 21, wherein the P+ region is shallower in depth than the P+ well.

20 26. A MOSFET according to claim 21, wherein the P+ region is between about approximately 0.1 and about approximately 0.3 microns in depth.

27. A MOSFET according to claim 21, wherein the P+ region is between about approximately 0.5 microns and about approximately 1.0 microns in width.

25 28. A MOSFET according to claim 21, wherein a width of the JFET region is between about approximately 2.0 and about approximately 3.6 microns.

29. A MOSFET according to claim 21, wherein the MOSFET has a reduced

30 electrical field on the gate oxide.

1/8

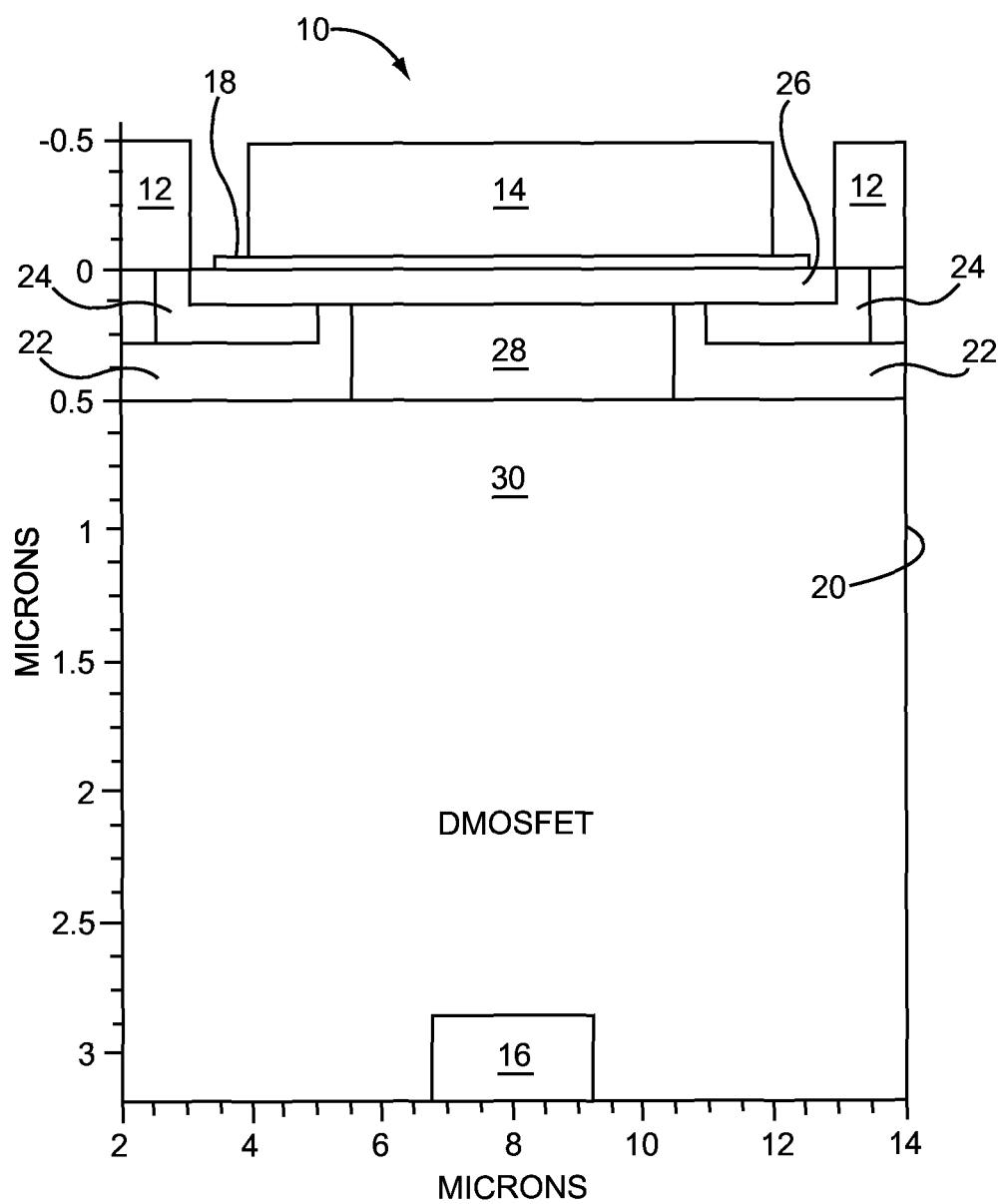


FIG. 1
(RELATED ART)

2/8

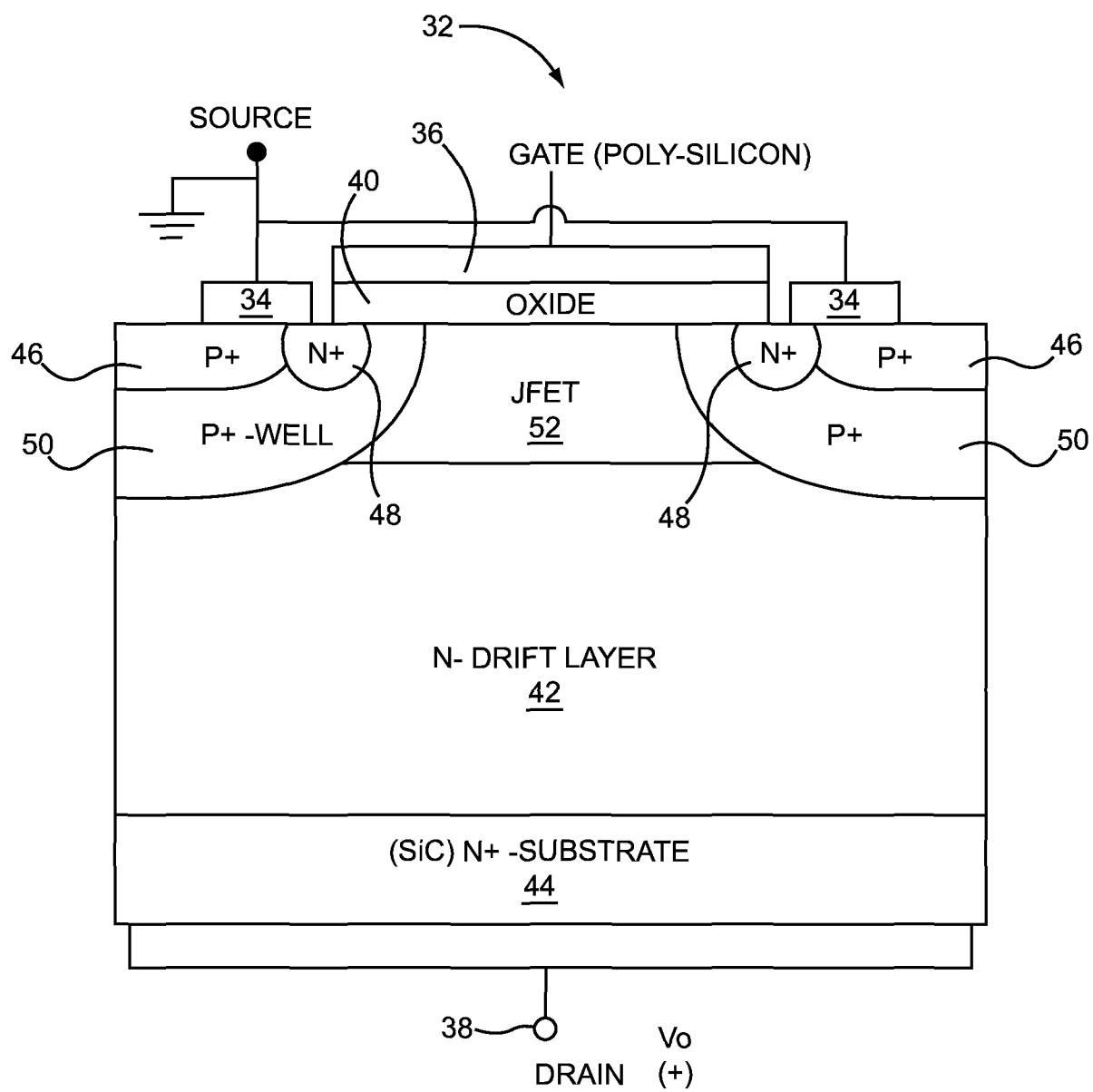


FIG. 2

3/8

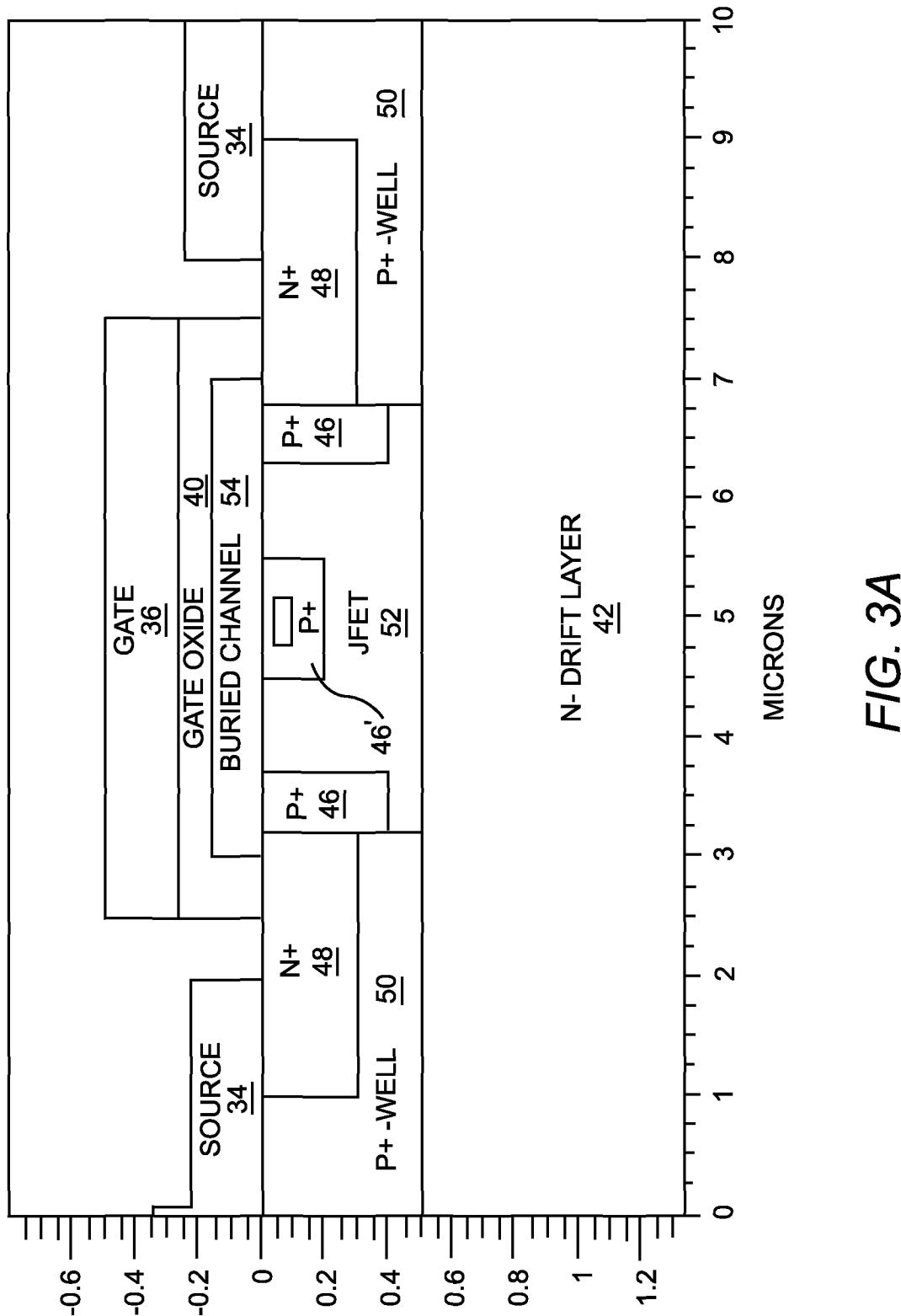
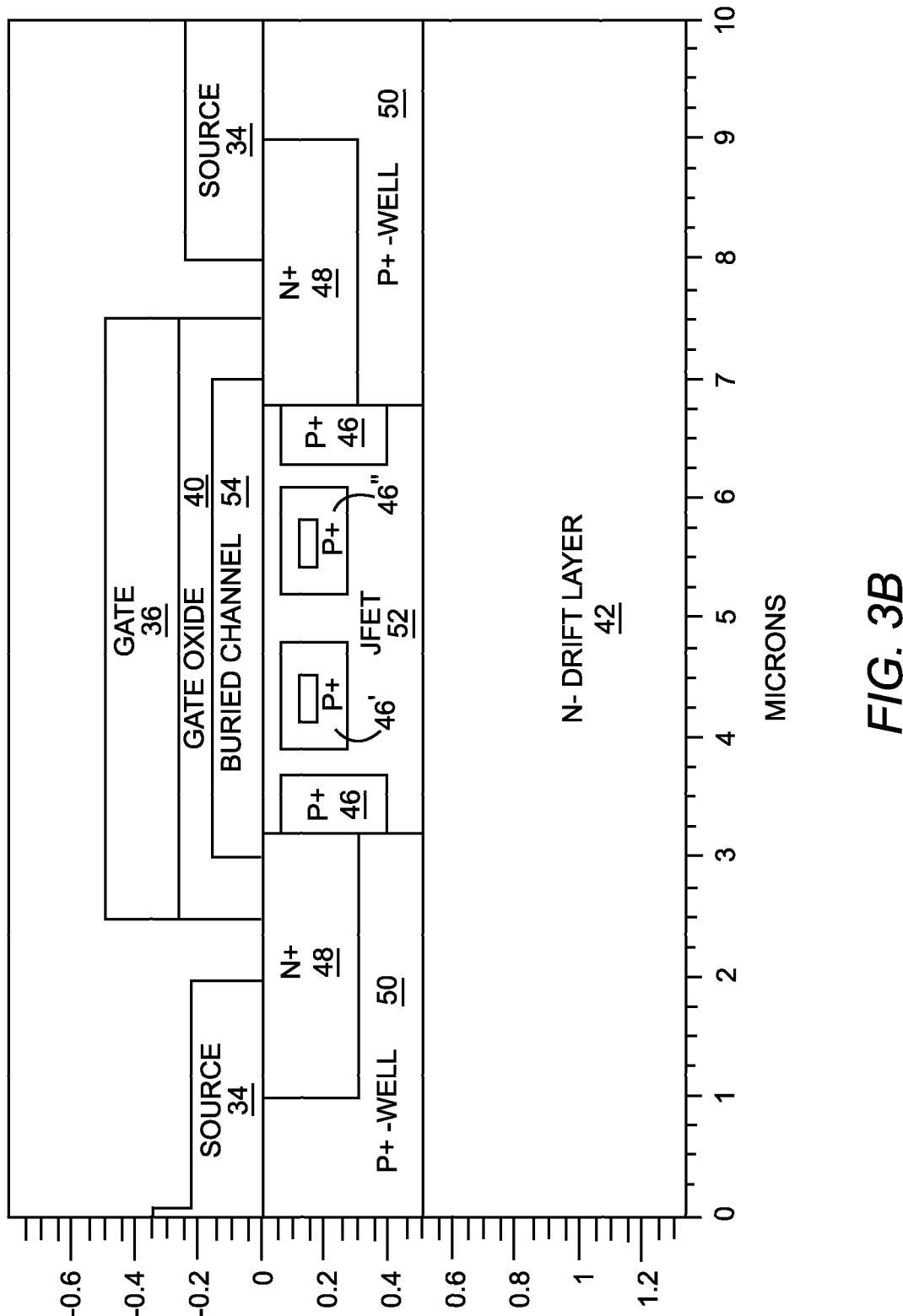


FIG. 3A

4/8



5/8

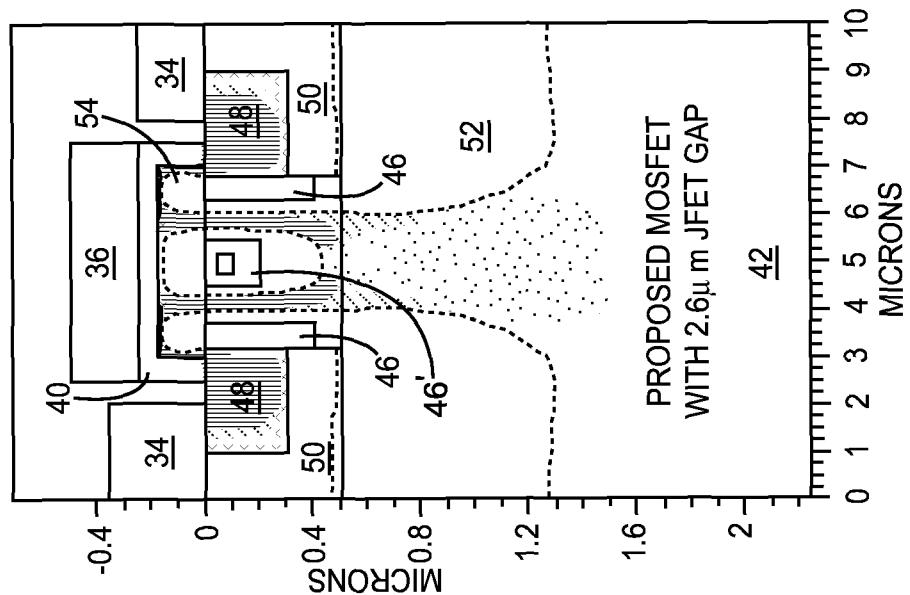


FIG. 4C

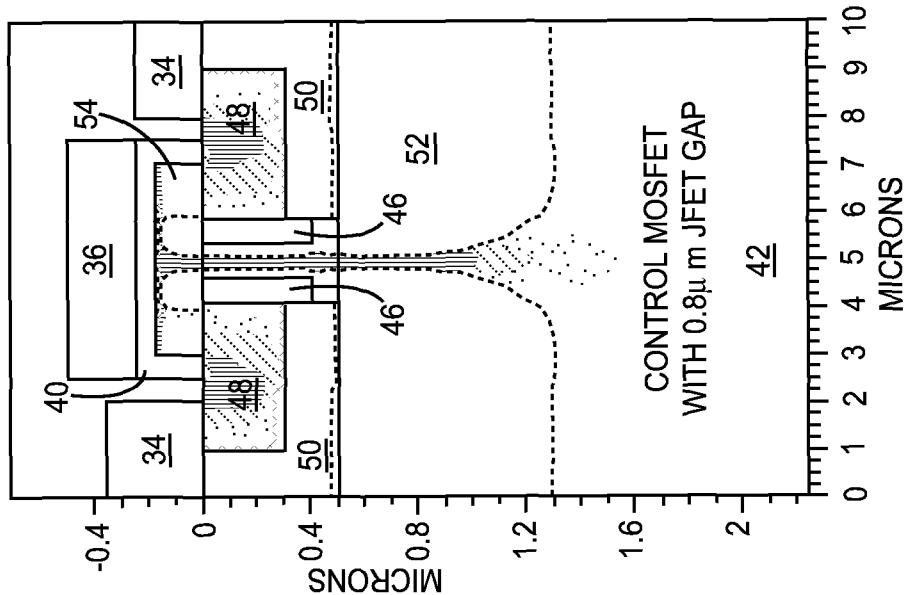


FIG. 4B

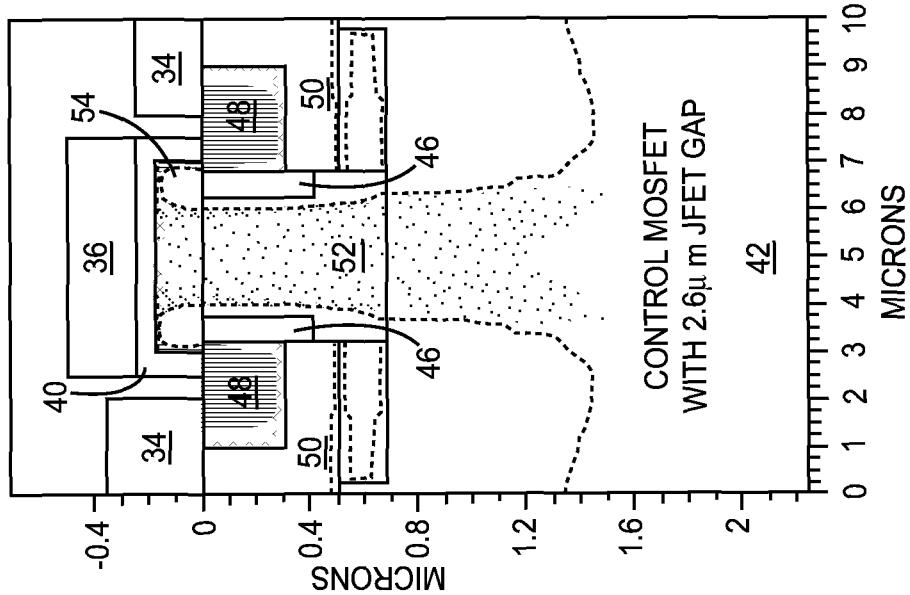


FIG. 4A

6/8

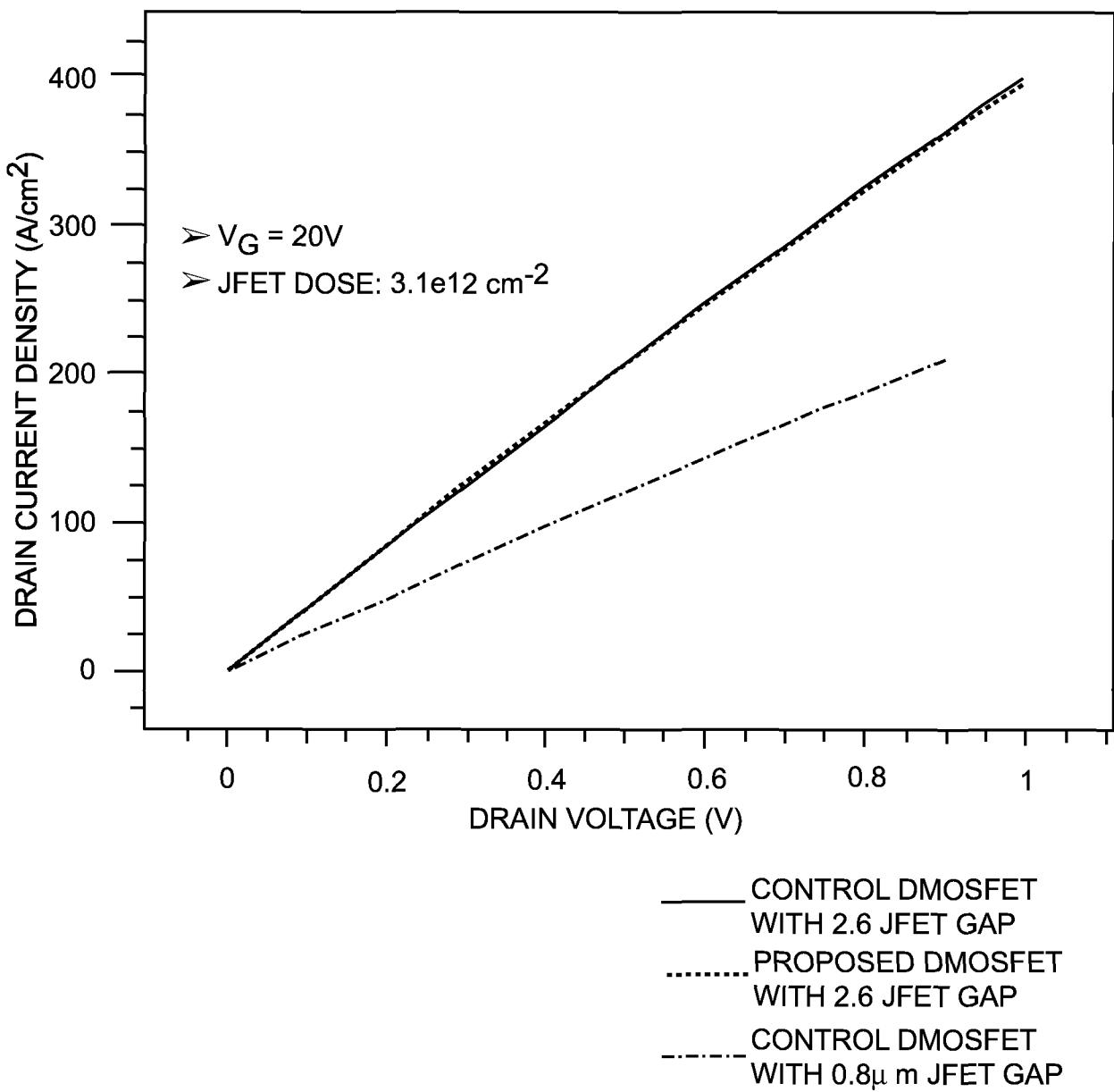


FIG. 5

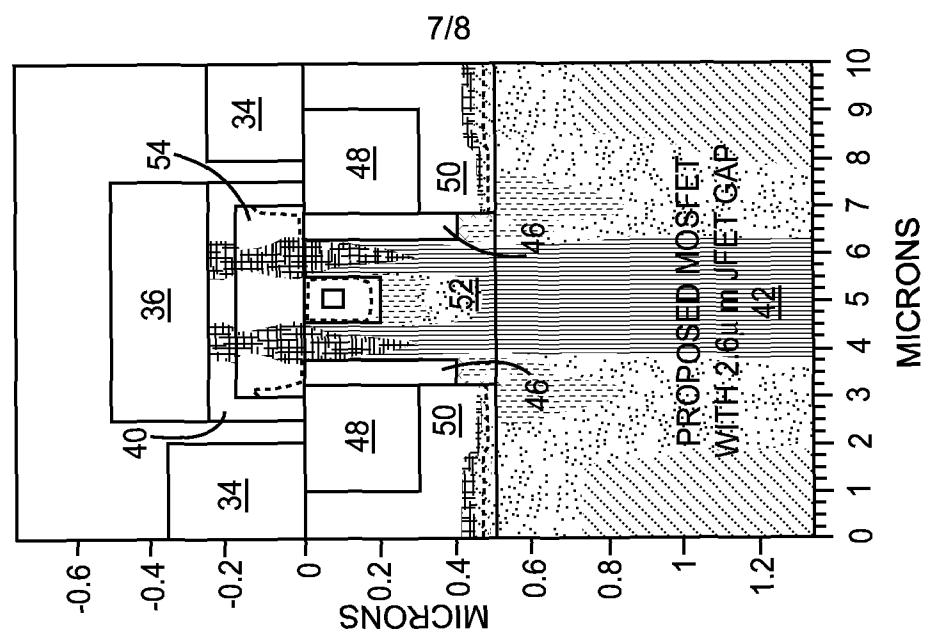


FIG. 6C

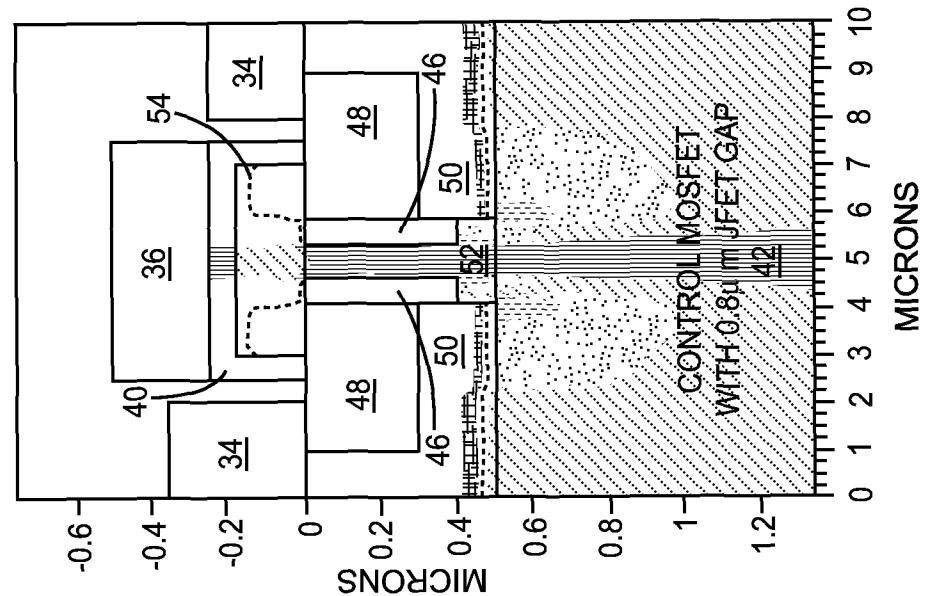


FIG. 6B

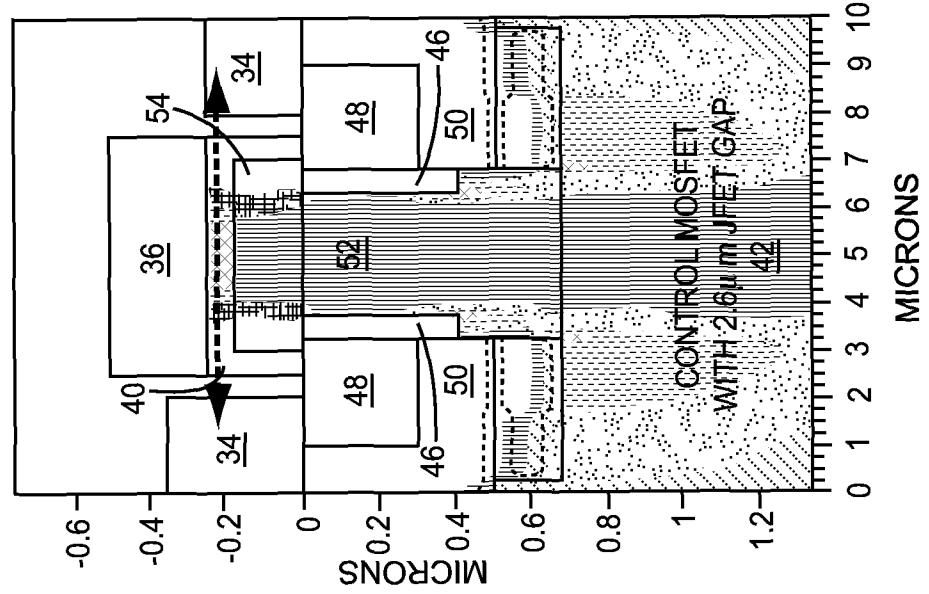


FIG. 6A

8/8

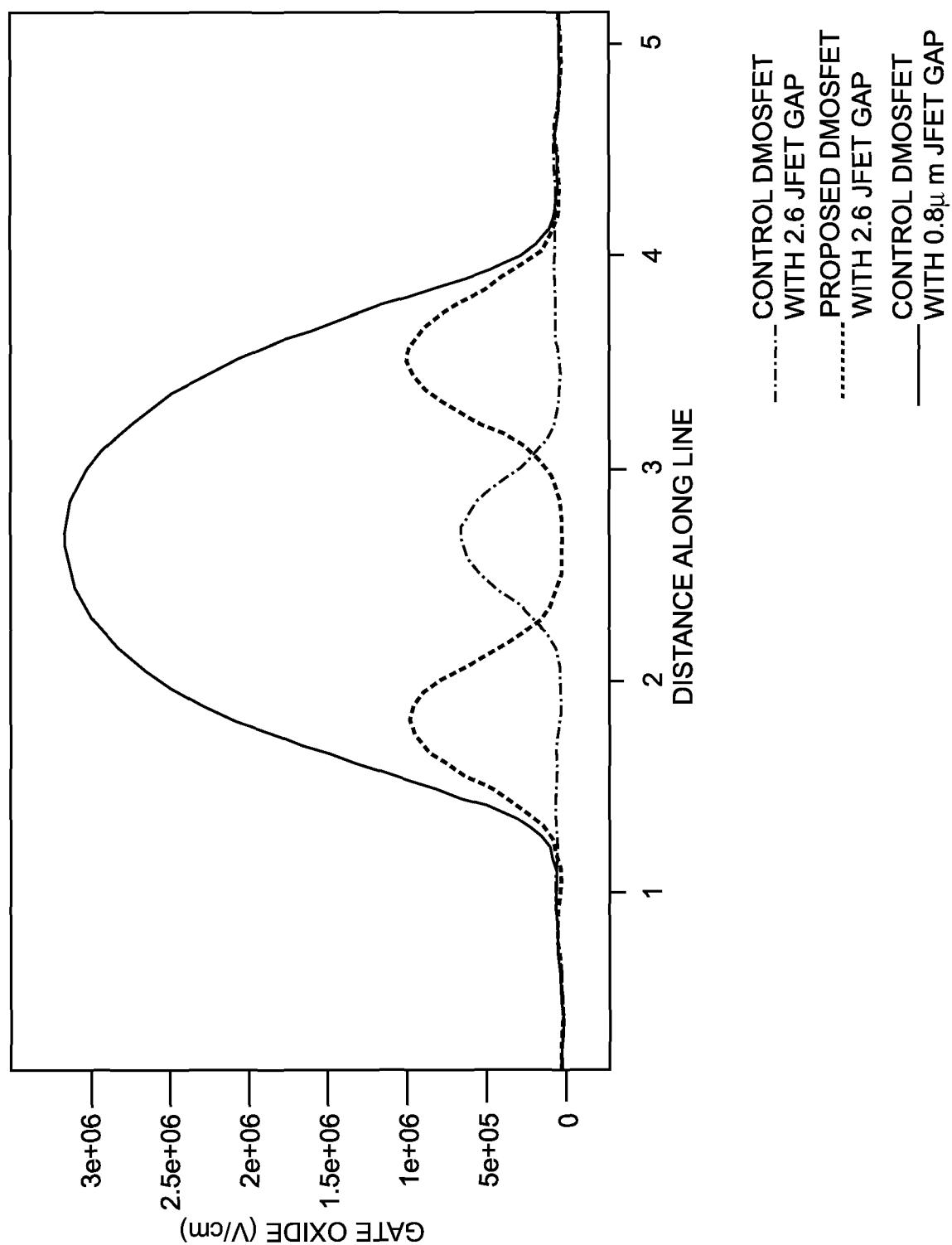


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/073093

A. CLASSIFICATION OF SUBJECT MATTER				
INV.	H01L29/78	H01L29/739	H01L29/749	H01L29/06
	H01L21/331	H01L21/332		H01L21/336
ADD.	H01L29/16			

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/235942 A1 (NAKAMURA K ET AL) 25 December 2003 (2003-12-25)	1-7
A	paragraph [0042] - paragraph [0062]; figures 1-3 paragraph [0072]; figure 7	8-10, 13, 15-17, 21, 23-25, 29

X	US 2011/057202 A1 (KONO H ET AL) 10 March 2011 (2011-03-10)	1-7
A	paragraph [0018] - paragraph [0045]; figures 1,2 paragraph [0058] - paragraph [0061]; figure 9	8-11, 13-15, 17, 18, 20-23, 25, 26, 28, 29

	-/-	

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier application or patent but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 March 2014	01/04/2014
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3046	Authorized officer Morvan, Denis

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/073093

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 429 392 A2 (MATSUSHITA ELECTRIC IND CO LTD ET AL) 16 June 2004 (2004-06-16) paragraph [0048] - paragraph [0049]; figure 3 paragraph [0026] - paragraph [0038]; figures 1,2 -----	1,2, 4-14, 16-22, 24-29
X	EP 1 737 042 A1 (KANSAI ELECTRIC POWER CO) 27 December 2006 (2006-12-27) paragraph [0024] - paragraph [0025]; figure 2 paragraph [0035] paragraph [0032] - paragraph [0033]; figure 4 -----	1-29
A	JP H07 78978 A (TOYOTA CENTRAL RES & DEV) 20 March 1995 (1995-03-20) abstract; figures 1,2 -----	1,3, 8-10,13, 15,21, 23,29
1		

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No PCT/US2013/073093

Patent document cited in search report	Publication date	Patent family member(s)			Publication date
US 2003235942	A1	25-12-2003	JP 4537646 B2		01-09-2010
			JP 2004022693 A		22-01-2004
			US 2003235942 A1		25-12-2003

US 2011057202	A1	10-03-2011	JP 2011060930 A		24-03-2011
			US 2011057202 A1		10-03-2011
			US 2013137253 A1		30-05-2013

EP 1429392	A2	16-06-2004	CN 1505170 A		16-06-2004
			EP 1429392 A2		16-06-2004
			KR 20040047717 A		05-06-2004
			US 2004104429 A1		03-06-2004

EP 1737042	A1	27-12-2006	EP 1737042 A1		27-12-2006
			JP 4237086 B2		11-03-2009
			JP 2005268731 A		29-09-2005
			US 2007200150 A1		30-08-2007
			WO 2005091372 A1		29-09-2005

JP H0778978	A	20-03-1995	NONE		
