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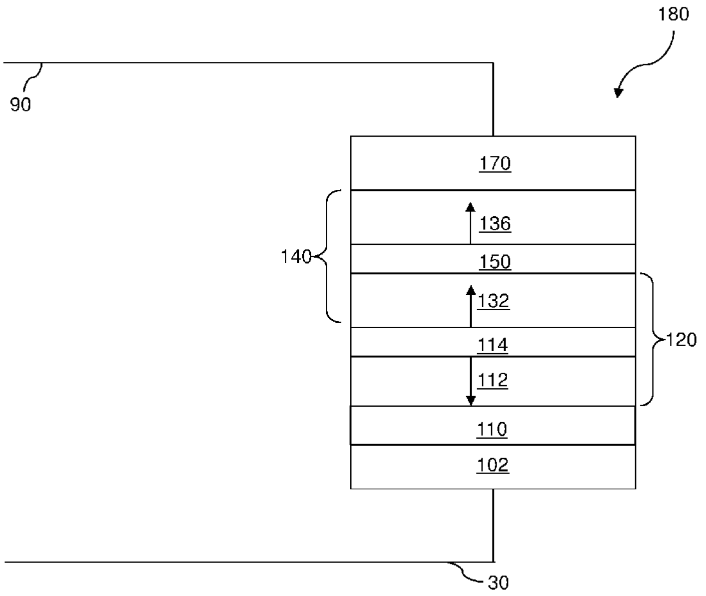

FIG. 2A

(57) **Abstract:** A magnetoresistive memory device includes a magnetic-exchange-coupled layer stack containing a free layer, a reference layer and an electrically conductive, non-magnetic interlayer exchange coupling layer located between the free layer and the reference layer, and an insulating spacer layer located in a series connection with the magnetic-exchange-coupled layer stack between a first electrode and a second electrode. The first electrode and the second electrode are configured to provide a programming voltage across the magnetic-exchange-coupled layer stack and the insulating spacer layer.

[Continued on next page]

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VOLTAGE-CONTROLLED INTERLAYER EXCHANGE COUPLING MAGNETORESISTIVE MEMORY DEVICE AND METHOD OF OPERATING THEREOF

RELATED APPLICATION

[0001] The present application claims the benefit of priority of U.S. Non-Provisional Patent Application Serial No. 16/250,403 filed on January 17, 2019, the entire content of which is incorporated herein by reference.

FIELD

[0002] The present disclosure relates generally to the field of magnetoresistive memory devices and specifically to a magnetoresistive memory device employing voltage-controlled interlayer exchange coupling to facilitate programming and methods of operating the same.

BACKGROUND

[0003] A magnetoresistive memory device can store information employing the difference in electrical resistance of a first configuration in which a free magnetization layer has a magnetization direction that is parallel to the magnetization of a reference magnetization layer and a second configuration in which the free magnetization layer has a magnetization direction that is antiparallel to the magnetization of the reference magnetization layer. Programming of the magnetoresistive memory device requires flipping of the direction of the magnetization of the free layer employing various external power source, which may be magnetic in nature or may employ a spin transfer mechanism.

[0004] Scalability of spin torque transfer magnetoresistive random access memory (STT-MRAM) devices require a higher than desired current for operation. Scalability of the STT-MRAM devices based on interfacial perpendicular magnetic anisotropy dictates a need to significantly enhance perpendicular magnetic anisotropy (PMA) to achieve required thermal stability for reliable information retention in MRAM devices. At the same time efficient magnetization manipulation is desired for low power consumption during writing information. The need to simultaneously have high energy barriers for retention and low energy barriers for efficient switching is a key challenge for systems with high PMA.

[0005] Voltage-controlled magnetic anisotropy (VCMA) is a more energy efficient method for magnetization switching since it is driven by voltage rather than by current. However, it is very challenging to achieve a large enough VCMA effect to overcome PMA. In addition, VCMA switching relies on precessional magnetization switching that has to be precisely controlled by the duration of the voltage pulse. This may result in large writing errors due to the distribution of magnetic properties in different memory cells.

SUMMARY

[0006] According to an aspect of the present disclosure, a magnetoresistive memory device includes a magnetic-exchange-coupled layer stack comprising a free layer, a reference layer and an electrically conductive, non-magnetic interlayer exchange coupling layer located between the free layer and the reference layer, and an insulating spacer layer located in a series connection with the magnetic-exchange-coupled layer stack between a first electrode and a second electrode. The first electrode and the second electrode are configured to provide a programming voltage across the magnetic-exchange-coupled layer stack and the insulating spacer layer.

[0007] According to another aspect of the present disclosure a method of operating a magnetoresistive memory device is provided. The device comprises a magnetic-exchange-coupled layer comprising a free layer, a reference layer and an electrically conductive, non-magnetic interlayer exchange coupling layer located between the free layer and the reference layer, and an insulating spacer layer located in a series connection with the magnetic-exchange-coupled layer stack between a first electrode and a second electrode. The method comprises applying a first polarity programming voltage between the first electrode and the second electrode across the magnetic-exchange-coupled layer stack and the insulating spacer layer to switch a magnetization of the free layer from a parallel state to an antiparallel state with the reference layer, and applying a second polarity programming voltage opposite to the first polarity voltage between the first electrode and the second electrode across the magnetic-exchange-coupled layer stack and the insulating spacer layer to switch the magnetization of the free layer from the antiparallel state to the parallel state with the reference layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 is a schematic diagram of a random access memory device including magnetoresistive memory cells of the present disclosure in an array configuration.

[0009] FIG. 2A illustrates a first configuration of an exemplary magnetoresistive memory cell according to an embodiment of the present disclosure.

[0010] FIG. 2B illustrates a second configuration of the exemplary magnetoresistive memory cell according to an embodiment of the present disclosure.

[0011] FIG. 3 schematically illustrates voltage induced changes in magnetic anisotropy energy for parallel and antiparallel configurations of the free layer in the exemplary magnetoresistive memory cells of the present disclosure.

[0012] FIG. 4A illustrates a third configuration of the exemplary magnetoresistive memory cell according to an embodiment of the present disclosure.

[0013] FIG. 4B illustrates a fourth configuration of the exemplary magnetoresistive memory cell according to an embodiment of the present disclosure.

[0014] FIG. 5A illustrates a change in the energy difference between the ferromagnetic configuration and the antiferromagnetic configuration as a function of applied electrical field across an insulating spacer layer for a case in which the metallic interlayer exchange coupling layer is two atomic layers thick according to a simulation of device characteristics of the exemplary magnetoresistive memory cell of the present disclosure.

[0015] FIG. 5B illustrates a change in the energy difference between the ferromagnetic configuration and the antiferromagnetic configuration as a function of applied electrical field across an insulating spacer layer for a case in which the metallic interlayer exchange coupling layer is three atomic layers thick according to a simulation of device characteristics of the exemplary magnetoresistive memory cell of the present disclosure.

[0016] FIG. 5C illustrates a change in the energy difference between the ferromagnetic configuration and the antiferromagnetic configuration as a function of applied electrical field across an insulating spacer layer for a case in which the metallic interlayer exchange coupling layer is four atomic layers thick according to a simulation of device characteristics of the exemplary magnetoresistive memory cell of the present disclosure.

[0017] FIG. 5D illustrates a change in the energy difference between the ferromagnetic configuration and the antiferromagnetic configuration as a function of applied electrical field across an insulating spacer layer for a case in which the metallic interlayer exchange coupling layer is five atomic layers thick according to a simulation of device characteristics of the exemplary magnetoresistive memory cell of the present disclosure.

[0018] FIG. 6 illustrates the dependence of the interlayer exchange coupling as a function of a lattice constant of magnesium oxide in the insulating spacer layer.

DETAILED DESCRIPTION

[0019] As discussed above, the embodiments of the present disclosure are directed to a magnetoresistive memory device employing voltage-controlled interlayer exchange coupling (VCEC) to facilitate programming the various aspects of which are described below. A VCEC MRAM device uses less energy for programming to induce the transition between an antiparallel state and a parallel state of the free layer than a corresponding STT-MRAM device and provides deterministic switching and higher accuracy than a corresponding VCMA MRAM device.

[0020] A VCEC MRAM device includes a stack containing an electrically conductive, non-magnetic interlayer exchange coupling layer located between the free and reference layers and an optional electrically insulating spacer layer, which acts as a resistor, located in series with the stack. The VCEC MRAM device is programmed by application of a voltage to the stack without applying (i.e., in the absence of) an external magnetic field. Thus, external magnets are preferably not used in the VCEC MRAM device. The state of the VCEC MRAM device can be sensed (i.e., read / determined) by utilizing the giant magnetoresistive (GMR) effect due to the presence of the non-magnetic, electrically conductive interlayer exchange coupling layer. In contrast, the state of the STT-MRAM device is sensed (i.e., read / determined) by the tunneling magnetoresistance (TMR) effect due to the presence of an electrically insulating tunneling barrier between the free and reference layers. Likewise, the VCMA MRAM device contains an insulating barrier layer between the free and reference layers. In contrast, the VCEC MRAM device preferably lacks an insulating tunneling barrier layer between the free and reference layers in the stack to promote exchange coupling between the ferromagnetic layers.

[0021] According to an aspect of the present disclosure, voltage-controlled interlayer exchange coupling (VCEC) is employed to reduce the energy barrier for transition between two magnetoresistive states. The inventors recognized that the VCEC effect can be at least one order of magnitude larger than the VCMA effect. Further, the polarity of the VCEC effect can be reversed by switching voltage polarity, thereby providing deterministic switching of the free layer in a magnetoresistive memory cell, in contrast to the VCMA MRAM devices which operate essentially as a toggle switch.

[0022] The drawings are not drawn to scale. Multiple instances of an element may be duplicated where a single instance of the element is illustrated, unless absence of duplication of elements is expressly described or clearly indicated otherwise. Same reference numerals refer to the same element or to a similar element. Elements having the same reference numerals are presumed to have the same material composition unless expressly stated otherwise. Ordinals such as “first,” “second,” and “third” are employed merely to identify similar elements, and different ordinals may be employed across the specification and the claims of the instant disclosure. As used herein, a first element located “on” a second element can be located on the exterior side of a surface of the second element or on the interior side of the second element. As used herein, a first element is located “directly on” a second element if there exist a physical contact between a surface of the first element and a surface of the second element. As used herein, an “in-process” structure or a “transient” structure refers to a structure that is subsequently modified.

[0023] As used herein, a “layer” refers to a material portion including a region having a thickness. A layer may extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer may be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer may be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer may extend horizontally, vertically, and/or along a tapered surface. A substrate may be a layer, may include one or more layers therein, and/or may have one or more layer thereupon, thereabove, and/or therebelow.

[0024] As used herein, a “layer stack” refers to a stack of layers. As used herein, a “line” or a “line structure” refers to a layer that has a predominant direction of extension, i.e., having a direction along which the layer extends the most.

[0025] Referring to FIG. 1, a schematic diagram is shown for a magnetoresistive memory device 500 including multiple magnetoresistive memory cells 180 of embodiments of the present disclosure. In one embodiment, the magnetoresistive memory device 500 can be configured as a magnetoresistive random access memory (MRAM) device containing a two-dimensional array or a three-dimensional array of magnetoresistive memory cell 180 of the embodiments of the present disclosure. As used herein, a "random access memory device" refers to a memory device containing memory cells that allow random access, e.g., access to any selected memory cell upon a command for reading the contents of the selected memory cell.

[0026] The magnetoresistive memory device 500 can include a memory array region 550 containing an array of the respective magnetoresistive memory cells 180 located at the intersection of the respective word lines 30 and bit lines 90. The magnetoresistive memory device 500 may also contain a row decoder 560 connected to the word lines 30, a combination of a programming and sense circuitry 570 (which can include programming transistors, sense amplifiers, and other bit line control circuitry) connected to the bit lines 90, a column decoder 580 connected to the bit lines 90 through the programming and sense circuitry 570, and a data buffer 590 connected to the programming and sense circuitry 570. Multiple instances of the magnetoresistive memory cells 180 are provided in an array configuration that forms the magnetoresistive memory device 500. As such, each of the magnetoresistive memory cells 180 can be a two-terminal device including a respective first electrode and a respective second electrode. It should be noted that the location and interconnection of elements are schematic and the elements may be arranged in a different configuration. Further, a magnetoresistive memory cell 180 may be manufactured as a discrete device, i.e., a single isolated device.

[0027] FIGS. 2A and 2B illustrate a first configuration and a second configuration of an exemplary magnetoresistive memory cell 180 according to an embodiment of the present disclosure, respectively. The magnetoresistive memory cell 180 can include a series connection of a magnetic-exchange-coupled layer stack 140 and an optional first insulating spacer layer 110, which functions as a resistor during programming and reading operations. As used herein, a "magnetic-exchange-coupled layer stack" includes a layer stack including a first ferromagnetic layer (e.g., reference layer), a magnetic exchange coupling layer, and a second ferromagnetic layer (e.g., free layer). The stack is configured such that the magnetic exchange coupling layer provides magnetic exchange coupling between the first ferromagnetic layer and the second ferromagnetic layer.

[0028] The magnetic-exchange-coupled layer stack 140 can include a first reference layer 132 having a fixed magnetization direction, a free layer 136 having an easy axis of magnetization that is parallel or antiparallel to the fixed magnetization direction, and an electrically conductive, non-magnetic interlayer exchange coupling layer 150 located between the first reference layer 132 and the free layer 136. Preferably, the coupling layer comprises a metallic material, such as a pure metal or metal alloy, to provide a metallic interlayer exchange coupling layer 150. According to an aspect of the present disclosure, the metallic interlayer exchange coupling layer 150 provides a variable magnetic exchange coupling of which the magnitude and the polarity depends on the magnitude and polarity of a voltage bias between the first reference layer 132 and the free layer 136. The first insulating spacer layer 110 includes an electrically insulating material in a series connection with the magnetic-exchange-coupled layer stack. As used herein, an "electrically insulating material" refers to a material having electrical conductivity less than 1.0×10^{-5} S/m. The first insulating spacer layer 110 acts as a resistor by reducing the electrical conductance of the magnetoresistive memory cell 180 so that the current flow and the power consumption of the magnetoresistive memory cell 180 is limited during operation.

[0029] The magnetoresistive memory cell 180 can include a first nonmagnetic electrode layer 102 and a second nonmagnetic electrode layer 170. The magnetic-exchange-coupled layer stack 140 and the first insulating spacer layer 110 are electrically connected in series between the first nonmagnetic electrode layer 102 and the second nonmagnetic electrode layer 170.

[0030] The first insulating spacer layer 110 can include any tunneling barrier material such as an electrically insulating material, for example magnesium oxide. Other suitable resistor materials, such as insulating materials, for example silicon oxide or aluminum oxide may also be used instead of or in addition to magnesium oxide. The thickness of the first insulating spacer layer 110 can be 0.7 nm to 1.3 nm, such as about 1 nm. In one embodiment, the first insulating spacer layer 110 preferably comprises, and/or consists essentially of, a magnesium oxide layer.

[0031] The first reference layer 132 can include a Fe layer, a Co layer, a Ni layer, a Co/Ni multilayer structure or a Co/Pt multilayer structure. The first reference layer 132 can additionally include a thin non-magnetic layer comprised of tantalum having a thickness of 0.2 nm ~ 0.5 nm and a thin CoFeB layer (having a thickness in a range from 0.5 nm to 3 nm). In one embodiment, the first reference layer 132 can comprise, and/or consist of, a first iron layer having a thickness in a range from two atomic layers (i.e., monolayers) of iron to five atomic layers of iron, such as three to four atomic layers of iron. For example, the first reference layer 132 can have a thickness of 2 to 7 nm, such as 3 to 6 nm.

[0032] The free layer 136 can include Fe, Co, Ni, or a ferromagnetic alloy including at least one of Fe, Co, and Ni (such as CoFeB) at a composition that provides positive uniaxial magnetic anisotropy. Alternatively, the free layer 136 can include a magnetic Heusler alloy, such as an alloy that does not include Fe, Co or Ni. In one embodiment, the free layer 136 can comprise, and/or consist essentially of, a second iron layer having a thickness in a range from two atomic layers of iron to forty atomic layers of iron, such as three to fifteen atomic layers of iron. For example, the free layer 136 can have a thickness of 2 to 30 nm, such as 3 to 12 nm.

[0033] The configuration in which the first reference layer 132 and the free layer 136 have respective positive uniaxial magnetic anisotropy provides bistable magnetization states for the free layer 136. The bistable magnetization states include a parallel state in which the free layer 136 has a magnetization (e.g., magnetization direction) that is parallel to the fixed vertical magnetization (e.g., magnetization direction) of the first reference layer 132, and an antiparallel state in which the free layer 136 has a magnetization (e.g., magnetization direction) that is antiparallel to the fixed vertical magnetization (e.g., magnetization direction) of the first reference layer 132.

[0034] The interlayer exchange coupling layer 150 includes an electrically conductive, non-magnetic material that can provide a voltage-dependent exchange coupling between the first reference layer 132 and the free layer 136 such that energy levels of a parallel state and an antiparallel state of the free layer 136 shift in opposite directions upon application of a voltage between the electrode layers 102 and 170 (e.g., upon application of a voltage between the first reference layer 132 and the free layer 136).

[0035] Suitable materials for the metallic interlayer exchange coupling layer 150 include non-magnetic electrically conductive materials, such as metallic materials (e.g., elemental metals and metal alloys), for example, including but not restricted to, Au, Cu, Cr, and/or Al and their alloys. In one embodiment, the metallic interlayer exchange coupling layer 150 can consist essentially of a metallic element selected from Au, Cu, Cr, and Al. In one embodiment, the interlayer exchange coupling layer 150 can have a thickness in a range from one atomic layer (i.e., monolayer) of the metallic element to five layers of the metallic element, such as from two to four atomic layers. For example, the interlayer exchange coupling layer 150 can have a thickness of 0.1 to 7 nm, such as 0.3 to 5 nm.

[0036] In one embodiment, the first reference layer 132 may be provided as a component of a first synthetic antiferromagnetic structure (SAF structure) 120. The first SAF structure

120 can include the first reference layer 132, a first fixed ferromagnetic layer 112 having a magnetization that is antiparallel to the fixed vertical magnetization, and a first antiferromagnetic coupling layer 114 located between the first reference layer 132 and the first fixed ferromagnetic layer 112 facing the first side of the first reference layer 132 opposite to the second side of the first reference layer 132 which faces the interlayer exchange coupling layer 150. The first antiferromagnetic coupling layer 114 has a thickness that induces an antiferromagnetic coupling between the first reference layer 132 and the first fixed ferromagnetic layer 112. In other words, the first antiferromagnetic coupling layer 114 can lock in the antiferromagnetic alignment between the magnetization of the first reference layer 132 and the magnetization of the first fixed ferromagnetic layer 112 to lock in place the magnetizations of the first reference layer 132 and the magnetization of the first fixed ferromagnetic layer 112. In one embodiment, the antiferromagnetic coupling layer can include ruthenium and can have a thickness in a range from 0.3 nm to 1 nm. Generally, the first SAF structure 120 includes the first reference layer 132, the first fixed ferromagnetic layer 112 having a magnetization that is antiparallel to the fixed magnetization direction of the first reference layer 132, and the first antiferromagnetic coupling layer 114 located between, and providing an antiferromagnetic coupling between, the first reference layer 132 and the first fixed ferromagnetic layer 112.

[0037] In one embodiment, a nonmagnetic electrode layer is located directly on a surface of the first insulating spacer layer 110, which may be the first nonmagnetic electrode layer 102 illustrated in FIG. 2A or the second nonmagnetic electrode layer 170 illustrated in FIG. 2B. The first nonmagnetic electrode layer 102 can be located on the side of the first SAF structure 120, and the second nonmagnetic electrode layer 170 can be located on the side of the free layer 136.

[0038] In one embodiment, a nonmagnetic electrode layer (such as the second nonmagnetic electrode layer 170) may be located directly on the free layer 136 as illustrated in FIG. 2A. In one embodiment, the first fixed ferromagnetic layer 112 can be in contact with the first insulating spacer layer 110, as illustrated in FIG. 2A. In one embodiment, the magnetoresistive memory cell 180 can include a nonmagnetic electrode layer (such as the first nonmagnetic electrode layer 102) in contact with the first fixed ferromagnetic layer 112, as illustrated in FIG. 2B.

[0039] Due to RKKY type of interactions, interlayer exchange coupling (IEC) exhibits oscillatory behavior as a function of the non-magnetic interlayer exchange coupling layer 150 thickness. Therefore the thickness of the non-magnetic interlayer exchange coupling layer 150 can be selected alone or in combination with the in-plane strain to achieve negligible IEC in the absence of applied voltage, while maintaining finite voltage induced interlayer exchange coupling.

[0040] Referring to FIG. 3, the VCEC based MRAM cell 180 works as follows. In the absence of applied voltage between the electrode layers 102, 170, IEC is zero or very small (i.e., close to zero). Magnetic anisotropy can be either perpendicular or in-plane since interlayer exchange coupling is not determined by the spin-orbit coupling. Applied voltage between the electrode layers 102, 170 results in a finite IEC biasing of the barrier. Thus, a large enough applied voltage leads to magnetization switching of the free layer 136. This control of the magnetization is deterministic because switching of voltage polarity reverses the sign of IEC. Written information can be read by measuring the electrical resistance of the MRAM cell 180. The resistance depends on the relative orientation of free layer 136 and first reference layer 132 magnetizations through the GMR effect. Since the GMR effect is lower than the TMR effect, the read signal of the VCEC based memory device is lower compared to a VCMA based memory device. However it is also possible to read information through the TMR effect in the VCEC based memory device by adding another resistor (e.g., barrier) layer and reference layer, which results in a double barrier magnetic tunneling junction (MTJ) as will be described in reference to FIGS. 4A and 4B below.

[0041] Thus, the VCEC based memory device (e.g., MRAM cell 180) is programmed by application of a positive or negative voltage to the device in absence of an external magnetic field using the voltage dependent interlayer exchange coupling, and is read by application of a voltage using the GMR or TMR effect depending on the device structure. For example, as shown in FIG. 3, application of a positive voltage switches the free layer 136 into the parallel state (P) with the first reference layer 132, while application of a negative voltage switches the free layer into the antiparallel state (AP) with the first refence layer. Thus, the applied voltage biases the energy barrier between the parallel and the antiparallel configurations. Reversing the voltage polarity deterministically switches the free layer 136 between the parallel state and antiparallel state. The IEC between the free layer 136 and the first reference layer 132 is zero or close to zero without applied voltage while it has a sufficiently large enough voltage induced part to overcome magnetic anisotropy of the free layer 136.

[0042] Optionally, each MRAM cell 180 can include a dedicated steering device, such an access transistor or diode configured to activate a respective stack 140 upon application of a suitable voltage to the steering device. The steering device may be electrically connected between the stack 140 and one of the respective word lines 30 or bit lines 90 of the respective MRAM cell 180. For example, the steering device may be connected between a word line 30 or bit line 90 and the respective electrode 102, 170 of the MRAM cell 180. In one embodiment, the word lines 30 provide signals to the first electrodes 102 and the bit lines 90 provide signals to the second electrodes 170 of the MRAM cells 180 either directly or through a steering device.

[0043] In one embodiment, the polarity of the voltage applied to the word line 30 can be changed depending on the polarity of the magnetization state to be programmed in the free layer 136. For example, a voltage of a first polarity can be applied to the word line 30 (with respect to the bit line 90) during a transition from an antiparallel state to a parallel state, and a voltage of a second polarity (which is the opposite of the first polarity) can be applied to the word line 30 during a transition from a parallel state to an antiparallel state. Further, variations in the circuitry for activating the stack 140 are also contemplated herein.

[0044] The programming and sense circuitry 570 can include a programming circuitry configured to apply a programming voltage pulse selected from a positive voltage pulse and a negative voltage pulse across the series connection of the magnetic-exchange-coupled layer stack 140 and the first insulating spacer layer 110 in a magnetoresistive memory cell 180. The magnitude of the programming voltage pulse can be selected to induce a transition into a different magnetic state of the free layer 136 in the selected magnetoresistive memory cell 180. For example, the magnitude of the programming voltage pulse can be selected such that the energy level of intermediate states between a parallel state and an antiparallel state illustrated in FIG. 3 is lower than the energy level of the initial magnetic state (which can be a parallel state or an antiparallel state) and higher than the energy level of the final magnetic state (i.e., a target magnetic state that is the opposite of the initial state) of the free layer 136. The programming voltage pulse can have an absolute magnitude in a range from 1 V to 10 V, such as from 1.5 V to 5.0 V, although lesser and greater absolute magnitudes of the programming voltage pulse may also be employed. The duration of the programming voltage pulse may be in a range from 1 ns to 30 ns, such as from 2 ns to 10 ns, although shorter and longer programming voltage durations can also be employed.

[0045] The magnetic coupling through the metallic interlayer exchange coupling layer 150 is voltage-controlled, and thus, is herein referred to as voltage-controlled exchange coupling (VCEC). The direction for the energy level shift for the parallel state of the magnetization of the free layer 136 due to the VCEC is the opposite of the direction for the energy level shift for the antiparallel state of the magnetization of the free layer 136 due to the VCEC. The magnitude of the energy level shift for the parallel state of the magnetization of the free layer 136 due to the VCEC can be the same, or substantially the same, as the energy level shift for the antiparallel state of the magnetization of the free layer 136 due to the VCEC. The direction for the energy level shift for the magnetic state of the magnetization of the free layer 136 due to the VCEC is determined by the sign of the exchange coupling provided by the metallic interlayer exchange coupling layer 150 and the polarity of the applied external bias voltage.

[0046] According to an aspect of the present disclosure, the applied voltage biases the energy barrier between the parallel state and the antiparallel state of the magnetization of the free layer 136. Reversing voltage polarity deterministically switches between the parallel state and the antiparallel state. In one embodiment, the magnetoresistive memory cell 180 can be designed such that the interlayer exchange coupling between free layer 136 and the first reference layer 132 is zero or substantially zero in the absence of external bias voltage across the first nonmagnetic electrode layer 102 and the second nonmagnetic electrode layer 170. Further, the magnetoresistive memory cell 180 can be designed such that the interlayer exchange coupling between free layer 136 and the first reference layer 132 is large enough to overcome the magnetic anisotropy of the free layer 136 wherein an external bias voltage is applied across the first nonmagnetic electrode layer 102 and the second nonmagnetic electrode layer 170 during operation of the magnetoresistive memory device 500. Relative orientation of the magnetizations between the free layer 136 and the first reference layer 132 can be controlled with the VCEC effect.

[0047] The programming and sense circuitry 570 can include a sense circuitry configured to apply a sense voltage pulse across a selected magnetoresistive memory cell 180. The magnitude of the sense voltage pulse is selected to prevent a change in a magnetic state of the free layer in the selected instance of the magnetoresistive memory cell. The sense voltage pulse can have an absolute magnitude in a range from 0.1 V to 4 V, such as from 0.3 V to 1.5 V, although lesser and greater magnitudes of the sense voltage pulse may also be employed. The duration of the sense voltage pulse may be in a range from 5 ns to 300 ns, such as from 10 ns to 50 ns, although shorter and longer programming voltage durations can also be employed.

[0048] In one embodiment, the information stored in each magnetoresistive memory cell 180 can be sensed through the giant magnetoresistive (GMR) effect, which offers differential conductance through a magnetoresistive memory cell 180 depending on the relative orientation of the magnetization of the free layer 136 and the magnetization of the first reference layer 132.

[0049] Referring to FIGS. 4A and 4B, an additional structure may be employed to stabilize the preferred direction of magnetization for the free layer 136 along the vertical direction. For example, a second synthetic antiferromagnetic (SAF) structure may be employed to lower the magnetic anisotropy energy for the parallel state and the antiparallel state of the magnetization of the free layer 136 relative to magnetization states that are not parallel or antiparallel to the fixed magnetization direction of the first reference layer 132. In this case, the information stored in each magnetoresistive memory cell 180 may be sensed through tunneling magnetoresistive (TMR) effect.

[0050] FIGS. 4A and 4B illustrate a third configuration and a fourth configuration of the magnetoresistive memory cell 180 of the present disclosure, respectively. The third configuration for the magnetoresistive memory cell 180 of FIG. 4A can be derived from the first configuration for the magnetoresistive memory cell 180 illustrated in FIG. 2A by inserting a series connection of a second insulating spacer layer 155 and a second synthetic antiferromagnetic (SAF) structure 160 between the magnetic-exchange-coupled layer stack

140 and the second nonmagnetic electrode layer 170. The second insulating spacer layer 155 can contact the free layer 136.

[0051] In the magnetoresistive memory cell 180 of FIG. 4A, the second synthetic antiferromagnetic structure includes an additional reference layer (which is herein referred to as a second reference layer 166), an additional fixed ferromagnetic layer (which is herein referred to as a second fixed ferromagnetic layer 162) having a magnetization that is antiparallel to a magnetization direction of the additional reference layer, and an additional antiferromagnetic coupling layer (which is herein referred to as a second antiferromagnetic coupling layer 164) located between, and providing an antiferromagnetic coupling between the additional reference layer and the additional fixed ferromagnetic layer. The second insulating spacer layer 155 can be located between the second reference layer 166 and the free layer 136.

[0052] The fourth configuration for the magnetoresistive memory cell 180 of FIG. 4B can be derived from the second configuration for the magnetoresistive memory cell 180 illustrated in FIG. 2B by providing the above described additional synthetic antiferromagnetic (SAF) structure (which is herein referred to as a second SAF structure 160) and the interlayer exchange coupling layer 150 between the first insulating spacer layer 110 and the free layer 136. In this configuration, the magnetic-exchange-coupled layer stack 140 includes the free layer 136, the second reference layer 166 and the interlayer exchange coupling layer 150 located between the free layer 136 and the second reference layer 166. The second insulating spacer layer 155 is provided between the free layer 136 and the first reference layer 132.

[0053] The second insulating spacer layer 155 can include any tunneling barrier material such as an electrically insulating material, for example magnesium oxide. The thickness of the second insulating spacer layer 155 can be 0.7 nm to 1.3 nm, such as about 1 nm. In one embodiment, the second insulating spacer layer 155 comprises, and/or consists essentially of, a magnesium oxide layer.

[0054] In one embodiment, the second nonmagnetic electrode layer 170 can be in contact with the second synthetic antiferromagnetic structure 160, as illustrated in FIG. 4A. In one embodiment, the first insulating spacer layer 110 can be located on the second synthetic antiferromagnetic structure 160, and the second nonmagnetic electrode layer 170 can be located on the first insulating spacer layer 110, as illustrated in FIG. 4B. In one embodiment, the magnetoresistive memory cell 180 can include a nonmagnetic electrode layer (such as the first nonmagnetic electrode layer 102) in contact with the first fixed ferromagnetic layer 112 as illustrated in FIG. 4B.

[0055] The programming of the magnetoresistive memory cells 180 of FIGS. 4A and 4B can be performed in the same manner as the programming of the magnetoresistive memory cells 180 of FIGS. 2A and 2B. Optionally, the magnitude of the programming voltage pulse may be increased to compensate for a voltage drop across the second insulating spacer layer 155 in the magnetoresistive memory cells 180 of FIGS. 4A and 4B.

[0056] The sensing of the magnetic states of the magnetoresistive memory cells 180 of FIGS. 4A and 4B can be performed in the same manner as the sensing of the magnetic states of the magnetoresistive memory cells 180 of FIGS. 2A and 2B with the modification that tunneling magnetoresistive measurements can be employed in lieu of giant magnetoresistive measurements. The sense voltages may be adjusted accordingly.

[0057] FIGS. 5A – 5D illustrate simulation results for a change in the energy difference between the ferromagnetic configuration and antiferromagnetic configuration as a function of applied electrical field across the first insulating spacer layer 110 for various materials and thicknesses of the metallic interlayer exchange coupling layer 150. FIG. 5A corresponds to the case in which the metallic interlayer exchange coupling layer 150 is two atomic layers thick; FIG. 5B corresponds to the case in which the metallic interlayer exchange coupling layer 150 is three atomic layers thick; FIG. 5C corresponds to the case in which the metallic interlayer exchange coupling layer 150 is four atomic layers thick; and FIG. 5D corresponds to the case in which the metallic interlayer exchange coupling layer 150 is five atomic layers thick. In each figure, the free layer 136 and the first reference layer 132 each comprise three monolayer thick iron layers. The results for cells containing Al, Cu and Au interlayer exchange coupling layers 150 are labeled in each figure.

[0058] The voltage-controlled exchange coupling (VCEC) energy (which is also referred to as voltage-controlled interlayer exchange coupling energy) is the difference (represented as $\Delta E(E) - \Delta E(0)$, in which $\Delta E = E_{AP} - E_P$) between the energy for the parallel alignment between the first reference layer 132 and the free layer 136 and the energy for the antiparallel alignment between the first reference layer 132 and the free layer 136. The voltage-controlled exchange coupling energy is linearly dependent on the applied external bias voltage across the first insulating spacer layer 110. Changing the polarity of the applied external bias voltage across the first insulating spacer layer 110 changes the sign of the voltage-controlled exchange coupling energy.

[0059] The external electrical bias voltage is applied between the first nonmagnetic electrode layer 102 and the second nonmagnetic electrode layer 170, a predominant portion (such as 99 %) of which is applied across the first insulating spacer layer 110 in the first and second configurations, or across the first and second insulating spacer layers (110, 155) in the third and fourth configurations.

[0060] The VCEC coefficient of proportionality between the voltage-controlled exchange coupling and the electrical field strength across the first insulating spacer layer 110 is tabulated as a function of the material of the metallic interlayer exchange coupling layer 150 and as a function of the thickness of the metallic interlayer exchange coupling layer 150 in Table 1. In other words, the VCEC coefficient is calculated as the total energy difference between parallel and antiparallel orientation of free and reference layers for different values of applied electric field, and exhibits linear dependence with voltage. Changing voltage polarity reverses sign of exchange coupling and IEC depends on the thickness of the interlayer exchange coupling layer 150.

[0061] Table 1 below shows the VCEC coefficient of proportionality in units of pJ/Vm between the voltage-controlled exchange coupling and the electrical field strength across the first insulating spacer layer 110 for various materials and thicknesses of the metallic interlayer exchange coupling layer 150 in the magnetoresistive memory cells 180 of embodiments present disclosure. The free layer 136 includes three monolayers of Fe, the first reference layer 132 includes three monolayers of Fe, and the first insulating spacer layer 110 includes MgO in the simulations.

TABLE 1

Number of Monolayers	Au	Cu	Al	Cr
1	2.0	0.7	-9.0	-1.2
2	-3.1	3.8	-12.0	-0.8
3	-4.0	-3.7	3.3	-4.2
4	-0.35	3.6	3.2	1.1
5	0.85	0.1	2.0	-1.0

[0062] According to an aspect of the present disclosure, the zero voltage exchange coupling energy is dependent on the strain in the first insulating spacer layer 110 and, if present, on the strain in the second insulating spacer layer 155. FIG. 6 shows the dependence of the interlayer exchange coupling as a function of the lattice constant of magnesium oxide in the first insulating spacer layer 110 calculated for a system with 4 monolayers of Al.

[0063] The interlayer exchange coupling in the absence of an external bias voltage strongly depends on the in-plane lattice constant (a0) of the first insulating spacer layer 110, which can be controlled by the strain. In the case where MgO is employed for the first insulating spacer layer 110, the interlayer exchange coupling in the absence of an external bias voltage is ferromagnetic for the equilibrium lattice constant of MgO (a_0 = 2.866 Angstroms). The interlayer exchange coupling becomes antiferromagnetic for larger and smaller lattice constants a_0. According to an aspect of the present disclosure, the lattice constant of the first insulating spacer layer 110, and/or the lattice constant of the second insulating spacer layer 155, if present, can be tuned to provide zero interlayer exchange coupling in the absence of an applied electrical bias voltage across the first nonmagnetic electrode layer 102 and the second nonmagnetic electrode layer 170. The value of a_0 can be tuned to be about 2.85 Angstrom to achieve an IEC value of about zero.

[0064] In contrast, the VCEC coefficient only weakly depends on the lattice constant of the first and/or second insulating spacer layers (110, 155) for lattice constants smaller than the equilibrium lattice constant. In the case where MgO is employed for an insulating spacer layer, the VCEC in the absence of an applied external voltage can be large with a reversed sign for large lattice constants of about 3.0 angstroms. This is shown in Table 2 below, which provides the VCEC coefficient of proportionality in units of pJ/Vm for different values of a_0 for an MRAM cell containing an MgO insulating spacer layer, three monolayer thick iron first reference layer, four monolayer thick aluminum interlayer coupling layer and three monolayer thick iron free layer.

[0065] TABLE 2: Dependence of the VCEC coefficient on the lattice parameter a_0 of MgO for a system with 4 monolayers of Al

a_0 (in Angstroms)	VCEC coefficient (in pJ/Vm)
2.8	2.1
2.83	2.4
2.85	2.8
2.866	3.2
3	-3.5

[0066] The various embodiments of the present disclosure can be employed to provide a magnetoresistive memory device 500 that can operate with low operational current. The switching of the magnetic state of a free layer 136 can be performed deterministically based on the polarity of the applied programming pulse, and without dependence on the duration of the programming voltage pulse. The magnetoresistive memory device 500 can be operated with low power and high reliability through the use of the voltage-controlled exchange coupling provided by the metallic interlayer exchange coupling layer 150.

[0067] According to embodiments of the present disclosure, a magnetoresistive memory device (500, 180) includes a magnetic-exchange-coupled layer stack 140 comprising a free layer 136, a reference layer 132 and an electrically conductive, non-magnetic interlayer exchange coupling layer 150 located between the free layer 136 and the reference layer 132, and an insulating spacer layer 110 located in a series connection with the magnetic-exchange-coupled layer stack 140 between a first electrode 102 and a second electrode 170. The first electrode and second electrode are configured to provide a programming voltage across the magnetic-exchange-coupled layer stack 140 and the insulating spacer layer 110.

[0068] In one embodiment, the electrically conductive, non-magnetic interlayer exchange coupling layer 150 comprises a metallic interlayer exchange coupling layer. The metallic interlayer exchange coupling layer 150 provides a voltage-dependent exchange coupling between the reference layer 132 and the free layer 136 such that energy levels of a parallel state and an antiparallel state of the free layer 136 shift in opposite directions upon application of respective first and second polarity voltages between the first and second electrodes (102, 170).

[0069] In another embodiment, the device (500, 180) lacks external magnets such that the magnetization state of the free layer 136 is configured to be programmed by giant magnetoresistive (GMR) effect in response to application of the programming voltage in the absence of an external magnetic field.

[0070] In one embodiment, the device 500 further comprises a programming circuitry 570 configured to apply the programming voltage selected from a positive voltage pulse and a negative voltage pulse between the first electrode 102 and the second electrode 170 across the magnetic-exchange-coupled layer stack 140 and the insulating spacer layer 110 to induce the free layer 136 to transition into a different magnetization state.

[0071] In one embodiment, the device 500 further comprises a sense circuitry 570 configured to apply a sense voltage pulse between the first electrode 102 and the second electrode 170, wherein a magnitude of the sense voltage pulse is selected to prevent a change a magnetization state of the free layer 136.

[0072] In one embodiment, the interlayer exchange coupling layer 150 consists essentially of a metallic element selected from Au, Cu, Cr, and Al, and the interlayer exchange coupling layer 150 has a thickness in a range from one atomic layer of the metallic element to five layers of the metallic element. In another embodiment, any other suitable electrically conductive, non-magnetic material that can provide exchange coupling may be used instead of or in addition to Au, Cu, Cr, or Al.

[0073] In one embodiment, the insulating spacer layer 110 comprises a magnesium oxide layer, the reference layer 132 comprises a first iron layer having a thickness in a range from two atomic layers of iron to forty atomic layers of iron, and the free layer 136 comprises a second iron layer having a thickness in a range from two atomic layers of iron to forty atomic layers of iron.

[0074] In another embodiment, the device (500, 180) further comprises a first synthetic antiferromagnetic structure 120 comprising the reference layer 132, a fixed ferromagnetic layer 112 having a magnetization that is antiparallel to the fixed magnetization direction of the reference layer 132, and an antiferromagnetic coupling layer 114 located between the reference layer 132 and the fixed ferromagnetic layer 112.

[0075] In another embodiment, the device (500, 180) further comprises a second synthetic antiferromagnetic structure 160 comprising an additional reference layer 166, an additional fixed ferromagnetic layer 162 having a magnetization that is antiparallel to a magnetization direction of the additional reference layer 166, and an additional antiferromagnetic coupling layer 164 located between the additional reference layer 166 and the additional fixed ferromagnetic layer 162, and an additional insulating spacer layer 155 located between the first electrode 102 and the second electrode 170.

[0076] In one embodiment, a method of operating the device (500, 180) includes applying a first polarity programming voltage between the first electrode 102 and the second electrode 170 across the magnetic-exchange-coupled layer stack 140 and the insulating spacer layer 110 to switch a magnetization of the free layer 136 from a parallel state to an antiparallel state with the reference layer 132, and applying a second polarity programming voltage opposite to the first polarity voltage between the first electrode 102 and the second electrode 170 across the magnetic-exchange-coupled layer stack 140 and the insulating spacer layer 110 to switch the magnetization of the free layer 136 from the antiparallel state to the parallel state with the reference layer 132.

[0077] In one embodiment, the magnetization of the free layer 136 is switched in response to application of the first polarity programming voltage and the second polarity programming voltage in the absence of an external magnetic field. In one embodiment, the first polarity voltage comprises a negative voltage pulse and the second polarity voltage comprises a positive voltage pulse. In one embodiment magnetization of the free layer is switched by giant magnetoresistive (GMR) effect.

[0078] In one embodiment, the method also includes applying a sense voltage pulse between the first electrode 102 and the second electrode 170 to read the magnetization of the free layer 136 by the giant magnetoresistive (GMR) effect or by the tunneling magnetoresistive (TMR) effect without changing a magnetization state of the free layer 136.

[0079] Although the foregoing refers to particular preferred embodiments, it will be understood that the disclosure is not so limited. It will occur to those of ordinary skill in the art that various modifications may be made to the disclosed embodiments and that such modifications are intended to be within the scope of the disclosure. Where an embodiment employing a particular structure and/or configuration is illustrated in the present disclosure, it is understood that the present disclosure may be practiced with any other compatible structures and/or configurations that are functionally equivalent provided that such substitutions are not explicitly forbidden or otherwise known to be impossible to one of ordinary skill in the art. All of the publications, patent applications and patents cited herein are incorporated herein by reference in their entirety.

WHAT IS CLAIMED IS:

1. A magnetoresistive memory device, comprising:

a first electrode;

a second electrode;

a magnetic-exchange-coupled layer stack comprising a free layer, a reference layer and an electrically conductive, non-magnetic interlayer exchange coupling layer located between the free layer and the reference layer; and

an insulating spacer layer located in a series connection with the magnetic-exchange-coupled layer stack between the first electrode and the second electrode,

wherein the first electrode and the second electrode are configured to provide a programming voltage across the magnetic-exchange-coupled layer stack and the insulating spacer layer.

2. The magnetoresistive memory device of Claim 1, wherein:

the electrically conductive, non-magnetic interlayer exchange coupling layer comprises a metallic interlayer exchange coupling layer; and

the metallic interlayer exchange coupling layer provides a voltage-dependent exchange coupling between the reference layer and the free layer such that energy levels of a parallel state and an antiparallel state of the free layer shift in opposite directions upon application of respective first and second polarity voltages between the first and second electrodes.

3. The magnetoresistive memory device of Claim 1, wherein:

an insulating tunneling barrier layer is not present between the free layer and the reference layer; and

the device lacks external magnets such that the magnetization state of the free layer is configured to be programmed by voltage-controlled interlayer exchange coupling (VCEC) in response to application of the programming voltage in the absence of an external magnetic field.

4. The magnetoresistive memory device of Claim 1, further comprising a programming circuitry configured to apply the programming voltage selected from a positive voltage pulse and a negative voltage pulse between the first electrode and the second electrode across the magnetic-exchange-coupled layer stack and the insulating spacer layer to induce the free layer to transition into a different magnetization state.

5. The magnetoresistive memory device of Claim 4, further comprising a sense circuitry configured to apply a sense voltage pulse between the first electrode and the second electrode, wherein a magnitude of the sense voltage pulse is selected to prevent a change in the magnetization state of the free layer.

6. The magnetoresistive memory device of Claim 1, wherein the interlayer exchange coupling layer consists essentially of a metallic element comprising Au, Cu, Cr or Al.

7. The magnetoresistive memory device of Claim 6, wherein:

the insulating spacer layer comprises a magnesium oxide layer;

the reference layer comprises a first iron layer; and the free layer comprises a second iron layer.

8. The magnetoresistive memory device of Claim 1, further comprising a first synthetic antiferromagnetic structure comprising the reference layer, a fixed ferromagnetic layer having a magnetization that is antiparallel to the fixed magnetization direction of the reference layer, and an antiferromagnetic coupling layer located between the reference layer and the fixed ferromagnetic layer.

9. The magnetoresistive memory device of Claim 8, further comprising:

a second synthetic antiferromagnetic structure comprising an additional reference layer, an additional fixed ferromagnetic layer having a magnetization that is antiparallel to a magnetization direction of the additional reference layer, and an additional antiferromagnetic coupling layer located between the additional reference layer and the additional fixed ferromagnetic layer; and

an additional insulating spacer layer located between the first electrode and the second electrode.

10. A method of operating a magnetoresistive memory device comprising a magnetic-exchange-coupled layer stack comprising a free layer, a reference layer and an electrically conductive, non-magnetic interlayer exchange coupling layer located between the free layer and the reference layer, and an insulating spacer layer located in a series connection with the magnetic-exchange-coupled layer stack between a first electrode and a second electrode, the method comprising:

applying a first polarity programming voltage between the first electrode and the second electrode across the magnetic-exchange-coupled layer stack and the insulating spacer layer to switch a magnetization of the free layer from a parallel state to an antiparallel state with the reference layer; and

applying a second polarity programming voltage opposite to the first polarity voltage between the first electrode and the second electrode across the magnetic-exchange-coupled layer stack and the insulating spacer layer to switch the magnetization of the free layer from the antiparallel state to the parallel state with the reference layer.

11. The method Claim 10, wherein the magnetization of the free layer is switched in response to application of the first polarity programming voltage and the second polarity programming voltage in the absence of an external magnetic field.

12. The method Claim 11, wherein the first polarity voltage comprises a negative voltage pulse and the second polarity voltage comprises a positive voltage pulse.

13. The method Claim 11, wherein the magnetization state of the free layer is programmed by voltage-controlled interlayer exchange coupling (VCEC).

14. The method Claim 13, further comprising applying a sense voltage pulse between the first electrode and the second electrode to read the magnetization of the free layer by the giant magnetoresistive (GMR) effect without changing a magnetization state of the free layer.

15. The method Claim 13, further comprising applying a sense voltage pulse between the first electrode and the second electrode to read the magnetization of the free layer by the tunneling

magnetoresistive (TMR) effect without changing a magnetization state of the free layer.

16. The method Claim 10, wherein the interlayer exchange coupling layer consists essentially of a metallic element comprising Au, Cu, Cr, or Al.

17. The method Claim 16, wherein:

the insulating spacer layer comprises a magnesium oxide layer;

the reference layer comprises a first iron layer having a thickness in a range from two atomic layers of iron to five atomic layers of iron; and

the free layer comprises a second iron layer having a thickness in a range from two atomic layers of iron to five atomic layers of iron.

18. The method Claim 10, further comprising a first synthetic antiferromagnetic structure comprising the reference layer, a fixed ferromagnetic layer having a magnetization that is antiparallel to the fixed magnetization direction of the reference layer, and an antiferromagnetic coupling layer located between the reference layer and the fixed ferromagnetic layer.

19. The method Claim 18, further comprising:

a second synthetic antiferromagnetic structure comprising an additional reference layer, an additional fixed ferromagnetic layer having a magnetization that is antiparallel to a magnetization direction of the additional reference layer, and an additional antiferromagnetic coupling layer located between the additional reference layer and the additional fixed ferromagnetic layer; and an additional insulating spacer layer located between the first electrode and the second electrode.

20. The method Claim 19, further comprising applying a sense voltage pulse between the first electrode and the second electrode to read the magnetization of the free layer by the tunneling magnetoresistive (TMR) effect without changing a magnetization state of the free layer.

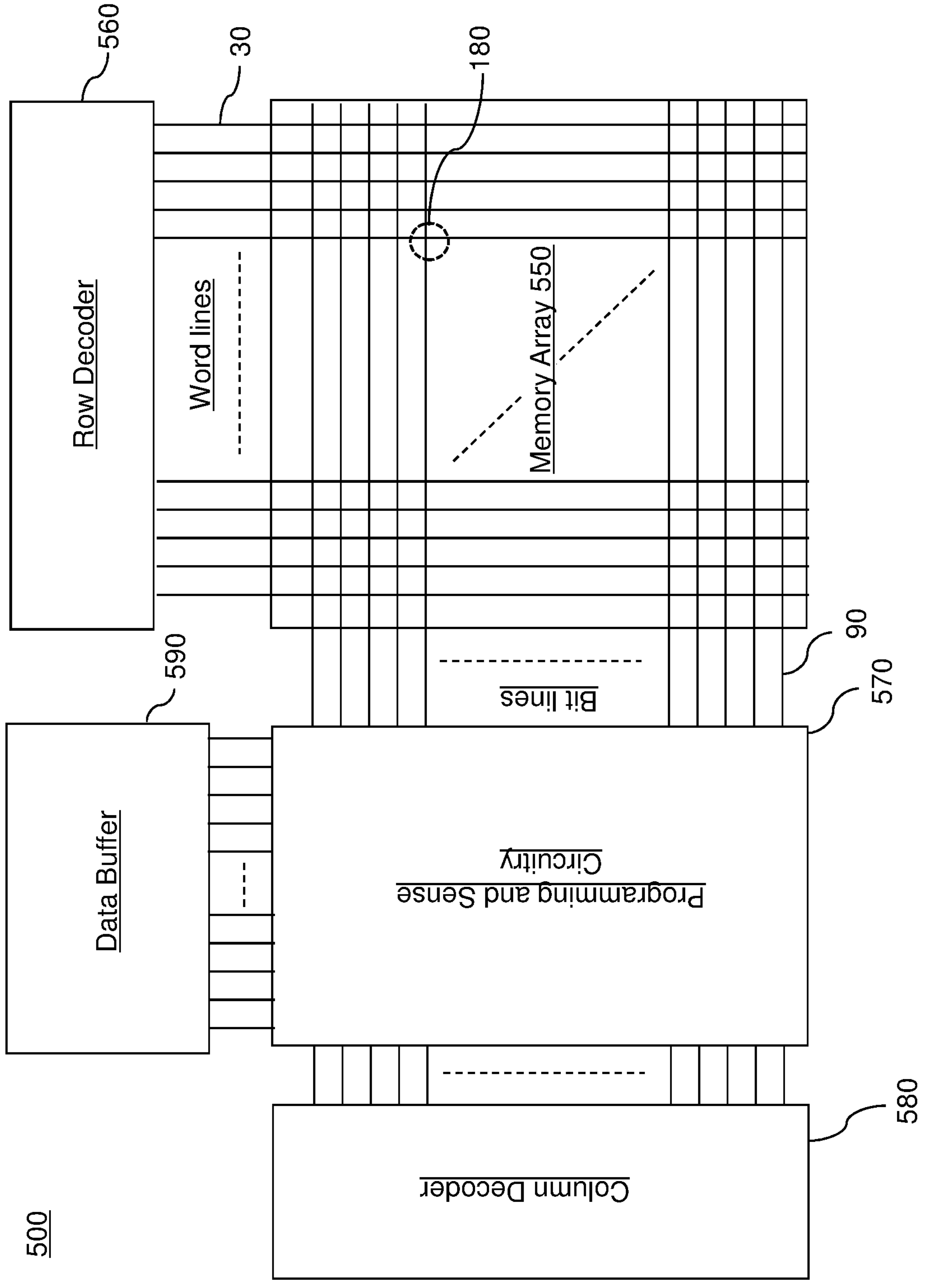
Row Decoder
560
30
180
Word lines
Memory Array 550
590
Data Buffer
Bit lines
90
570
Programming and Sense Circuitry
Column Decoder
580
500

FIG. 1

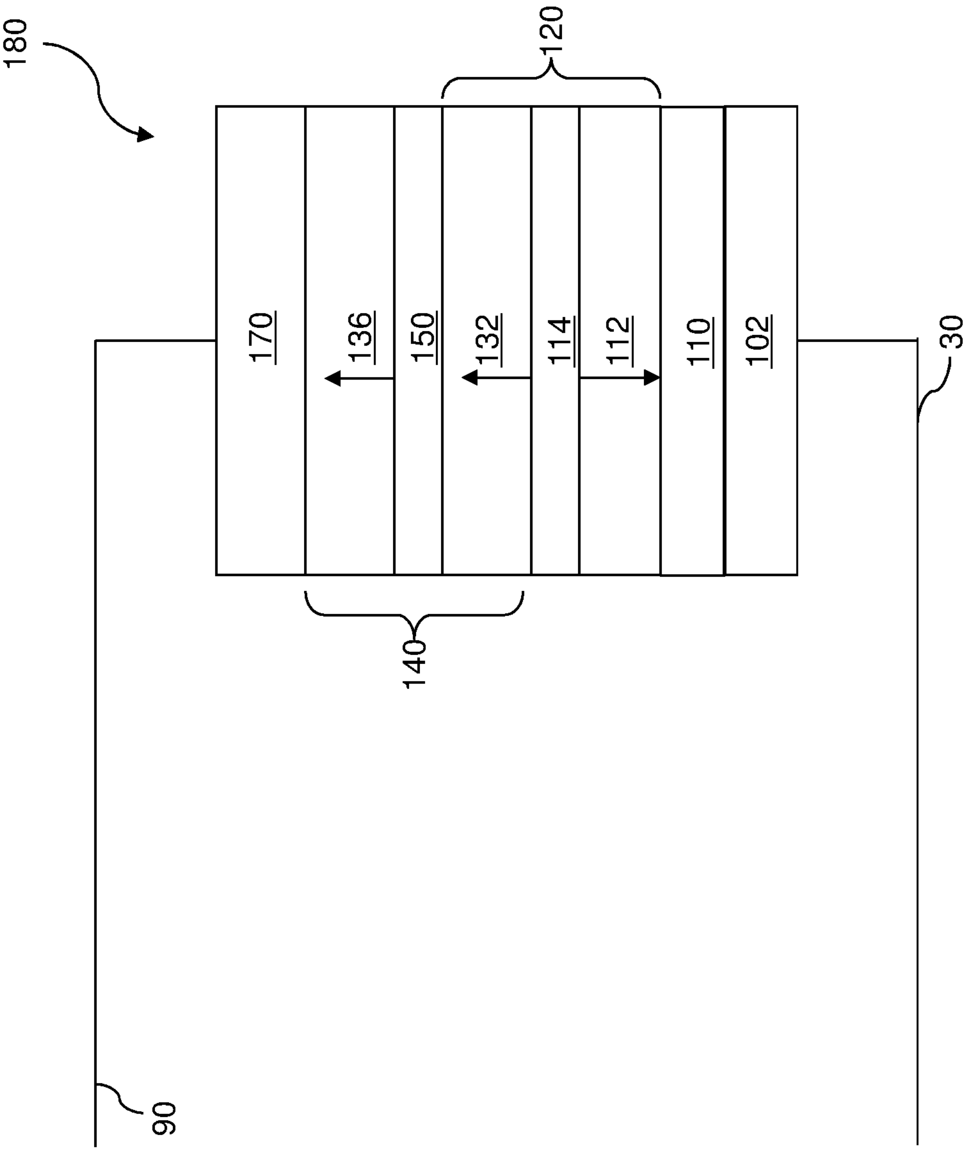

FIG. 2A

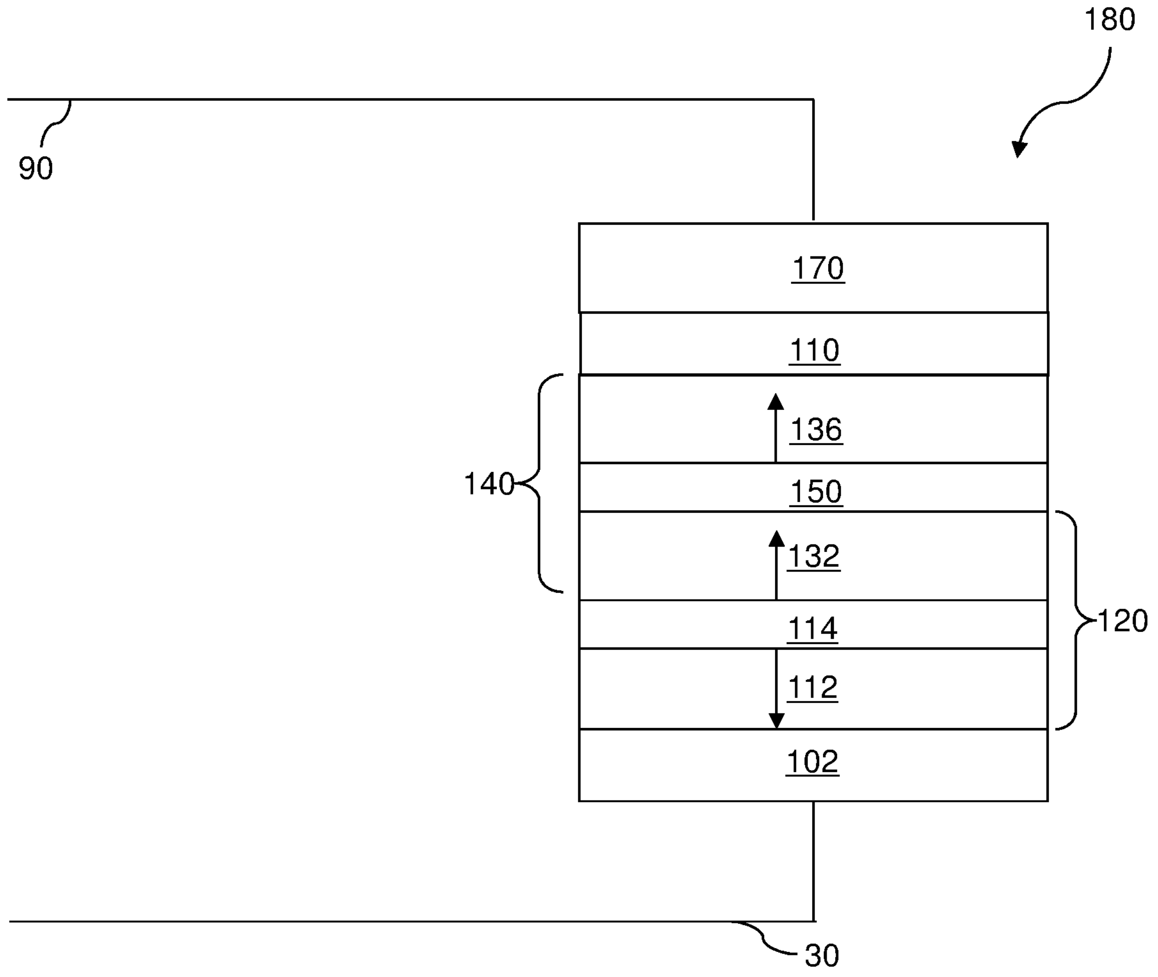

FIG. 2B

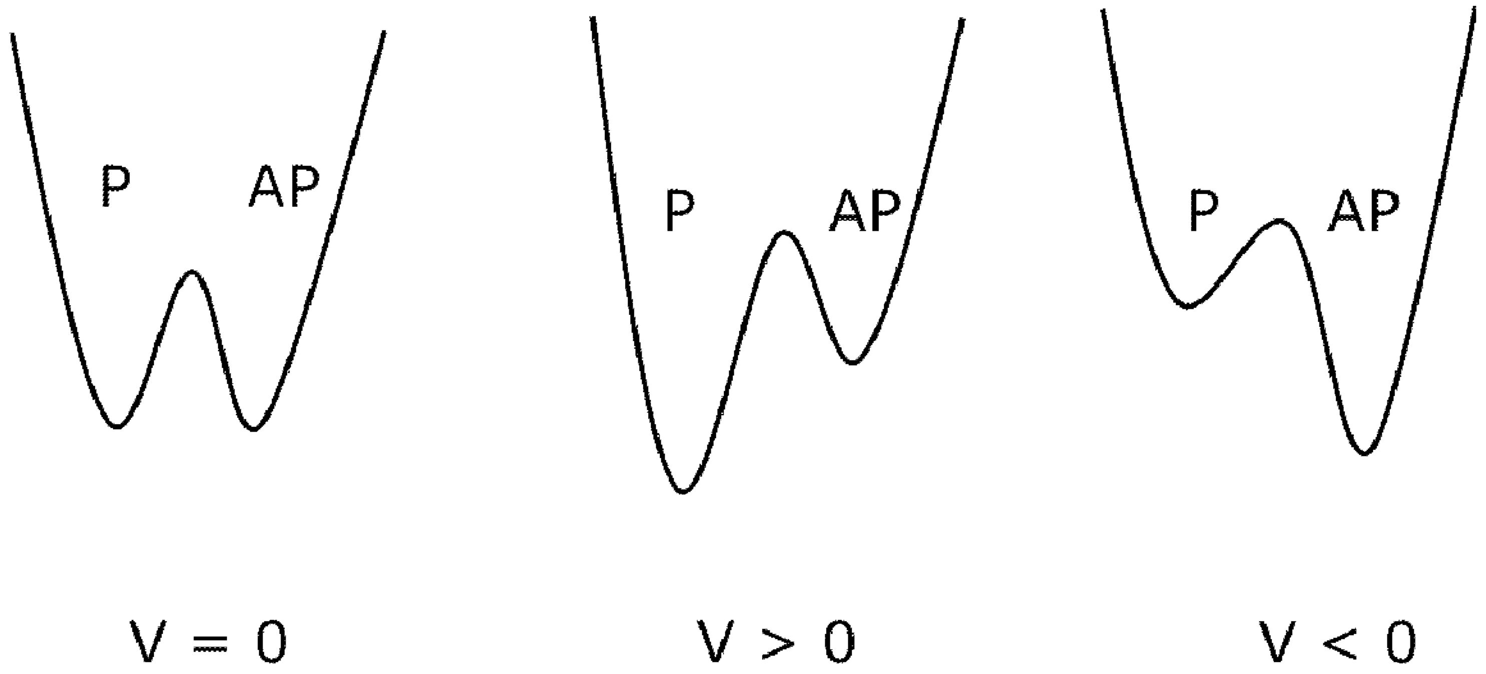

FIG. 3

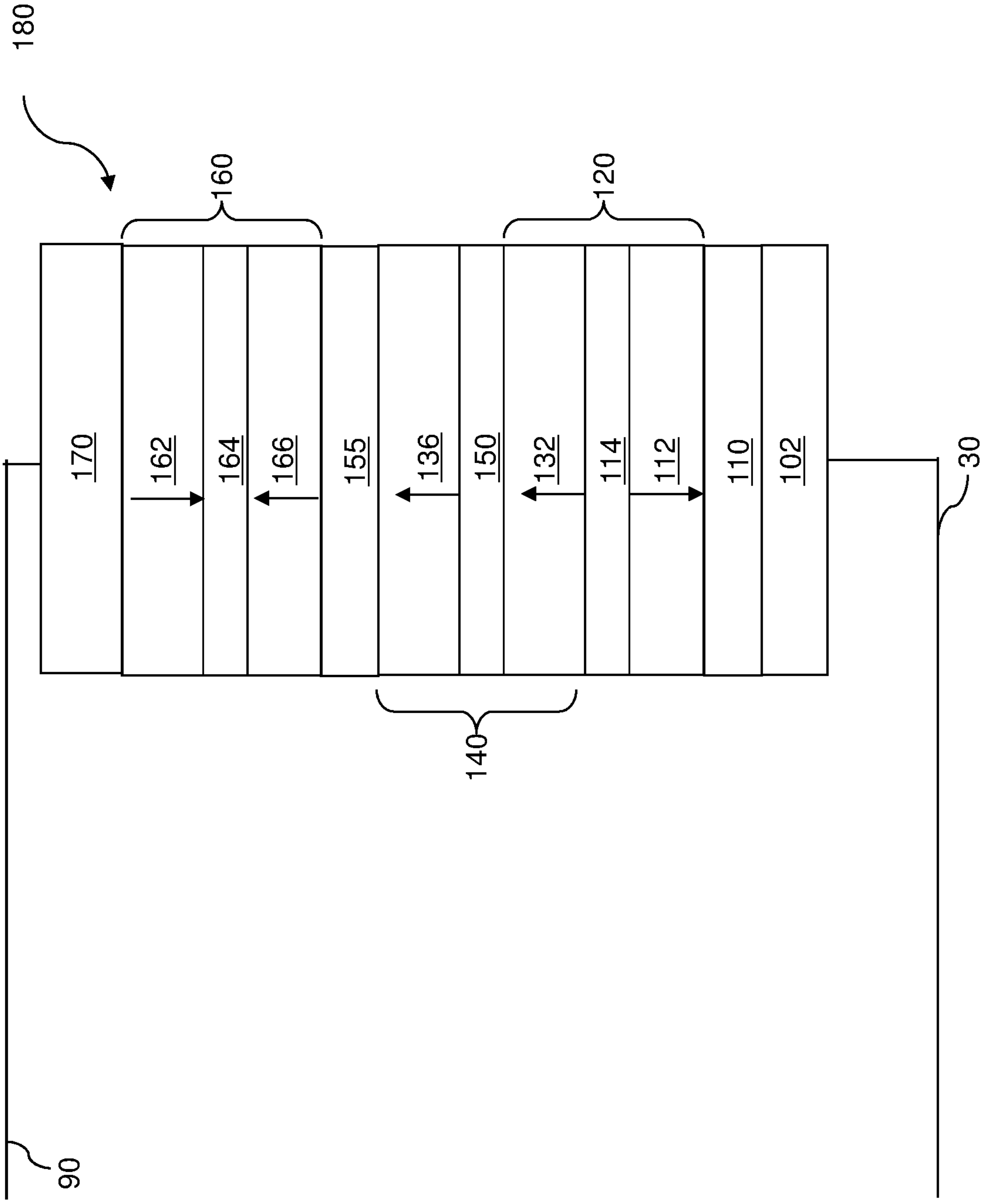
180
160
120
170
162
164
166
155
136
150
132
114
112
110
102
30
140
90

FIG. 4A

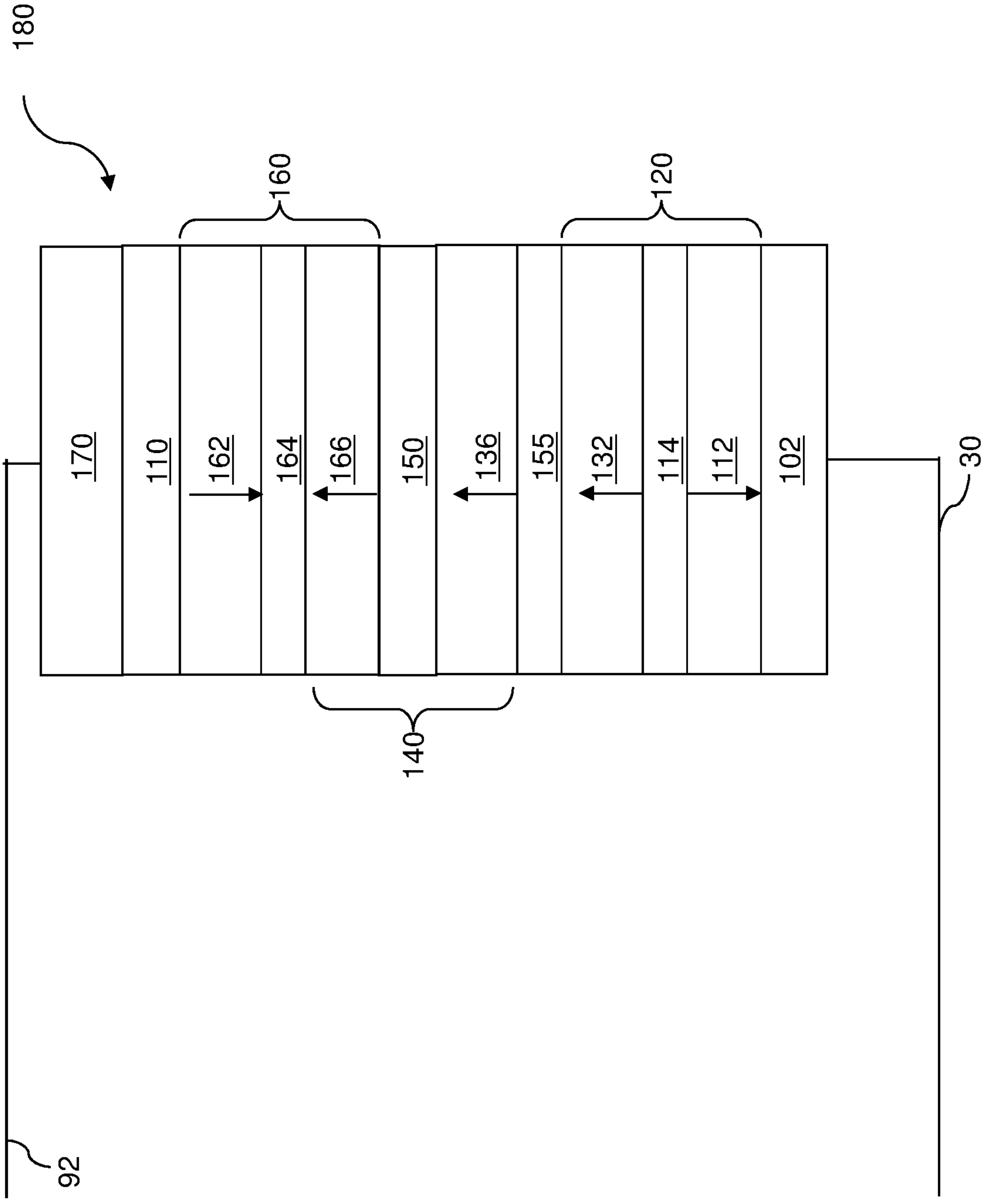
180
160
120
170
110
162
164
166
150
136
155
132
114
112
102
30
140
92

FIG. 4B

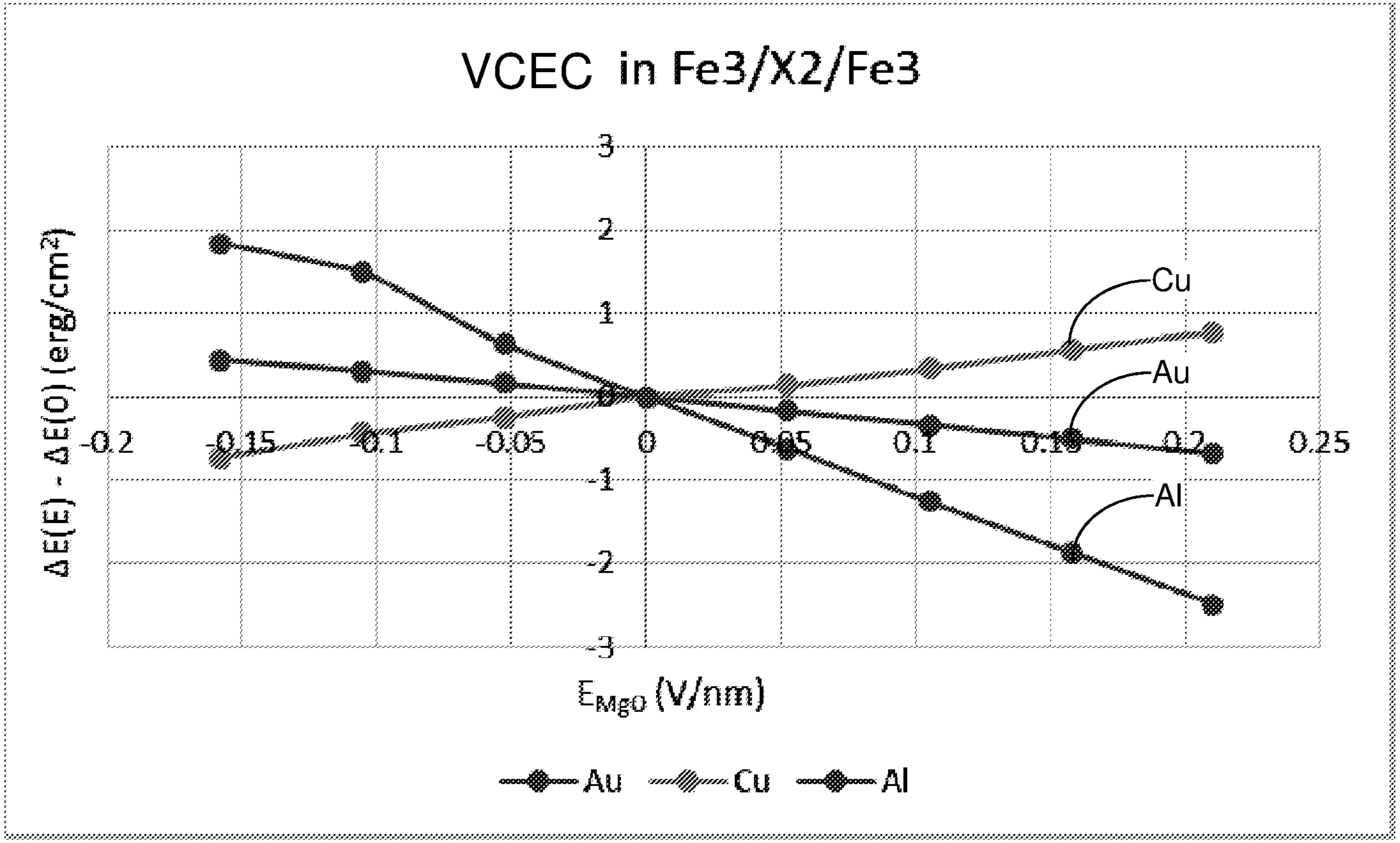
VCEC in Fe3/X2/Fe3
ΔE(E) - ΔE(0) (erg/cm²)
3
2
1
0
-1
-2
-3
-0.2
-0.15
-0.1
-0.05
0
0.05
0.1
0.15
0.2
0.25
E_MgO (V/nm)
Cu
Au
Al
Au
Cu
Al

FIG. 5A

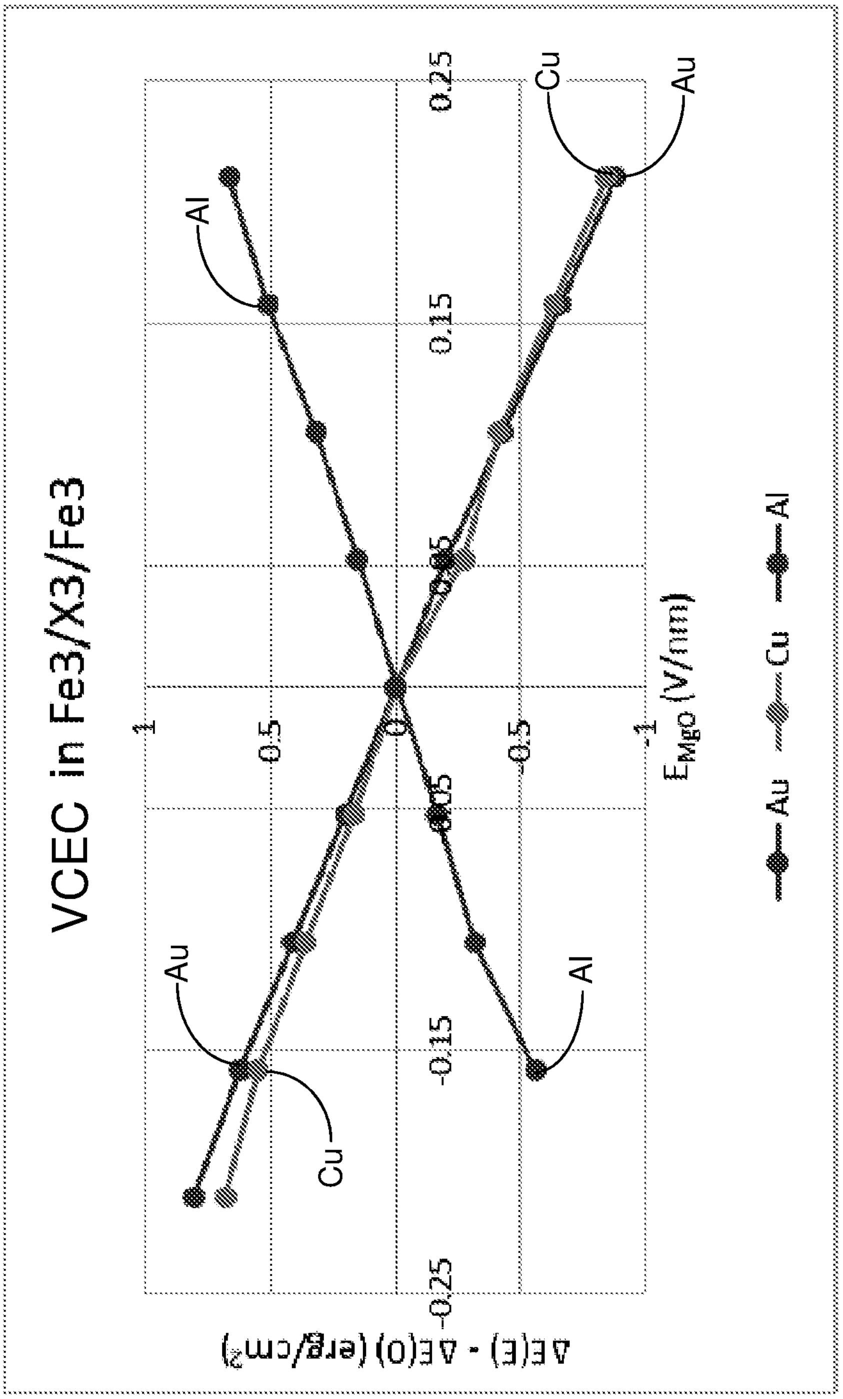
VCEC in Fe3/X3/Fe3
ΔE(E) - ΔE(0) (erg/cm²)
1
0.5
0
-0.5
-1
-0.25
-0.15
-0.05
0.05
0.15
0.25
E_MgO (V/nm)
Au
Cu
Al
Al
Au
Cu
Au
Cu
Al

FIG. 5B

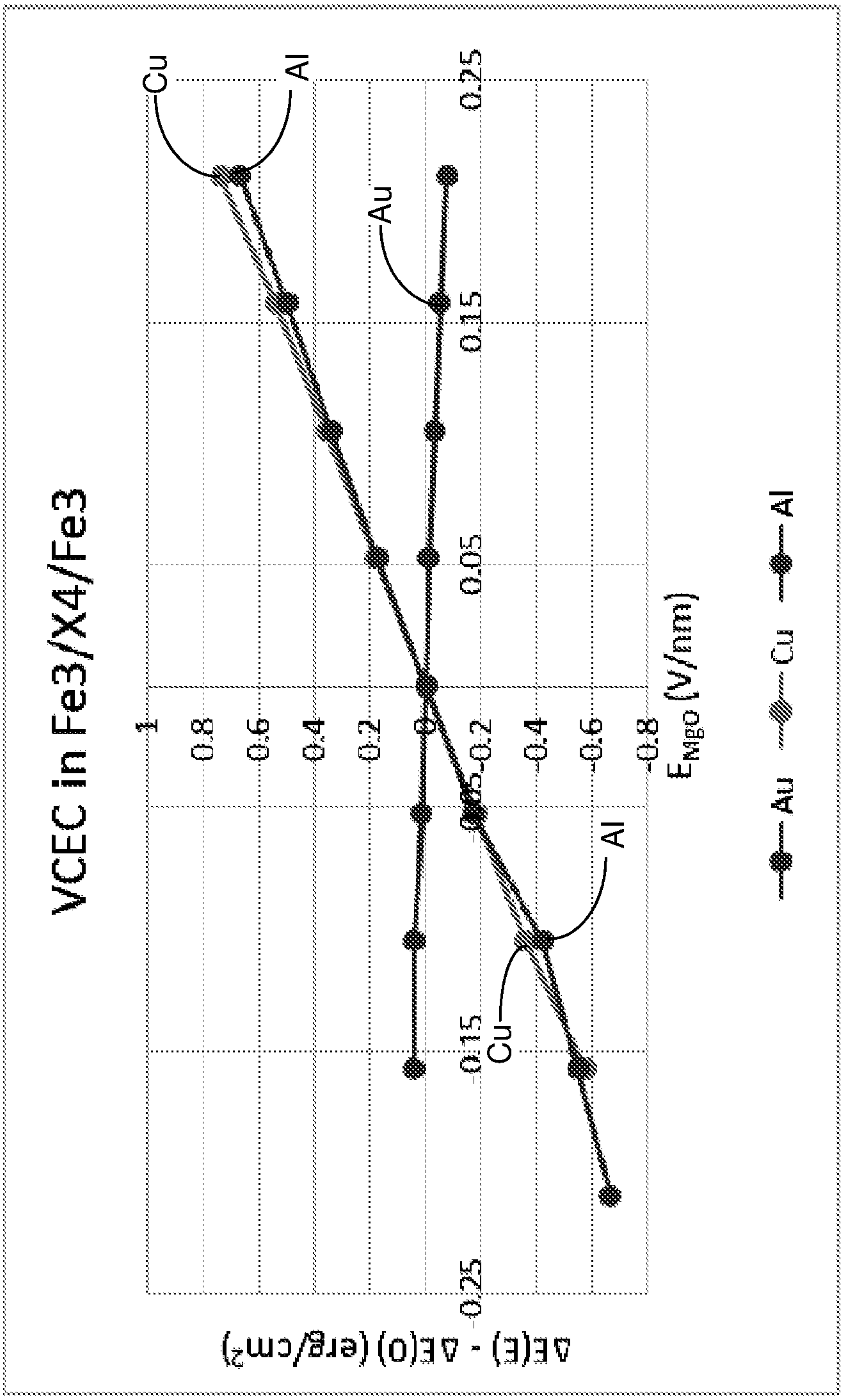
VCEC in Fe3/X4/Fe3
ΔE(E) - ΔE(0) (erg/cm²)
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-0.25
-0.15
-0.05
0.05
0.15
0.25
E_MgO (V/nm)
Cu
Al
Au
Al
Cu
Au
Cu
Al

FIG. 5C

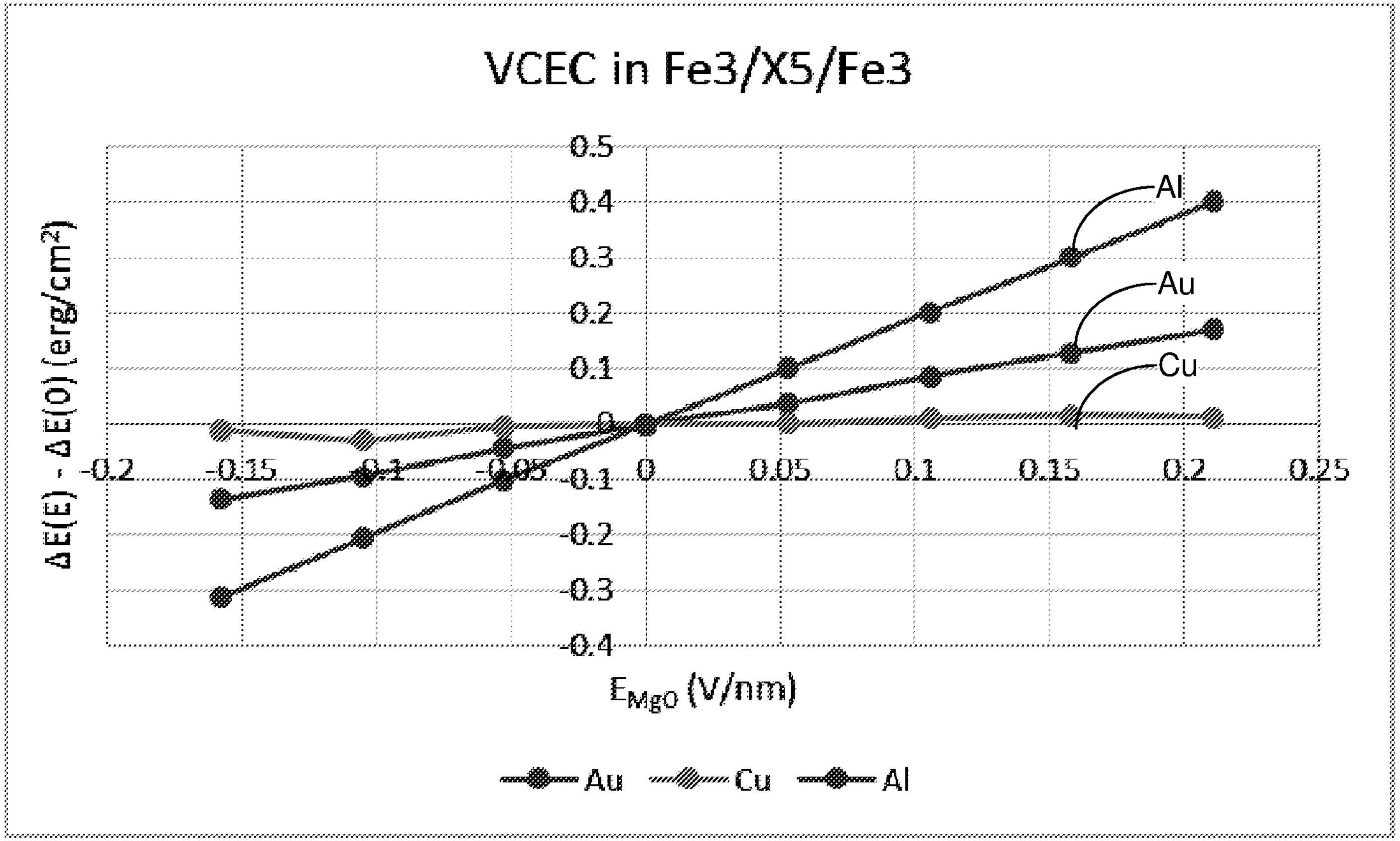
VCEC in Fe3/X5/Fe3
0.5
0.4
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
-0.4
-0.2
-0.15
-0.1
-0.05
0
0.05
0.1
0.15
0.2
0.25
ΔE(E) - ΔE(0) (erg/cm²)
E_MgO (V/nm)
Al
Au
Cu
Au
Cu
Al

FIG. 5D

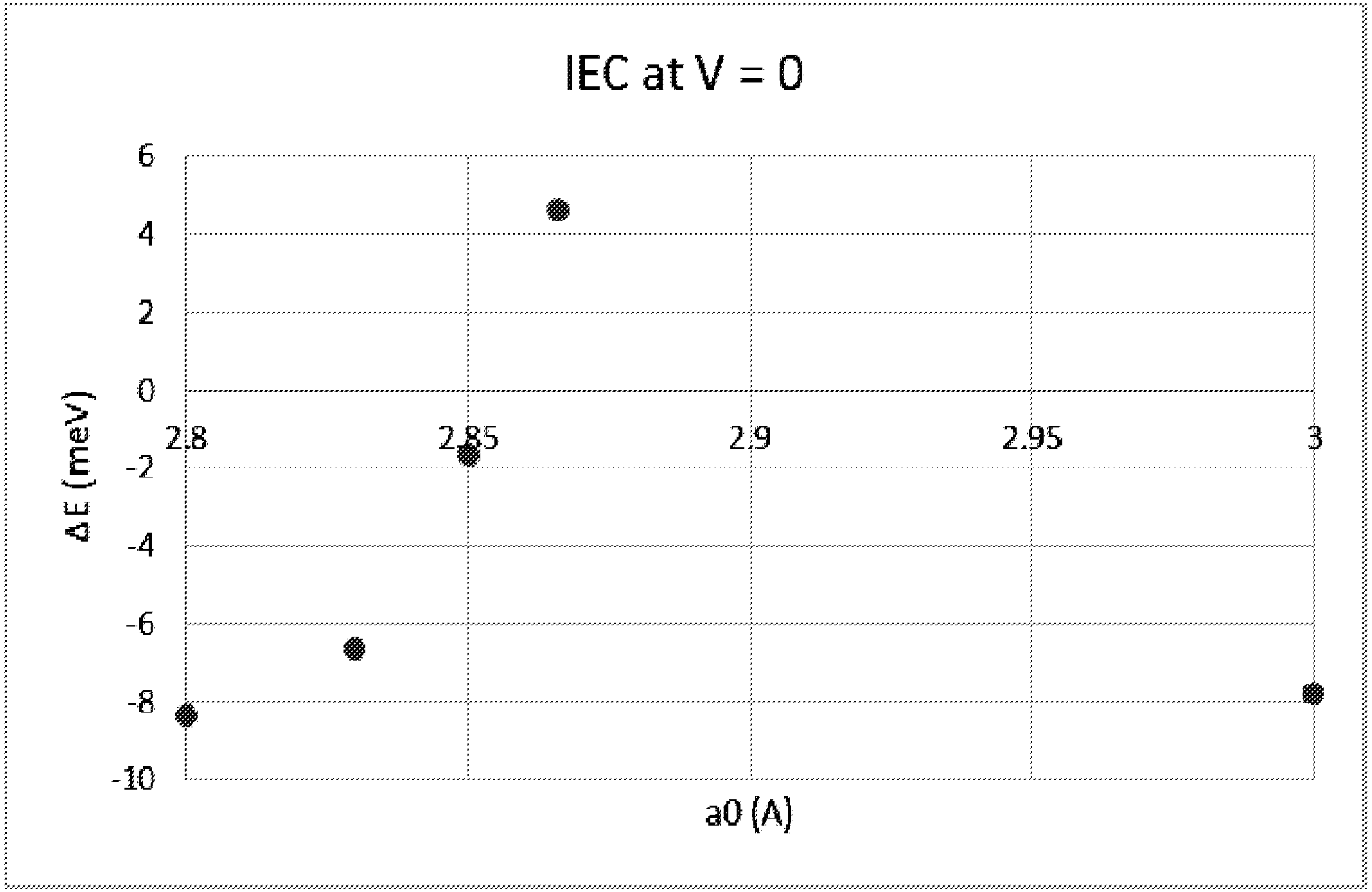

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/062573

A. CLASSIFICATION OF SUBJECT MATTER
IPC (20200101) G01R 33/09, G11C 11/16, B82Y 25/00
CPC (20130101) G01R 33/09, G11C 11/161, B82Y 25/00
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC (20200101) G01R 33/09, G11C 11/16, B82Y 25/00
CPC (20130101) G01R 33/09, G11C 11/161, B82Y 25/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Databases consulted: Google Patents, Orbit
Search terms used: MRAM, layer. volatage, VCEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2011007560 A1 COMMISSARIAT A L'ENERGIE ATOMIQUE ET AUX ENERGIESALTERNATIVES 03 Jan 2011 (2011/01/03) Tje whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search 09 Mar 2020	Date of mailing of the international search report 09 Mar 2020
Name and mailing address of the ISA: Israel Patent Office Technology Park, Bldg.5, Malcha, Jerusalem, 9695101, Israel Email address: pctoffice@justice.gov.il	Authorized officer TAIEB - SABO Hagit Telephone No. 972-73-3927245

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2019/062573

Patent document cited search report	Publication date	Patent family member(s)	Publication Date
US 2011007560 A1	03 Jan 2011	US 2011007560 A1	13 Jan 2011
		US 8279666 B2	02 Oct 2012
		EP 2436035 A1	04 Apr 2012
		FR 2946183 A1	03 Dec 2010
		FR 2946183 B1	23 Dec 2011
		KR 20120027390 A	21 Mar 2012
		WO 2010136527 A1	02 Dec 2010