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(54) TRANSFERRING DATA INFORMATION

(71) We, TELEFONAKTIEBOLAGET L M ERICSSON, a company organised under the laws of Sweden, of S-126 25 Stockholm, Sweden, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to transferring data information.

A single working data processor which is intended for process control in real time executes an instruction sequence which constitutes the control program of the process. The instructions of the sequence are successively executed, each during its execution clock unit determined by means of clock pulses and in an order which has to be flexible considering that data information pieces are received from the controlled process quite arbitrarily and asynchronously related to the clock pulses but have to be processed in real time. It is known in computer techniques in this connection to introduce different degrees of priority, to divide the sequence into uninterruptable subsequences the last-executed instruction of which is a so-called jump instruction, to register a newly-arrived data information piece in a so-called interrupt register, and due to a marking of a requested information transfer having priority to jump to a transfer subsequence comprising a transfer instruction. By means of the transfer subsequence, the sequence that has been up to now is interrupted, the registered data information piece is distributed and a return point for the continued sequence execution is determined. Such a known real technique is described for example in the article "Design of a Microprogram Control for a Processor in an Electronic Switching System", the author of which is T. F. Storey and which is published in "The Bell System Technical Journal", February 1976, Vol. 55, No. 2, p. 183—232.

The asynchronism between the execution clock pulses of the sequence and the data information pieces being received from the process is rather easily mastered by the single working data processor. The clock pulses are used to activate the interrupt register for writing or reading, and thanks to the subsequences and jump instructions—as it is generally expressed by way of introduction and as will be explained below—executing periods appear which each comprises, due to a requested information transfer, only one transfer instruction. The present invention, however, does not relate to real-time-single working but proposes a method and an arrangement for transferring data information to parallel-working data processor parts which execute one instruction sequence each.

The term "parallel-working" is known as hereinafter used means that two data processor parts which are substantially identical process in parallel data information pieces coming from an undoubled equipment by means of the same instruction sequence, the results produced by the parts being continously compared with each other whereby differences of the results owing to equipment or program faults start a malfunction alarm. From that it follows that the working in parallel demands, for the execution of the same instruction sequence by the processor parts, a synchronism which absolutely comprises frequency equality of the clock pulses controlling the executions. An arrangement of delay circuits renders it possible to carry out the comparison operation in spite of a constant phase displacement between corresponding execution periods but preferably the synchronization in addition to the frequency equality ought to comprise phase coincidence as well. Concerning a doubling of processor parts in order to increase the operational reliability, there are still more known principals which demand less for the

synchronism but the present invention only relates to the doubling resulting in a parallel-synchronous co-operation, which in a publication by J. Martin, "Design of Real Time Computer Systems", 1967, Englewood Clifts is designated "twin-configuration" and which is also described in United Kingdom Patents Nos. 1,166,057 and 1,484,331.

In Patent No. 1,166,057 it is assumed that the frequency equality and phase coincidence exist. A transfer of a data information to the twin-configuration is therefore achieved without venturing the necessary equality of the instruction sequencies in a simple way, for example by registering the data information in parallel in two interrupt registers belonging to a computer each according to the above-mentioned description for single working.

In the twin-configuration according to Patent No. 1,484,331, frequency equality exists in combination with such a constant phase displacement that the so-called executive processor when executing the same instruction sequence always leads before the so-called reserve processor. One realizes that the above-mentioned arrangement of two interrupt registers each to select, when information transfer is requested a transfer instruction without considering the constant phase displacement results in different instruction sequences and consequently in malfunction alarm if the phase displacement is of such a high degree that a request for transfer is marked at the same time in the two computers during non-corresponding execution periods. In this case, however, only the executive processor is fed with the undoubled data information pieces and thanks to a special updating technique, instruction sequence identify is continued after a new-arrived data information piece in spite of the constant phase displacement by means of processing the un-doubled data information piece as updating data.

In practice the hitherto discussed constant synchronization conditions do not exist but, due to tolerance limits which have to be allowed, there are phase displacements slowly varying around a mean value. Even if this mean value of the phase displacements, which in Patent No. 1,166,057 corresponds to the ideal phase coincidence and in Patent No. 1,484,331 corresponds to the constant phase displacement, is mastered in the above-mentioned manner, the variations around a mean value are not mastered in any hitherto known twin-configuration, if the divergence from the mean value sometimes is bigger than simultaneously relevant execution periods.

According to one aspect of this invention there is provided a method of transferring data information pieces to two parallel-working data processor parts which execute the same instruction sequence in corresponding periods each of which comprises the execution of at most one transfer instruction due to a requested data information transfer, the requests for data information transfers appearing asynchronously compared with the execution of the instruction sequence, and wherein such time displacements between corresponding periods may occur that a transfer request is marked during periods of the two data processor parts which are not corresponding to each other, the method comprising the steps of:—

a) registering the said data information pieces one at a time,

b) generating a marking signal in response to each registration of a data information piece,

c) counting the numbers of periods executed in the respective processor parts,

d) registering a transfer number when a marking signal is generated, the transfer number being the counted number of periods if the instruction sequence is executed in corresponding periods in the two data processor parts, and the bigger counted number of periods if the instruction sequence is executed in the two data-processor parts in non-corresponding periods,

e) sending respective transfer signals to the respective processor parts which the said registered transfer number corresponds to the respective counted numbers of periods, and

f) transferring the registered data information piece to the two processor parts when they respectively execute a transfer instruction in response to the respective transfer signal.

According to another aspect of this invention there is provided an arrangement for transferring data information pieces, comprising two parallel-working data processor parts which execute the same instruction sequence in corresponding periods each of which comprises the execution of at most one transfer instruction due to a requested data information transfer, the requests for data information transfers appearing asynchronously compared with the execution of the instruction sequence, and wherein such time displacements between corresponding periods may occur that a transfer request is marked during periods of the two data processor parts which are not corresponding to each other, the arrangement further comprising means for:—

a) registering the said data information pieces one at a time,

b) generating a marking signal in response to each registration of a data information piece,

c) counting the numbers of periods executed in the respective processor parts,

d) registering a transfer number when a marking signal is generated, the transfer number being the counted number of periods if the instruction sequence is executed in corresponding periods in the two data processor parts, and the bigger counted number of periods if the instruction sequence is executed in the two data processor parts in non-corresponding periods,

e) sending respective transfer signals to the respective processor parts when the said registered transfer number corresponds to the respective counted numbers of periods, and

f) transferring the registered data information piece to the two processor parts when they respectively execute a transfer instruction in response to the respective transfer signal.

The invention will now be described by way of example with reference to the accompanying drawings, Figure 1 of which shows an arrangement and a buffer register from which data information pieces are transferred to two parallel-working data processor parts and Figures 2 to 4 of which show diagrams of the execution of an instruction sequence and the time-sharing of the information transfers.

Figure 1 shows two parallel-working data processor parts DA and DB each of which is provided with an information input II, a transfer signal input TSI and two outputs 01 and 02. Figure 2 is a time diagram showing how one of the data processor parts executes parts of an instruction sequence. The instructions are executed in instruction execution clock units. The execution clock units for jump instructions are for example designated JIm to JIm+3. The jump instructions are modifiable and finish one instruction subsequence each. The number of instructions of the subsequences varies and consequently different subsequence execution times SS are obtained. In Figure 2 it is assumed that for example SSm+3<SSm+2.

Besides the execution clock units for jump instructions and instruction subsequences, Figure 2 shows execution periods EPn and EPn+1. The limit between two successive periods is passed when it is too late to modify the only jump instruction being associated with this limit so that it is jumped to a transfer subsequence which comprises a transfer instruction during the execution of which the data processor part receives a data information piece through the information input II. The modification is initiated by means of a transfer signal TS which is received on the transfer signal input TSI in connection with a requested information transfer. It is possible, but not necessary, that each jump instruction is allotted a period limit. Likewise, the following general definition of the manner by which the data processor part executes the instruction sequence leaves it open whether a transfer signal results in a transfer subsequence or only in the insertion of a transfer instruction between two subsequences. The definition means that a transfer signal TS which activates the transfer signal input during the execution period EPn according to Figure 2 selects only one transfer instruction whose execution clock unit TIn+1 is included in the transfer period EPn+1. The output 01 of the data processor part is activated during the execution clock unit TIn+1 for the transfer instruction. Finally, Figure 2 shows indication pulses IP, which the output 02 of the data processor part emits at each period limit. As a conclusion, however, with the aid of Figure 4, a variation will be described according to which the indication pulses indicate a limit each between two successive subsequences.

The indication pulses generated in respective data processor parts are received according to Figure 1 by two numerators NA and NB respectively which are set on an equal number when the processor parts begin parallel-synchronous co-operation and which then count the number of periods being executed in the respective processor parts. A first comparator C1 in a transfer signal generator TSG compares the counting numbers being obtained by means of the numerators and indicating together at an arbitrary time whether the data processor parts execute the two corresponding instruction sequences in corresponding or non-corresponding periods. The first comparator is of a conventional type, which when receiving the counting numbers a and b activates its first or its second output if $a>b$ or $b>a$ respectively. The transfer signal generator also comprises a reversing switch RS in order to feed a number register NR through a gate arrangement G1 with counting numbers coming either from the one or from the other of the numerators NA and NB. According to Figure 1, the reversing switch consists of two gate arrangements, the first of which is connected to the numerator NA and to the first comparator output and the second of which is connected to the numerator NB and to the second comparator output. As long as the

gate arrangement G1 is activated, the number register registers the corresponding counter number of the two numerators and the bigger of the counted numbers, respectively, which is obtained depending on whether the instruction sequence is executed in corresponding and non-corresponding periods, respectively in the data processor parts. The transfer signal generator also comprises two second comparators C2A and C2B each having its first input connected to one of the numerators and its output connected to the transfer signal input TS1 of that data processor part which feeds this numerator and its second input connected through a gate arrangement G2 to the output of the number register. The comparators C2A and C2B are of a conventional type, the outputs of which are activated at equal input signals.

Figure 1 shows an information buffer register IB of the known "first in—first out" type in which data information pieces coming in at arbitrary times are buffer-stored. The buffer register is provided with an indication output X which is activated if at least one information piece is stored. The data information pieces are transferred through a gate arrangement G3 to an information register IR in an information registration unit IRU and from there through two gate arrangements GA and GB to the information inputs II of the data processor parts DA and DB. The indication output X is also connected to the information registration unit, more precisely to the first input of a gate G4 the second input of which is activated by means of a gate G5 only if two flip-flops FFA and FFB take the same stable first state *s*1. This first state is set when the execution of the instruction sequence begins and when the execution of a transfer instruction is finished. To achieve this, the flip-flops FFA and FFB each are provided with a first input which is activated by a trailing edge and which together with the control input of the gate arrangement GA or GB respectively is connected to the output 01 of the data processor part DA or DB respectively. The gate G4 has its output connected to the gate arrangement G3 and to the second inputs of the flip-flops FFA and FFB. During the parallel-synchronous co-operation the information registration unit therefore performs the following operation. On the condition that the transfer of a first data information piece to the processor parts is finished and that the buffer register stores a second data information piece, the second information piece is registered in the information register from which it is read by means of the gate arrangements GA and GB, which are activated when the processor parts execute a transfer instruction each being allotted to this second information piece.

In connection with each writing in the information register IR, the gate G5 of the information registration unit is de-activated and remains de-activated during the whole of the belonging transfer operation but is activated, at least for a short while, when a transfer operation is finished. According to Figure 1, this conduct of the gate G5 is utilized by using its logic ZEROS as marking signals each belonging to a registration in the information register and each controlling the gate arrangements G1 and G2 of the transfer signal generator TSG. Consequently, a marking of an information transfer request stops the transfer of the coupled numbers to the number register NR, the contents of which during the associated transfer operation being designated as transfer number *t*. By means of the gate arrangement G2 which is provided with an inverting input, it is achieved that the second comparators C2A and C2B compare the momentary counted numbers *a* and *b* being obtained from the numerators NA, NB with the transfer number only, and so two transfer signals belonging to a respective transfer operation are generated, and the data processor parts DA and DB, independently of a relative phase displacement, receive separately the transfer signals during the execution period being determined by means of the transfer number *t*.

Figure 3 contains a number of time diagrams showing an example how to transfer, by means of the above-mentioned arrangement, data information pieces to two parallel-synchronously co-operating processor parts the coincidence start of which, in order to execute the same instruction sequence, appear from coincident execution periods having the counted number 0 in two execution time diagrams designated EA and EB. After a certain time, a phase displacement *td* has arisen between periods with corresponding counted numbers and the phase displacement results in that the counted numbers being registered according to the time diagram RN in the number register until the beginning of the period being determined by means of the counted number $n+3$ coincide with corresponding counted numbers according to the diagram EA. A marking time diagram M and a buffer-in time diagram BI show that the gate G5 in the information registration unit is activated until two data information pieces at the instants D1 and D2 come to the buffer register shortly after each other during the period having the counted number $n+3$ in the diagram EA. The first incoming information piece is immediately registered

in the information register while the latter is buffer stored in the buffer register. $n+3$ becomes the transfer number $t1$ which belongs to the instant D1 and which is compared with the counted numbers according to the diagrams EA and EB. The comparator C2A generates immediately after the first information registration a transfer signal TS1A shown in a time diagram TSA for transfer signals to the data processor part DA, by means of which signal a transfer instruction is selected the execution clock unit TI1A of which is included according to the time diagram EA in the transfer period having the counted number $n+4$. When the numerator NB according to the time diagram EB reaches the counted number $n+3$, a transfer signal TS1B is transferred according to the time diagram TSB for transfer signals to the data processor part DB, and the signal TS1B causes a transfer instruction to be executed during an execution clock unit TI1B shown in the time diagram EB. During the execution clock units TI1A and TI1B, respective gate arrangements GA and GB are activated through the outputs 01 of the processor parts in order to transfer to the processor parts the information piece which has come in first. According to the time diagram M, the gate G5 is activated at the end of the execution clock unit TI1B but only for a short while because the buffer register still stores the second data information piece which has come in at the instant D2 and which is now registered in the information register. The time diagram RN for registered counted numbers shows that the short activation of gate G5 results in that $n+4$ is registered as transfer number $t2$ which belongs to the second information piece having come at instant D2. According to the assumed example in Figure 3, both numerators NA and NB contain the counted numbers $n+4$ and therefore the time diagrams TSA and TSB show second transfer signals TS2A and TS2B with coincident leading edges, due to which transfer instructions are selected, the execution clock units TI2A and TI2B of which according to the time diagrams EA and EB are included in a respective transfer period having the counted number $n+5$. Finally, the time diagram M shows that the marking signal for the second information transfer finishes at the same time as the transfer execution clock unit TI2B which causes, according to the time diagram RN, the number register to register $n+6$ as the momentary biggest counted number according to the time diagrams EA and EB.

The use of the now described method and arrangement guarantees the quickest possible transfer operations and that the processor parts have the same instruction sequence independent of asynchronism between the requests for information transfer and the instruction executions, and above all independent of phase displacements between the instruction executions of the processor parts. If the data processor parts DA and DB according to Figure 1 are designed in such a way that the numerators NA and NB do not count the execution periods EP defined by means of Figure 2, but that executed subsequences are counted instead, then the transfer number generated in a transfer signal generator TSG is modified by means of a conventional +1-adder which is series-connected to the number register NR. Then, the gate arrangement G2 is superfluous because in this case it never happens that one of the comparators C2A and C2B receives corresponding input signals as long as there is no request for information transfer. That the modification due to subsequence counting is necessary is described by means of a time diagram in Figure 4, the references of which correspond with the references used in Figures 2 and 3. It is assumed that the two numerators NA and NB according to the diagrams EA and EB have been stepped to a counted number m when according to diagram M a request for transfer is marked. Without the +1-adder both transfer signals should be generated immediately. Consequently, the jump instruction should be modified which is executed by the data processor part DA and which is contained in the subsequence having the counted number m and the execution clock unit JIAm of which is shown in the diagram EA, but for the data processor part DB it should according to diagram EB be too late to modify the corresponding jump instruction having an execution clock unit JIBm. The jump instructions and also the subsequences which obtain the counted number $m+1$ should no longer correspond, that is the co-operation should be disturbed. By means of the +1-addition, the jump instruction which is defined by means of the transfer number $t=m+1$ is changed in both processor parts. However, the transfer operations become on average longer when counting sub-sequences than when counting execution periods.

WHAT WE CLAIM IS:—

1. A method of transferring data information pieces to two parallel-working data processor parts which execute the same instruction sequence in corresponding periods each of which comprises the execution of at most one transfer instruction due to a requested data information transfer, the requests for data information transfers appearing asynchronously

compared with the execution of the instruction sequence, and wherein such time displacements between corresponding periods may occur that a transfer request is marked during periods of the two data processor parts which are not corresponding to each other, the method comprising the steps of:—

a) registering the said data information pieces one at a time,

b) generating a marking signal in response to each registration of a data information piece,

c) counting the numbers of periods executed in the respective processor parts,

d) registering a transfer number when a marking signal is generated, the transfer number being the counted number of periods if the instruction sequence is executed in corresponding periods in the two data processor parts the bigger counted number of periods if the instruction sequence is executed in the two data processor parts in non-corresponding periods.

e) sending respective transfer signals to the respective processor parts when the said registered transfer number corresponds to the respective counter numbers of periods, and

f) transferring the registered data information piece to the two processor parts when they respectively execute a transfer instruction in response to the respective transfer signal.

2. A method according to claim 1, wherein the registering of the said data information pieces comprises the step of registering the end of the execution of a respective transfer instruction and permitting by means of the end registrations a new data information piece registration only when the previous data information piece is transferred to both processor parts.

3. A method according to claim 1 or 2, wherein the determining of a transfer includes a +1-adding operation.

4. An arrangement for transferring data information pieces, comprising two parallel-working data processor parts which execute the same instruction sequence in corresponding periods each of which, comprises the execution of at most one transfer instruction due to a requested data information transfer, the requests for data information transfers appearing asynchronously compared with the execution of the instruction sequence, and wherein such time displacements between corresponding periods may occur that a transfer request is marked during periods of the two data processor parts which are not corresponding to each other, the arrangement further comprising means for:—

a) registering the said data information pieces one at a time,

b) generating a marking signal in response to each registration of a data information piece,

c) counting the numbers of periods executed in the respective processor parts,

d) registering a transfer number when a marking signal is generated, the transfer number being the counted number of periods if the instruction sequence is executed in corresponding periods in the two data processor parts, and the bigger counted number of periods if the instruction sequence is executed in the two data processor parts in non-corresponding periods,

e) sending respective transfer signals to the respective processor parts when the said registered transfer number corresponds to the respective counter numbers of periods, and

f) transferring the registered data information piece to the two processor parts when they respectively execute a transfer instruction in response to the respective transfer signal.

5. An arrangement according to claim 4, for transferring data information pieces from an information buffer register to information input circuits each belonging to one of the two parallel-working data processor parts each designed to execute the same instruction sequence in corresponding periods and to indicate by means of an output circuit the limits of the said execution periods each of which, due to a requested data information transfer, comprises the execution of at most one transfer instruction in which the activation of the respective information input circuit is included, each processor part being provided with a transfer signal input in order to, when there is a request for an information transfer, receive a transfer signal due to which the associated transfer instruction is selected, the arrangement comprising:—

a) two numerators each being connected to one of the said output circuits of the processor parts,

b) an information registration unit to register the said data information pieces one at a time, being connected to the said buffer register and input circuits and comprising a marking signal generator in order to generate a marking signal in connection with a data information piece registration,

c) control devices connected to the said marking signal generator,

d) a number registration unit to register transfer numbers, being connected to the said control devices,

e) a reversing switch device to connect the number registration unit to one of the

said numerators, whereby the connection to the numerator containing a smaller counting compared to the other numerator is broken, and

f) two comparators having first inputs connected to the number register unit and each having a second input connected to one of the said numerators and each having an output connected to the said transfer signal input of the processor part connected to the last-mentioned numerator, in order to generate the said transfer signal when there is a correspondance between the transfer number and the counted number obtained from the numerator.

6. An arrangement according to claim 5, wherein the said information registration unit comprises an information register, a reading output of which is connected to the said information input circuits and a writing output of which is connected to the said information buffer register through a gate arrangement, a control input of which is connected to a reaction gate in the said marking signal generator, which further comprises two bistable flip-flops connected to the data processor parts respective to the said reaction gate in order to register by means of one stable state the end of the activation of an input circuit each, and to register by means of the second stable state a change of the contents of the information register, which marking signal generator furthermore comprises a marking gate, inputs of which are connected to the said flip-flops and an output of which, constituting the output of the marking signal generator, is connected to a first input of the reaction gate, a second input of which is connected to an output of the buffer register to indicate that this contains at least one data information piece.

7. An arrangement according to claim 5 or 6, wherein the said number registration unit comprises a series connection of +1-adder and a number register.

8. A method of transferring data information pieces, substantially as herein described with reference to the accompanying drawings.

9. An arrangement for transferring data information pieces, substantially as herein described with reference to the accompanying drawings.

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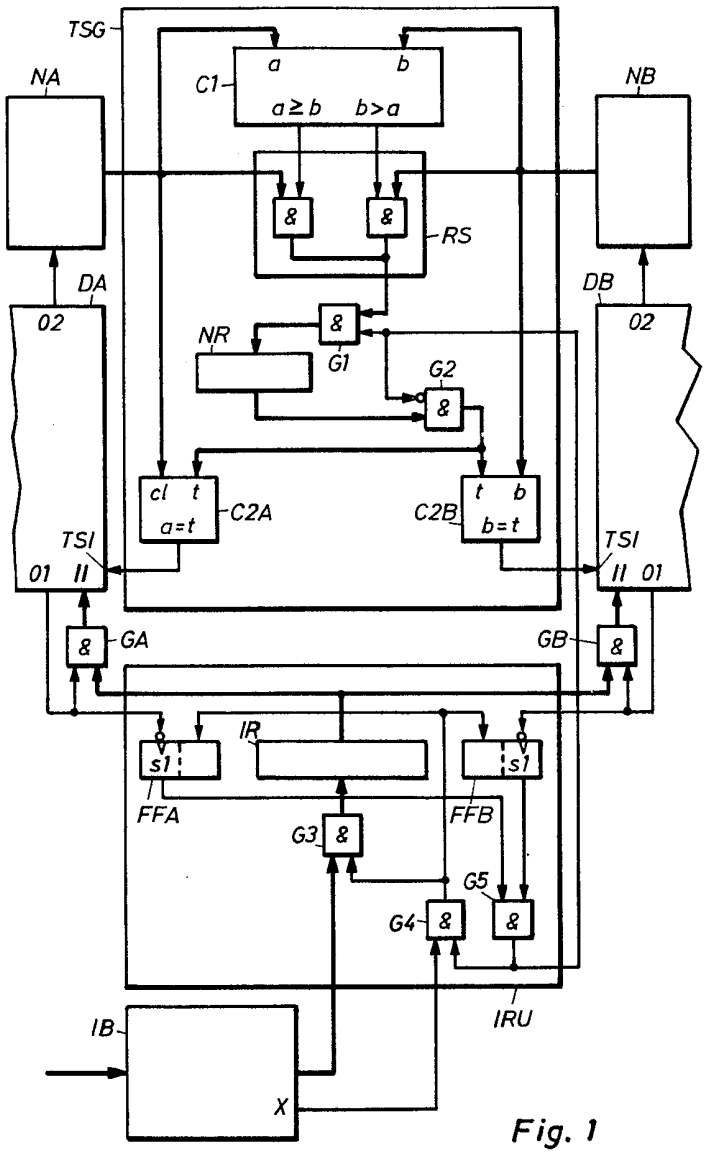
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Fig. 1

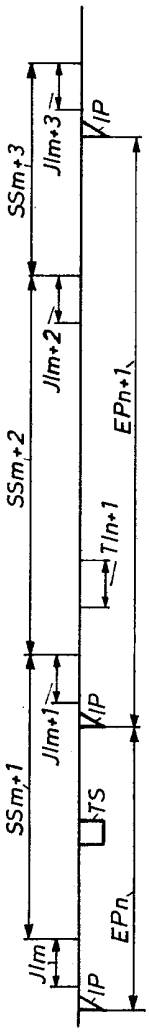

Fig. 2

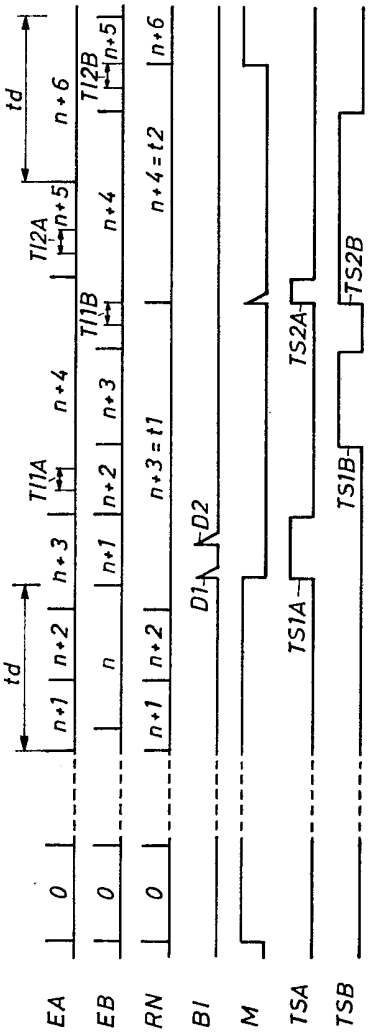

Fig. 3

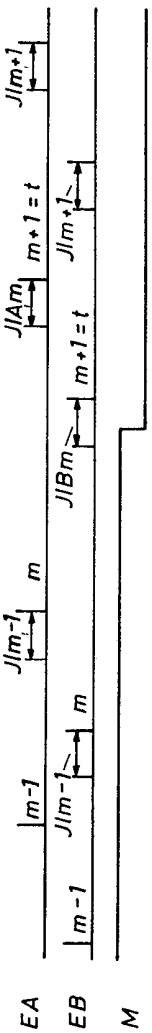

Fig. 4