

(19) World Intellectual Property Organization
International Bureau



PCT



(10) International Publication Number
WO 2008/019391 A1

(43) International Publication Date
14 February 2008 (14.02.2008)

(51) International Patent Classification:
***H03K 17/06* (2006.01) *H02J 7/00* (2006.01)**

(21) International Application Number: PCT/US2007/075672

(22) International Filing Date: 10 August 2007 (10.08.2007)

(25) Filing Language: English

(26) **Publication Language:** English

(30) Priority Data:

60/822,193	11 August 2006 (11.08.2006)	US
11/609,894	12 December 2006 (12.12.2006)	US

(71) Applicant (for all designated States except US): CIRRUS LOGIC, INC. [US/US]; 2901 Via Fortuna, Austin, TX 78746 (US).

(72) **Inventor:** MELANSON, John, L.; 901 West 9th Street, #201, Austin, TX 78703 (US).

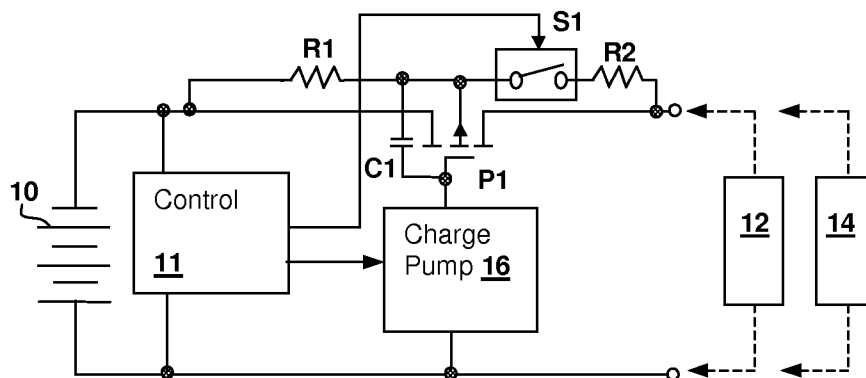
(74) **Agent: HARRIS, Andrew, Mitchell;** Mitch Harris Attorney At Law, L.l.c., P.o. Box 515, Lakemont, GA 30552-0515 (US).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GO, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(54) Title: CHARGE-PUMP BIASED BATTERY PROTECTION CIRCUIT



(S7) Abstract: A battery protection circuit provides improved efficiency, reduced power dissipation, and reduced complexity in battery powered (P1) such that the voltage between the pass transistor gate and the drain/source terminals of the pass transistor have a magnitude greater than the battery voltage, reducing the voltage drop across the pass transistor. The charge pump may be controlled in conformity with a sensed current through the pass transistor, so that at times of lower current loads, power is conserved. The bulk (body) of the pass transistor can be controlled using a resistor (R1) coupling a battery terminal to the bulk and a single switch (S1) coupling the bulk to a charger/load connection terminal, permitting a single pass transistor to be used for charging and discharging.



CHARGE-PUMP BIASED BATTERY PROTECTION CIRCUIT**FIELD OF THE INVENTION**

5

[0001] The present invention relates generally to battery protection circuits, and more specifically, to a charge-pump biased battery protection circuit having reduced leakage, improved efficiency and reduced complexity.

10

BACKGROUND OF THE INVENTION

[0002] Devices incorporating rechargeable batteries, such as Lithium ion (Li^+) batteries and Nickel metal hydride (NiMH) batteries, typically incorporate circuits that protect the battery during charging and discharging. U.S. Patent 6,670,790 to Stellberger, incorporated herein by reference, details several such battery protection circuits, which typically include one or more pass transistors with gate control electronics that limit the current during discharging and charging of the battery. The protection circuits also typically completely disables the discharging action when the battery output voltage falls to too low a level, i.e., when the internal resistance of the battery rises too high due to the level of discharge.

25

[0003] However, such battery protection circuits are inefficient in that the voltage drop across the pass transistor is substantial, causing a waste of available battery energy as dissipation in the pass transistor during discharge. In

5 particular, during intervals of high current drain, the energy loss and power dissipation due to the pass transistor voltage drop are typically substantial. The result is reduced battery cycle life as well as a requirement for pass transistors and/or heat management with the capability to handle the dissipation
10 during such intervals, making it difficult to integrate such circuits on a die with other circuits.

[0004] In the improvement introduced in the above-incorporated U.S. Patent Application, the number of required
15 pass transistors is reduced to one, by control of the bulk (body) voltage of a single enhancement field-effect transistor (FET) so that conduction can be provided in either direction through the pass transistor. However, the management of the bulk voltage requires two switches as shown in Figure 2 of the above-
20 incorporated U.S. Patent Application and the separate control of the switches introduces further complexity in the control circuit. Further, the voltage drop across even a single FET can still have a significant impact on efficiency and power dissipation during intervals of heavy discharge.

[0005] Therefore, it would be desirable to provide a battery protection circuit that has improved efficiency and reduced power dissipation. It would further be desirable to provide such
5 a battery protection circuit that uses a single pass transistor, but has reduced control circuit complexity.

DISCLOSURE OF THE INVENTION

[0006] The above stated objectives of providing a battery protection circuit having improved efficiency, reduced power
5 dissipation and that uses a single pass transistor with a reduced-complexity control circuit, are accomplished in a charge-pump biased battery protection circuit.

[0007] The battery protection circuit includes a pair of
10 battery terminals for connecting a battery and a pair of input/ output terminals for alternatively connecting one of a charger or a load, depending on whether the battery is being charged or used to power the load(discharged). A pass transistor is coupled between one of the battery terminals and
15 the input/output terminals for controlling current passing between the battery and the charger or load. A charge pump supplies a voltage to the gate of the pass transistor so that the voltage between the gate and drain/source terminals of the transistor has a magnitude greater than the voltage across the
20 battery terminals, providing a reduced voltage drop across the pass transistor. The charge pump voltage may be reduced during times of lower current drain as measured by a current-sensing circuit.

25 **[0008]** The bulk (body) of the pass transistor is controlled

in conformity with the current flow direction through the pass transistor, so that the bulk is biased to prevent conduction with the drain/source connections. A resistor is coupled between the bulk and the battery terminal that is connected to the drain/source connection of the pass transistor. A single switch is coupled between the bulk and the input/output terminal that is connected to the other drain/source connection of the pass transistor. Controlling the switch controls the current flow through the pass transistor.

10

[0009] The foregoing and other objectives, features, and advantages of the invention will be apparent from the following, more particular, description of the preferred embodiment of the invention, as illustrated in the accompanying drawings.

15

DESCRIPTION OF THE DRAWINGS

[0010] **Figure 1** is a schematic diagram depicting a battery protection circuit in accordance with an embodiment of the invention.

[0011] **Figure 2** is a schematic diagram depicting a battery protection circuit in accordance with another embodiment of the invention.

[0012] **Figure 3** is a schematic diagram depicting a battery protection circuit in accordance with yet another embodiment of the invention.

[0013] **Figure 4** is a schematic diagram depicting a battery protection circuit in accordance with still another embodiment of the invention.

[0014] **Figure 5** is a schematic diagram depicting a control circuit that may be used to implement control circuit **11** of Figures **1A**, **1B**, **2A**, and **2B**.

[0015] **Figure 6** is a signal diagram depicting signals within the battery protection circuits of Figures **1A**, **1B**, **2A**, and **2B**.

BEST MODE FOR CARRYING OUT THE INVENTION

[0016] The present invention encompasses a battery protection circuit for incorporation within battery-powered devices, and in particular, that can be incorporated within an integrated circuit. The battery protection circuit provides improvement in that a single pass transistor having a smaller area can be used and/or a lower voltage drop is provided across the pass transistor, raising the efficiency of the circuit while lowering power dissipation. Further, the increase in gate to drain/source connection voltage increases the breakdown voltage of the circuit, which aids in preventing damage due to improper charger voltage application to the charger terminals or in the case of charger failure or over-voltage conditions. A charge pump is used to raise the gate voltage of the pass transistor to a voltage level beyond the range of the battery/charger power supply voltages, so that the resistance of the pass transistor is reduced during charging and discharging of the battery. The charge pump may be disabled during low current discharge conditions, so that battery power is not wasted operating the charge pump when the power consumed by the charge pump approaches that of the power savings in the pass transistor.

[0017] Referring now to **Figure 1**, a battery protection circuit in accordance with an embodiment of the present invention is shown. A battery **10** is coupled to either a load **12** or a charger **14**, depending on whether the battery is being charged by the charger or discharged to the load, by a pass transistor **P1**, which in the depicted embodiment is an enhancement mode field effect transistor (FET). A charge pump **16**, provides for charging the gate of pass transistor **P1** to a voltage beyond the range of the voltage of battery **10**, providing for a gate voltage that turns on transistor **P1**. In the depicted embodiment, the output of charge pump **16** is a negative voltage less than the voltage at the negative terminal of battery **10**. However, it is understood that an N-channel FET may be used to provide battery protection, and would then be connected between the negative terminal of battery **10** and the negative input/output terminal that connects to load **12** or charger **14**. In such an embodiment, the charge pump voltage is a positive level exceeding that of the battery **10** positive terminal voltage.

[0018] A control circuit **11**, provides control of charge pump **16** so that charge pump is only activated during times of charging or during high current discharge conditions, so that power is not wasted operating charge pump **16** when little or no

current is being drained from battery **10**. Details of various discharge sensing arrangements will be described below with reference to Figures 2-4. When charger **14** is not connected or is not powered, switch **S1** disconnects a path through resistor **R2** to the positive input/output terminal in response to control circuit **11**. When charger **14** is supplying a charging voltage, switch **S1** is closed.

Resistor **R2** may not be needed, depending on the resistance of switch **S1**. Resistor **R1** couples the bulk of transistor **P1** to battery **10**, so that when switch **S1** is open or when switch **S1** is closed and no charger is connected, the body of transistor **P1** is held at the positive terminal voltage of battery **10**. Switch **S1** is deactivated when battery **10** is in a discharged state, so that further discharge does not occur through a connected charger **14**, if charger **14** is connected but un-powered. A capacitor **C1** may be provided to stabilize the bulk voltage of transistor **P1**, which otherwise may be pulled below the drain/source connection voltages, for example, when a momentary short-circuit or reverse charger polarity is caused across the input/output terminals.

[0019] Referring now to **Figure 2**, a battery protection circuit in accordance with another embodiment of the invention is shown. The depicted embodiment is similar in structure and function to the embodiment of Figure 1, and therefore only

differences between them will be described below. In the embodiment of **Figure 2**, a current sensing circuit that can provide an indication of pass transistor drain-source current level to control circuit **11** is included. Current sensing is provided by two current mirrors implemented by transistors **P2** and **P3**. Transistors **P2** and **P3** are sized much smaller than transistor **P1**, and provide currents to control circuit **11** that are proportional to the current through transistor **P1** while transistor **P1** is operating in the active region in either direction. Transistor **P2** is utilized to sense the current through transistor **P1** during charging, and transistor **P3** is utilized to sense the current through transistor **P1** when battery **10** is being discharged. Control circuit **11** then can compare the appropriate current indication to threshold levels to determine when the current level provided to load **12** is low enough that it is advantageous to disable charge pump **16** to save power.

[0020] Referring now to **Figure 3**, a battery protection circuit in accordance with yet another embodiment of the invention is shown. The depicted embodiment is similar in structure and operation to the embodiment of Figures 1 and 2, and therefore only differences between them will be described below. In the embodiment of **Figure 3**, another current sensing circuit that can provide an indication of pass transistor drain-

11

source current level to control circuit **11** is included. Current sensing is provided by a series resistor **R4**. The voltage drop across resistor **R4** is detected by control circuit **11** to directly measure the current through transistor **P1**.

5

[0021] Referring now to **Figure 4**, a battery protection circuit in accordance with still another embodiment of the invention is shown. The depicted embodiment is similar in structure and operation to the embodiment of Figures 1-3, and therefore only differences between them will be described below. In the embodiment of **Figure 4**, another current sensing circuit that can provide an indication of pass transistor drain-source current level to control circuit **11** is included. Current sensing is provided by directly measuring the voltage drop across the drain/source connections of transistor **P1**. The drain-source voltage drop is detected by control circuit **11** to directly measure the current through transistor **P1**, taking into account whether or not charge pump **16** is boosting the gate voltage of transistor **P1**.

15
20

[0022] A second charge pump **16A** is included to boost the bulk voltage of transistor **P1** to a voltage higher than the voltage at the positive terminal of battery **10**, in particular when the battery is discharged, so that pass transistor **P1** is

biased further into the cut-off region. Optionally, during times of high current drain in the discharging state, charge pump **16A** can set the bulk voltage of pass transistor **P1** to a level slightly below that of the drain/source connections of

5 transistor **P1**, so that the junctions between the body and the drain/source elements is biased just below turn-on. Biasing the junctions in this manner produces a behavior similar to that of a junction FET (JFET), further reducing the on-resistance of transistor **P1**. A switch **S2** is provided to de-couple charge pump
10 **16A** during charging and during discharge if charge pump **16A** is not utilized to bias the gate of transistor **P1** below the drain/source connections of transistor **P1**.

[0023] Referring now to **Figure 5**, an exemplary control

15 circuit **11** and charge pumps **16,16A** are shown, as may be used in the above-illustrated battery protection circuits. Control circuit **11** includes a logic **42** that controls switches **S40**, **S42** and **S43** of charge pumps **16,16A**, as well as a switch **S41** that controls the application of the output of charge pump **16** to the
20 gate of pass transistor **P1**. Switch **S41** selects between the output of charge pump **16** during heavy discharge, ground (**-Vbatt**) during periods of light discharge and (**+Vbatt**) to turn off transistor **P1** when the battery is discharged below a minimum charge level or when the battery is charged above a maximum

charge level. The sense voltage **V_{sense}** provided by one of the techniques illustrated in the circuits of Figures 1-4 is compared to a set of threshold voltages **V_{t1}-V_{t4}** by a set of corresponding comparators **K1-K4** that determine whether the battery is charging or discharging, and further whether the battery is over-discharged or charged to a maximum level. The outputs of comparators **K1-K4** is sensed by logic **42**, which sets the various switch and charge pump states described above with reference to Figures 1-3.

[0024] Charge pumps **16** and **16A** are illustrated as charge pumps that receive clock (pulse) signals from logic **42**, which is coupled to an oscillator **40** for providing a clock source. Logic **42** gates the clock signal from oscillator **40** independently to provide pulse signals that independently activate charge pumps **16** and **16A**, when their action is needed as described above to bias the bulk and gate of transistor **P1**. Capacitors **C40**, **C42** are charged when the corresponding pulse signal is in a logic high state through switch **S40**, **S42** and then the charge is applied in opposite polarity through switch **S40**, **S42** to an output capacitor **C41**, **C43** which may be provided the gate and bulk capacitances of pass transistor **P1**. A switch **S43** provides for changing the polarity of charge pump **16A** in response to control logic **11** to optionally pull the bulk of transistor **P1** slightly above the

drain/source connection voltage levels during heavy discharge as described above.

[0025] Referring now to **Figure 6**, operation of the above-
5 described circuits is depicted in a signal diagram. Prior to time **T1** the battery is discharged at a low rate, but from time **T1** to time **T2**, a higher rate of discharge begins. As the drain-source voltage V_{DS} of transistor **P1** increases due to the higher discharge current I_{DS} , the gate voltage V_G is lowered at time **T2**
10 by the action of charge pump **16** in response to the detected level of I_{DS} and/or V_{DS} . The result is that V_{DS} decreases, resulting in the output voltage to the load V_{in_out} increasing slightly as shown. At time **T3**, control circuit **11** detects that battery **10** has become discharged to the minimum allowable value
15 and the **S1ctl** signal is asserted to disable switch **S1**. Also, charge pump **16** is deactivated and the gate of transistor **P1** is raised to the level of the battery positive terminal voltage, turning off transistor **P1**. At time **T4**, a charger is connected, switch **S1** is enabled, and charge pump **16** is activated and the
20 battery begins to charge. At time **T5**, control logic **11** detects that the battery has reached the maximum charge level and charge pump **16** is disabled, preventing overcharging by disabling transistor **P1**.

[0026] While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form, and details may be made
5 therein without departing from the spirit and scope of the invention.

CLAIMS

WHAT IS CLAIMED IS:

1. A battery protection circuit for charging a battery from a
5 charger and discharging said battery to a load, said circuit
comprising:

a pair of battery terminals for connecting said battery;

an input-output terminal for connecting at least one of
said load and said charger;

10 a pass transistor having a first drain/source connection
coupled to a given one of said battery terminals and a second
drain/source connection coupled to said input-output terminal;
and

a charge-pump circuit having an output coupled to a gate
15 of said pass transistor, wherein said charge pump circuit
charges said gate of said pass transistor to a gate voltage such
that a magnitude of a voltage between said gate of said pass
transistor and said first drain/source connection is greater
than a magnitude of a voltage across said battery terminals.

20
2. The battery protection circuit of Claim 1, further comprising
a current-sensing circuit for sensing a magnitude of a current
provided to said load, wherein an output of said current-sensing
circuit is coupled to a control input of said charge pump, and
25 wherein said charge pump only charges said gate of said pass

transistor to cause said magnitude of said gate-to-drain voltage of said pass transistor to exceed said magnitude of said voltage across said battery terminals when said magnitude of said current is greater than a threshold current level.

5

3. The battery protection circuit of Claim 2, wherein said current-sensing circuit comprises a current mirror for mirroring a current through said pass transistor.

10

4. The battery protection circuit of Claim 2, wherein said current-sensing circuit comprises a sense resistor coupled in series with one of said drain/source connections.

15

5. The battery protection circuit of Claim 2, wherein said current-sensing circuit comprises a detector for detecting a level of voltage difference between said first drain/source connection and said second drain/source connection of said pass transistor.

20

6. The battery protection circuit of Claim 1, wherein said pass transistor further comprises a bulk terminal connected to a body of said pass transistor, and wherein said circuit further comprises:

a first resistor coupled between said given battery terminal and said bulk terminal;

a switch coupled between said input-output terminal and said bulk terminal; and

5 a control circuit coupled to a control input of said switch, wherein said switch is set to a conducting state when a charging current is supplied to said input-output terminal to charge said battery and wherein said switch is set to a non-conducting state when a discharging current is supplied from
10 said battery to said input-output terminal.

7. The battery protection circuit of Claim 6, further comprising a capacitor coupled from said bulk terminal to said gate of said pass transistor, whereby changes in a voltage of said bulk
15 terminal due to changes in said voltage at said input-output terminal are reduced.

8. The battery protection circuit of Claim 1, further comprising a second charge pump having an output coupled to a body of said
20 pass transistor, for charging said body of said pass transistor to a voltage having a polarity opposite a polarity of said gate voltage with respect to both of said drain/source terminals of said pass transistor.

9. A battery protection circuit for charging a battery from a charger and discharging said battery to a load, said circuit comprising:

a pair of battery terminals for connecting said battery;

5 an input-output terminal for connecting at least one of said load and said charger;

a pass transistor having a first drain/source connection coupled to a given one of said battery terminals and a second drain/source connection coupled to said input-output terminal;

10 a first resistor connected between said given battery terminal and a bulk terminal of said pass transistor;

a switch coupled between said input-output terminal and said bulk terminal; and

a control circuit coupled to a control input of said switch, wherein said switch is set to a conducting state when a charging current is supplied to said input-output terminal to charge said battery and wherein said switch is set to a non-conducting state when a discharging current is supplied from said battery to said input-output terminal.

20

10. The battery protection circuit of Claim 9, further comprising a second resistor coupled between said input-output terminal and said bulk terminal in series with said switch.

11. The battery protection circuit of Claim 9, further comprising a capacitor coupled from said bulk terminal to a gate of said pass transistor, whereby changes in a voltage of said bulk terminal due to changes in a voltage at said input-output
5 terminal are reduced.

12. A method for protecting a battery when charging said battery from a charger and discharging said battery to a load, said method comprising:

10 controlling a current passing between said battery and one of said charger and said load using a pass transistor; and
charging a gate of said pass transistor to a gate voltage such that a magnitude of a gate-to-drain voltage of said pass transistor is greater than a magnitude of a voltage across said
15 battery.

13. The method of Claim 12, further comprising detecting a magnitude of said current, and wherein said charging is performed only when said determining determines that said
20 magnitude of said current is greater than said threshold.

14. The method of Claim 12, further comprising:

setting a body voltage of said pass transistor by a circuit having a first resistor coupling said body to said load and a switch coupling said body to said battery; and

5 opening said switch when said current is passing from said battery to said load.

15. The method of Claim 12, further comprising charging a body of said pass transistor to a voltage having a polarity opposite
10 a polarity of said gate voltage with respect to both drain/source terminals of said pass transistor.

16. A method for protecting a battery when charging said battery from a charger and discharging said battery to a load, said
15 method comprising:

controlling a current passing between said battery and one of said charger and load using a pass transistor;

setting a body voltage of said pass transistor by a circuit having a first resistor coupling said body to said load
20 and a switch coupling said body to said battery; and

opening said switch when said current is passing from said battery to said load.

17. The method of Claim 16, further comprising limiting a current through said switch with a second resistor coupled in series with said switch.

5 18. The method of Claim 16, further comprising charging a body of said pass transistor to a voltage having a polarity opposite a polarity of said gate voltage with respect to both drain/source terminals of said pass transistor.

10 19. A battery protection circuit for charging a battery from a charger and discharging said battery to a load, said circuit comprising:

a pair of battery terminals for connecting said battery;

an input-output terminal for connecting at least one of

15 said load and said charger;

a pass transistor having a first drain/source connection coupled to a given one of said battery terminals and a second drain/source connection coupled to said input-output terminal;

a charge-pump circuit having an output coupled to a gate
20 of said pass transistor, wherein said charge pump circuit charges said gate of said pass transistor to a gate voltage such that a magnitude of a voltage between said gate of said pass transistor and said first drain/source connection is greater than a magnitude of a voltage across said battery terminals;

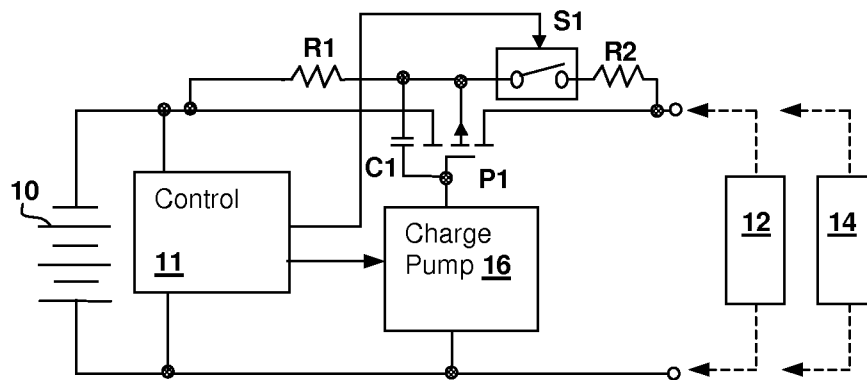
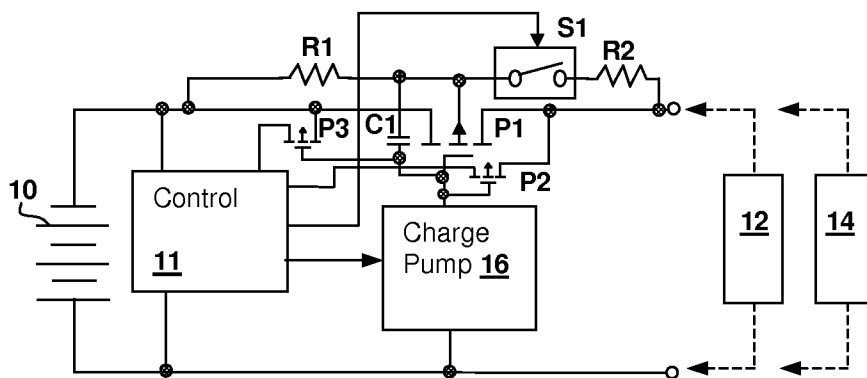
a first resistor connected between said given battery terminal and a bulk terminal of said pass transistor;

a switch coupled between said input-output terminal and said bulk terminal; and

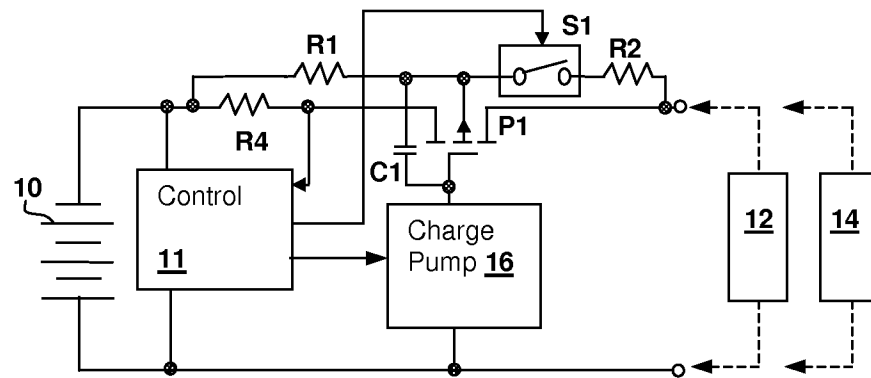
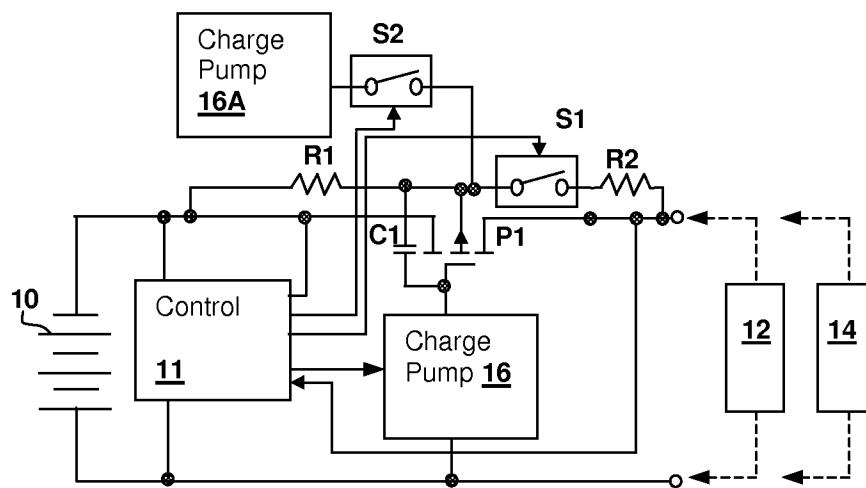
5 a control circuit coupled to a control input of said switch, wherein said switch is set to a conducting state when a charging current is supplied to said input-output terminal to charge said battery and wherein said switch is set to a non-conducting state when a discharging current is supplied from
10 said battery to said input-output terminal.

20. The battery protection circuit of Claim 19, further comprising a second charge pump having an output coupled to a body of said pass transistor, for charging said body of said
15 pass transistor to a voltage having a polarity opposite a polarity of said gate voltage with respect to both of said drain/source terminals of said pass transistor.

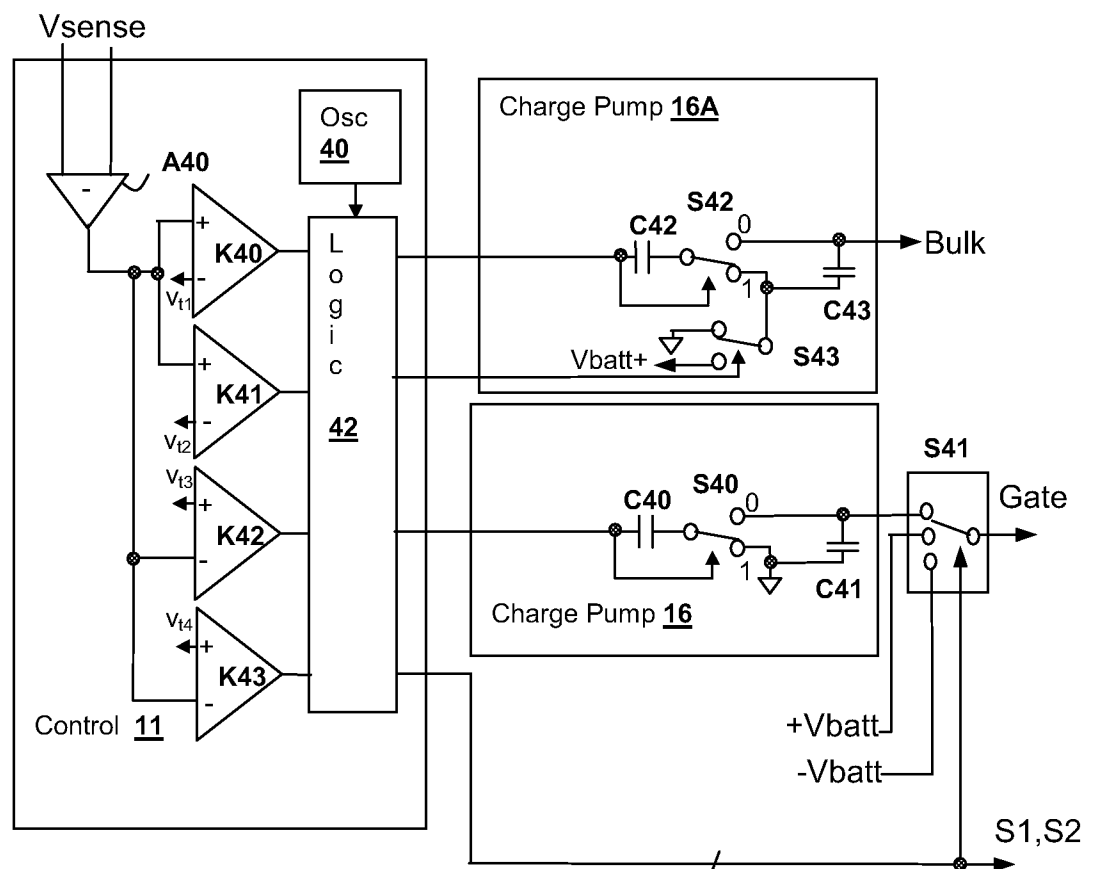
1/4

**Fig. 1****Fig. 2**

2/4

**Fig. 3****Fig. 4**

3/4

**Fig. 5**

4/4

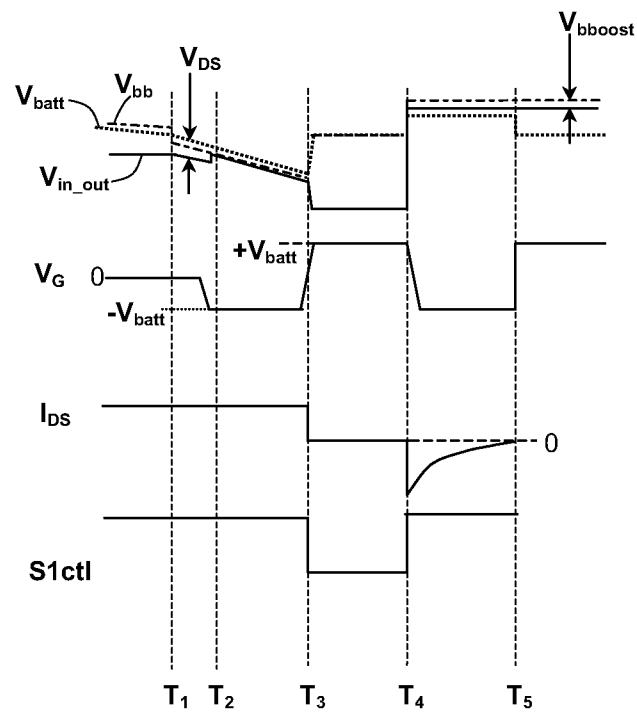


Fig. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/075672

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K17/06 H02J7/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K H02J H01M G05F H02H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 400 209 B1 (MATSUYAMA TOSHIYUKI [JP] ET AL) 4 June 2002 (2002-06-04) column 2, line 58 - column 3, line 16; figure 5	1,12
X	US 2005/040792 A1 (NAIR RAJENDRAN [US]) 24 February 2005 (2005-02-24) paragraph [0021]; figures 1,2	1,12
X	EP 0 626 745 A (SILICONIX INC [US]) 30 November 1994 (1994-11-30) column 6, line 17 - column 7, line 27; figures 3,4	1,12
X	EP 0 729 185 A (TEXAS INSTRUMENTS FRANCE [FR]; TEXAS INSTRUMENTS INC [US] TEXAS INSTRU) 28 August 1996 (1996-08-28) page 6, line 21 - line 31; figure 1	1,12
	----- -/--	

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier document but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- "&" document member of the same patent family

Date of the actual completion of the international search

19 November 2007

Date of mailing of the international search report

30/11/2007

Name and mailing address of the ISA/
European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Braccini, Roberto

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/075672

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 670 790 B2 (STELLBERGER ACHIM [DE]) 30 December 2003 (2003-12-30) cited in the application abstract; figure 6 -----	9,10,16, 17
A	US 5 933 046 A (RAMET SERGE [FR] ET AL) 3 August 1999 (1999-08-03) the whole document -----	1-20

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/075672

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 6400209	B1	04-06-2002	JP	2001051730 A	23-02-2001
US 2005040792	A1	24-02-2005	NONE		
EP 0626745	A	30-11-1994	DE	69417286 D1	29-04-1999
			DE	69417286 T2	19-08-1999
			JP	3387631 B2	17-03-2003
			JP	7184318 A	21-07-1995
			US	5539610 A	23-07-1996
EP 0729185	A	28-08-1996	DE	69632880 D1	19-08-2004
			DE	69632880 T2	16-12-2004
			FR	2731111 A1	30-08-1996
			JP	8340112 A	24-12-1996
US 6670790	B2	30-12-2003	EP	1320168 A1	18-06-2003
			US	2003122525 A1	03-07-2003
US 5933046	A	03-08-1999	FR	2738424 A1	07-03-1997