

July 5, 1966

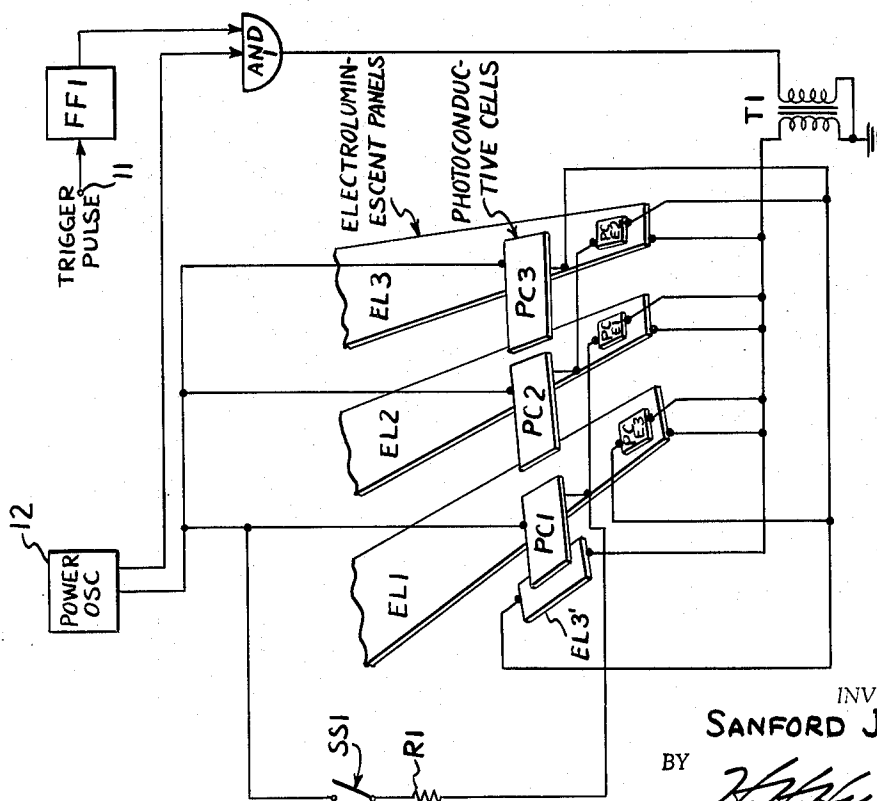
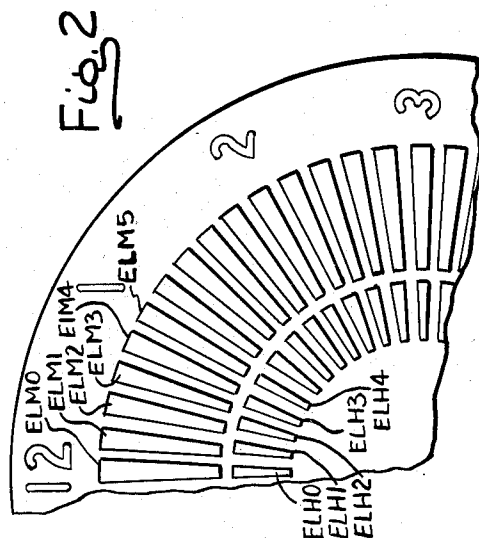
S. J. DEMBY

3,258,906

SOLID STATE CLOCK

Filed March 4, 1964

3 Sheets-Sheet 1



INVENTOR.
SANFORD J. DEMBY
BY *H. H. Kulse*
ATTY.

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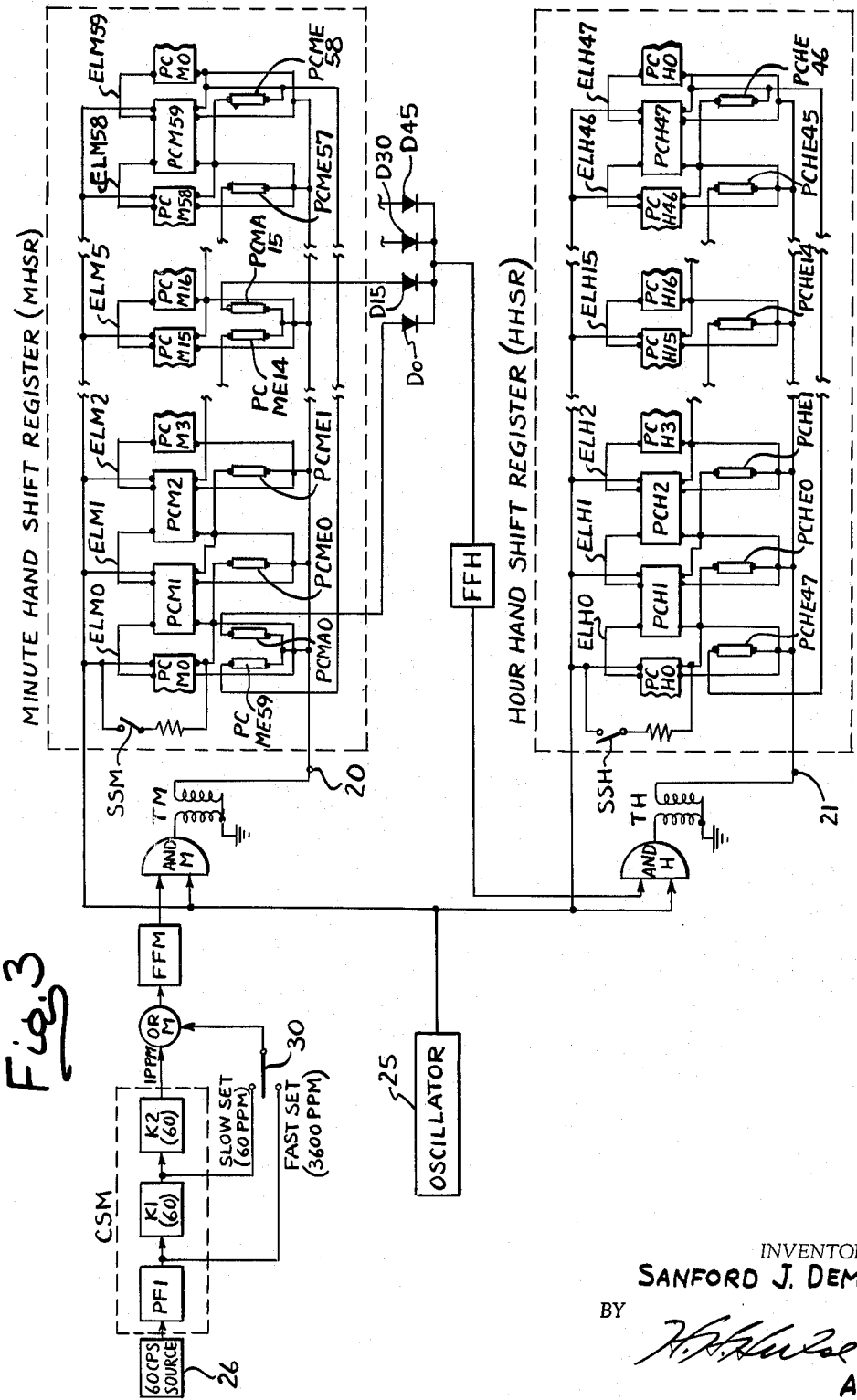
S. J. DEMBY

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SOLID STATE CLOCK

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3 Sheets-Sheet 2



INVENTOR.
SANFORD J. DEMBY
BY
[Signature]
ATTY.

July 5, 1966

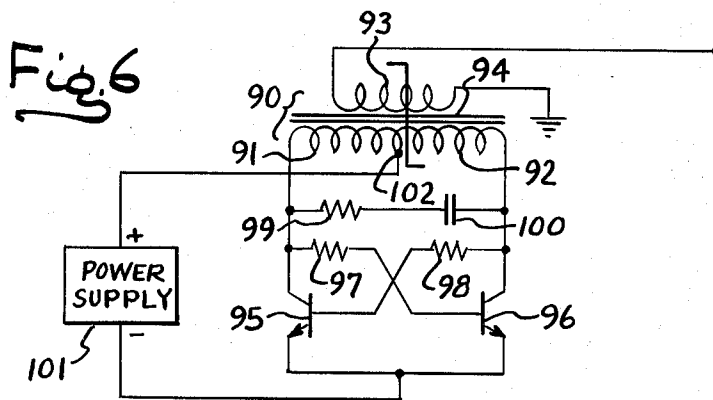
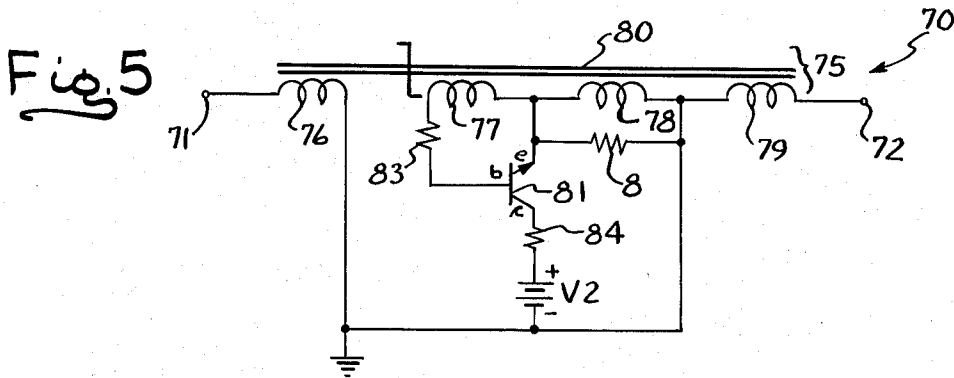
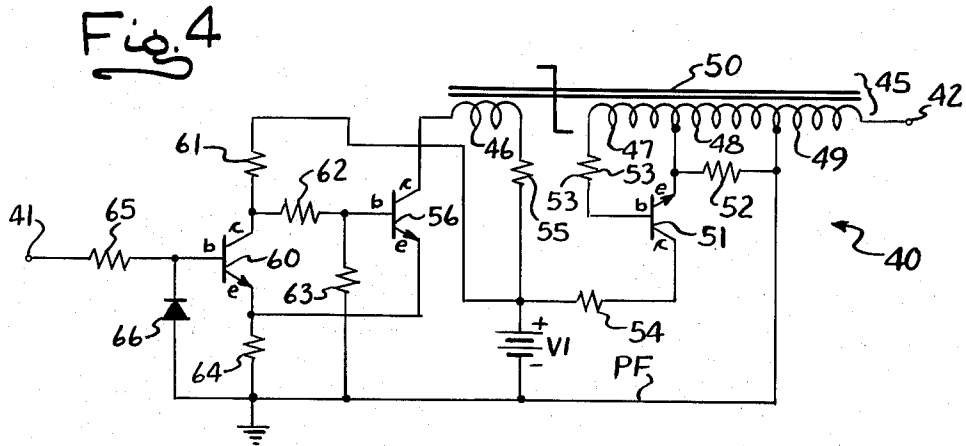
S. J. DEMBY

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SOLID STATE CLOCK

Filed March 4, 1964

3 Sheets-Sheet 3



INVENTOR.
SANFORD J. DEMBY
BY *[Signature]*
ATTY.

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3,258,906

SOLID STATE CLOCK

Sanford J. Demby, Bronx, N.Y., assignor to General Time Corporation, New York, N.Y., a corporation of Delaware

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10 Claims. (Cl. 58-50)

The present invention relates to a solid state clock and more specifically to a solid state clock employing shift registers which include electroluminescent panels oriented at positions on a clockface corresponding to the positions of the clock hands, the panels being selectively illuminated to indicate the time.

A primary object of this invention is to provide a new and improved clock having no moving parts which has little thickness and which may be readily applied to a flat wall. Another object is to provide such a solid state clock characterized by accuracy, stability, and long life and which is particularly susceptible to being made in large size to produce a spectacular, eye-catching display for advertising and promotional purposes. Still another object is to provide a new and improved shift register characterized by accuracy, stability, and long life.

More specifically, an object of this invention is to provide a solid state clock utilizing at least two sets of electroluminescent panels, wherein each set includes a plurality of electroluminescent panels or rods which, for example, are radially oriented on a circular clockface at positions corresponding to the positions of the clock hands, which are selectively illuminated to indicate the time, and which may be readily seen either in the dark or under normal conditions of illumination. Further along these lines, an object of this invention is to provide a solid state clock of this type wherein two sets of panels are provided, illuminated panels in the sets respectively representing the positions of the minute and hour hands of the clock.

A still more specific object of the present invention is to provide a solid state clock employing a pair of shift registers each including a plurality of electroluminescent panels, characterized in that succeeding ones of the electroluminescent panels are illuminated in response to the application of input pulses to the shift registers. A related object is to provide a solid state clock of this type characterized in that the time relationships between the applications of input pulses to the shift registers are varied according to different time functions so that succeeding ones of the panels in one shift register are controllably illuminated to indicate the movement of the minute hand and succeeding ones of the panels in the other shift register are controllably illuminated to indicate the movement of the hour hand.

Another primary object of the present invention is to provide a new and improved shift register employing electroluminescent panels.

An additional object is to provide a new and improved frequency divider.

Other objects and advantages of this invention will become apparent upon reading the attached detailed description and upon reference to the drawings, in which:

FIGURE 1 illustrates a shift register employing electroluminescent panels which is constructed in accordance with the teachings of the present invention;

FIG. 2 is a fragmentary view of the face of a clock illustrating the positions of electroluminescent panels thereon which are connected in shift registers or ring counters;

FIG. 3 is a schematic diagram of a solid state clock employing shift registers as shown in FIG. 1;

FIG. 4 is a schematic diagram of a typical magnetic

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pulse former which may be utilized in the solid state clock of FIG. 3;

FIG. 5 is a schematic diagram of a typical magnetic counter which may be utilized in the solid state clock of FIG. 3; and

FIG. 6 is a schematic diagram of a magnetic oscillator which may be utilized in the solid state clock of FIG. 3.

While the invention has been described in connection with certain preferred embodiments, it is to be understood that the invention is not to be limited to the disclosed embodiments but, on the contrary, the invention is intended to cover the various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

In accordance with one feature of the present invention, a shift register (ring counter) is provided which employs a plurality of electroluminescent panels as succeeding stages thereof. More specifically, such a shift register is provided wherein means are provided for responding to an input pulse to (1) cause the next succeeding panel to be illuminated and (2) cause the previously illuminated panel to be extinguished.

Referring to FIG. 1, an exemplary shift register (ring counter) is illustrated which employs a plurality of electroluminescent panels EL1-EL3. The shift register has an input terminal 11 to which input pulses are applied for causing the panels EL1-EL3 to be selectively and successively illuminated. In response to the application of a pulse to the input terminal 11, a monostable flip-flop FF1, i.e., a "one-shot" multivibrator, is triggered to provide an output pulse having a predetermined amplitude and time period. The output of the flip-flop FF1 is transmitted to a gate AND1 causing the gate to be opened for the predetermined time period so that the output of a power oscillator 12 is transmitted therethrough to the primary of a "step-up" transformer T1. The secondary of the transformer T1 is connected to the electroluminescent panels EL1-EL3 so that a "trigger" voltage signal is applied to the panels during the time period when an output pulse is provided by the flip-flop FF1. The "trigger" signal is insufficient in amplitude to cause the panels to be illuminated and, as will be apparent, is in essence an auxiliary illuminating power signal which causes a conditioned panel to be illuminated.

For the purpose of conditioning one of the panels EL1-EL3 to be illuminated in response to the application of a "trigger" signal thereto, "conditioning" photoconductive cells PC1-PC3 are physically mounted adjacent the panels in overlapping, spaced relationship therewith. Thus, cell PC1 is mounted to partially overlap panel EL1, cell PC2 is mounted to partially overlap panels EL1 and EL2, and cell PC3 is mounted to partially overlap panels EL2 and EL3. The output of the power oscillator 12 is electrically connected to the panels EL1-EL3 through the respective photoconductive cells PC1-PC3, the voltage signal provided across the panels by the oscillator constituting the main illuminating signal. As is well known, photoconductive cells are resistive elements and the resistance values thereof are dependent upon the amount of light projected thereon. Accordingly, when an electroluminescent panel is in the non-illuminated or off condition, the associated photoconductive cells will be in their high resistive states and the conduction therethrough from the power oscillator 12 is such that the voltage signals applied across the electroluminescent panels electrically associated therewith are insufficient to cause illumination thereof. Conversely, when an electroluminescent panel is illuminated, the light emitted thereby is projected onto the associated photoconductive cells so that the resistances thereof are reduced. In response to the reduction in resistance of a photoconductive cell, a greater voltage signal is applied

across the electroluminescent panel electrically associated therewith which conditions the panel for illumination in response to the application of a "trigger" signal thereto. Since the main illuminating signal and the "trigger" or auxiliary signal are both derived from the oscillator 12, it follows that these signals will be in phase.

For a better understanding of the illuminating operation, let it be assumed that initially the panel EL1 is partially illuminated. Under such conditions, light emitted from the panel EL1 on the cells PC1 and PC2 causes the resistance values thereof to be reduced. The reduction in resistance of the cell PC1 allows for the voltage applied to the panel EL1 from the oscillator 12 to increase, resulting in greater illumination of the panel and thus further reduction in the resistance of cells PC1 and PC2. As a result, a regenerative action takes place causing the panel EL1 to become fully illuminated. On the other hand, the reduction in resistance of the cell PC2 merely conditions the panel EL2 for illumination since the conduction therethrough from the power oscillator 12 is still not sufficient for the panel EL2 to be illuminated. However, when a subsequent "trigger" signal is applied to the panel EL2 it is of such phase and magnitude that, when added to the signal applied to the panel EL2 by the power oscillator through the cell PC2, it causes the panel EL2 to become partially illuminated. In response to the partial illumination of the panel EL2, light is emitted therefrom onto the cell PC2 causing the resistance thereof to be further reduced. A similar regenerative action then takes place with respect to panel EL2 causing this panel to become fully illuminated. The light emitted by panel EL2 also projects onto the cell PC3 causing the panel EL3 to become conditioned for illumination in response to the next succeeding "trigger" signal.

For the purpose of causing the first panel EL1 to be conditioned for illumination when the last panel EL3 is illuminated, a supplementary electroluminescent panel EL3' is mounted in overlapping, facing relationship with the cell PC1 and is electrically connected in parallel with the panel EL3. Thus, when the panel EL3 is illuminated, the panel EL3' is also illuminated and the light therefrom projects onto the cell PC1 causing the resistance thereof to be reduced so that the panel EL1 is conditioned for illumination.

In order to cause the next preceding electroluminescent panel to be extinguished or turned off when a panel is illuminated, "extinguishing" photoconductive cells PCE1-PCE3 are provided. As may be seen, each of these photoconductive cells is electrically connected in parallel with one electroluminescent panel and is mounted in overlapping, spaced relationship with the next-succeeding electroluminescent panel so that the light emitted from the next-succeeding panel is projected thereon. For example, the cell PCE1 is electrically connected in parallel with the panel EL1 but is mounted adjacent the panel EL2. Thus, when the panel EL2 is illuminated, the resistance of the cell PCE1 is reduced to a low value which effectively short-circuits the panel EL1 causing the panel to be extinguished.

Presuming all of the electroluminescent panels are initially in the off conditions, i.e., the panels are extinguished, it will be apparent that some means must be provided for initially illuminating the first panel EL1. For this purpose, a resistor R1 is connected in parallel with the photoconductive cell PC1 through a start switch SS1. When the switch SS1 is momentarily closed, the cell PC1 is shunted by the resistor R1 causing a lesser amount of voltage to be applied across the cell PC1 and a greater amount of voltage to be applied across the panel EL1. In response to the increased voltage applied thereacross, the panel EL1 is partially illuminated causing light to be emitted thereby which is projected onto the panel PC1. The light projected on the panel PC1 causes the resistance thereof to be reduced so that a still greater voltage is applied across the panel EL1 causing more

light to be emitted therefrom which in turn causes the resistance of the cell PC1 to be further reduced. Thus, a regenerative action takes place whereby the panel EL1 becomes fully illuminated.

A brief description of the overall operation for the shift register illustrated in exemplary form in FIG. 1 may be helpful in providing a better understanding of the present invention. Let it be assumed that initially all of the electroluminescent panels are extinguished so that the cells are all in high resistive states. Under such conditions, the voltage provided across the panels by the power oscillator 12 is insufficient to cause the panels to be illuminated. When the start switch SS1 is momentarily closed, the panel EL1 becomes partially illuminated and, due to the above-described regenerative action, the panel becomes fully illuminated. Light from the panel EL1 is projected on a portion of the cell PC2 causing the resistance thereof to be reduced so that a greater voltage is provided across the panel EL2 by the oscillator 12. However, the voltage is still insufficient to cause the panel EL2 to become illuminated and the panel is merely conditioned for illumination.

In response to the application of a pulse to the input terminal 11, the "one-shot" multivibrator FF1 is rendered operative to provide an output pulse which opens the gate AND1 for a predetermined period of time so that the output of the power oscillator 12 is permitted to pass therethrough to the primary of the "step-up" transformer T1. As a result, a "trigger" signal is induced in the secondary of the transformer T1 which is of such phase and magnitude that, when added to the signal directly applied to the panel EL2 by the power oscillator 12 through the cell PC2, it causes the panel EL2 to become partially illuminated.

The panel EL2 becomes fully illuminated due to the above-described regenerative action of the network. When the panel EL2 becomes fully illuminated, the light emitted thereby projects onto the extinguishing photoconductive cell PCE1 causing the resistance thereof to be reduced to a low value which effectively shorts-out the panel EL1 causing the EL1 panel to be extinguished. The extinguishment of the panel EL1 is enhanced by the reverse regenerative action of the series combination of the cell PC1 and the panel EL1. The light from the panel EL2 is also projected onto the cell PC3 causing the resistance thereof to be reduced so that the panel EL3 is conditioned for illumination in response to the next "trigger" signal. In like manner, when the panel EL3 becomes fully illuminated, it causes the panel EL2 to be extinguished and causes the panel EL1 to be conditioned for illumination.

In view of the foregoing, it will be apparent that the magnitude of the "trigger" signal applied to the panels from the secondary of the transformer T1 must be such that, unless the resistance of the associated series connected "conditioning" cell has been reduced in response to illumination of the next preceding panel, a given electroluminescent panel will not be illuminated. Additionally, it will be apparent that the time period of the output produced by the "one-shot" multivibrator must be no longer than the time required to turn on a single electroluminescent element; otherwise, the ring will continually step at a rate determined by the time constants of the photoconductive cells and electroluminescent panels.

Though the shift register has been disclosed with three electroluminescent panels representing stages thereof, it will be apparent that the shift register may be expanded to include an indefinitely large number of electroluminescent panel stages connected in like manner.

In accordance with another feature of the present invention, a solid state clock may be formed utilizing the principles of the above-described shift register. More specifically, the electroluminescent panels of at least two shift registers are positioned in arrays corresponding to the positions of the clock hands and pulses are applied

to the respective shift registers at prescribed times so that selected electroluminescent panels are controllably illuminated, indicating the positions of the clock hands, and a running visual indication of the time is provided.

Referring to FIG. 2, a fragmentary view of the face of a clock is illustrated wherein electroluminescent panels or rods are positioned at selected intervals on the clock-face. A conventional, circular clockface is shown for purposes of illustration though it will be apparent the clock may take any unconventional, noncircular form such as a linear clockface arrangement. From the exemplary arrangement it will be apparent that sixty electroluminescent panels ELM0-ELM59 are arranged radially in a circular array at positions corresponding to the sixty-minute positions for the minute hand. Additionally, forty-eight electroluminescent panels ELH0-ELH47 are arranged radially in a circular array, within the circular minute-hand array, at positions corresponding to forty-eight positions for the hour hand.

A block diagram of an exemplary form of the solid state clock is shown in FIG. 3. The exemplary clock includes a "minute-hand" shift register MHRSR and an "hour-hand" shift register HHRSR, both being constructed in accordance with the teachings of the above-described shift register illustrated in FIG. 1. As may be seen, the panels ELM0-ELM59 form a part of the shift register MHRSR, and the panels ELH0-ELH47 form a part of the shift register HHRSR. For causing selected ones of the electroluminescent panels in the shift registers MHRSR and HHRSR to be illuminated, input pulses ("trigger" pulses) must be applied to input terminals 20 and 21 of the shift registers at prescribed times so that the panels in the respective shift registers are successively illuminated.

In keeping with this feature of the present invention, circuitry is provided for applying input pulses to the terminals 20 and 21 of the respective shift registers MHRSR and HHRSR so that the electroluminescent panels therein are selectively illuminated in accordance with the desired positions of the clock hands. As may be seen, the circuitry includes means for applying "minute" input pulses ("trigger" pulses) to the input terminal 20 of the minute-hand shift register MHRSR so that the panels ELM0-ELM59 are selectively illuminated to indicate the succeeding positions of the minute hand. Likewise, the circuitry includes means for applying "hour" input pulses ("trigger" pulses) to the input terminal 21 of the hour-hand shift register HHRSR so that the panels ELH0-ELH47 are selectively illuminated to indicate the succeeding positions of the hour hand.

The circuitry for applying "minute" input pulses or trigger pulses to the input terminal 20 of the minute hand shift register MHRSR includes an oscillator 25 which corresponds to the oscillator 12 in FIG. 1. The oscillator 25 is connected to the input terminal 20 through a gate ANDM and a "step-up" transformer TM, the gate ANDM being controlled by a monostable flip-flop or "one-shot" multivibrator FFM.

In response to the application of a pulse to the input of flip-flop FFM, the gate ANDM is opened for a time period which is long enough to permit a "minute" pulse to be applied to the input terminal 20, the "minute" pulse causing the next-succeeding electroluminescent panel to be illuminated. Since a "minute" pulse must be applied to the input terminal 20 at the end of each one-minute time period, it will be apparent that the flip-flop FFM must be triggered once every minute.

For the purpose of triggering the flip-flop FFM at one-minute intervals, a "minute" counter-storage unit CSM is provided which has its output connected to the input of the flip-flop FFM through a gate ORM. As may be seen, the storage unit CSM has its input connected to a sixty cycle per second (c.p.s.) source 26. Additionally, the storage unit CSM includes a pulse former PF1 for pro-

viding an output pulse having a constant volt-second content in response to each cycle of the sixty c.p.s. source and includes a pair of counters K1 and K2 which, for the desired operation, are respectively filled in response to every sixty input pulses applied thereto, the counters being designed to provide an output pulse when filled. The counters K1 and K2 are suitably of the type described in copending application Serial No. 267,273, entitled "Magnetic Counter and Pulse Forming Circuit," filed March 22, 1963, assigned to the assignee of the present invention. Thus, an output pulse is provided by the storage unit CSM in response to the production of thirty-six hundred pulses by the pulse former PF1 which corresponds to the production of thirty-six hundred cycles of the sixty c.p.s. source. Since a sixty c.p.s. source operates at a rate of thirty-six hundred cycles per minute, output pulses will be produced by the storage unit CSM and applied to the flip-flop FFM at a rate of one pulse per minute.

The circuitry for applying "hour" input or triggering pulses to the input terminal 21 of the hour-hand shift register HHRSR also includes the oscillator 25. As may be seen, the output of the oscillator 25 is connected to the input terminal 21 through a gate ANDH and a "step-up" transformer TH, the gate ANDH also being controlled by a monostable flip-flop or "one-shot" multivibrator FFH. In response to the application of a pulse to the input of the flip-flop FFH, the gate ANDH is opened for a time period which is long enough to permit an "hour" pulse to be applied to the input terminal 21, the "hour" pulse causing the next-succeeding electro-luminescent panel to be illuminated. Since the shift register HHRSR includes forty-eight electroluminescent panels, it will be apparent that an "hour" pulse must be applied to the input terminal 21 every fifteen minutes for the desired operation of the clock. Accordingly, means must be provided for applying a pulse to the input of the flip-flop FFH every fifteen minutes.

For this latter purpose, "actuating" photoconductive cells PCMA0, PCMA15, PCMA30 and PCMA45 are respectively mounted in overlapping spaced relationship with the electroluminescent panels ELM0, ELM15, ELM30 and ELM45 which represent the four quarter-hour or fifteen-minute positions of the minute hand. As may be seen, the input terminal 20 of the minute hand shift register MHRSR is connected to the flip-flop FFH through the "actuating" photoconductive cells and associated diodes D0, D15, D30 and D45. When a "minute" input pulse is applied to the input terminal 20 of the shift register MHRSR and one of the selected electroluminescent panels is illuminated, the light from the panel projects onto the associated one of the "actuating" photoconductive cells causing the resistance thereof to be reduced so that, in essence, the cell appears as a short-circuit. As a result, the "minute" pulse is transmitted through the cell and the associated diode to the flip-flop FFH. The flip-flop FFH is rendered operative in response to the "minute" pulse causing the gate ANDH to be opened for a prescribed time period so that an "hour" input pulse is applied to the input terminal 21 of the hour-hand shift register HHRSR. Since an "hour" input pulse is applied to the input terminal 21 only at times when the electroluminescent panels ELM0, ELM15, ELM30 and ELM45 are illuminated, it follows that "hour" input pulses are applied thereto every fifteen minutes.

In view of the fact that one pulse is applied to the flip-flop FFH in response to the application of fifteen input pulses to the shift register MHRSR, it follows that the exemplary minute hand shift register MHRSR functions as a frequency divider for the purpose of controlling the operation of the hour-hand shift register HHRSR. Though a 15:1 division ratio is provided in the exemplary arrangement, it will be apparent that a similar shift register may be provided having any desired division ratio.

In order to allow for the setting of the solid state clock, a set switch 30 is provided for controlling the application of pulses to the flip-flop FFM from either the pulse former PF1 or the counter K1. When the switch 30 is in its lower position, the output of the pulse former PF1 will be connected through the gate ORM to the flip-flop FFM so that pulses will be applied thereto at a rate of thirty-six hundred pulses per minute. It follows that the electroluminescent panels in the shift register MHSR will be successively illuminated at a stepping rate of thirty-six hundred steps per minute, whereas the electroluminescent panels in the shift register HHRS will be successively illuminated at a stepping rate of two hundred and forty steps per minute. Thus, the clock may be rapidly set. If the switch 30 is in its upper position, the output of the counter K1 will be connected to the input of the flip-flop FFM through the gate ORM so that pulses are applied thereto at a rate of sixty pulses per minute. Under such conditions the electroluminescent panels in the shift register MHSR will be successively illuminated at a stepping rate of sixty steps per minute, whereas the electroluminescent panels in the shift register HHRS will be successively illuminated at a stepping rate of four steps per minute. Thus, the clock may be set at a slower rate when the switch is in this position.

The details of operation of the shift registers MHSR and HHRS will not be set forth but rather reference may be made to the above description of the shift register in FIG. 1. However, a brief description of the overall operation of the clock illustrated in FIG. 3 may be helpful in providing a better understanding of the present invention. For this purpose, let it be assumed that initially the electroluminescent panels ELM0 and ELH0 in the respective shift registers MHSR and HHRS are illuminated so that the clock indicates the time to be 12:00. Under such conditions, light from the panel ELM0 projects onto the photocell PCM1 causing the resistance thereof to be reduced so that the panel ELM1 is conditioned for illumination. Likewise, light from the panel ELH0 projects onto the cell PCH1 causing the resistance thereof to likewise be reduced so that the panel ELH1 is conditioned for illumination.

When a one-minute time period has passed, an output pulse will be provided by the storage unit CSM which is transmitted to the flip-flop FFM through the gate ORM. The flip-flop FFM in turn provides an output which opens the gate ANDM for a prescribed time period so that the output of the oscillator 25 is transmitted through the gate to the step-up transformer TM, causing a "minute" input pulse to be applied to the panels ELM0-ELM59 of shift register MHSR through the input terminal 20. In response to the application of the "minute" input pulse thereto, the panel ELM1 is partially illuminated, causing light therefrom to be projected onto the cell PCM1 so that the resistance thereof is further reduced. Due to the regenerative action described hereinabove with respect to FIG. 1, panel ELM1 becomes fully illuminated. The light from the panel ELM1 also projects onto the "extinguishing" photoconductive cell PCME0 causing the resistance thereof to be greatly reduced so that, in essence, the panel ELM0 is short-circuited by the cell PCME0 and the panel ELM0 is extinguished. At this time, the clock indicates the time to be 12:01.

In response to the production of subsequent output pulses by the storage unit CSM, the panels in the shift register MHSR are successively illuminated indicating the movement of the minute hand of the clock. When the panel ELM15 is illuminated indicating the time to be 12:15, the light therefrom projects onto the "actuating" photoconductive cell PCMA15 causing the resistance thereof to be greatly reduced so that the cell appears, in essence, as a short-circuit. The "minute" input pulse which triggered the panel ELM15 to illumination is then transmitted through the cell PCMA15 and the associated

diode D15 to the flip-flop FFH, causing the flip-flop to be rendered operative. The flip-flop FFH provides an output which causes the gate ANDH to be opened for a prescribed time period so that the output of the oscillator 25 is transmitted through the gate ANDH to the step-up transformer TH causing an "hour" input pulse to be applied to the panels ELM0-ELH47 of the hour-hand shift register HHRS through input terminal 21. In response to the "hour" pulse, the panel ELH1 is partially illuminated. The light emitted by the panel ELH1 projects onto the photoconductive cell PCH1 causing the resistance thereof to be further reduced and, due to the above-described regenerative action, the panel ELH1 becomes fully illuminated. The light emitting from the panel ELH1 also is projected onto the "extinguishing" photoconductive cell PCHE0 causing the resistance thereof to be greatly reduced so that, in essence, the cell PCHE0 appears as a short-circuit across the panel ELH0 and the panel ELH0 is extinguished. At this time, the clock will indicate a time of 12:15. As will be apparent, the remaining electroluminescent panels in the shift register HHRS will be successively illuminated in response to the triggering of flip-flop FFH, each succeeding panel being illuminated at the end of the next succeeding fifteen-minute time period.

In view of the foregoing, it will be apparent that a solid state clock has been provided which employs shift registers utilizing electroluminescent panels as the successive stages thereof.

Referring to FIG. 4, a pulse former 40 is illustrated which may be utilized in the above-described solid state clock. However, the invention is not intended to be limited to the use of such a pulse former, but rather is intended to cover the use of any desired pulse former. Reference may be made to the U.S. Patent 2,897,380, issued July 28, 1959, to C. Neitzert for the details of construction and operation for the pulse former. Briefly stated, the pulse former has an input terminal 41 and an output terminal 42. Power is supplied to the pulse former by a power supply designated as V1. The heart of the pulse former is a saturable reactor 45 having an input winding 46, a triggering winding 47, a reset winding 48 and an output winding 49, all wound on a core 50 constructed of material having a substantially rectangular hysteresis loop. A transistor 51 has its input circuit connected across the triggering winding 47 and has its output circuit connected in series with the reset winding 48.

In response to each input pulse, the saturation of the core is exceeded and, when the saturating input pulse is abruptly terminated, a voltage is induced in the triggering winding 47 due to the sudden collapse of excess flux which triggers the transistor 51 so that current flows through the reset winding 48. The resulting flow of current in the reset winding 48 not only drives the core 50 toward its opposite condition of saturation, but also induces a voltage in the triggering winding 47 which causes still further current to flow through the transistor output circuit to a point where a condition of negative saturation is achieved in the core of the reactor. This restores the pulse former to its initial state in readiness to receive a subsequent input signal and induces an output pulse at the output terminal 42 having a predetermined constant volt-second content. A damping resistor 52 is connected in parallel with the reset winding 48, base current for the transistor 51 is limited by a series resistor 53, and current in the transistor output circuit is limited by a series resistor 54. Additionally, a resistor 55 is connected in series with the input winding 46 to limit the current flow therethrough.

Since, in the exemplary embodiment, the input signal for the pulse former is supplied by the sixty c.p.s. A-C source, the pulse former shown in FIG. 4 includes an amplifier-limiter stage interposed between the input terminal 41 and the input winding 46. The amplifier-limiter has been provided for the purpose of transforming the sine wave output of the sixty c.p.s. source into a square wave signal so that the operation of the pulse

former shown in FIG. 4 is enhanced thereby. Additionally, a gating transistor 56 is interposed between the amplifier-limiter and the input winding 46 for controlling the flow of current through the input winding in response to the square wave output of the amplifier-limiter.

The amplifier-limiter includes a transistor 60 having (1) its collector connected to the positive terminal of the voltage source V1 through a resistor 61 and connected to ground through a resistor 62, the base terminal of transistor 56 and a resistor 63 (the resistors 61-63 functioning as a voltage-dividing network), (2) its emitter connected to ground through a resistor 64, and (3) its base connected to the input terminal 41 through a resistor 65 and connected to ground through a diode 66. When a positive potential is provided at the input terminal 41, it is applied to the base of the transistor through resistor 65. Diode 66 is connected so as to be non-conductive for positive input potentials. The transistor 60 is rendered conductive by the positive input potential since it is of the NPN type so that current flows therethrough. Current flowing through the resistor 60 causes the potential at the collector thereof to drop which in turn alters the voltage-dividing effect of resistors 61-63 so that the potential at the base of transistor 56 drops proportionately. In response to the dropping potential at the base thereof, transistor 56 is rendered nonconductive so that the flow of current through the input winding 46 is rapidly terminated. Conversely, when a negative potential is provided at the input terminal 41, the diode 66 clamps the base of transistor 60 to ground since current flows therethrough and through the resistor 65 so that transistor 60 is rendered nonconductive and the potential at the collector thereof rises toward the potential of the source V1. In response to the rising collector voltage, the potential at the base of transistor 56 rises proportionately so that transistor 56 is rendered conductive causing current to flow through the input winding 46. Thus, a square wave signal is applied to the base of transistor 56 by the amplifier-limiter in response to the application of a sine wave input signal to the input terminal 41, the square wave signal being the inverse of the sine wave signal since the output is negative going when the input is positive going and vice versa.

It will be apparent that the amplifier-limiter may be omitted if the pulse former is designed to respond to a sine wave input. Additionally, the amplifier-limiter may be omitted if a clean square wave input signal is applied to the input terminal 41 of the pulse former, i.e., a square wave source is provided rather than a sixty c.p.s. A.-C. source.

Referring to FIG. 5, a counter 70 is illustrated which may be utilized in the above-described solid state clock and which is also constructed in accordance with the teachings of the above-mentioned Neitzert patent. In like manner, the invention is not intended to be limited to the use of such a counter, but rather is intended to cover the use of any desired counter. Briefly stated, the counter has an input terminal 71 and an output terminal 72. Power is supplied to the counter by a power supply designated as V2. The heart of the counter is a saturable reactor 75 having an input winding 76, a triggering winding 77, a reset winding 78 and an output winding 79, wound on a core 80 constructed of material having a substantially rectangular hysteresis loop. A transistor 81 has its input circuit connected across the triggering winding 77 and has its output circuit connected in series with the reset winding 78. The material of the core is so chosen and the counter is so constructed that, when an input pulse is applied to the winding, the magnetization of the core is advanced one step from negative saturation toward the condition of positive saturation.

The number of pulses required for positive saturation to be attained depends upon the cumulative energy content of the input pulses. When a prescribed number of input pulses cause the saturation of the core to be exceeded and the saturating input pulse is abruptly termi-

nated, a voltage is induced in the triggering winding 77 due to the sudden collapse of excess flux which triggers the transistor 81 so that current flows through the reset winding 78. The resulting flow of current in the reset winding not only drives the core toward the opposite condition of saturation, but also induces a voltage in the triggering winding 77 which causes still further current to flow through the transistor output circuit to the point where a condition of negative saturation is achieved in the core of the reactor. This restores the device to its initial state in readiness to receive a new series of input pulses and induces an output pulse in the output winding 79 which appears at the output terminal 72.

To prevent operation of the transistor 81 in response to small changes in flux which occur during each step of advancement toward saturation, a damping resistor 82 is placed in parallel with the reset winding 78. Moreover, to limit the base current of the transistor in the face of a large voltage induced in the triggering winding, a series resistor 83 is used. Finally, there is provided in series with the collector of transistor 81 a low value resistor 84 for the purpose of limiting the reset current which not only tends to protect the transistor, but which also limits the load which is placed upon the power supply V2.

In the exemplary arrangement, two counters K1 and K2 have been utilized in the storage unit CSM. However, it will be apparent that any desired number of counters may be cascaded or connected in tandem so long as pulses are produced by the storage unit CSM at a rate of one pulse per minute.

Referring to FIG. 6, a schematic diagram of a typical oscillator which may be utilized in the above-described solid state clock is illustrated. The exemplary oscillator is a magnetic oscillator including a saturable transformer 90 having a pair of main windings 91 and 92 and an output winding 93 all wound about a core 94. The core is formed of a readily saturable magnetic material having a generally rectangular hysteresis loop. For driving the core into its opposite conditions of saturation, which may for convenience be termed positive and negative saturation, the windings 91 and 92 are energized by transistors 95 and 96 having base or control circuits which are alternately energized by feedback or "cross" connections including resistors 97 and 98. To improve the output wave form of the oscillator, a resistor 99 and a capacitor 100 are connected in series across the windings 91 and 92. Since the transistors 95 and 96 are of the NPN type, the positive terminal of a power supply 101 is connected to the center terminal 102 of the transformer main windings 91 and 92 for feeding the collectors of the transistors, whereas the emitters of the transistors are connected to the negative terminal of the source.

In operation of the oscillator, application of the supply voltage causes both of the transistors 95 and 96 to tend to conduct, but because of a slight inherent unbalance in the circuit, one transistor will normally tend to conduct more heavily than the other. Conduction in the predominating transistor induces a voltage in the associated transformer winding which is in such a direction as to forward bias the transistor so that the predominating transistor tends to conduct more heavily. In response to conduction of the predominating transistor, the potential at the collector thereof drops and, since the base of the other transistor is connected thereto through the "cross" connection, the other transistor is rendered nonconductive. When saturation of the core is reached, the rate of change of flux decreases, hence, by transformer action, induced forward biasing voltage decreases and the current in the conducting transistor decreases so that the potential at the collector rises. The rising collector potential turns on the former nonconducting transistor and the conduction in this transistor induces a voltage in the associated transformer winding which is in such a direction as to forward bias this transistor so that this transistor tends to conduct more heavily. Conduction in the second transistor causes

the potential at the collector thereof to drop so that the former conducting transistor is rendered nonconductive. The current flowing in the second transistor now drives the core to the opposite condition of saturation. This cycle is repeated at a rate which is directly proportional to the applied voltage and inversely proportional to the saturation flux and the number of turns in the transformer winding. Voltage pulses are induced in the output winding 93, as the core switches from one condition of saturation to the other condition of saturation and back again and the voltage pulses constitute the output signal of the oscillator, the output signal provided by the exemplary oscillator being a square wave type output.

For greater details of the disclosed magnetic oscillator, reference may be made to the co-pending application S.N. 210,410 of Wilmer C. Anderson et al., filed July 17, 1962, which is assigned to the same assignee.

Though a magnetic oscillator has been disclosed and described, it will be apparent that any desired oscillator may be utilized in the above-described solid state clock and the invention is therefore not intended to be limited to the disclosed oscillator.

Though the above-described solid state clock has been illustrated with means being provided to regulate the illumination of electroluminescent panels in shift registers only to indicate the positions of the minute and hour hands, it will be obvious to one skilled in the art that a second hand shift register may be provided and additional means, constructed in accordance with the above teachings, may be added for regulating the illumination of the electroluminescent panels in the second hand shift register to indicate the succeeding positions of the second hand. Accordingly, the invention is intended to cover means for regulating the illumination of electroluminescent panels in shift registers to indicate the positions of the three clock hands, i.e., the second, minute and hour hands.

I claim as my invention:

1. In a solid state clock, the combination which comprises, at least two sets of electroluminescent panels, each set including a plurality of electroluminescent panels positioned on the clockface in an array at intervals corresponding to the successive positions of a clock hand represented thereby, means associated with each set of panels for causing a panel to be illuminated when effectively associated therewith, means for initially associating the illuminating means with a selected panel in each set, means including a plurality of photoconductive cells associated with each set of panels and responsive to the partial illumination of a panel in a set (1) for conditioning the next succeeding panel in that set for illumination, (2) for disassociating the illuminating means from the then illuminated panel in that set so that it is extinguished, and (3) for effectively associating the illuminating means with the partially illuminated panel so that it is fully illuminated, and means associated with each set of panels and momentarily operative according to different prescribed time functions in respect of each set for causing a conditioned panel in a set to be partially illuminated so that the panels in each set are successively illuminated to indicate the positions of the clock hands represented thereby and means including a plurality of extinguishing photoconductive cells associated with said electroluminescent panels and responsive to the illumination of each panel for causing the next preceding panel to be extinguished.

2. In a solid state clock, the combination which comprises, at least two sets of electroluminescent panels, each set including a plurality of electroluminescent panels positioned on the clockface in an array at intervals corresponding to the successive positions of a clock hand represented thereby, means associated with each set of panels for causing a panel to be illuminated when effectively associated therewith, means for initially associating the illuminating means with a selected panel in each set, means including photoconductive cells associated with

each set of panels and responsive to the partial illumination of a panel in a set (1) for conditioning the next succeeding panel in that set for illumination, (2) for disassociating the illuminating means from the then illuminated panel in that set so that it is extinguished, and (3) for effectively associating the illuminating means with the partially illuminated panel so that it is fully illuminated, and means associated with each set of panels and momentarily operative according to different prescribed time functions in respect of each set for causing a conditioned panel in a set to be partially illuminated so that the panels in each set are successively illuminated to indicate the positions of the clock hands represented thereby.

3. In a solid state clock, the combination which comprises, two sets of electroluminescent panels, one set including a plurality of panels positioned on the clockface in an array at minute intervals corresponding to succeeding positions of the minute hand, the other set including a plurality of panels positioned on the clockface in an array at intervals corresponding to succeeding positions of the hour hand, means associated with each set of panels for causing a panel to be illuminated when effectively associated therewith, means for initially associating the illuminating means with a selected panel in each set, means including a plurality of photoconductive cells associated with the minute hand panels responsive to the illumination of each minute hand panel and operative at one-minute time intervals for effectively associating the illuminating means with the next succeeding panel to the then illuminated panel and for causing the then illuminated panel to be extinguished so that the panels are successively illuminated to indicate the positions of the minute hand, and means associated with the hour hand panels responsive to the illumination of selected minute hand panels for effectively associating the illuminating means with the next succeeding panel to the then illuminated panel and for causing the then illuminated panel to be extinguished so that the panels are successively illuminated to indicate the positions of the hour hand.

4. In a solid state clock, the combination which comprises, two sets of electroluminescent panels, each including a plurality of panels, the panels in one set being positioned on the clockface in an array at minute intervals corresponding to the successive positions of the minute hand, the panels in the other set being positioned on the clockface in an array at intervals corresponding to successive positions of the hour hand, a plurality of conditioning photoconductive cells equal in number to the minute hand panels and mounted in overlapping, spaced relationship therewith, a plurality of conditioning photoconductive cells equal in number to the hour hand panels and mounted in overlapping, spaced relationship therewith, each photoconductive cell associated with a pair of adjacent electroluminescent panels so that light emitting from the associated panels when illuminated is projected thereon to reduce the resistance thereof, means for applying illuminating power to each electroluminescent panel through a photoconductive cell associated therewith and with the next preceding panel so that each panel is conditioned for illumination when the next preceding panel is illuminated, means for applying auxiliary illuminating power to the minute hand panels at the end of each one-minute time period so that a panel conditioned for illumination is illuminated, means for applying auxiliary illuminating power to the hour hand panels in response to the illumination of selected minute hand panels so that a panel conditioned for illumination is illuminated after the passage of a prescribed time period, and means including a photoconductive cell independently associated with each electroluminescent panel and responsive to the illumination of the associated panel for causing the next preceding panel to be extinguished.

5. In a solid state clock, the combination which comprises, two sets of electroluminescent panels, each includ-

ing a plurality of panels, the panels in one set being positioned on the clockface in an array at minute intervals corresponding to the successive positions of the minute hand, the panels in the other set being positioned on the clockface in an array at intervals corresponding to successive positions of the hour hand, a plurality of conditioning photoconductive cells equal in number to the minute hand panels and mounted in overlapping, spaced relationship therewith, a plurality of conditioning photoconductive cells equal in number to the hour hand panels and mounted in overlapping, spaced relationship therewith, each photoconductive cell associated with a pair of adjacent electroluminescent panels so that light emitting from the associated panels when illuminated is projected thereon to reduce the resistance thereof, means for applying illuminating power to each electroluminescent panel through a photoconductive cell associated therewith and with the next preceding panel so that each panel is conditioned for illumination when the next preceding panel is illuminated, means for applying auxiliary illuminating power to the minute hand panels for a prescribed time period at the end of each one-minute time period so that a panel conditioned for illumination is illuminated, means for applying auxiliary illuminating power to the hour hand panels in response to the illumination of selected minute hand panels so that a panel conditioned for illumination is illuminated after the passage of a prescribed time period, means including a photoconductive cell independently associated with each electroluminescent panel and responsive to the illumination of the associated panel for causing the next preceding panel to be extinguished, and means operable to cyclically apply auxiliary illuminating power to the minute hand panels at a desired rate so that the clock may be set thereby.

6. An electronic clock comprising the combination of a clock face including at least two sets of electroluminescent panels, each set including a plurality of electroluminescent panels which are positioned in an array at intervals corresponding to successive positions of a selected clock hand, a source of timed electrical pulses for controlling the time of illumination of said panels, means including a plurality of conditioning photoconductive cells associated with each set of panels and responsive to the illumination of each panel for conditioning the next succeeding panel in that set for illumination in response to the next pulse whereby the panels in each set are successively illuminated in response to said timed pulses to indicate the succeeding positions of the clock hand represented thereby, power supply means for applying illuminating power to each electroluminescent panel and operatively associated with said conditioning photoconductive cells and said source of timed electrical pulses for illuminating the conditioned panel in response to each timed pulse, and means including a plurality of extinguishing photoconductive cells associated with said electroluminescent panels and responsive to the illumination of each panel for causing the next preceding panel to be extinguished.

7. An electronic clock comprising the combination of a clock face including at least two sets of electroluminescent panels, each set including a plurality of electroluminescent panels which are positioned in an array at intervals corresponding to successive positions of a selected clock hand, a source of timed electrical pulses for controlling the time of illumination of said panels, power supply means operatively associated with said panels for supplying power to said panels to illuminate the same, and means including a plurality of conditioning photoconductive cells associated with each set of panels and responsive to the illumination of each panel for conditioning the next succeeding panel in that set for illumination in response to the next succeeding pulse so that the next succeeding pulse causes said power supply means to be operatively connected to said next succeeding panel

for illuminating the same whereby the panels in each set are successively illuminated in response to said timed pulses to indicate the succeeding positions of the clock hand represented thereby and means including a plurality of extinguishing photoconductive cells associated with said electroluminescent panels and responsive to the illumination of each panel for causing the next preceding panel to be extinguished.

8. An electronic clock comprising the combination of a clock face including at least two sets of electroluminescent panels, each set including a plurality of electroluminescent panels which are positioned in an array at intervals corresponding to successive positions of a selected clock hand, a source of timed electrical pulses for controlling the time of illumination of said panels, power supply means operatively associated with said panels for supplying power to said panels to illuminate the same, and means including a plurality of conditioning photoconductive cells associated with each set of panels and responsive to the illumination of each panel for switching said power supply means to the next succeeding panel in that set in response to the next timed pulse whereby the panels in each set are successively illuminated in response to said timed pulses to indicate the succeeding positions of the clock hand represented thereby and means including a plurality of extinguishing photoconductive cells associated with said electroluminescent panels and responsive to the illumination of each panel for causing the next preceding panel to be extinguished.

9. An electronic clock comprising the combination of a clock face including at least two sets of electroluminescent panels, each set including a plurality of electroluminescent panels which are positioned in an array at intervals corresponding to successive positions of a selected clock hand, a source of timed electrical pulses for controlling the time of illumination of said panels, power supply means operatively associated with said panels for supplying power to said panels to illuminate the same, and means including a plurality of conditioning photoconductive cells associated with each set of panels and responsive to the illumination of said panels for operatively connecting said power supply means to successive panels in response to said timed pulses whereby the panels in each set are successively illuminated in response to said timed pulses to indicate the succeeding positions of the clock hand represented thereby and means including a plurality of extinguishing photoconductive cells associated with said electroluminescent panels and responsive to the illumination of each panel for causing the next preceding panel to be extinguished.

10. In a solid state clock, the combination which comprises a plurality of electroluminescent panels positioned on the clock face in an array at intervals corresponding to successive positions of a clock hand, a plurality of conditioning photoconductive cells equal in number to the electroluminescent panels and mounted in overlapping, spaced relationship therewith, each photoconductive cell associated with a pair of adjacent electroluminescent panels so that light emitting from the associated panels when illuminated is projected thereon to reduce the resistance thereof, a power source for applying illuminating power to each electroluminescent panel through a first photoconductive cell associated therewith and with the next preceding panel so that each panel is conditioned for illumination in response to illumination of the next preceding panel, means for applying auxiliary illuminating power to said panels at the end of selected time periods so that a panel conditioned for illumination is illuminated after the passage of a prescribed time period, said first photoconductive cell associated with the illuminated panel responding to the illumination thereof to lock the illuminated panel to the source of illuminating power, and means including a second photoconductive cell independently associated with each electroluminescent panel and

responsive to the illumination of the associated panel for causing the next preceding panel to be extinguished.

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LOUIS J. CAPOZI, *Primary Examiner.*

LEO SMILOW, *Examiner.*

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