US 20160225808A1

(19) **United States**
(12) **Patent Application Publication**
KUROKAWA
(10) **Pub. No.: US 2016/0225808 A1**
(43) **Pub. Date: Aug. 4, 2016**

(54) **IMAGING DEVICE AND ELECTRONIC DEVICE**

(71) Applicant: **Semiconductor Energy Laboratory Co., Ltd.**, Atsugi-shi (JP)

(72) Inventor: **Yoshiyuki KUROKAWA**, Sagamihara (JP)

(21) Appl. No.: **15/007,308**

(22) Filed: **Jan. 27, 2016**

(30) **Foreign Application Priority Data**

Jan. 30, 2015 (JP) 2015-016743

Publication Classification

(51) **Int. Cl.**
H01L 27/146 (2006.01)
H01L 29/786 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 27/14616*** (2013.01); ***H01L 29/7869*** (2013.01)

(57) **ABSTRACT**

A highly sensitive imaging device that can perform imaging even under a low illuminance condition is provided. One electrode of a photoelectric conversion element is electrically connected to one of a source electrode and a drain electrode of a first transistor and one of a source electrode and a drain electrode of a third transistor. The other of the source electrode and the drain electrode of the first transistor is electrically connected to a gate electrode of the second transistor. The other electrode of the photoelectric conversion element is electrically connected to a first wiring. A gate electrode of the first transistor is electrically connected to a second wiring. When a potential supplied to the first wiring is HVDD, the highest value of a potential supplied to the second wiring is lower than HVDD.

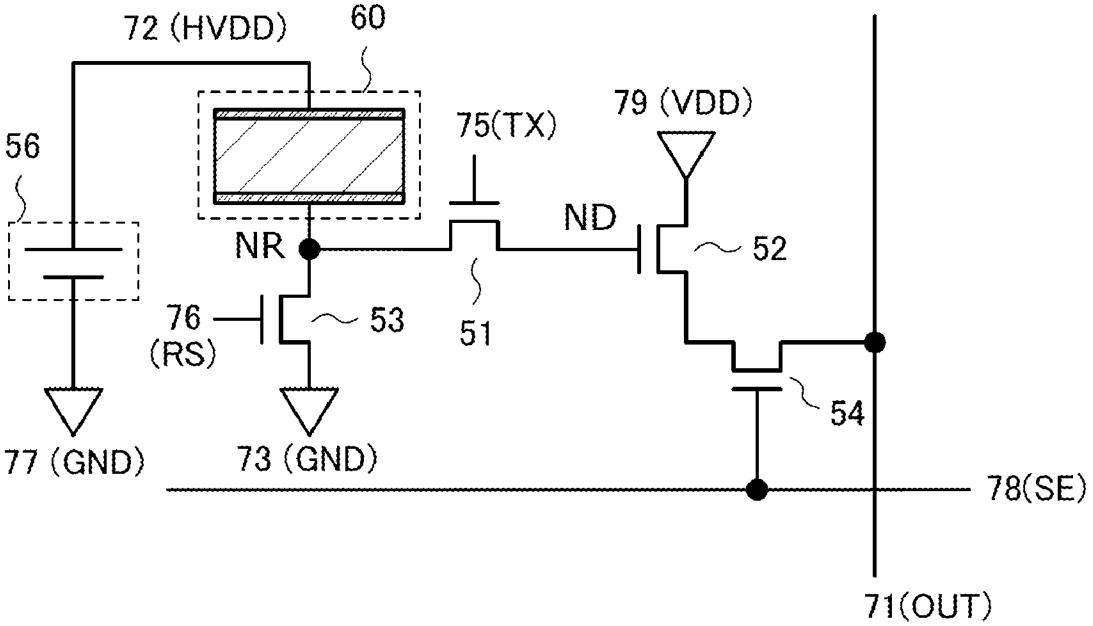


FIG. 1

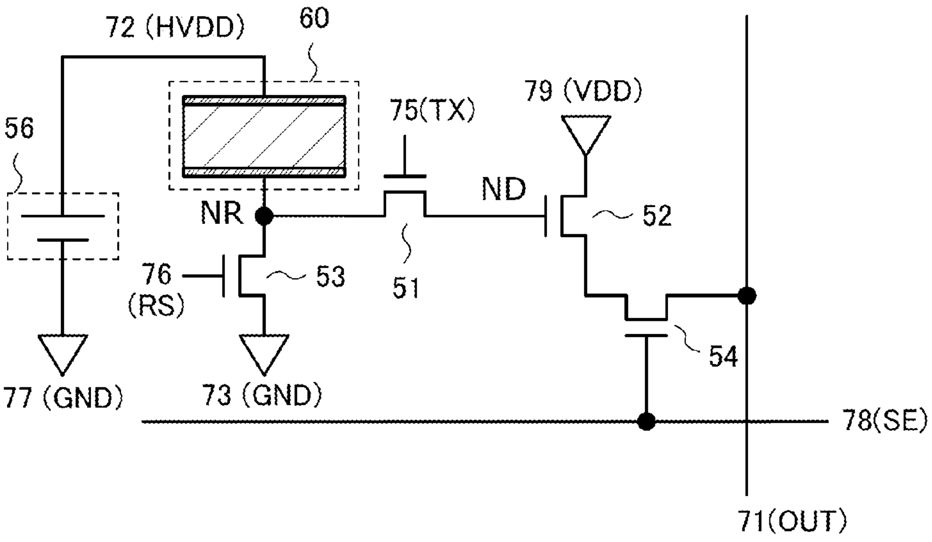
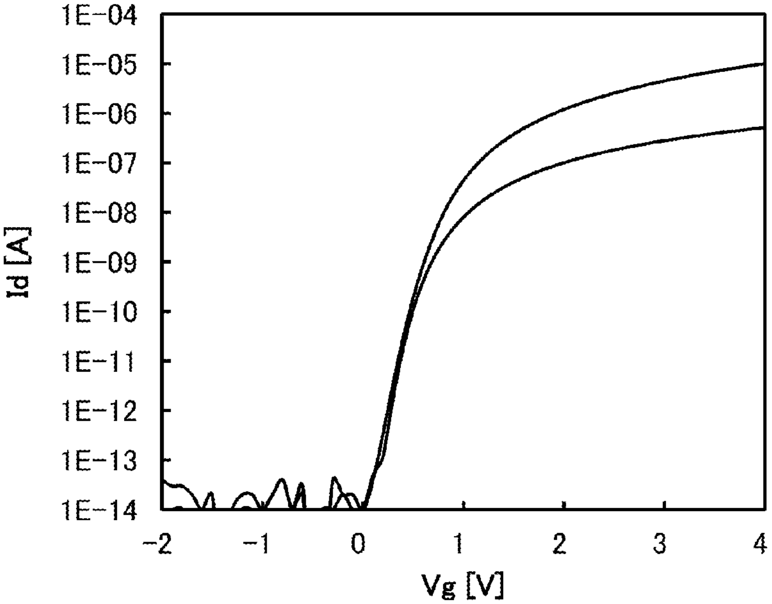

72 (HVDD)
60
56
75(TX)
79 (VDD)
NR
ND
52
76
(RS)
53
51
54
77 (GND)
73 (GND)
78(SE)
71(OUT)

FIG. 2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1E-05
1E-06
1E-07
1E-08
1E-09
1E-10
1E-11
1E-12
1E-13
1E-14
Id [A]
-2
-1
0
1
2
3
4
Vg [V]

FIG. 3

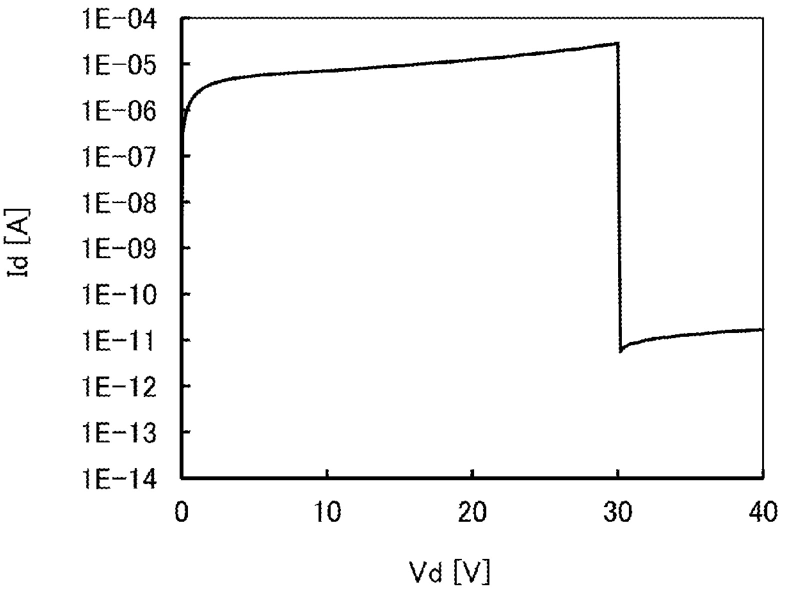

1E-04
1E-05
1E-06
1E-07
1E-08
1E-09
1E-10
1E-11
1E-12
1E-13
1E-14
Id [A]
0
10
20
30
40
Vd [V]

FIG. 4

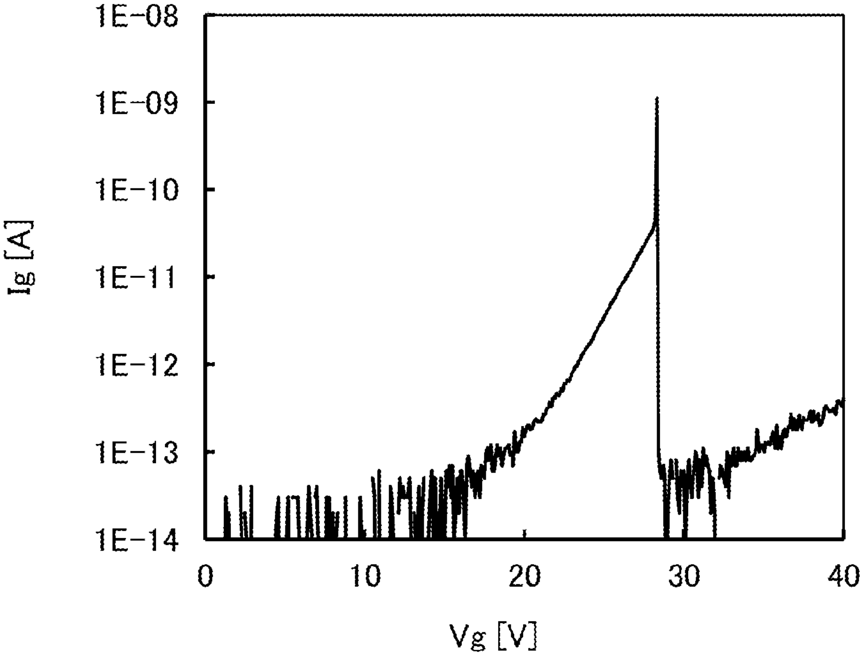


FIG. 5

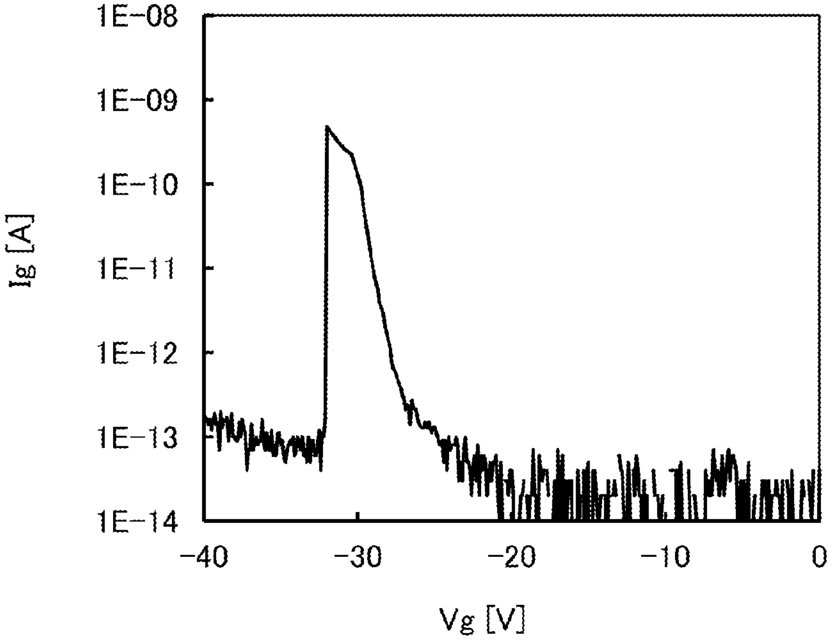


FIG. 6

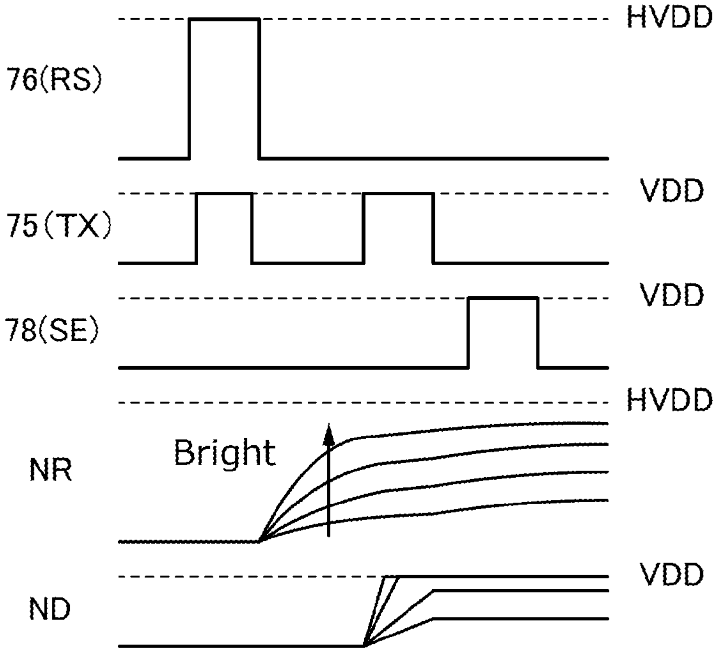


FIG. 7A

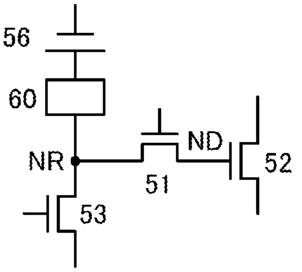


FIG. 7B

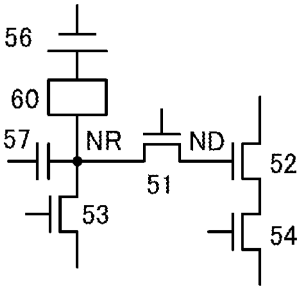


FIG. 7C

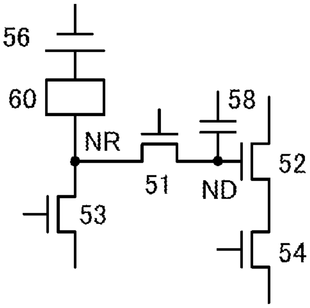


FIG. 7D

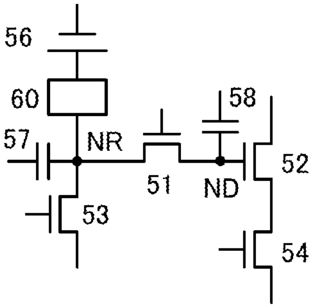


FIG. 7E

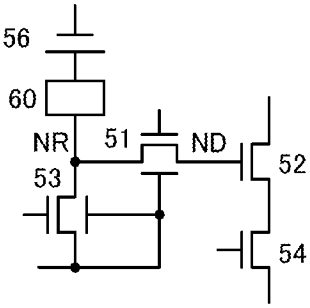


FIG. 7F

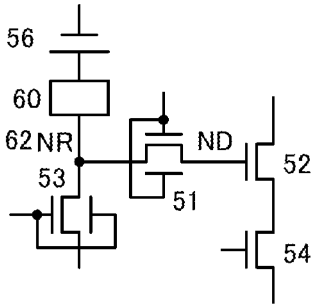


FIG. 7G

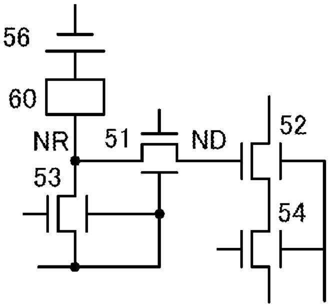


FIG. 7H

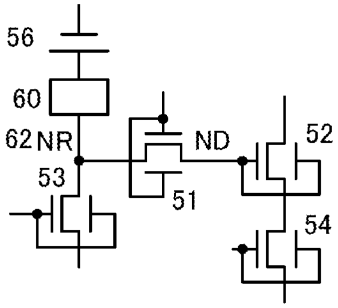


FIG. 8

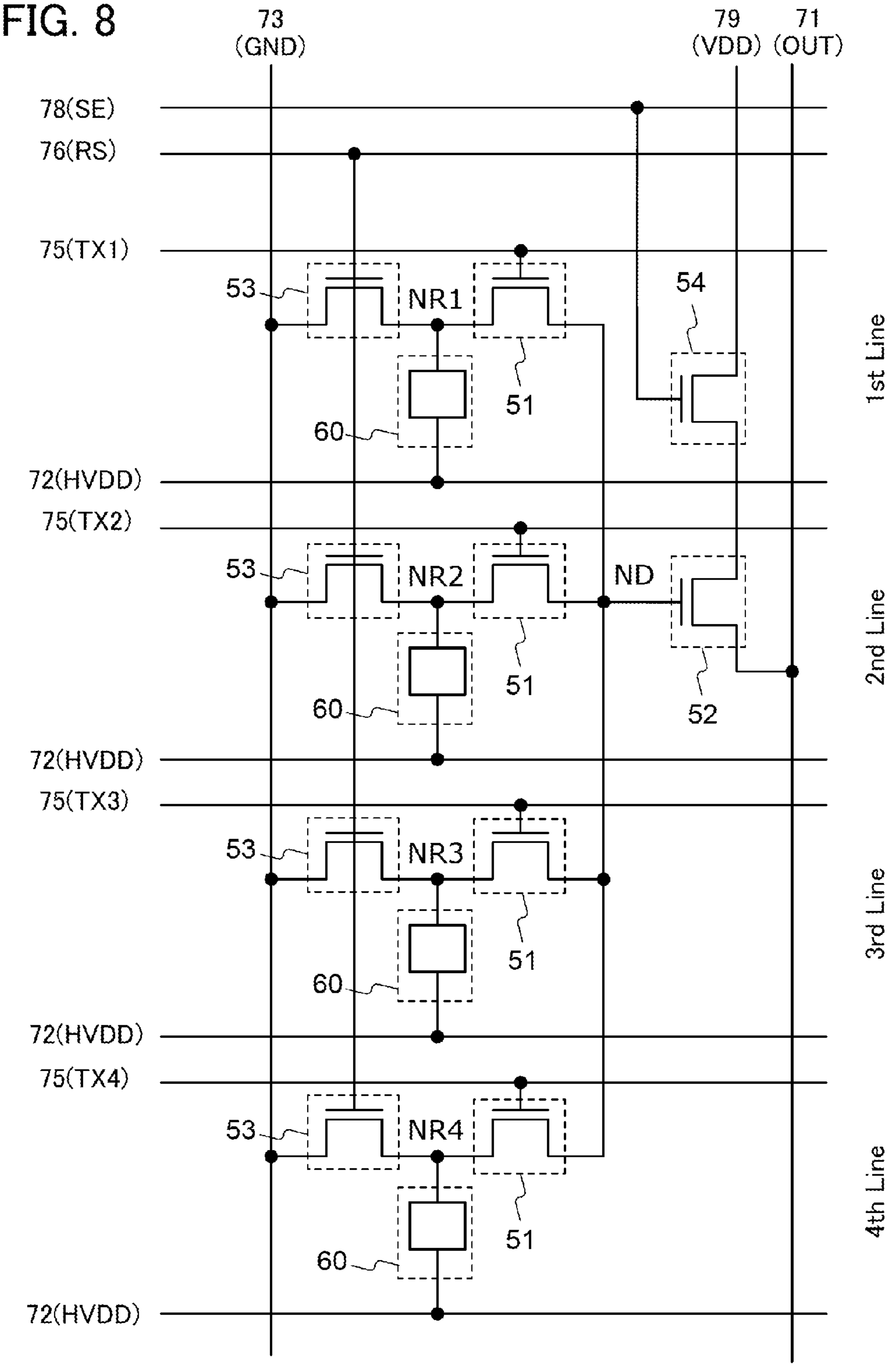

73 (GND)
79 (VDD)
71 (OUT)
78(SE)
76(RS)
75(TX1)
53
NR1
54
51
60
72(HVDD)
75(TX2)
53
NR2
ND
51
60
52
72(HVDD)
75(TX3)
53
NR3
51
60
72(HVDD)
75(TX4)
53
NR4
51
60
72(HVDD)
1st Line
2nd Line
3rd Line
4th Line

FIG. 9A

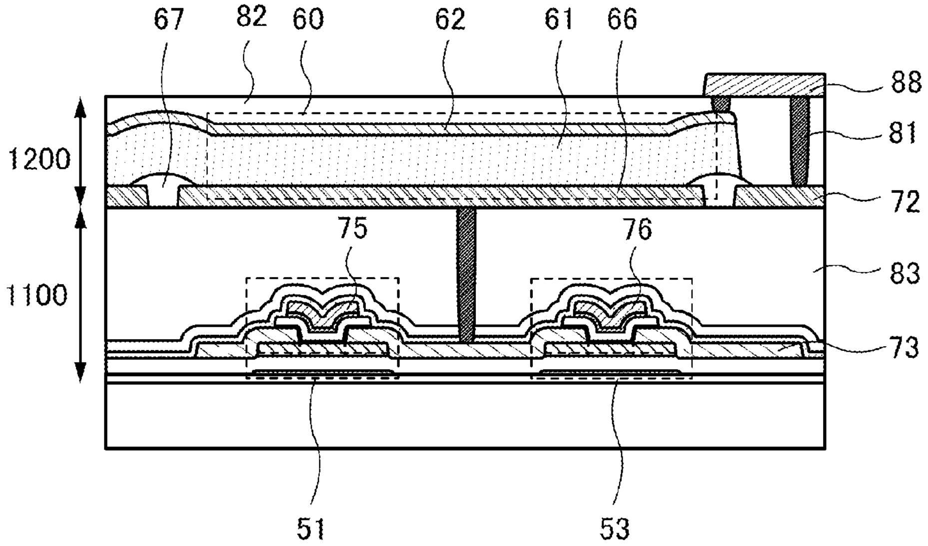


FIG. 9B

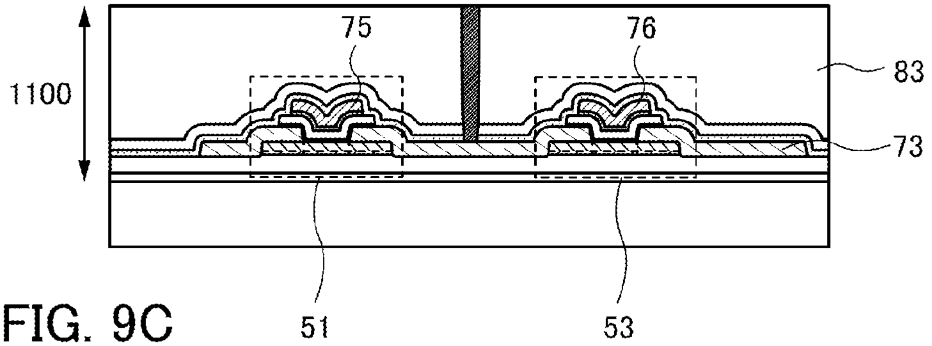


FIG. 9C

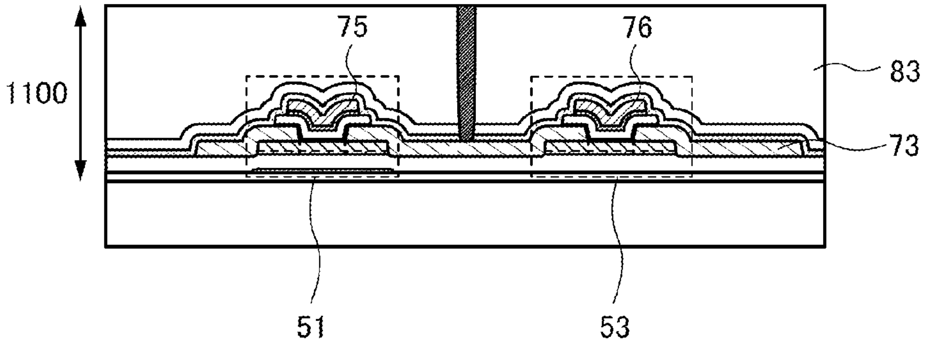


FIG. 10A

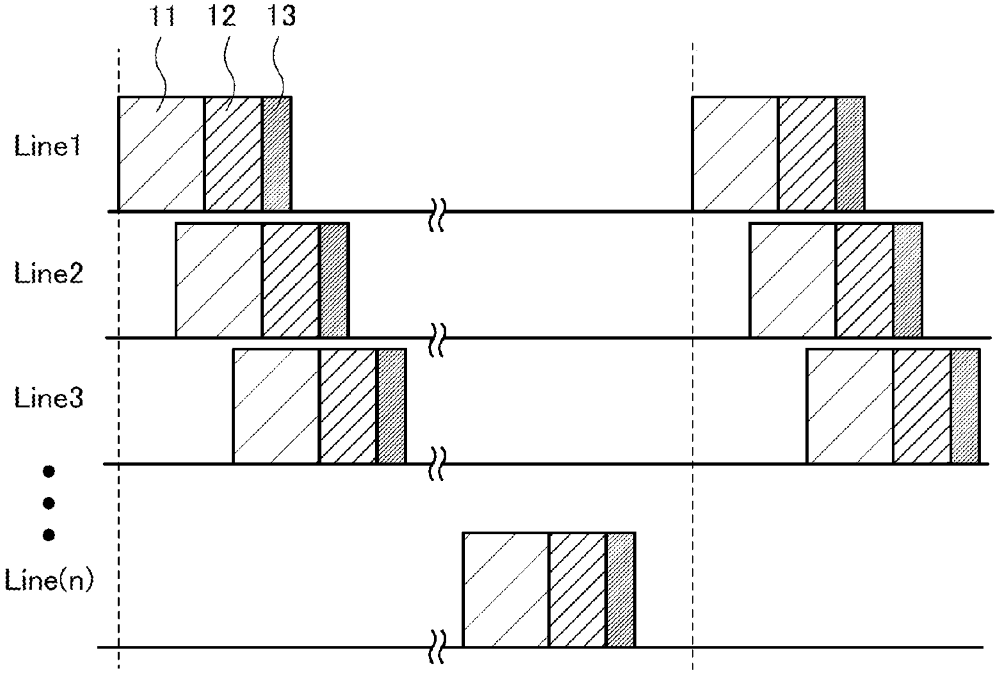


FIG. 10B

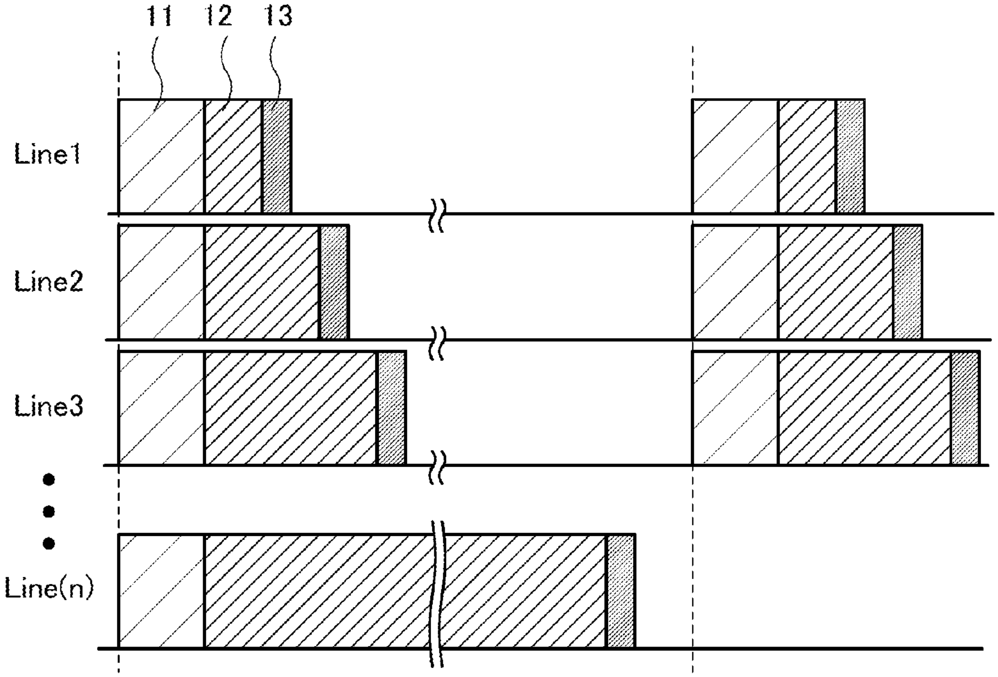


FIG. 11A

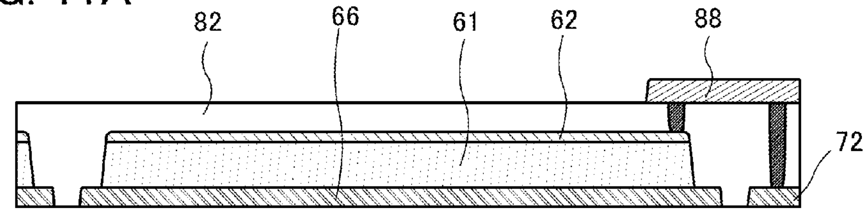


FIG. 11B

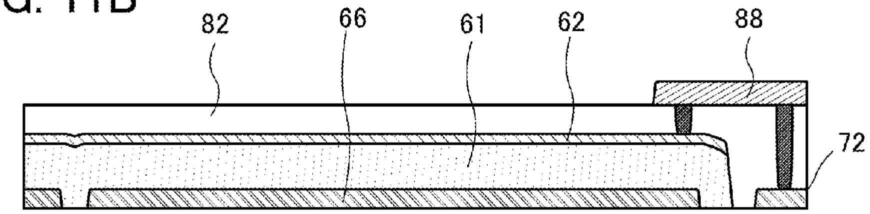


FIG. 11C

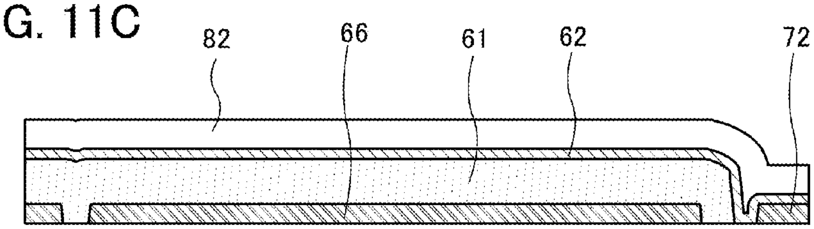


FIG. 11D

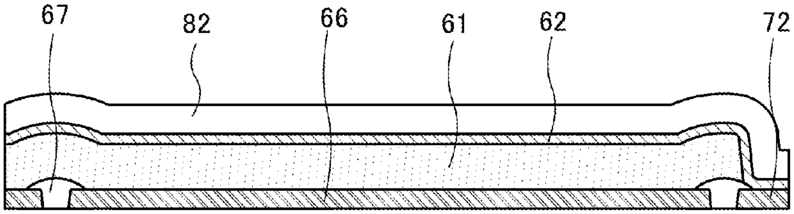


FIG. 12A

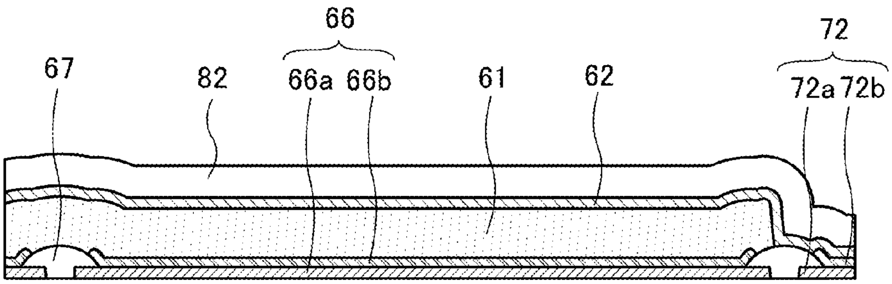


FIG. 12B

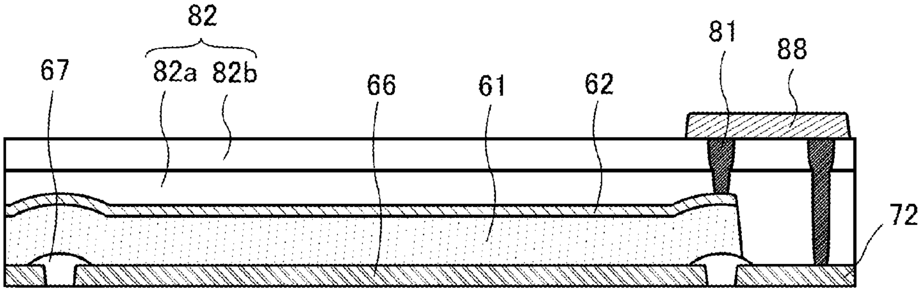


FIG. 13

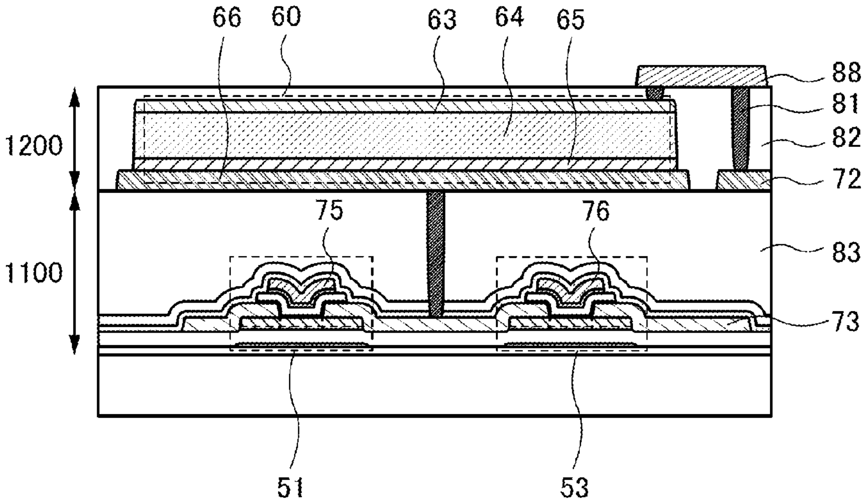


FIG. 14A

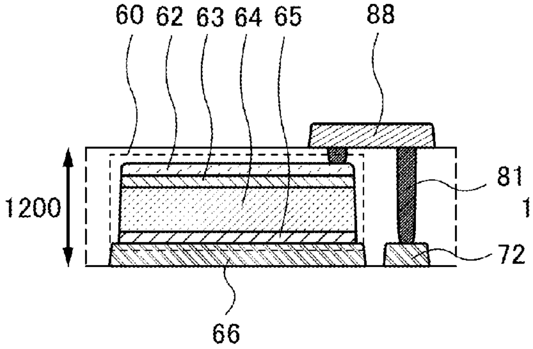


FIG. 14B

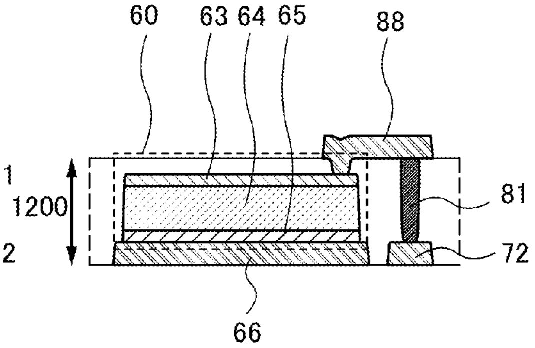


FIG. 14C

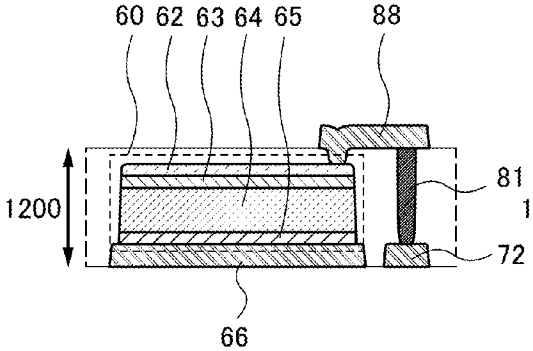


FIG. 14D

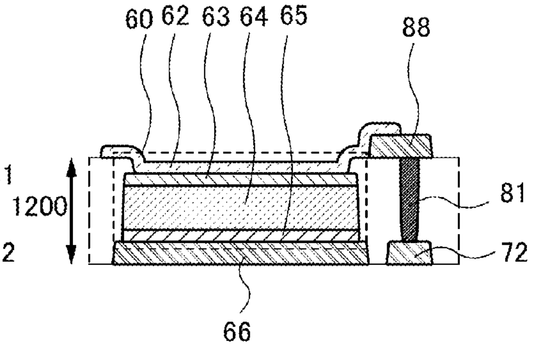


FIG. 14E

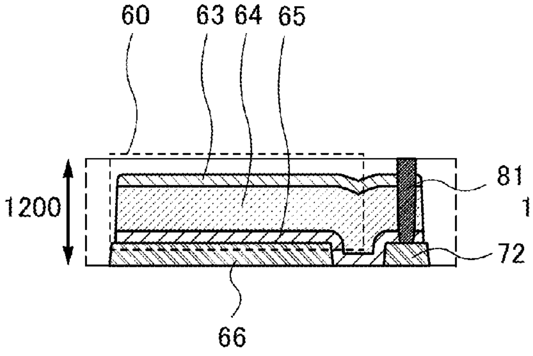


FIG. 14F

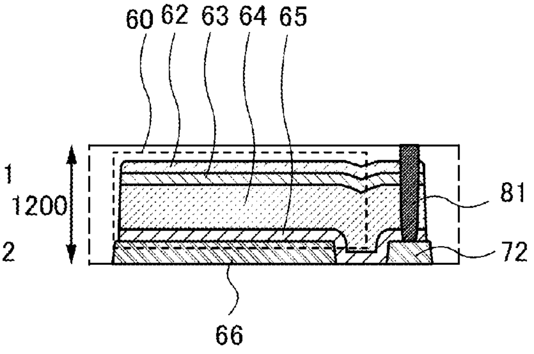


FIG. 15

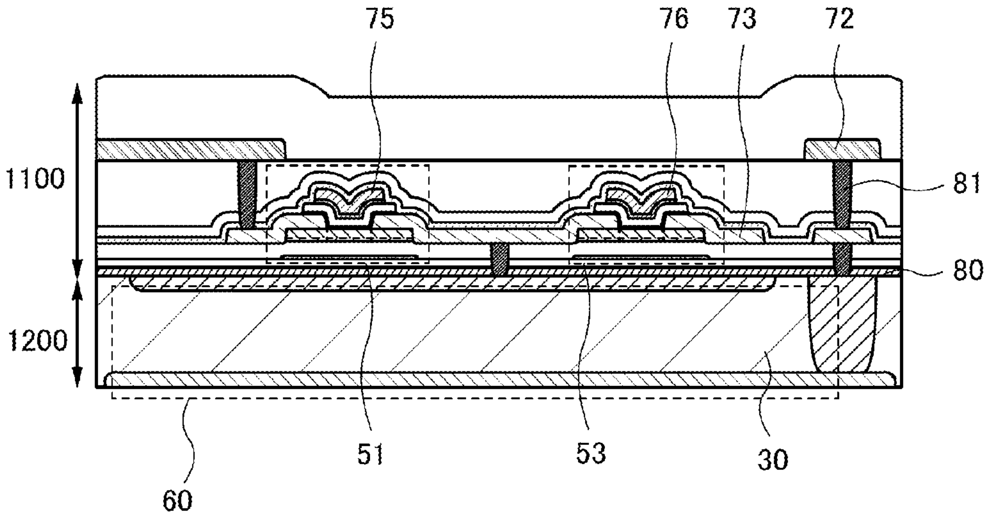


FIG. 16A

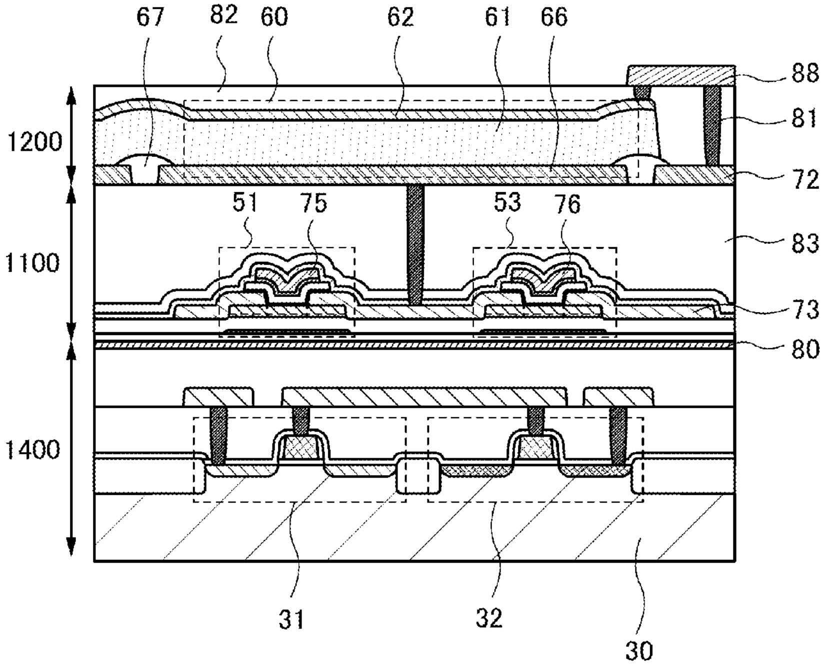


FIG. 16B

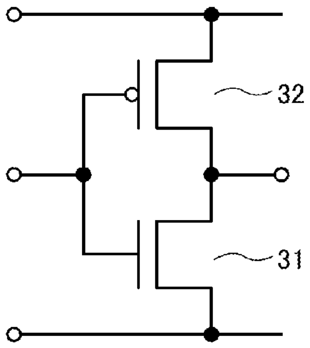


FIG. 16C

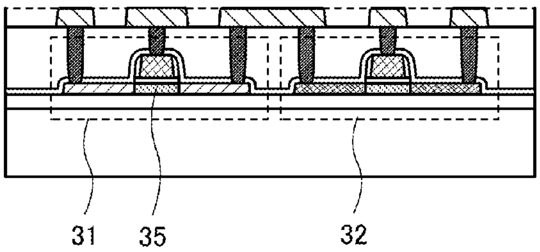


FIG. 17

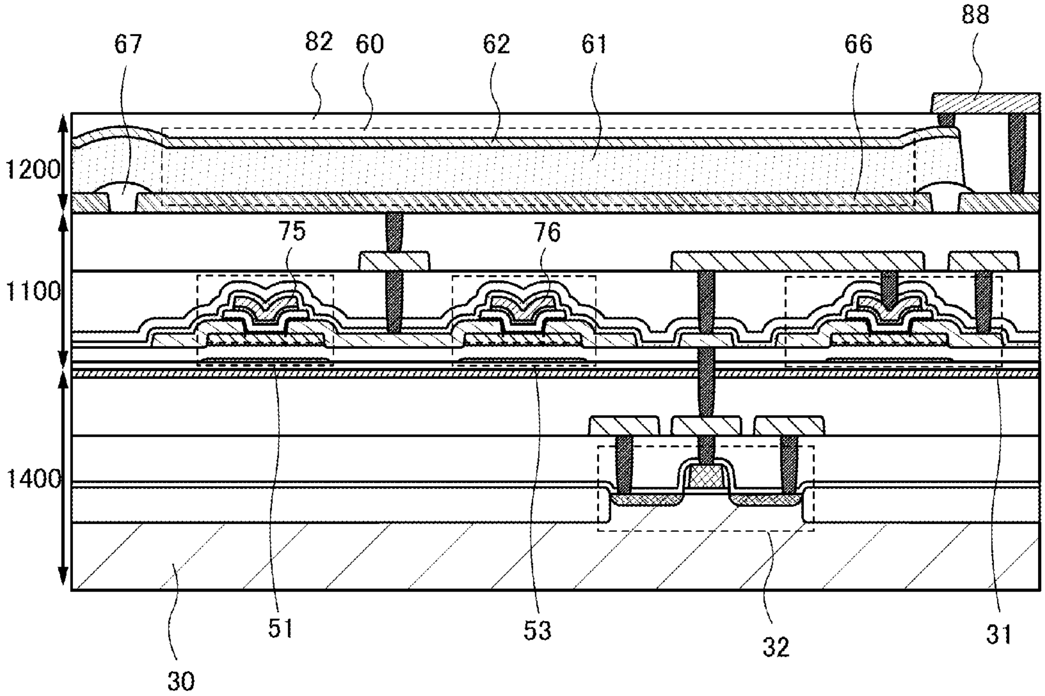


FIG. 18A

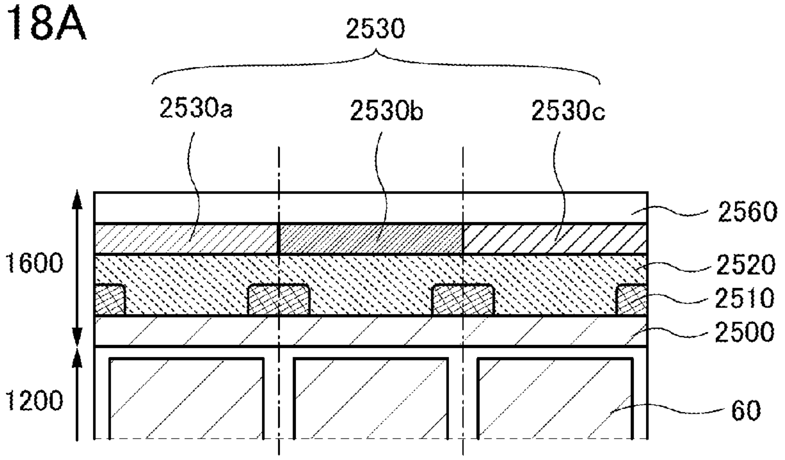


FIG. 18B

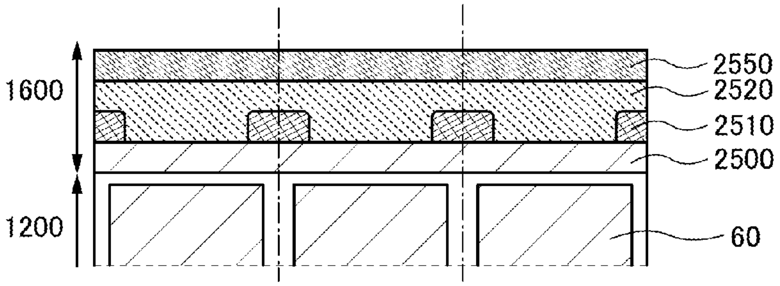


FIG. 18C

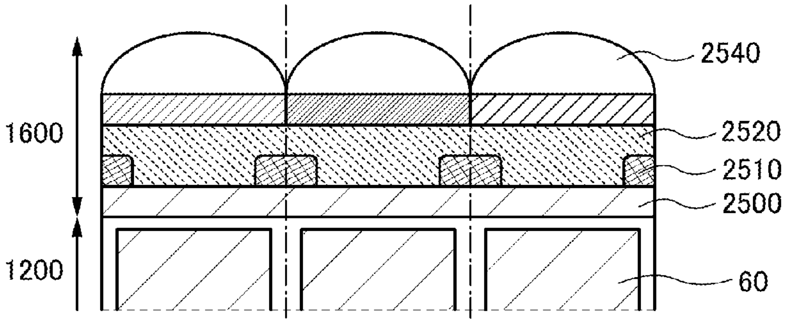


FIG. 19

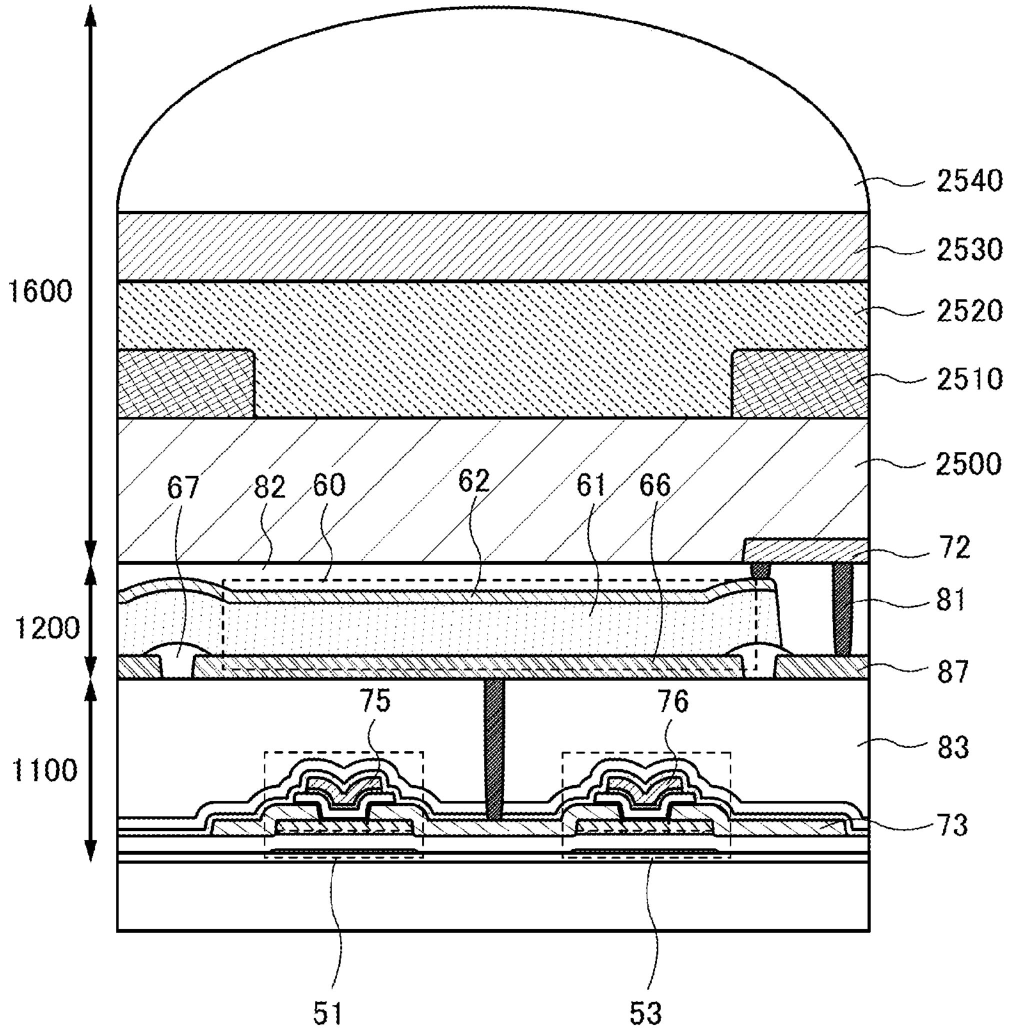
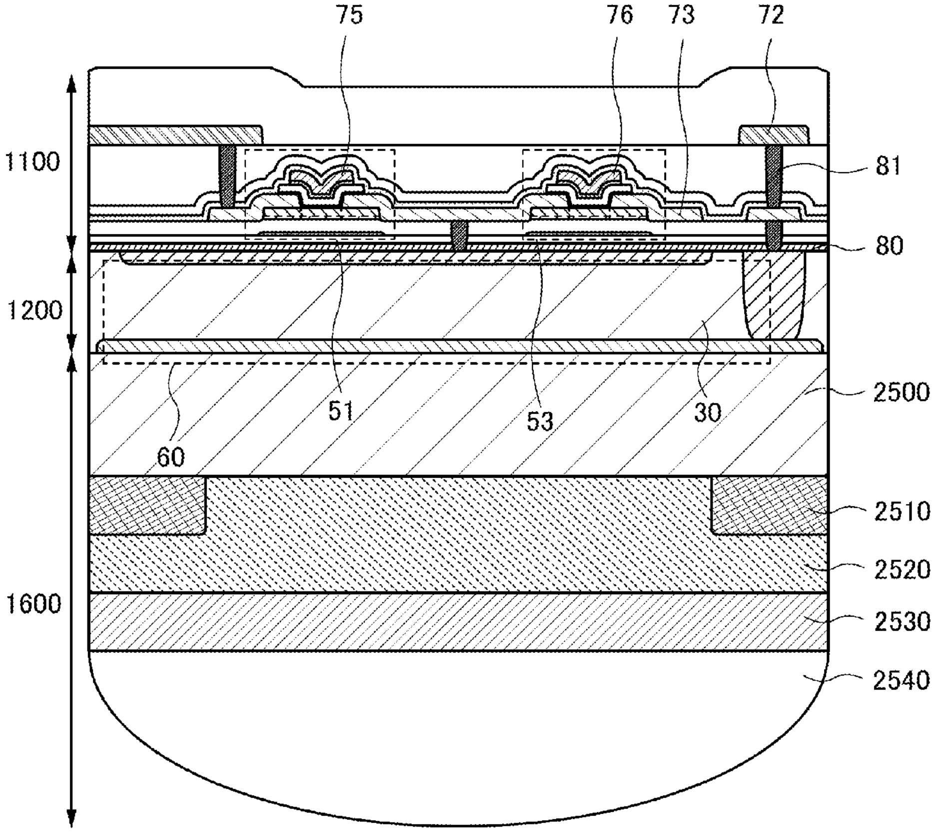

2540
2530
1600
2520
2510
2500
67
82
60
62
61
66
72
81
1200
87
75
76
83
1100
73
51
53

FIG. 20


75
76
73
72
1100
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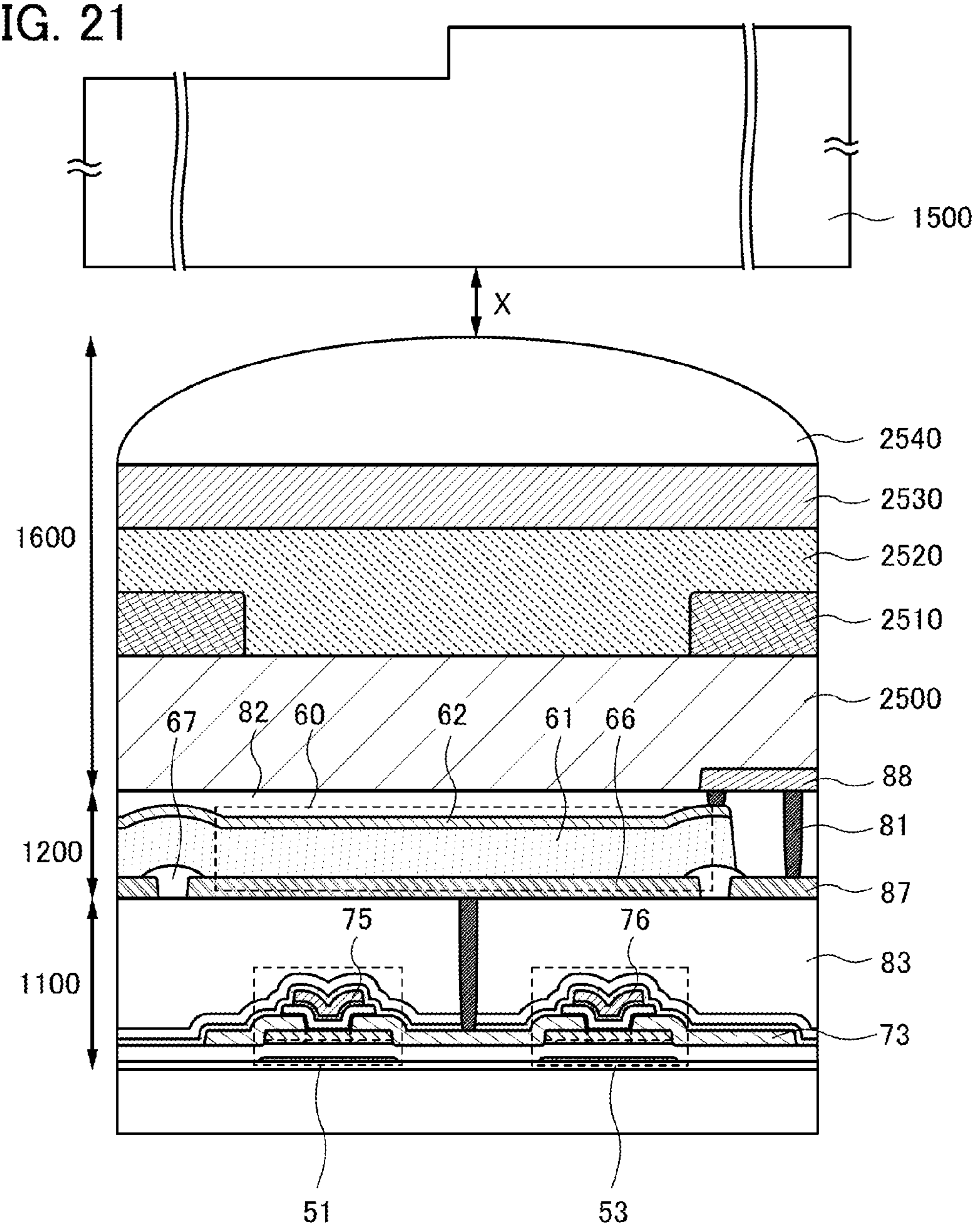
80
1200
2500
51
53
30
60
2510
2520
1600
2530
2540

FIG. 21


1500
X
1600
2540
2530
2520
2510
2500
67
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88
81
1200
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1100
83
73
51
53

FIG. 22

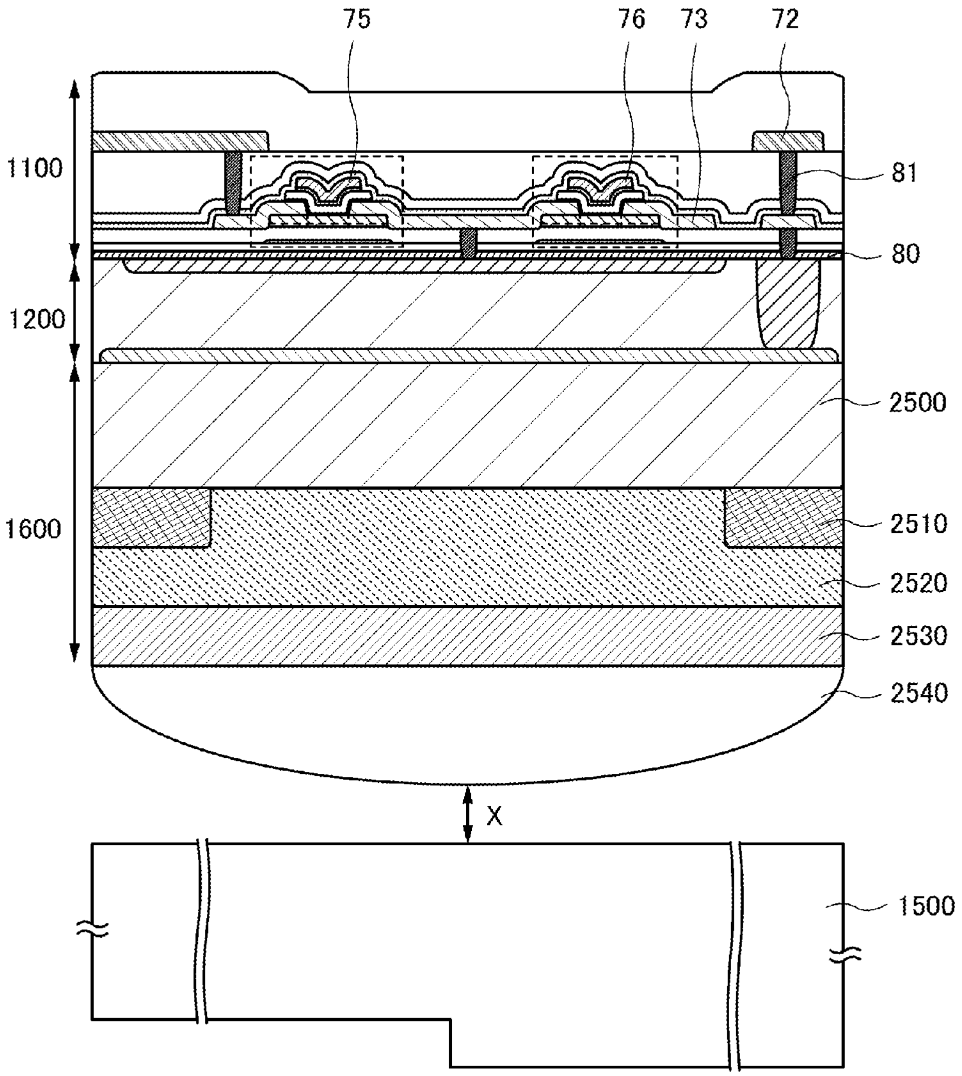


FIG. 23A1

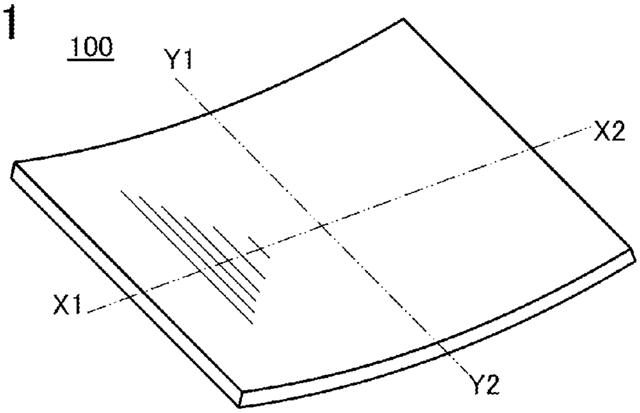


FIG. 23A2

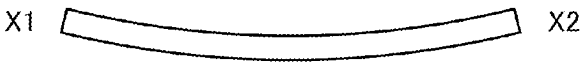


FIG. 23A3

FIG. 23B1

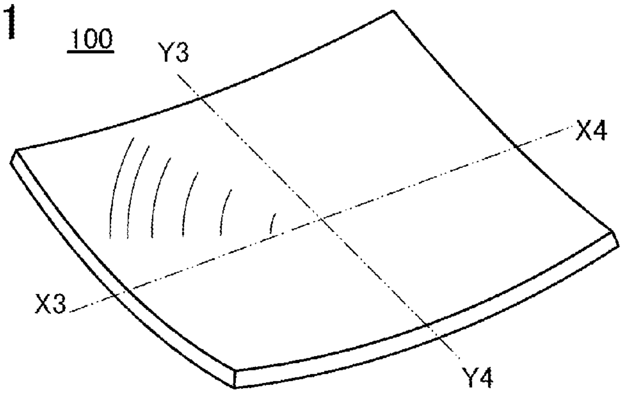


FIG. 23B2

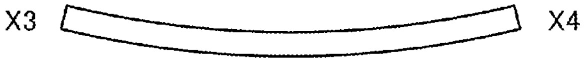


FIG. 23B3

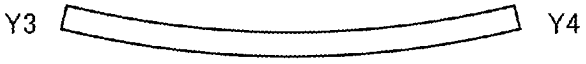


FIG. 24A

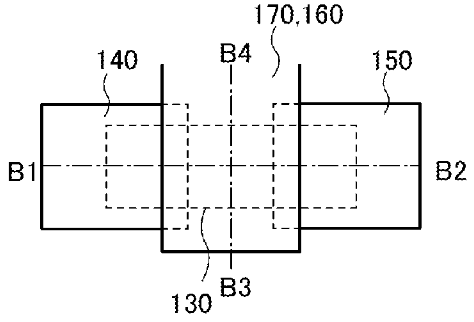


FIG. 24B

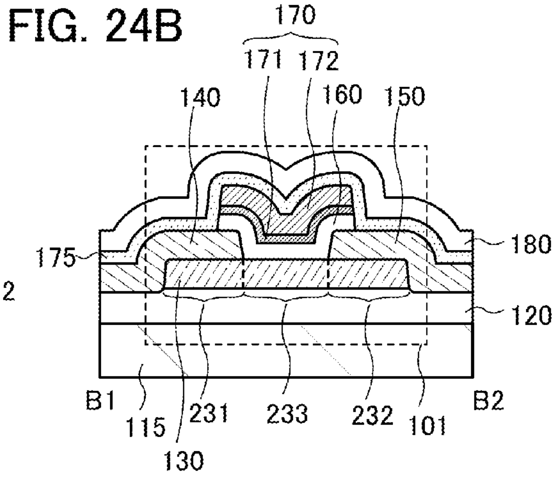


FIG. 24C

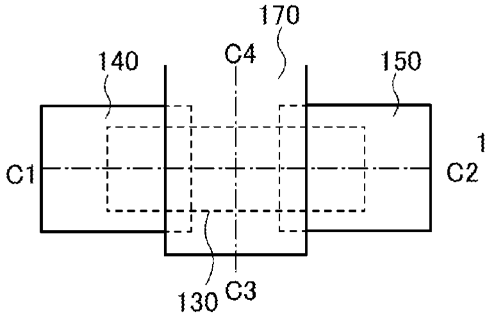


FIG. 24D

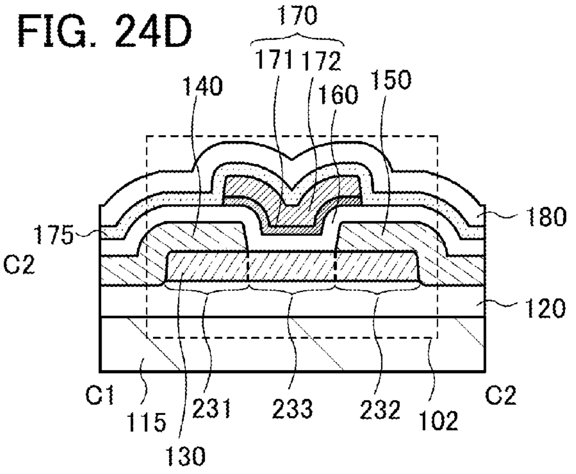


FIG. 24E

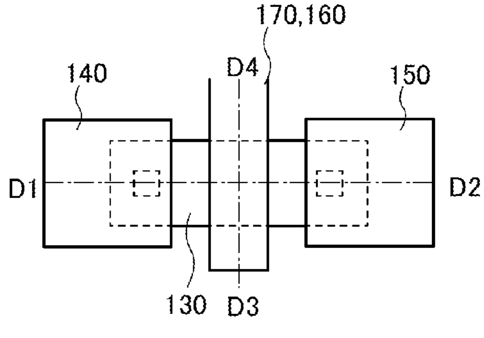


FIG. 24F

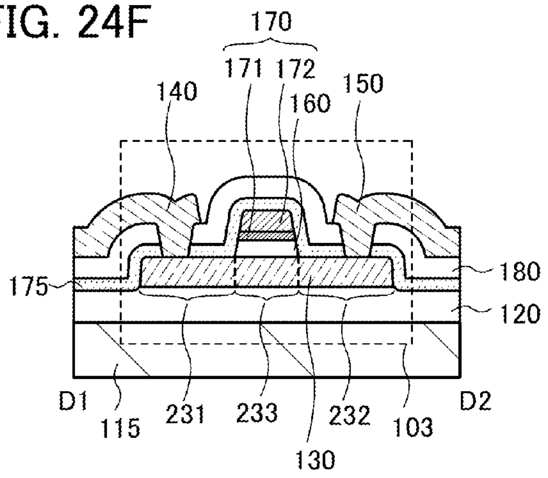


FIG. 25A

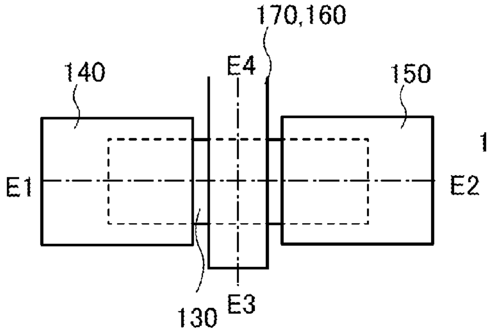


FIG. 25B

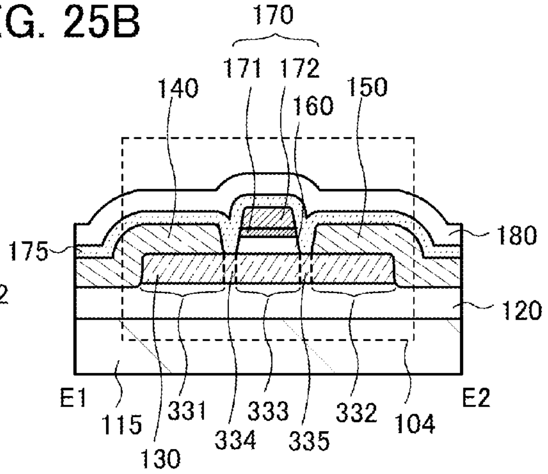


FIG. 25C

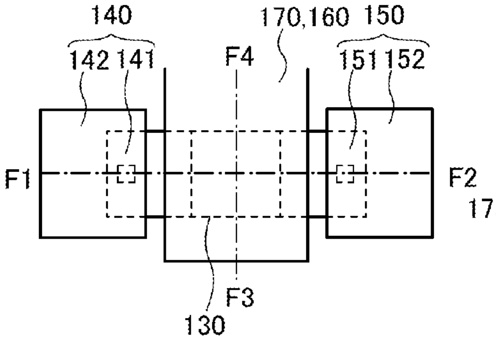


FIG. 25D

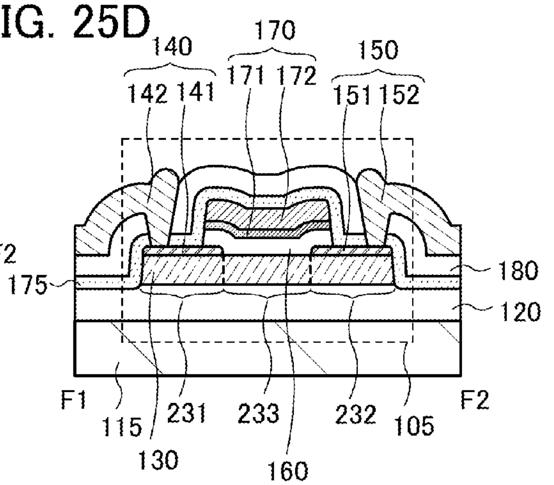


FIG. 25E

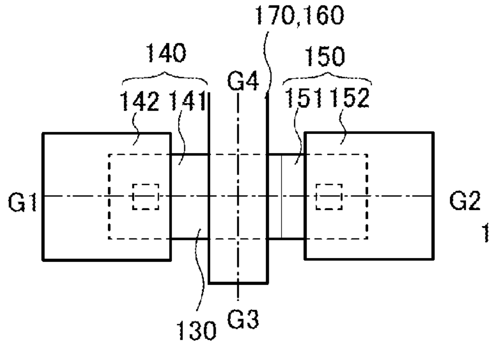


FIG. 25F

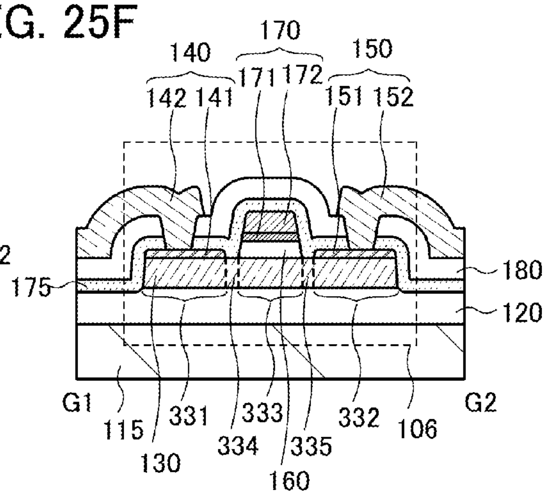


FIG. 26A

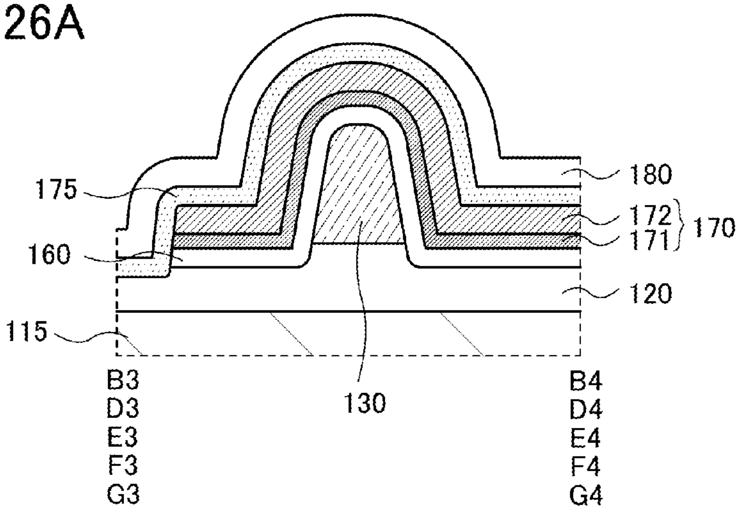


FIG. 26B

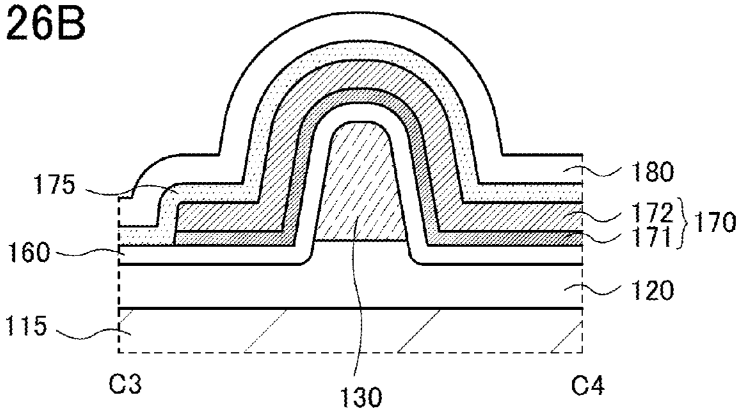


FIG. 26C

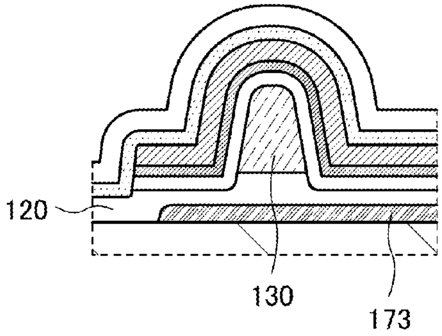


FIG. 26D

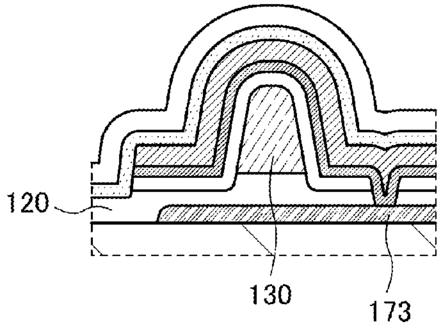


FIG. 27A

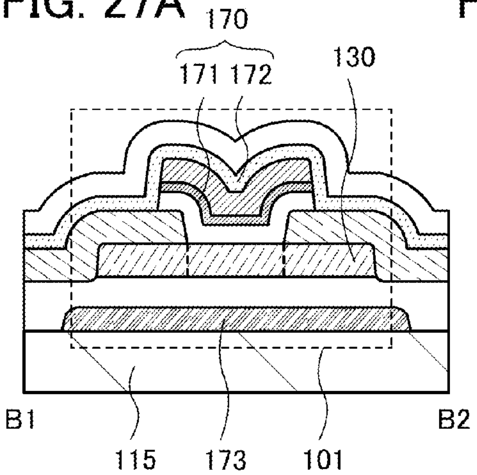


FIG. 27B

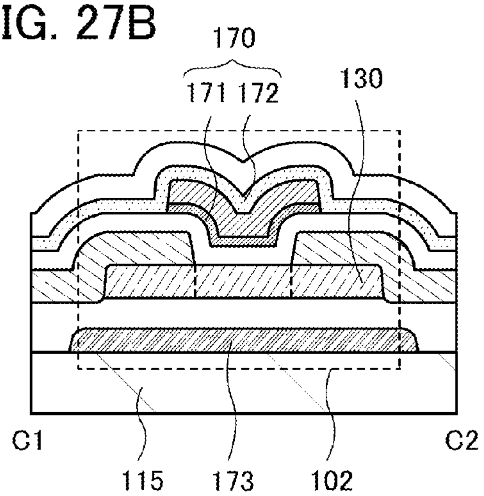


FIG. 27C

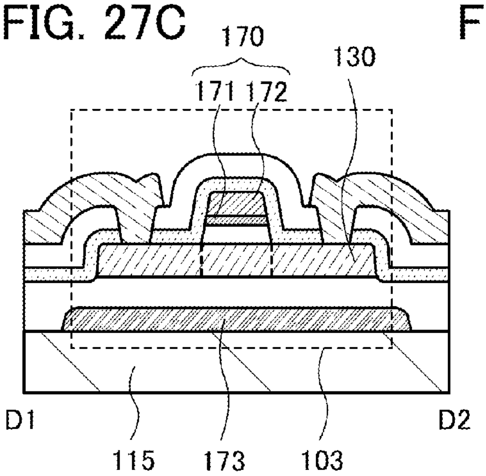


FIG. 27D

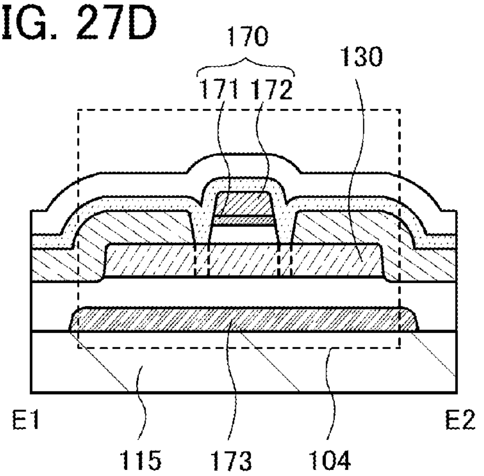


FIG. 27E

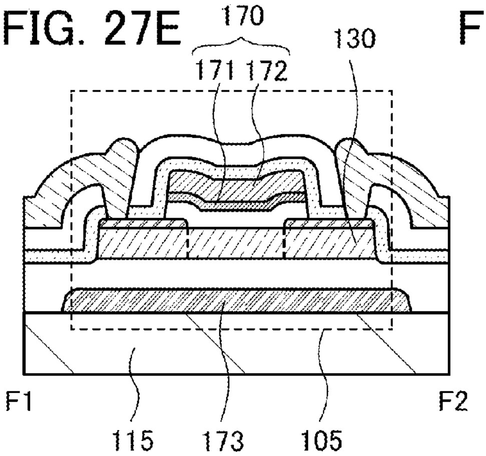


FIG. 27F

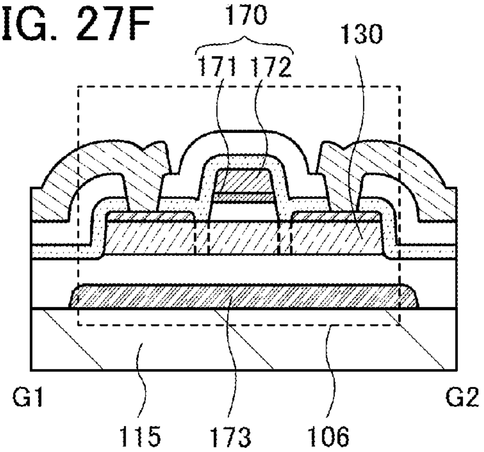


FIG. 28A

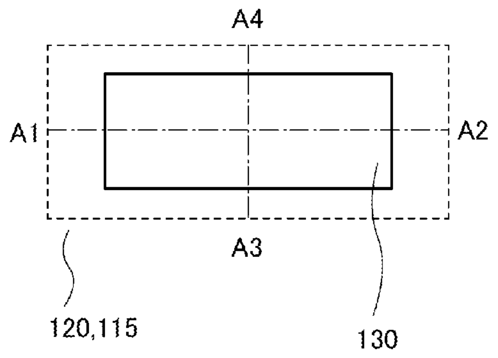


FIG. 28B

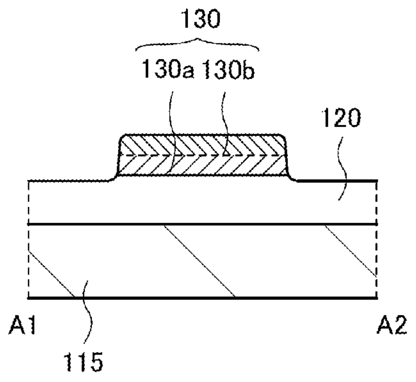


FIG. 28C

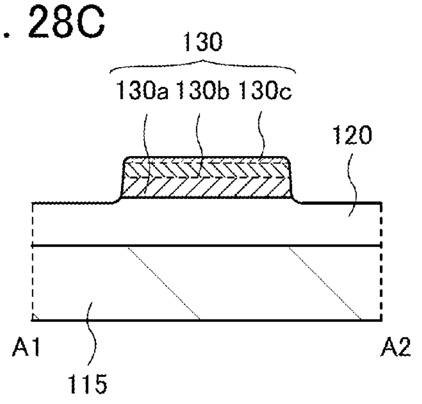


FIG. 28D

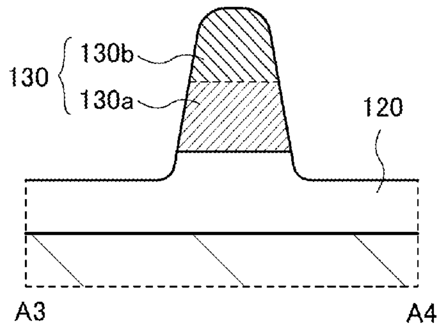


FIG. 28E

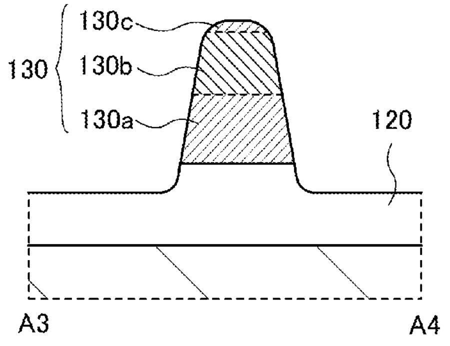


FIG. 29A

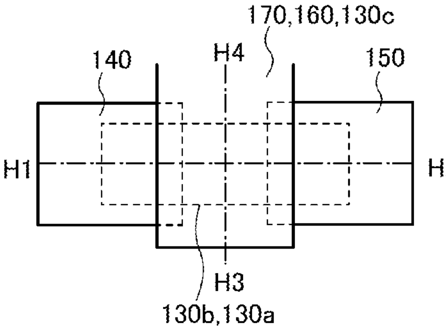


FIG. 29B

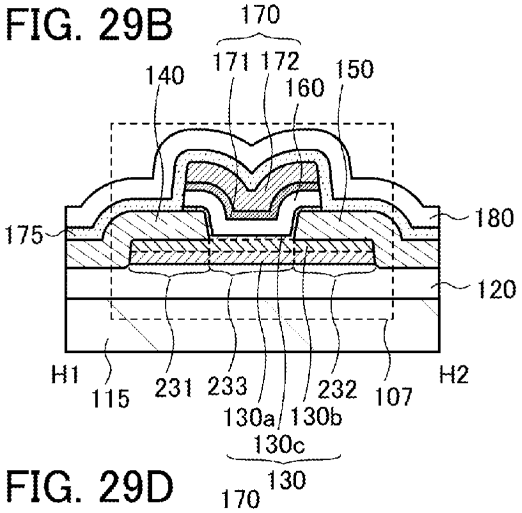


FIG. 29C

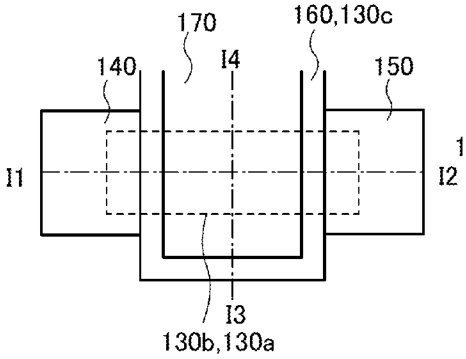


FIG. 29D

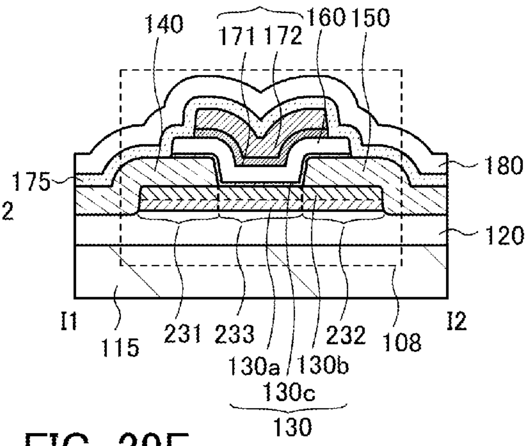


FIG. 29E

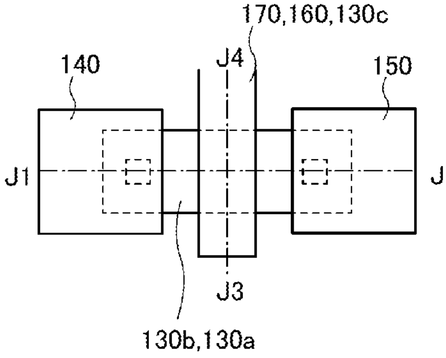


FIG. 29F

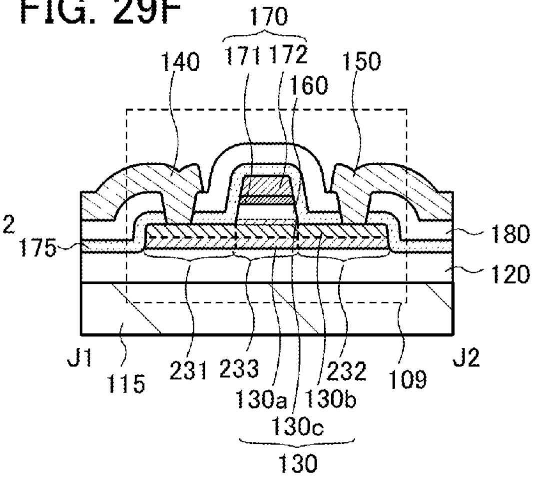


FIG. 30A

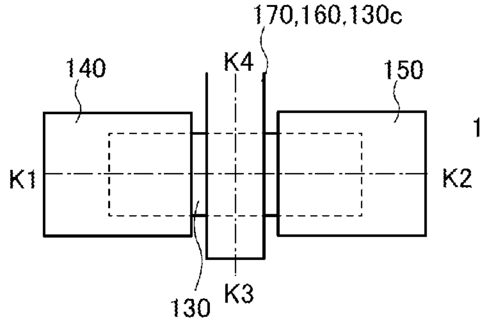


FIG. 30B

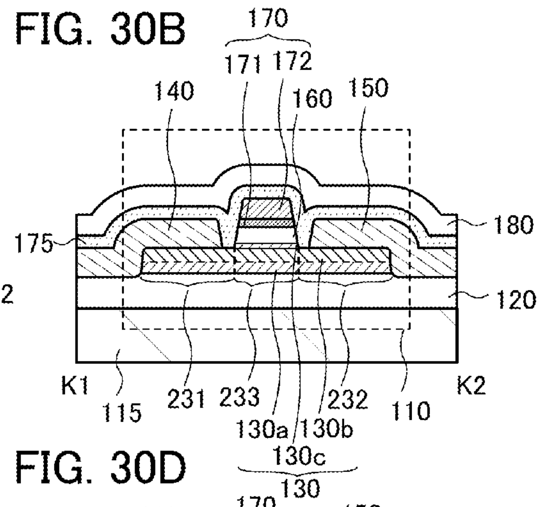


FIG. 30C

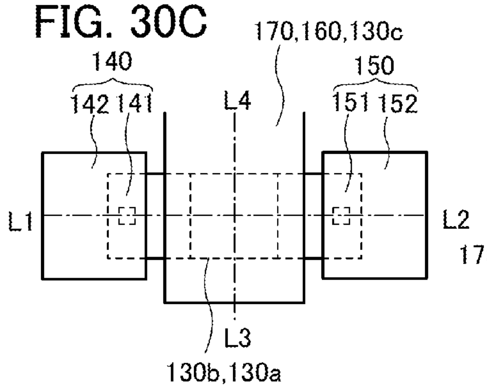


FIG. 30D

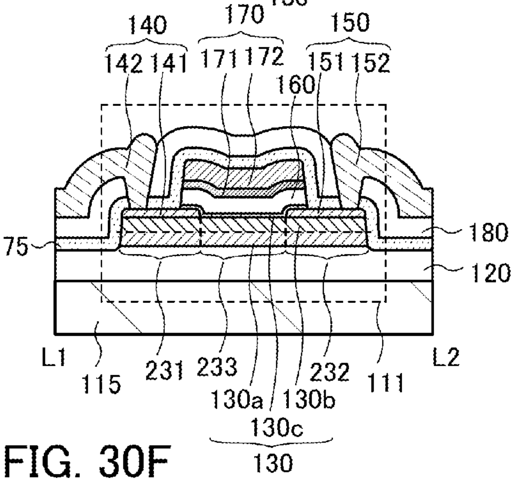


FIG. 30E

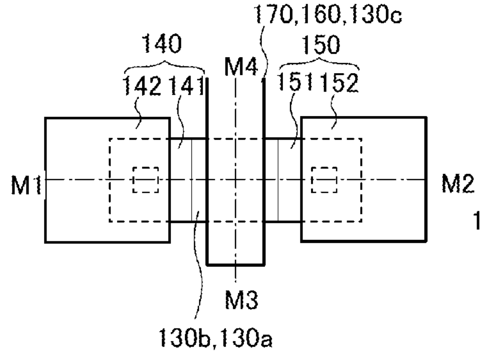


FIG. 30F

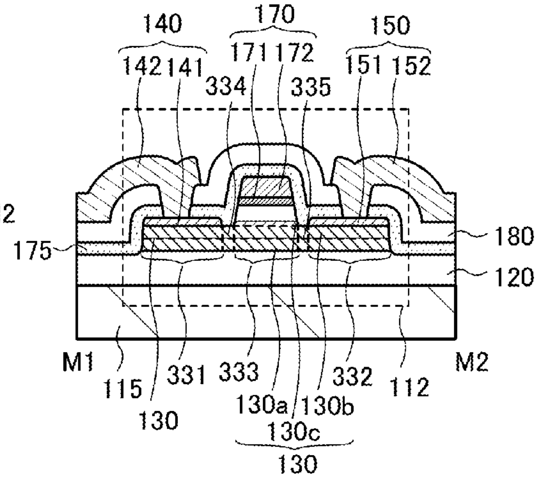


FIG. 31A

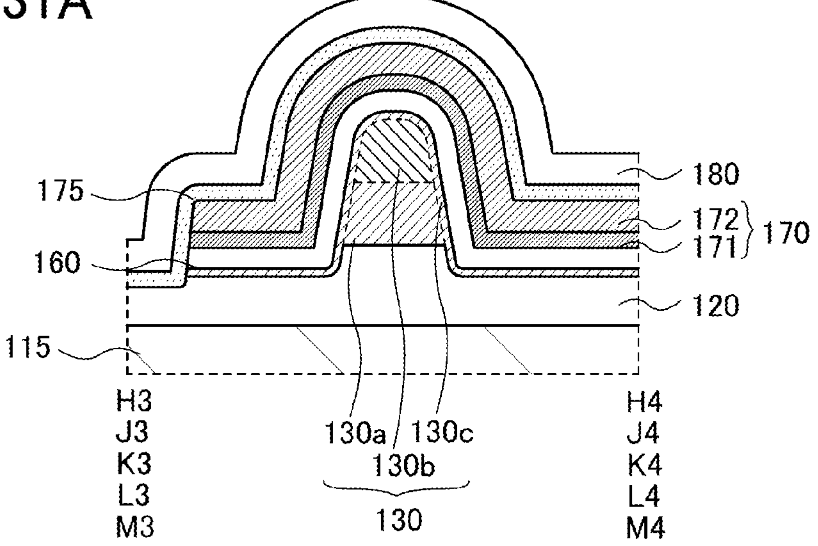


FIG. 31B

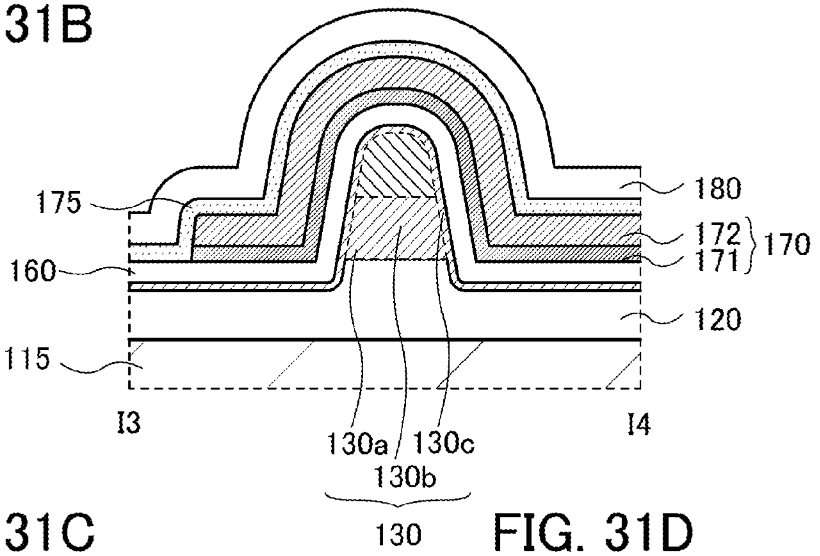


FIG. 31C

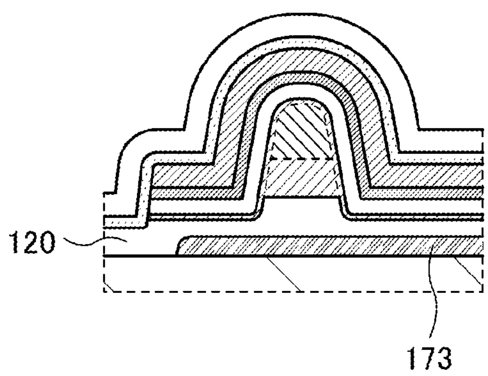


FIG. 31D

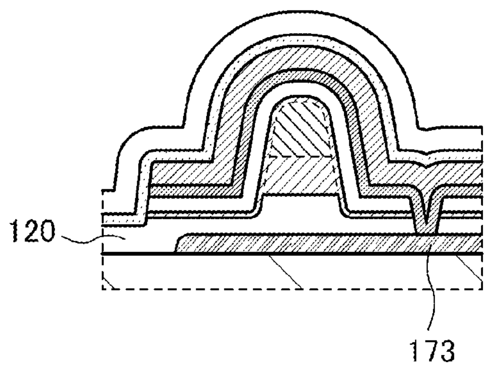


FIG. 32A

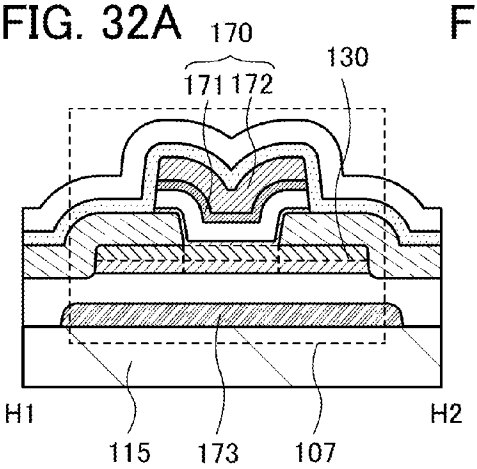


FIG. 32B

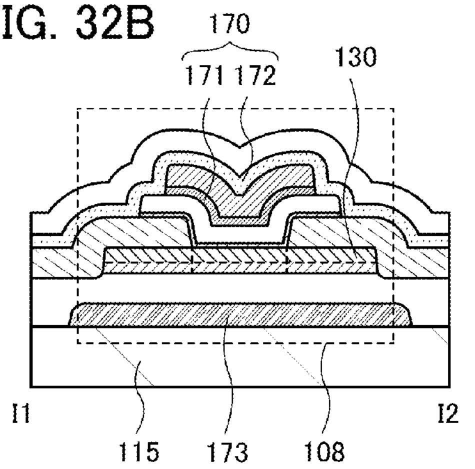


FIG. 32C

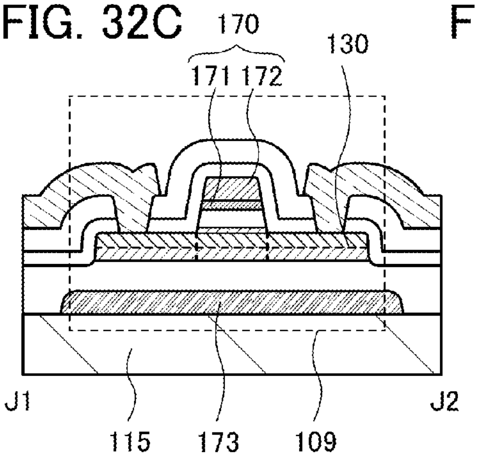


FIG. 32D

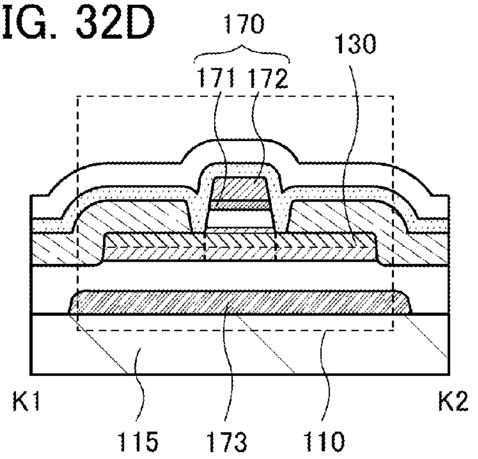


FIG. 32E

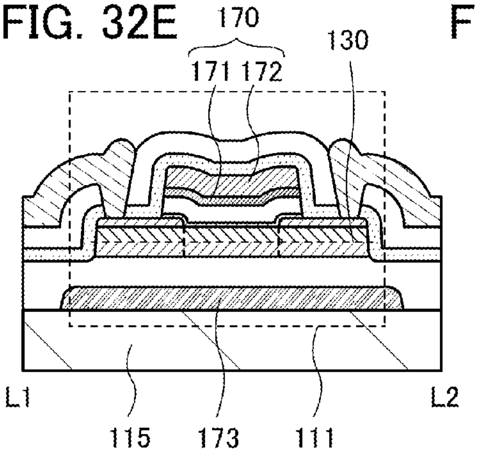


FIG. 32F

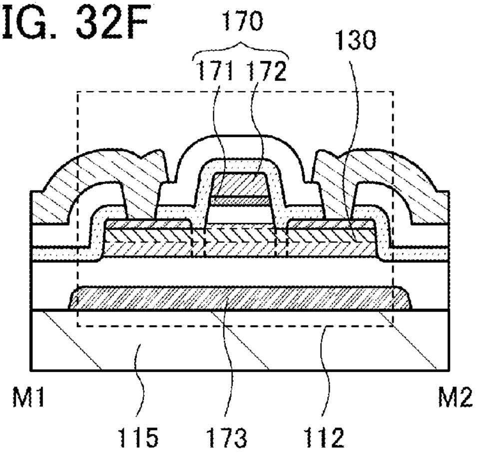


FIG. 33A

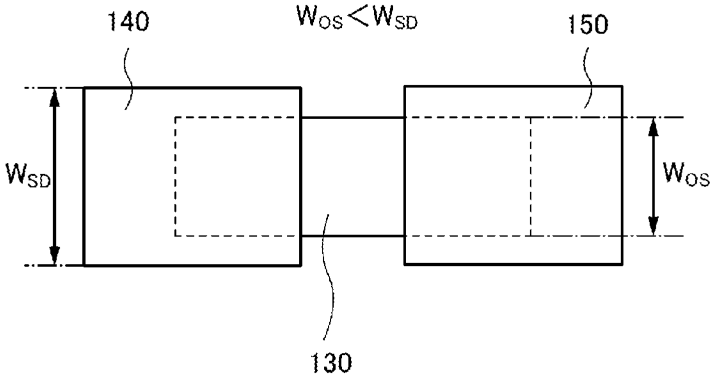


FIG. 33B

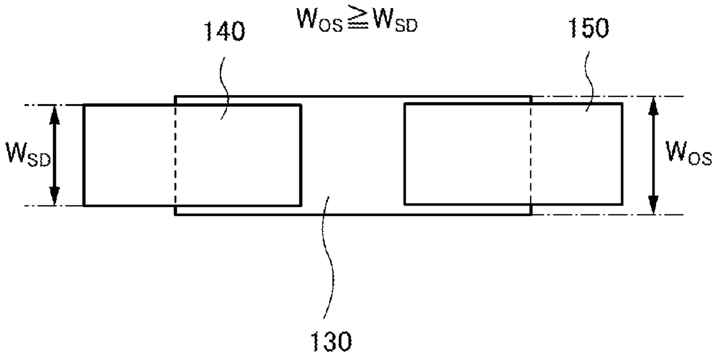


FIG. 33C

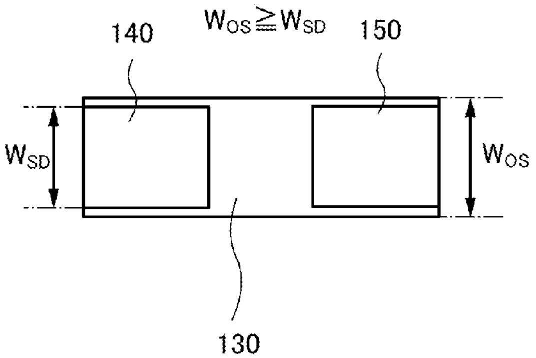


FIG. 34A

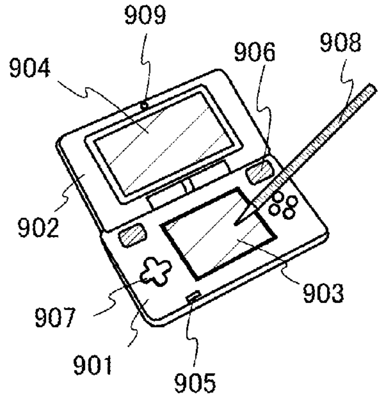


FIG. 34B

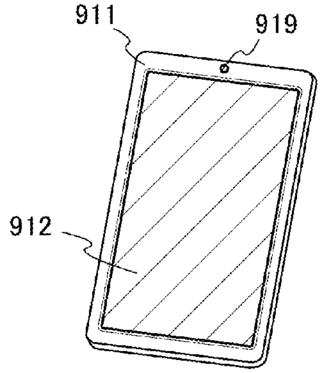


FIG. 34C

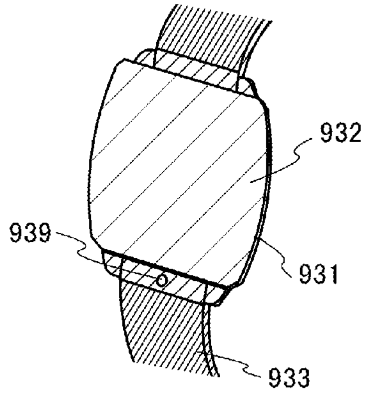


FIG. 34D

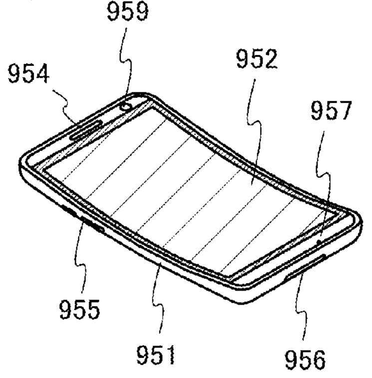


FIG. 34E

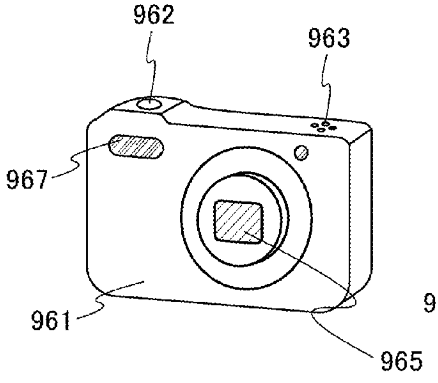


FIG. 34F

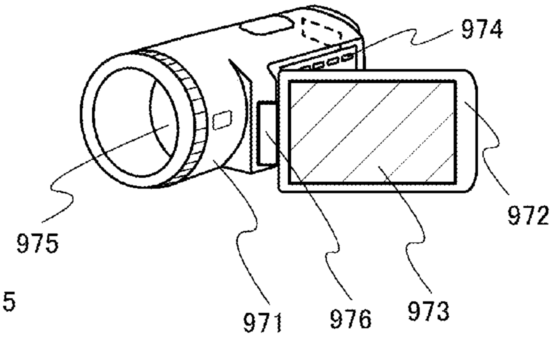


FIG. 35

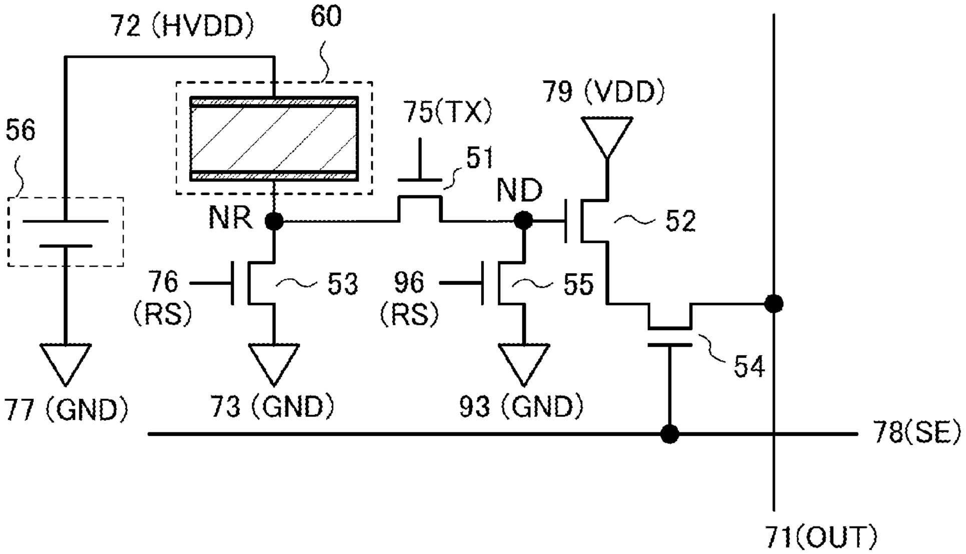

72 (HVDD)
60
56
75(TX)
51
79 (VDD)
ND
52
NR
76
(RS)
53
96
(RS)
55
54
77 (GND)
73 (GND)
93 (GND)
78(SE)
71(OUT)

FIG. 36

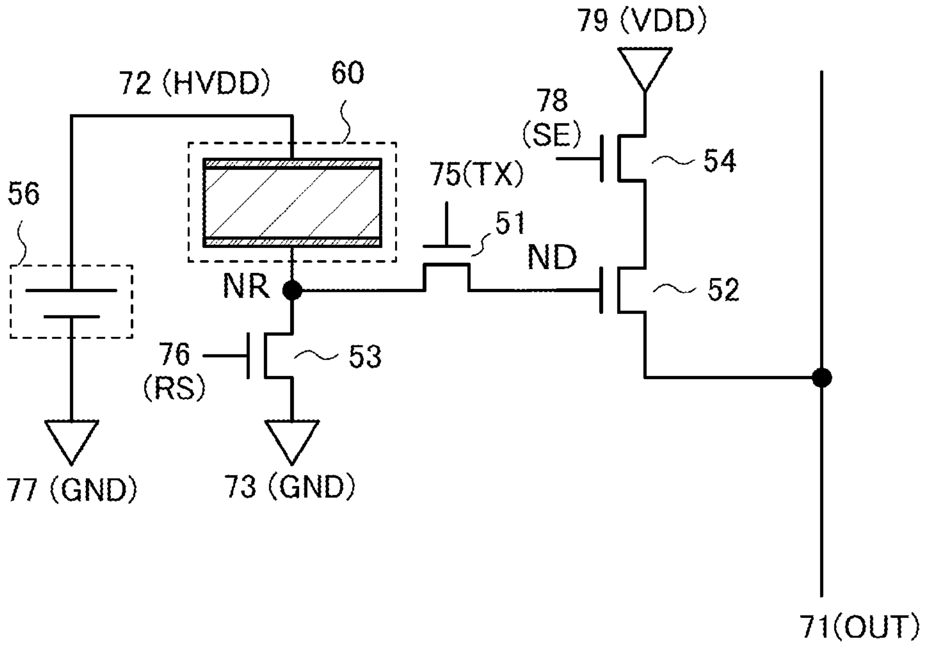

79 (VDD)
72 (HVDD)
60
78
(SE)
54
75(TX)
56
51
ND
NR
52
76
(RS)
53
77 (GND)
73 (GND)
71(OUT)

FIG. 37A

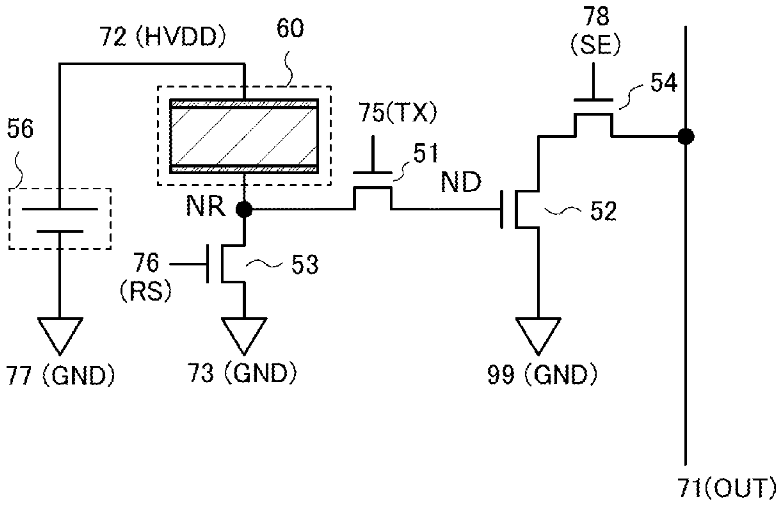


FIG. 37B

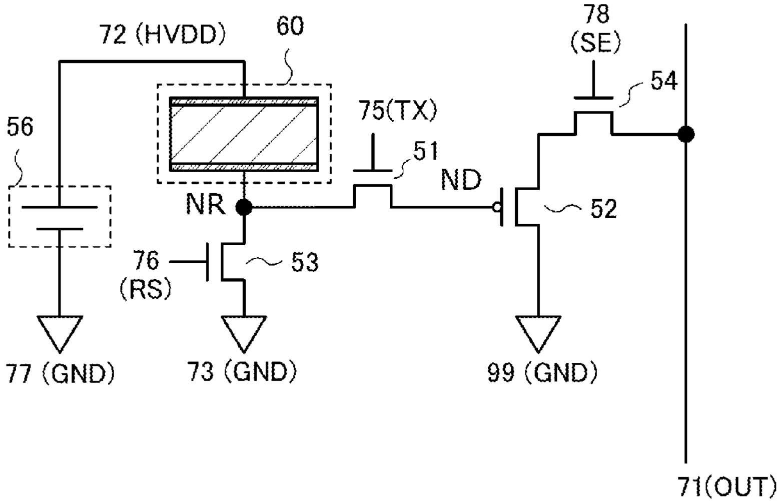
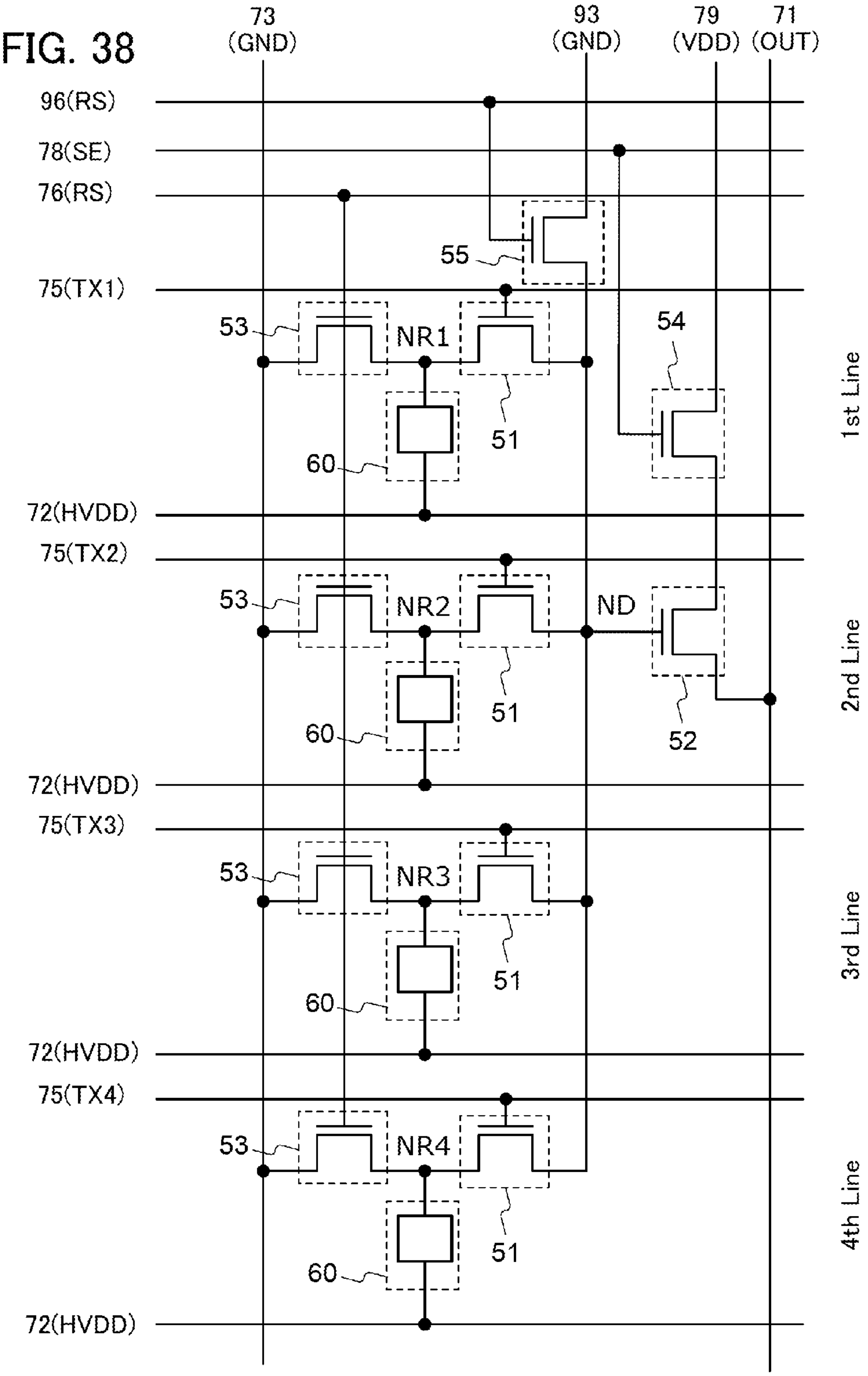


FIG. 38


73 (GND)
93 (GND)
79 (VDD)
71 (OUT)
96(RS)
78(SE)
76(RS)
55
75(TX1)
53
NR1
54
51
60
72(HVDD)
1st Line
75(TX2)
53
NR2
ND
51
52
60
72(HVDD)
2nd Line
75(TX3)
53
NR3
51
60
72(HVDD)
3rd Line
75(TX4)
53
NR4
51
60
72(HVDD)
4th Line

IMAGING DEVICE AND ELECTRONIC DEVICE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] One embodiment of the present invention relates to an imaging device including an oxide semiconductor.

[0003] Note that one embodiment of the present invention is not limited to the above technical field. The technical field of one embodiment of the invention disclosed in this specification and the like relates to an object, a method, or a manufacturing method. One embodiment of the present invention relates to a process, a machine, manufacture, or a composition of matter. Specifically, examples of the technical field of one embodiment of the present invention disclosed in this specification include a semiconductor device, a display device, a liquid crystal display device, a light-emitting device, a lighting device, a power storage device, a storage device, an imaging device, a method for driving any of them, and a method for manufacturing any of them.

[0004] In this specification and the like, a semiconductor device generally means a device that can function by utilizing semiconductor characteristics. A transistor and a semiconductor circuit are embodiments of semiconductor devices. In some cases, a storage device, a display device, an imaging device, or an electronic device includes a semiconductor device.

[0005] 2. Description of the Related Art

[0006] A technique by which transistors are formed using semiconductor thin films formed over a substrate having an insulating surface has attracted attention. The transistor is used in a wide range of electronic devices such as an integrated circuit (IC) and a display device. A silicon-based semiconductor is widely known as a semiconductor material applicable to the transistor. As another material, an oxide semiconductor has attracted attention.

[0007] For example, a technique for forming a transistor using zinc oxide or an In—Ga—Zn-based oxide semiconductor as an oxide semiconductor is disclosed (see Patent Documents 1 and 2).

[0008] Patent Document 3 discloses an imaging device in which a transistor including an oxide semiconductor and having extremely low off-state current is used in part of a pixel circuit and a transistor including silicon with which a complementary metal oxide semiconductor (CMOS) circuit can be formed is used in a peripheral circuit.

REFERENCE

[0009] Patent Document 1: Japanese Published Patent Application No. 2007-123861

[0010] Patent Document 2: Japanese Published Patent Application No. 2007-096055

[0011] Patent Document 3: Japanese Published Patent Application No. 2011-119711

SUMMARY OF THE INVENTION

[0012] To obtain a high-resolution image, an image sensor that includes a highly integrated pixel array is needed. To highly integrate pixels, per-pixel area needs to be reduced.

[0013] In the case where the area of a pixel is reduced, the light-receiving area of a photoelectric conversion element included in the pixel also needs to be reduced. When the light-receiving area of the photoelectric conversion element is reduced, it might be difficult to perform imaging under a low illuminance condition because of the decrease in sensitivity to light.

[0014] An object of one embodiment of the present invention is to provide an imaging device that easily performs imaging under a low illuminance condition. Another object of one embodiment of the present invention is to provide a low-power imaging device. Another object of one embodiment of the present invention is to provide an imaging device that is suitable for high-speed operation. Another object of one embodiment of the present invention is to provide an imaging device with high resolution. Another object of one embodiment of the present invention is to provide a highly integrated imaging device. Another object of one embodiment of the present invention is to provide an imaging device with a wide dynamic range. Another object of one embodiment of the present invention is to provide an imaging device that can be used in a wide temperature range. Another object of one embodiment of the present invention is to provide an imaging device with a high aperture ratio. Another object of one embodiment of the present invention is to provide an imaging device with high reliability. Another object of one embodiment of the present invention is to provide a novel imaging device or the like. Another object of one embodiment of the present invention is to provide a novel semiconductor device or the like.

[0015] The description of these objects does not disturb the existence of other objects. In one embodiment of the present invention, there is no need to achieve all the objects. Other objects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like. Other objects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

[0016] One embodiment of the present invention relates to a highly sensitive imaging device that can perform imaging even under a low illuminance condition.

[0017] One embodiment of the present invention is an imaging device that includes a first transistor, a second transistor, a third transistor, a fourth transistor, and a photoelectric conversion element. One electrode of the photoelectric conversion element is electrically connected to one of a source electrode and a drain electrode of the first transistor. The one electrode of the photoelectric conversion element is electrically connected to one of a source electrode and a drain electrode of the third transistor. The other of the source electrode and the drain electrode of the first transistor is electrically connected to a gate electrode of the second transistor. One of a source electrode and a drain electrode of the second transistor is electrically connected to one of a source electrode and a drain electrode of the fourth transistor. The other electrode of the photoelectric conversion element is electrically connected to a first wiring. A gate electrode of the first transistor is electrically connected to a second wiring. When a potential supplied to the first wiring is HVDD, the highest value of a potential supplied to the second wiring is lower than HVDD.

[0018] In the above structure, the other of the source electrode and the drain electrode of the second transistor is electrically connected to a third wiring. When the potential supplied to the first wiring is HVDD, a potential supplied to the third wiring is VDD, and HVDD is higher than VDD, the highest value of the potential supplied to the second wiring can be VDD.

[0019] The first transistor and the third transistor can each include an oxide semiconductor in an active layer. The oxide semiconductor preferably includes In, Zn, and M (M is Al, Ti, Ga, Sn, Y, Zr, La, Ce, Nd, or Hf).

[0020] The second transistor and the fourth transistor can each include silicon in an active layer or an active region.

[0021] According to one embodiment of the present invention, an imaging device that easily performs imaging under a low illuminance condition can be provided. A low-power imaging device can be provided. An imaging device that is suitable for high-speed operation can be provided. An imaging device with high resolution can be provided. A highly integrated imaging device can be provided. An imaging device with a wide dynamic range can be provided. An imaging device that can be used in a wide temperature range can be provided. An imaging device with a high aperture ratio can be provided. An imaging device with high reliability can be provided. A novel imaging device or the like can be provided. A novel semiconductor device or the like can be provided.

[0022] Note that one embodiment of the present invention is not limited to these effects. For example, depending on circumstances or conditions, one embodiment of the present invention might produce another effect. Furthermore, depending on circumstances or conditions, one embodiment of the present invention might not produce any of the above effects.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] In the accompanying drawings:

[0024] FIG. **1** illustrates a pixel circuit;

[0025] FIG. **2** shows I_d-V_g characteristics of an OS transistor;

[0026] FIG. **3** shows withstand voltage characteristics of an OS transistor;

[0027] FIG. **4** shows withstand voltage characteristics of an OS transistor;

[0028] FIG. **5** shows withstand voltage characteristics of an OS transistor;

[0029] FIG. **6** is a timing chart illustrating operation of imaging;

[0030] FIGS. **7**A to **7**H are circuit diagrams each illustrating a pixel circuit;

[0031] FIG. **8** is a circuit diagram illustrating a pixel circuit;

[0032] FIGS. **9**A to **9**C are cross-sectional views each illustrating the structure of an imaging device;

[0033] FIGS. **10**A and **10**B are timing charts illustrating operations of a global shutter system and a rolling shutter system, respectively;

[0034] FIGS. **11**A to **11**D are cross-sectional views each illustrating connection of a photoelectric conversion element;

[0035] FIGS. **12**A and **12**B are cross-sectional views each illustrating connection of a photoelectric conversion element;

[0036] FIG. **13** is a cross-sectional view illustrating the structure of an imaging device;

[0037] FIGS. **14**A to **14**F are cross-sectional views each illustrating connection of a photoelectric conversion element;

[0038] FIG. **15** is a cross-sectional view illustrating the structure of an imaging device;

[0039] FIGS. **16**A to **16**C are cross-sectional views and a circuit diagram illustrating the structure of an imaging device;

[0040] FIG. **17** is a cross-sectional view illustrating the structure of an imaging device;

[0041] FIGS. **18**A to **18**C are cross-sectional views each illustrating the structure of an imaging device;

[0042] FIG. **19** is a cross-sectional view illustrating the structure of an imaging device;

[0043] FIG. **20** is a cross-sectional view illustrating the structure of an imaging device;

[0044] FIG. **21** is a cross-sectional view illustrating the structure of an imaging device;

[0045] FIG. **22** is a cross-sectional view illustrating the structure of an imaging device;

[0046] FIGS. **23**A**1**, **23**A**2**, **23**A**3**, **23**B**1**, **23**B**2**, and **23**B**3** illustrate a bent imaging device;

[0047] FIGS. **24**A to **24**F are top views and cross-sectional views illustrating a transistor;

[0048] FIGS. **25**A to **25**F are top views and cross-sectional views illustrating a transistor;

[0049] FIGS. **26**A to **26**D each illustrate a cross section of a transistor in a channel width direction;

[0050] FIGS. **27**A to **27**F each illustrate a cross section of a transistor in a channel length direction;

[0051] FIGS. **28**A to **28**E are a top view and cross-sectional views illustrating a semiconductor layer;

[0052] FIGS. **29**A to **29**F are top views and cross-sectional views illustrating a transistor;

[0053] FIGS. **30**A to **30**F are top views and cross-sectional views illustrating a transistor;

[0054] FIGS. **31**A to **31**D each illustrate a cross section of a transistor in a channel width direction;

[0055] FIGS. **32**A to **32**F each illustrate a cross section of a transistor in a channel length direction;

[0056] FIGS. **33**A to **33**C are top views each illustrating a transistor;

[0057] FIGS. **34**A to **34**F illustrate electronic devices;

[0058] FIG. **35** illustrates a pixel circuit;

[0059] FIG. **36** illustrates a pixel circuit;

[0060] FIGS. **37**A and **37**B each illustrate a pixel circuit;

[0061] FIG. **38** illustrates a pixel circuit.

DETAILED DESCRIPTION OF THE INVENTION

[0062] Embodiments will be described in detail with reference to the drawings. Note that the present invention is not limited to the following description. It will be readily appreciated by those skilled in the art that modes and details of the present invention can be modified in various ways without departing from the spirit and scope of the present invention. The present invention therefore should not be construed as being limited to the following description of the embodiments. In structures of the invention described below, the same portions or portions having similar functions are denoted by the same reference numerals in different drawings, and the description thereof is not repeated in some cases. The same components are denoted by different hatching patterns in different drawings, or the hatching patterns are omitted in some cases.

[0063] For example, in this specification and the like, an explicit description "X and Y are connected" means that X and Y are electrically connected, X and Y are functionally connected, and X and Y are directly connected. Accordingly, without being limited to a predetermined connection relationship, for example, a connection relationship shown in drawings or texts, another connection relationship is included in the drawings or the texts.

[0064] Here, each of X and Y denotes an object (e.g., a device, an element, a circuit, a wiring, an electrode, a terminal, a conductive film, or a layer).

[0065] Examples of the case where X and Y are directly connected include the case where an element that enables electrical connection between X and Y (e.g., a switch, a transistor, a capacitor, an inductor, a resistor, a diode, a display element, a light-emitting element, or a load) is not connected between X and Y, and the case where X and Y are connected without the element that enables electrical connection between X and Y provided therebetween.

[0066] For example, in the case where X and Y are electrically connected, one or more elements that enable electrical connection between X and Y (e.g., a switch, a transistor, a capacitor, an inductor, a resistor, a diode, a display element, a light-emitting element, or a load) can be connected between X and Y. Note that the switch is controlled to be turned on or off. That is, the switch is conducting or not conducting (is turned on or off) to determine whether current flows therethrough or not. Alternatively, the switch has a function of selecting and changing a current path. Note that the case where X and Y are electrically connected includes the case where X and Y are directly connected.

[0067] For example, in the case where X and Y are functionally connected, one or more circuits that enable functional connection between X and Y (e.g., a logic circuit such as an inverter, a NAND circuit, or a NOR circuit; a signal converter circuit such as a D/A converter circuit, an A/D converter circuit, or a gamma correction circuit; a potential level converter circuit such as a power supply circuit (e.g., a step-up circuit or a step-down circuit) or a level shifter circuit for changing the potential level of a signal; a voltage source; a current source; a switching circuit; an amplifier circuit such as a circuit that can increase signal amplitude, the amount of current, or the like, an operational amplifier, a differential amplifier circuit, a source follower circuit, or a buffer circuit; a signal generation circuit; a storage circuit; or a control circuit) can be connected between X and Y. Note that for example, in the case where a signal output from X is transmitted to Y even when another circuit is provided between X and Y, X and Y are functionally connected. The case where X and Y are functionally connected includes the case where X and Y are directly connected and X and Y are electrically connected.

[0068] Note that in this specification and the like, an explicit description "X and Y are electrically connected" means that X and Y are electrically connected (i.e., the case where X and Y are connected with another element or another circuit provided therebetween), X and Y are functionally connected (i.e., the case where X and Y are functionally connected with another circuit provided therebetween), and X and Y are directly connected (i.e., the case where X and Y are connected without another element or another circuit provided therebetween). That is, in this specification and the like, the explicit description "X and Y are electrically connected" is the same as the explicit description "X and Y are connected."

[0069] For example, the case where a source (or a first terminal or the like) of a transistor is electrically connected to X through (or not through) Z1 and a drain (or a second terminal or the like) of the transistor is electrically connected to Y through (or not through) Z2, or the case where a source (or a first terminal or the like) of a transistor is directly connected to part of Z1 and another part of Z1 is directly connected to X while a drain (or a second terminal or the like) of the transistor is directly connected to part of Z2 and another part of Z2 is directly connected to Y, can be expressed by using any of the following expressions.

[0070] The expressions include, for example, "X, Y, a source (or a first terminal or the like) of a transistor, and a drain (or a second terminal or the like) of the transistor are electrically connected to each other, and X, the source (or the first terminal or the like) of the transistor, the drain (or the second terminal or the like) of the transistor, and Y are electrically connected to each other in that order," "a source (or a first terminal or the like) of a transistor is electrically connected to X, a drain (or a second terminal or the like) of the transistor is electrically connected to Y, and X, the source (or the first terminal or the like) of the transistor, the drain (or the second terminal or the like) of the transistor, and Y are electrically connected to each other in that order," and "X is electrically connected to Y through a source (or a first terminal or the like) and a drain (or a second terminal or the like) of a transistor, and X, the source (or the first terminal or the like) of the transistor, the drain (or the second terminal or the like) of the transistor, and Y are connected in that order." When the connection order in a circuit structure is defined by an expression similar to the above examples, a source (or a first terminal or the like) and a drain (or a second terminal or the like) of a transistor can be distinguished from each other to specify the technical scope.

[0071] Other examples of the expressions include "a source (or a first terminal or the like) of a transistor is electrically connected to X through at least a first connection path, the first connection path does not include a second connection path, the second connection path is a path between the source (or the first terminal or the like) of the transistor and a drain (or a second terminal or the like) of the transistor, Z1 is on the first connection path, the drain (or the second terminal or the like) of the transistor is electrically connected to Y through at least a third connection path, the third connection path does not include the second connection path, and Z2 is on the third connection path." It is also possible to use the expression "a source (or a first terminal or the like) of a transistor is electrically connected to X through at least Z1 on a first connection path, the first connection path does not include a second connection path, the second connection path includes a connection path through the transistor, a drain (or a second terminal or the like) of the transistor is electrically connected to Y through at least Z2 on a third connection path, and the third connection path does not include the second connection path." Still another example of the expressions is "a source (or a first terminal or the like) of a transistor is electrically connected to X through at least Z1 on a first electrical path, the first electrical path does not include a second electrical path, the second electrical path is an electrical path from the source (or the first terminal or the like) of the transistor to a drain (or a second terminal or the like) of the transistor, the drain (or the second terminal or the like) of the transistor is electrically connected to Y through at least Z2 on a third electrical path, the third electrical path does not include a fourth electrical path, and the fourth electrical path is an electrical path from the drain (or the second terminal or the like) of the transistor to the source (or the first terminal or the like) of the transistor." When the connection path in a circuit structure is defined by an expression similar to the above examples, a source (or a first terminal or the like) and a drain (or a second terminal or the like) of a transistor can be distinguished from each other to specify the technical scope.

[0072] Note that these expressions are examples and there is no limitation on the expressions. Here, X, Y, Z1, and Z2 each denote an object (e.g., a device, an element, a circuit, a wiring, an electrode, a terminal, a conductive film, or a layer).

[0073] Even when independent components are electrically connected to each other in a circuit diagram, one component has functions of a plurality of components in some cases. For example, when part of a wiring also functions as an electrode, one conductive film functions as the wiring and the electrode. Thus, the term "electrical connection" in this specification also means such a case where one conductive film has functions of a plurality of components.

[0074] Note that the terms "film" and "layer" can be interchanged with each other depending on circumstances or conditions. For example, the term "conductive layer" can be changed into the term "conductive film" in some cases. In addition, the term "insulating film" can be changed into the term "insulating layer" in some cases.

[0075] Note that in general, a potential (voltage) is relative and is determined depending on the amount relative to a certain potential. Therefore, even when the expression "ground", "GND", or the like is used, the potential is not necessarily 0 V. For example, the "ground potential" or "GND" might be defined using the lowest potential in a circuit as a reference. Alternatively, the "ground potential" or "GND" might be defined using an intermediate potential in a circuit as a reference. In those cases, a positive potential and a negative potential are set using the potential as a reference.

Embodiment 1

[0076] In this embodiment, an imaging device that is one embodiment of the present invention is described with reference to drawings.

[0077] FIG. **1** illustrates a pixel circuit that can be used for an imaging device in one embodiment of the present invention. The pixel circuit includes a transistor **51**, a transistor **52**, a transistor **53**, a transistor **54**, and a photoelectric conversion element **60**.

[0078] One electrode of the photoelectric conversion element **60** is electrically connected to one of a source electrode and a drain electrode of the transistor **51**. The one electrode of the photoelectric conversion element **60** is electrically connected to one of a source electrode and a drain electrode of the transistor **53**. The other of the source electrode and the drain electrode of the transistor **51** is electrically connected to a gate electrode of the transistor **52**. One of a source electrode and a drain electrode of the transistor **52** is electrically connected to one of a source electrode and a drain electrode of the transistor **54**.

[0079] The other electrode of the photoelectric conversion element **60** is electrically connected to a wiring **72** (HVDD). A gate electrode of the transistor **51** is electrically connected to a wiring **75** (TX). The other of the source electrode and the drain electrode of the transistor **52** is electrically connected to a wiring **79** (VDD). A gate electrode of the transistor **53** is electrically connected to a wiring **76** (RS). The other of the source electrode and the drain electrode of the transistor **53** is electrically connected to a wiring **73** (GND). The other of the source electrode and the drain electrode of the transistor **54** is electrically connected to a wiring **71** (OUT). A gate electrode of the transistor **54** is electrically connected to a wiring **78** (SE). The wiring **72** (HVDD) is electrically connected to one terminal of a high voltage power source **56**. The other terminal of the high voltage power source **56** is electrically connected to a wiring **77** (GND).

[0080] The wiring **71** (OUT) can function as an output line that outputs a signal from a pixel. The wiring **73** (GND), the wiring **77** (GND), and the wiring **79** (VDD) can function as power supply lines. For example, the wiring **73** (GND) and the wiring **77** (GND) can function as low potential power supply lines, and the wiring **79** (VDD) can function as a high potential power supply line. The wiring **75** (TX), the wiring **76** (RS), and the wiring **78** (SE) can function as signal lines that control the on/off states of the transistors.

[0081] Note that the wiring **73** (GND) and the wiring **77** (GND) may be provided as one wiring. In addition, the potentials of the two wirings are not limited to GND, and may be any potentials as long as they are sufficiently lower than a potential supplied to the wiring **79** (VDD).

[0082] The photoelectric conversion element **60** exhibits photoelectric characteristics when a potential HVDD that is high voltage is applied. Note that in this embodiment, the potential HVDD is higher than a potential VDD supplied to the wiring **79** (VDD). To increase light detection sensitivity under a low illuminance condition, it is preferable to use a photoelectric conversion element formed using a material that causes avalanche charge multiplication as the photoelectric conversion element **60**. To cause avalanche charge multiplication, comparatively high voltage (HVDD) is needed. Thus, the high voltage power source **56** is capable of supplying HVDD, and HVDD is supplied to the other electrode of the photoelectric conversion element **60** through the wiring **72** (HVDD).

[0083] The transistor **51** can function as a transfer transistor for transferring the potential of a charge accumulation portion (NR) that changes in response to output of the photoelectric conversion element **60** to a charge accumulation portion (ND). The transistor **53** can function as a reset transistor that initializes the potentials of the charge accumulation portion (NR) and the charge accumulation portion (ND). The transistor **52** can function as an amplifying transistor that outputs a signal based on the potential of the charge accumulation portion (ND). The transistor **54** can function as a selection transistor that selects a pixel from which a signal is read.

[0084] In the case where high voltage is applied to the photoelectric conversion element **60**, a transistor to be connected to the photoelectric conversion element **60** needs to withstand the high voltage. As the high withstand voltage transistor, for example, a transistor including an oxide semiconductor in an active layer (hereinafter referred to as an OS transistor) can be used. Specifically, OS transistors are preferably used as the transistors **51** and **53**.

[0085] Here, FIG. **2** shows static characteristics (drain voltage (V_d)=0.1 V and 3.3 V) of an OS transistor with channel length L/channel width W=0.35 μm/0.8 μm and a gate insulating film thickness (obtained by conversion) of 20 nm (a physical film thickness of 31 nm). FIG. **3** shows drain breakdown voltage characteristics of the transistor at gate voltage (V_g)=0 V and source voltage (V_s)=0 V. FIG. **4** shows positive gate breakdown voltage characteristics of the transistor at V_s=V_d=0 V. FIG. **5** shows negative gate breakdown voltage characteristics of the transistor at V_s=V_d=0 V. As shown in FIG. **2**, FIG. **3**, FIG. **4**, and FIG. **5**, the OS transistor has high withstand voltage electrical characteristics.

[0086] Since the OS transistor has a wide bandgap (>3.0 eV) semiconductor, drain withstand voltage depends not on junction withstand voltage but on the gate insulating film thickness. The OS transistor is less likely to generate a short channel effect, so that the drain withstand voltage is increased by making the gate insulating film thicker and normally-off transistor characteristics are easily obtained. The OS transistor withstands a bias of higher than 20 V that is necessary for avalanche charge multiplication of the photoelectric conversion element. Note that the failure mode of the OS transistor is dielectric breakdown.

[0087] Note that in this specification, the high withstand voltage transistor refers to a transistor that can withstand desired high voltage without electrical breakdown. For example, in the high withstand voltage transistor, desired high voltage can be applied to a gate electrode without breakdown when GND is applied to a source electrode and a drain electrode. Alternatively, in the high withstand voltage transistor, desired high voltage can be applied to the drain electrode without breakdown when GND is applied to the source electrode and the gate electrode. Alternatively, in the high withstand voltage transistor, desired high voltage can be applied to the drain electrode without breakdown when GND is applied to the source electrode and VDD is applied to the gate electrode.

[0088] Although the transistors **51** and **53** give high priority to switching characteristics, the transistor **52** gives high priority to amplifying characteristics; thus, a transistor with high on-state current is preferably used. Therefore, a transistor including silicon in an active layer or an active region (hereinafter referred to as a Si transistor) is preferably used as the transistor **52**.

[0089] Note that the highest potential of the charge accumulation portion (NR) can be HVDD. However, in the case where an n-channel transistor is used as the transistor **51**, the potential of the charge accumulation portion (ND) is not higher than the highest potential that is applied to the gate electrode of the transistor **51**. More properly, the potential of the charge accumulation portion (ND) is not higher than a potential obtained by subtracting the threshold voltage (V_{th}) of the transistor **51** from the highest potential that is applied to the gate electrode of the transistor **51**. For example, even if the potential of the charge accumulation portion (NR) is HVDD, the highest potential of the charge accumulation portion (ND) is VDD when the highest potential that is applied to the wiring **75** (TX) is VDD. More properly, the potential of the charge accumulation portion (ND) is $VDD-V_{th}$. Note that in the following description, V_{th} of the transistor **51** is regarded as low voltage, and the description of Vth of the transistor **51** is omitted when the potential of the charge accumulation portion (ND) is described.

[0090] In other words, when the transistor **51** is normally-off, the potential VDD that is lower than the potential HVDD is power supply voltage for reading. Therefore, high voltage is not applied to the gate electrode of the transistor **52**, so that the use of a Si transistor that includes a thin gate insulating film and has comparatively not so high withstand voltage as the transistor **52** does not pose a problem.

[0091] When the transistors **51** to **54** have the above structures, it is possible to manufacture an imaging device that has high light detection sensitivity under a low illuminance condition and can output a signal with little noise. Since the imaging device has high light detection sensitivity, light capturing time can be shortened and imaging can be performed at high speed.

[0092] Next, operation of the pixel is described with reference to a timing chart in FIG. **6**. Note that in the following description of an operation example, HVDD and GND are supplied to the wiring **76** (RS) connected to the gate electrode of the transistor **53** as an "H" potential and an "L" potential, respectively. In addition, VDD and GND are supplied to the wiring **75** (TX) connected to the gate electrode of the transistor **51** as an "H" potential and an "L" potential, respectively. Furthermore, VDD is supplied to the wiring **79** (VDD) connected to the source electrode of the transistor **52**. Other potentials also can be supplied to the wirings.

[0093] First, if the wiring **76** (RS) is set at "H" and the wiring **75** (TX) is set at "H," the potentials of the charge accumulation portion (NR) and the charge accumulation portion (ND) are each set to a reset potential (GND) (that is, reset operation). Note that in reset operation, VDD may be supplied to the wiring **76** (RS) as an "H" potential.

[0094] Next, if the wiring **76** (RS) is set at "L" and the wiring **75** (TX) is set at "L," the potential of the charge accumulation portion (NR) changes (that is, accumulation operation). The potential of the charge accumulation portion (NR) is changed from GND to HVDD at the maximum depending on the intensity of light that enters the photoelectric conversion element **60**.

[0095] If the wiring **75** (TX) is set at "H" subsequent to the accumulation operation, charge in the charge accumulation portion (NR) is transferred to the charge accumulation portion (ND) (that is, transfer operation).

[0096] Although the potential of the charge accumulation portion (NR) is changed depending on the intensity of light that enters the photoelectric conversion element **60** in the accumulation operation, VDD is supplied to the gate electrode of the transistor **51**; thus, when the potential of the charge accumulation portion (ND) reaches VDD, the transistor **51** is turned off. Therefore, the potential of the charge accumulation portion (ND) is changed from the reset potential (GND) to VDD at the maximum. In other words, VDD is applied to the gate electrode of the transistor **52** at the maximum.

[0097] Note that although the wiring **75** (TX) is set at "L" in the accumulation operation in FIG. **6**, the wiring **75** (TX) may be set at "H." In that case, the potential of the charge accumulation portion (ND) is changed in accordance with the potential change of the charge accumulation portion (NR); however, VDD is supplied to the gate electrode of the transistor **51**. Therefore, when the potential of the charge accumulation portion (ND) reaches VDD, the transistor **51** is turned off. Thus, the potential of the charge accumulation portion (ND) is changed from the reset potential (GND) to VDD at the maximum. In other words, also in such a case, VDD is applied to the gate electrode of the transistor **52** at the maximum.

[0098] Note that if the wiring **75** (TX) is set at "L" in the accumulation operation, the influence of noise caused by the transistor **51** can be reduced. In contrast, if the wiring **75** (TX) is set at "H," the influence of noise caused by switching of the transistor **51** can be reduced.

[0099] If the wiring **76** (RS) is set at "L," the wiring **75** (TX) is set at "L," and the wiring **78** (SE) is set at "H" subsequent to the transfer operation, a signal based on the potential of the charge accumulation portion (ND) can be output to the wiring **71** (OUT). In other words, an output signal based on the intensity of light that enters the photoelectric conversion element **60** in the accumulation operation can be obtained.

[0100] In the above operation, the highest voltages applied to the terminals of the transistors are as follows. In some cases, HVDD is applied to the source electrode of the transistor **51**, and VDD is applied to the gate electrode and the drain electrode of the transistor **51**. In some cases, HVDD is applied to the gate electrode and the drain electrode of the transistor **53**, and GND is applied to the source electrode of the transistor **53**. In some cases, VDD is applied to the source electrode, the drain electrode, and the gate electrode of the transistor **52**. In some cases, VDD is applied to the source electrode, the drain electrode, and the gate electrode of the transistor **54**. Therefore, the transistors **51** and **53** need to withstand the high voltage HVDD. In contrast, it is enough for the transistors **52** and **54** to withstand VDD.

[0101] Note that the pixel circuit used for the imaging device in one embodiment of the present invention may have a structure in FIG. **35**. In the pixel circuit in FIG. **35**, one of a source electrode and a drain electrode of a transistor **55** is connected to the charge accumulation portion (ND) in FIG. **1**. The other of the source electrode and the drain electrode of the transistor **55** is connected to a wiring **93** (GND). A gate electrode of the transistor **55** is connected to a wiring **96** (RS). The wiring **93** (GND) can have the same potential as the wiring **73** (GND). The wiring **96** (RS) is a signal line for controlling the transistor **55** and can be supplied with a potential similar to that of the wiring **76** (RS). The wiring **76** (RS) and the wiring **96** (RS) can be supplied with different potentials. Furthermore, the wiring **76** (RS) and the wiring **96** (RS) can be electrically connected to each other.

[0102] In the pixel circuit structure in FIG. **1**, the reset operation of the charge accumulation portion (ND) is performed by turning on the transistors **51** and **53**. However, in the structure in FIG. **35**, the charge accumulation portion (ND) can be reset without operation of the transistor **51**; thus, imaging noise can be reduced.

[0103] In the circuit structure in FIG. **1**, the transistor **54** is provided between the transistor **52** and the wiring **71** (OUT). However, as illustrated in FIG. **36**, the transistor **54** may be provided between the transistor **52** and the wiring **79** (VDD).

[0104] In the circuit structure in FIG. **1**, the other of the source electrode and the drain electrode of the transistor **52** is connected to the high potential power supply line (the wiring **79** (VDD)). However, as illustrated in FIG. **37**A, the other of the source electrode and the drain electrode of the transistor **52** may be connected to a low potential power supply line (a wiring **99** (GND)). As illustrated in FIG. **37**B, the transistor **52** may be replaced with a p-channel transistor.

[0105] As another structure of the pixel circuit in one embodiment of the present invention, the transistor **54** may be omitted as illustrated in FIG. **7**A. As illustrated in FIG. **7**B, a capacitor **57** may be provided for the charge accumulation portion (NR). As illustrated in FIG. **7**C, a capacitor **58** may be provided for the charge accumulation portion (ND). As illustrated in FIG. **7**D, the capacitors **57** and **58** may be provided. Note that any of the structures in FIGS. **7**A to **7**D can be optionally combined with any of the structures in FIG. **35**, FIG. **36**, and FIGS. **37**A and **37**B.

[0106] The transistors **51** and **53** in the pixel circuit may each include a back gate as illustrated in FIGS. **7**E and **7**F. FIG. **7**E illustrates a structure in which a constant potential is applied to the back gates, which enables control of the threshold voltage. FIG. **7**F illustrates a structure in which the back gates are supplied with the same potential as front gates, which enables an increase in on-state current. The transistors **51** to **54** may each include a back gate as illustrated in FIGS. **7**G and **7**H. The circuits in FIG. **1**, FIGS. **7**A to **7**D, FIG. **35**, FIG. **36**, FIGS. **37**A and **37**B can also have transistors having back gates. Moreover, a structure in which the same potential is applied to a front gate and a back gate, a structure in which a constant potential is applied to a back gate, and a structure without a back gate may be optionally combined as necessary for the transistors included in one pixel circuit.

[0107] Note that the pixel circuit may have a structure in which the transistors **52** and **54** are shared among a plurality of pixels as illustrated in FIG. **8**. FIG. **8** illustrates a structure in which the transistors **52** and **54** are shared among a plurality of pixels in a perpendicular direction; however, the transistors **52** and **54** may be shared among a plurality of pixels in a horizontal direction or in a horizontal and perpendicular direction. Such a structure can reduce the number of transistors included in one pixel. As illustrated in FIG. **38**, the charge accumulation portion (ND) may have the reset transistor **55**.

[0108] Although FIG. **8** and FIG. **38** each illustrate a structure in which the transistors **52** and **54** are shared among four pixels, the transistors **52** and **54** may be shared among two pixels, three pixels, or five or more pixels. Note that the structure in FIG. **8** or FIG. **38** can be optionally combined with any of the structures in FIGS. **7**A to **7**H, FIG. **36**, and FIGS. **37**A and **37**B.

[0109] Such a structure can provide an imaging device that includes a highly integrated pixel array. Alternatively, an imaging device that easily performs imaging under a low illuminance condition can be provided.

[0110] Next, specific structure examples of the imaging device in one embodiment of the present invention are described below with reference to drawings. FIG. **9**A is an example of a cross-sectional view of the imaging device in one embodiment of the present invention and illustrates an example of specific connection between the photoelectric conversion element **60** and the transistors **51** and **53** which are included in the pixel in FIG. **1**. Note that FIG. **9**A does not illustrate the transistors **52** and **54**. The imaging device includes a layer **1100** including the transistors **51** to **54** and a layer **1200** including the photoelectric conversion element **60**.

[0111] Although the wirings, the electrodes, and conductors **81** are illustrated as independent components in cross-sectional views in this embodiment, some of them are provided as one component in some cases when they are electrically connected to each other. In addition, a structure in which a gate electrode, a source electrode, or a drain electrode of the transistor is connected to the wirings through the conductor **81** is only an example, and the gate electrode, the source electrode, and the drain electrode of the transistor might each function as a wiring.

[0112] In addition, insulating layers **82** and **83** and the like that function as protective films, interlayer insulating films, or planarization films are provided over the components. For example, an inorganic insulating film such as a silicon oxide film or a silicon oxynitride film can be used as each of the insulating layers **82** and **83** and the like. Alternatively, an organic insulating film such as an acrylic resin film or a polyimide resin film may be used. Top surfaces of the insulating layers **82** and **83** and the like are preferably planarized by chemical mechanical polishing (CMP) or the like as necessary.

[0113] In some cases, one or more of the wirings and the like illustrated in the drawing are not provided or a wiring, a transistor, or the like that is not illustrated in the drawing is included in each layer. In addition, a layer that is not illustrated in the drawing might be included. Furthermore, one or more of the layers illustrated in the drawing are not included in some cases.

[0114] It is particularly preferable to use OS transistors as the transistors **51** and **53**.

[0115] Extremely low off-state current of the OS transistor can widen the dynamic range of imaging. In the circuit structure of the pixel illustrated in FIG. **1**, a decrease in the intensity of light entering the photoelectric conversion element **60** reduces the potential of the charge accumulation portion (ND). Since the OS transistor has extremely low off-state current, current based on a gate potential can be accurately output even when the gate potential is extremely low. Thus, it is possible to widen the detection range of illuminance, i.e., the dynamic range.

[0116] A period during which charge can be held in the charge accumulation portion (ND) and the charge accumulation portion (NR) can be extremely long owing to the low off-state current of the transistors **51** and **53**. Therefore, a global shutter system in which accumulation operation is performed in all the pixels at the same time can be used without a complicated circuit structure and operation method.

[0117] In general, in an imaging device where pixels are arranged in a matrix, a rolling shutter system is employed in which imaging operation **11**, retention operation **12**, and read operation **13** are performed row by row as illustrated in FIG. **10**A. In the case of employing the rolling shutter system, simultaneousness of imaging is lost. Therefore, when an object moves, an image is distorted.

[0118] As a result, in one embodiment of the present invention, it is preferable to employ a global shutter system in which the imaging operation **11** can be performed simultaneously in all the rows and the read operation **13** can be sequentially performed row by row as illustrated in FIG. **10**B. By employing the global shutter system, simultaneousness of imaging in all the pixels in the imaging device can be secured, and an image with little distortion can be easily formed even when an object moves.

[0119] In addition, the OS transistor has lower temperature dependence of change in electrical characteristics than a Si transistor, and thus can be used in an extremely wide range of temperatures. Therefore, an imaging device and a semiconductor device that include the OS transistors are suitable for automobiles, aircrafts, and spacecrafts.

[0120] Moreover, the OS transistor has higher drain breakdown voltage than the Si transistor. In a photoelectric conversion element in which a selenium-based material is used for a photoelectric conversion layer, comparatively high voltage (e.g., 10 V or higher) is preferably applied to cause an avalanche phenomenon easily. Therefore, by combination of the OS transistor and the photoelectric conversion element in which the selenium-based material is used for the photoelectric conversion layer, a highly reliable imaging device can be obtained.

[0121] Note that although each transistor includes a back gate in FIG. **9**A, as illustrated in FIG. **9**B, each transistor does not necessarily include a back gate. Alternatively, as illustrated in FIG. **9**C, one or more transistors, for example, only the transistor **51** may include a back gate. The back gate might be electrically connected to a corresponding front gate of the transistor. Alternatively, different fixed potentials might be supplied to the back gate and the front gate. Note that the presence or absence of the back gate can also be applied to another imaging device described in this embodiment.

[0122] A variety of elements can be used as the photoelectric conversion element **60** provided in the layer **1200**. FIG. **9**A illustrates the photoelectric conversion element **60** including a selenium-based material for a photoelectric conversion layer **61**. The photoelectric conversion element **60** including a selenium-based material has high external quantum efficiency with respect to visible light. In the photoelectric conversion element, a highly sensitive sensor in which the amount of amplification of electrons with respect to the amount of incident light by an avalanche phenomenon is large can be obtained. Furthermore, the selenium-based material has a high light absorption coefficient, which leads to an advantage that the photoelectric conversion layer **61** is easily formed to be thin.

[0123] Amorphous selenium or crystalline selenium can be used as a selenium-based material. Crystalline selenium can be obtained by, for example, depositing amorphous selenium and then performing heat treatment. When the crystal grain size of crystalline selenium is smaller than a pixel pitch, variation in characteristics between pixels can be reduced. Moreover, crystalline selenium has higher spectral sensitivity and light-absorption coefficient than those of amorphous selenium.

[0124] Furthermore, the photoelectric conversion layer **61** may be a layer including a compound of copper, indium, and selenium (CIS). Alternatively, a layer including a compound of copper, indium, gallium, and selenium (CIGS) may be used. With the CIS layer or the CIGS layer, a photoelectric conversion element that can utilize an avalanche phenomenon in a manner similar to that of a single layer of selenium can be formed.

[0125] In the photoelectric conversion element **60** including a selenium-based material, for example, the photoelectric conversion layer **61** can be provided between a light-transmitting conductive layer **62** and the electrode **66** formed using a metal material or the like. CIS and CIGS are p-type semiconductors and may be formed in contact with an n-type semiconductor such as cadmium sulfide or zinc sulfide to form a j unction.

[0126] Comparatively high voltage (e.g., 10 V or higher) is preferably applied to the photoelectric conversion element to cause the avalanche phenomenon. Since the OS transistor has higher drain breakdown voltage than the Si transistor, comparatively high voltage can be easily applied to the photoelectric conversion element. Therefore, by combination of the OS transistor with high drain breakdown voltage and the photoelectric conversion element in which the selenium-based material is used for the photoelectric conversion layer, a highly sensitive, highly reliable imaging device can be obtained.

[0127] Although the photoelectric conversion layer **61** and the light-transmitting conductive layer **62** are not divided between pixel circuits in FIG. **9**A, the photoelectric conversion layer **61** and the light-transmitting conductive layer **62** may be divided between circuits as illustrated in FIG. **11**A. Furthermore, a partition wall **67** formed using an insulator is preferably provided in a region between pixels where the electrode **66** is not provided so as not to generate a crack in the photoelectric conversion layer **61** and the light-transmitting conductive layer **62**; however, the partition wall **67** is not necessarily provided as illustrated in FIG. **11**B. Although the light-transmitting conductive layer **62** and the wiring **72** are connected to each other through a wiring **88** and the conductor **81** in FIG. **9**A, the light-transmitting conductive layer **62** and the wiring **72** may be in direct contact with each other as in FIGS. **11**C and **11**D.

[0128] The electrode **66**, the wiring **72**, and the like may each be a multilayer. For example, as illustrated in FIG. **12**A, the electrode **66** can include two conductive layers **66***a* and **66***b* and the wiring **72** can include two conductive layers **72***a* and **72***b*. In the structure of FIG. **12**A, for example, the conductive layers **66***a* and **72***a* may be made of a low-resistance metal or the like, and the conductive layers **66***b* and **72***b* may be made of a metal or the like that exhibits an excellent contact property with the photoelectric conversion layer **61**. Such a structure improves the electrical properties of the photoelectric conversion element. Furthermore, even when the conductive layer **72***a* contains a metal that causes electrolytic corrosion, which occurs when some kinds of metal are in contact with the light-transmitting conductive layer **62**, electrolytic corrosion can be prevented because the conductive layer **72***b* is placed between the conductive layer **72***a* and the light-transmitting conductive layer **62**.

[0129] The conductive layers **66***b* and **72***b* can be formed using, for example, molybdenum, tungsten, or the like. The conductive layers **66***a* and **72***a* can be formed using, for example, aluminum, titanium, or a stack of titanium, aluminum, and titanium that are layered in that order.

[0130] The insulating layer **82** and the like may each be a multilayer. For example, as illustrated in FIG. **12**B, the conductor **81** has a difference in level in the case where the insulating layer **82** includes insulating layers **82***a* and **82***b* that have different etching rates. In the case where another insulating layer used as an interlayer insulating film or a planarization film is a multilayer, the conductor **81** also has a difference in level. Although the insulating layer **82** is formed using two layers here, the insulating layer **82** and another insulating layer may each be formed using three or more layers.

[0131] Note that the partition wall **67** can be formed using an inorganic insulator, an insulating organic resin, or the like. The partition wall **67** may be colored black or the like in order to shield the transistors and the like from light and/or to determine the area of a light-receiving portion in each pixel.

[0132] Alternatively, a PIN diode element or the like formed using an amorphous silicon film, a microcrystalline silicon film, or the like may be used as the photoelectric conversion element **60**.

[0133] FIG. **13** illustrates an example in which a thin film PIN photodiode is used as the photoelectric conversion element **60**. In the photodiode, a p-type semiconductor layer **65**, an i-type semiconductor layer **64**, and an n-type semiconductor layer **63** are stacked in that order. The i-type semiconductor layer **64** is preferably formed using amorphous silicon. The n-type semiconductor layer **63** and the p-type semiconductor layer **65** can each be formed using amorphous silicon, microcrystalline silicon, or the like that includes a dopant imparting the corresponding conductivity type. A photodiode in which a photoelectric conversion layer is formed using amorphous silicon has high sensitivity in a visible light wavelength region, and therefore can easily sense weak visible light.

[0134] In the photoelectric conversion element **60** in FIG. **13**, the p-type semiconductor layer **65** is electrically connected to the electrode **66** that is electrically connected to the transistors **51** and **53**. Furthermore, the n-type semiconductor layer **63** is electrically connected to the wiring **72** through the conductor **81**.

[0135] Furthermore, any of examples illustrated in FIGS. **14**A to **14**F may be applied to the structure of the photoelectric conversion element **60** having a configuration of a PIN thin film photodiode and the connection between the photoelectric conversion element **60** and the wirings. Note that the structure of the photoelectric conversion element **60** and the connection between the photoelectric conversion element **60** and the wirings are not limited thereto, and other configurations may be applied.

[0136] FIG. **14**A illustrates a structure provided with the light-transmitting conductive layer **62** in contact with the n-type semiconductor layer **63** of the photoelectric conversion element **60**. The light-transmitting conductive layer **62** functions as an electrode and can increase the output current of the photoelectric conversion element **60**.

[0137] For the light-transmitting conductive layer **62**, the following can be used: indium tin oxide; indium tin oxide containing silicon; indium oxide containing zinc; zinc oxide; zinc oxide containing gallium; zinc oxide containing aluminum; tin oxide; tin oxide containing fluorine; tin oxide containing antimony; graphene; or the like. The light-transmitting conductive layer **62** is not limited to a single layer, and may be a stacked layer of different films.

[0138] FIG. **14**B illustrates a structure in which the n-type semiconductor layer **63** of the photoelectric conversion element **60** is directly connected to the wiring **88**.

[0139] FIG. **14**C illustrates a structure in which the light-transmitting conductive layer **62** in contact with the n-type semiconductor layer **63** of the photoelectric conversion element **60** is provided, and the wiring **88** is electrically connected to the light-transmitting conductive layer **62**.

[0140] FIG. **14**D illustrates a structure in which an opening portion exposing the n-type semiconductor layer **63** is provided in an insulating layer covering the photoelectric conversion element **60**, and the light-transmitting conductive layer **62** that covers the opening portion is electrically connected to the wiring **88**.

[0141] FIG. **14**E illustrates a structure provided with the conductor **81** that penetrates the photoelectric conversion element **60**. In the structure, the wiring **72** is electrically connected to the n-type semiconductor layer **63** through the conductor **81**. Note that in the drawing, the wiring **72** appears to be electrically connected to the electrode **66** through the p-type semiconductor layer **65**. However, resistance in the lateral direction of the p-type semiconductor layer **65** is high; therefore, when an appropriate distance is provided between the wiring **72** and the electrode **66**, the resistance between the wiring **72** and the electrode **66** is extremely high. Thus, the photoelectric conversion element **60** can have diode characteristics without a short circuit between the anode and the cathode. Note that two or more conductors **81** that are electrically connected to the n-type semiconductor layer **63** may be provided.

[0142] FIG. **14**F illustrates a structure in which the photoelectric conversion element **60** in FIG. **14**E is provided with the light-transmitting conductive layer **62** in contact with the n-type semiconductor layer **63**.

[0143] Note that each of the photoelectric conversion elements **60** in FIGS. **14**D to **14**F has an advantage of having a large light-receiving area because wirings and the like do not overlap with a light-receiving region.

[0144] Alternatively, as illustrated in FIG. **15**, the photoelectric conversion element **60** can be a photodiode including a silicon substrate **30** as a photoelectric conversion layer.

[0145] The photoelectric conversion element **60** formed using the selenium-based material, amorphous silicon, or the like can be formed through general semiconductor manufacturing processes such as a deposition process, a lithography process, and an etching process. Furthermore, the resistance of the selenium-based material is high; thus, a structure in which the photoelectric conversion layer **61** is not divided between the circuits can be employed as illustrated in FIG. **9**A. Therefore, the imaging device in one embodiment of the present invention can be manufactured with a high yield at low cost. Meanwhile, to form a photodiode including the silicon substrate **30** as the photoelectric conversion layer, processes with high difficulty, such as a polishing process and a bonding process, are needed.

[0146] Furthermore, the imaging device in one embodiment of the present invention may be stacked over the silicon substrate **30** including circuits. For example, as illustrated in FIG. **16**A, the pixel circuit may overlap with a layer **1400** that includes transistors **31** and **32** whose active regions are formed in the silicon substrate **30**.

[0147] The circuit formed in the silicon substrate **30** is capable of reading a signal output from the pixel circuit and converting the signal; for example, the circuit can include a CMOS inverter as illustrated in the circuit diagram in FIG. **16**B. A gate electrode of the transistor **31** (n-channel transistor) is electrically connected to a gate electrode of the transistor **32** (p-channel transistor). One of a source electrode and a drain electrode of one transistor is electrically connected to one of a source electrode and a drain electrode of the other transistor. The other of the source electrode and the drain electrode of the one transistor is electrically connected to a wiring, and the other of the source electrode and the drain electrode of the other transistor is electrically connected to another wiring.

[0148] Furthermore, the silicon substrate **30** is not limited to a bulk silicon substrate and can be a substrate made of germanium, silicon germanium, silicon carbide, gallium arsenide, aluminum gallium arsenide, indium phosphide, gallium nitride, or an organic semiconductor.

[0149] As illustrated in FIG. **16**C, the transistors **31** and **32** may each be a transistor including an active layer **35** formed using a silicon thin film. The active layer **35** can be formed using polycrystalline silicon or single crystal silicon of a silicon-on-insulator (SOI) structure.

[0150] Here, as illustrated in FIG. **15** and FIG. **16**A, an insulating layer **80** is provided between a region including an oxide semiconductor transistor and a region including a Si transistor (a Si photodiode in FIG. **15**).

[0151] Dangling bonds of silicon are terminated with hydrogen in insulating layers provided in the vicinities of the active regions of the transistors **31** and **32**. Therefore, hydrogen has an effect of improving the reliability of the transistors **31** and **32**. Meanwhile, hydrogen in insulating layers which are provided in the vicinity of the oxide semiconductor layer that is the active layer of the transistor **51** or the like causes generation of carriers in the oxide semiconductor layer. Therefore, hydrogen might reduce the reliability of the transistor **51** or the like. Consequently, in the case where one layer including the transistor formed using a silicon-based semiconductor material and the other layer including the OS transistor are stacked, it is preferable that the insulating layer **80** having a function of preventing diffusion of hydrogen be provided between the layers. Hydrogen is confined in the one layer by the insulating layer **80**, so that the reliability of the transistors **31** and **32** can be improved. Furthermore, diffusion of hydrogen from the one layer to the other layer is inhibited, so that the reliability of the transistor **51** or the like can also be improved.

[0152] The insulating layer **80** can be, for example, formed using aluminum oxide, aluminum oxynitride, gallium oxide, gallium oxynitride, yttrium oxide, yttrium oxynitride, hafnium oxide, hafnium oxynitride, or yttria-stabilized zirconia (YSZ).

[0153] Note that as illustrated in FIG. **16**A, a circuit (e.g., a driver circuit) formed using the silicon substrate **30**, the transistor **51** or the like, and the photoelectric conversion element **60** can overlap with each other; thus, the integration degree of pixels can be increased. In other words, the resolution of the imaging device can be increased. For example, the imaging device is suitable for an imaging device whose number of pixels is 4K2K, 8K4K, 16K8K, or the like. Note that the transistor **52**, the transistor **54**, and the like included in the pixel circuit may have a region that overlaps with the transistor **51** or the like and the photoelectric conversion element **60**.

[0154] In the imaging device in FIG. **16**A, no photoelectric conversion element is provided on the silicon substrate **30**. Therefore, an optical path for the photoelectric conversion element **60** can be secured without being influenced by the transistors or wirings, and a pixel with a high aperture ratio can be formed.

[0155] The imaging device in one embodiment of the present invention can have a structure in FIG. **17**.

[0156] The imaging device in FIG. **17** is a modification example of the imaging device in FIG. **16**A. A CMOS inverter is formed using an OS transistor and a Si transistor.

[0157] Here, the transistor **32** is a p-channel Si transistor provided in the layer **1400**, and the transistor **31** is an n-channel OS transistor provided in the layer **1100**. When only the p-channel transistor is provided on the silicon substrate **30**, a step of forming a well, an n-type impurity layer, or the like can be skipped.

[0158] Although selenium is used for the photoelectric conversion element **60** in the imaging device in FIG. **17**, a PIN thin film photodiode may be used as in FIG. **13**.

[0159] In the imaging device in FIG. **17**, the transistor **31** can be formed in the same process as the transistors **51** and **53** formed in the layer **1100**. Thus, the manufacturing process of the imaging device can be simplified.

[0160] Note that the structure of the transistor and the photoelectric conversion element included in each of the imaging devices described in this embodiment is only an example. Therefore, for example, one or more of the transistors **51** to **54** can be formed using a transistor in which an active region or an active layer includes silicon or the like. Furthermore, either one or both the transistors **31** and **32** can be formed using a transistor including an oxide semiconductor layer as an active layer.

[0161] FIG. **18**A is a cross-sectional view of an example of a mode in which a color filter and the like are added to the imaging device. The cross-sectional view illustrates part of a region including pixel circuits for three pixels. An insulating layer **2500** is formed over the layer **1200** where the photoelectric conversion element **60** is formed. As the insulating layer **2500**, for example, a silicon oxide film with a high visible-light transmitting property can be used. In addition, a silicon nitride film may be stacked as a passivation film. Furthermore, a dielectric film of hafnium oxide or the like may be stacked as an anti-reflection film.

[0162] A light-blocking layer **2510** may be formed over the insulating layer **2500**. The light-blocking layer **2510** has a function of inhibiting color mixing of light passing through the color filter. The light-blocking layer **2510** can be formed using a metal layer of aluminum, tungsten, or the like, or a stack including the metal layer and a dielectric film functioning as an anti-reflection film.

[0163] An organic resin layer **2520** can be formed as a planarization film over the insulating layer **2500** and the light-blocking layer **2510**. A color filter **2530** is formed in each pixel. For example, a color filter **2530***a*, a color filter **2530***b*, and a color filter **2530***c* each have a color of red (R), green (G), blue (B), yellow (Y), cyan (C), magenta (M), or the like, so that a color image can be obtained.

[0164] A light-transmitting insulating layer **2560** or the like can be provided over the color filter **2530**.

[0165] As illustrated in FIG. **18**B, an optical conversion layer **2550** may be used instead of the color filter **2530**. Such a structure enables the imaging device to capture images in various wavelength regions.

[0166] For example, when a filter that blocks light having a wavelength shorter than or equal to that of visible light is used as the optical conversion layer **2550**, an infrared imaging device can be obtained. When a filter that blocks light having a wavelength shorter than or equal to that of near infrared light is used as the optical conversion layer **2550**, a far infrared imaging device can be obtained. When a filter that blocks light having a wavelength longer than or equal to that of visible light is used as the optical conversion layer **2550**, an ultraviolet imaging device can be obtained.

[0167] Furthermore, when a scintillator is used as the optical conversion layer **2550**, an imaging device that captures an image visualizing the intensity of radiation and is used for an X-ray imaging device, for example, can be obtained. Radiation such as X-rays passes through an object to enter a scintillator, and then is converted into light (fluorescence) such as visible light or ultraviolet light owing to a phenomenon known as photoluminescence. Then, the photoelectric conversion element **60** detects the light to obtain image data. Furthermore, the imaging device having the structure may be used in a radiation detector or the like.

[0168] A scintillator contains a substance that, when irradiated with radiation such as X-rays or gamma-rays, absorbs energy of the radiation to emit visible light or ultraviolet light. For example, a resin or ceramics in which any of Gd_2O_2S:Tb, Gd_2O_2S:Pr, Gd_2O_2S:Eu, BaFCl:Eu, NaI, CsI, CaF_2, BaF_2, CeF_3, LiF, LiI, and ZnO is dispersed can be used.

[0169] In the photoelectric conversion element **60** including a selenium-based material, radiation such as X-rays can be directly converted into charge; thus, the scintillator is not necessarily used.

[0170] A microlens array **2540** may be provided over the color filters **2530***a*, **2530***b*, and **2530***c*. Light penetrating lenses included in the microlens array **2540** goes through the color filters positioned thereunder to reach the photoelectric conversion element **60**. Note that a region other than the layer **1200** in FIGS. **18**A to **18**C is referred to as a layer **1600**.

[0171] The specific structure of the imaging device in FIG. **18**C is illustrated in FIG. **19** by taking an example of the imaging device in FIG. **9**A. In addition, the specific structure of the imaging device in FIG. **18**C is illustrated in FIG. **20** by taking an example of the imaging device in FIG. **15**.

[0172] The imaging device in one embodiment of the present invention may be combined with a diffraction grating **1500** as illustrated in FIG. **21** and FIG. **22**. An image of an object through the diffraction grating **1500** (i.e., a diffraction pattern) can be scanned into a pixel, and an input image (an object image) can be formed from a captured image in the pixel by arithmetic processing. In addition, the use of the diffraction grating **1500** instead of a lens can reduce the cost of the imaging device.

[0173] The diffraction grating **1500** can be formed using a light-transmitting material. An inorganic insulating film such as a silicon oxide film or a silicon oxynitride film can be used, for example. Alternatively, an organic insulating film such as an acrylic resin film or a polyimide resin film may be used. Alternatively, a stack of the inorganic insulating film and the organic insulating film may be used.

[0174] In addition, the diffraction grating **1500** can be formed by a lithography process using a photosensitive resin or the like. Alternatively, the diffraction grating **1500** can be formed by a lithography process and an etching process. Alternatively, the diffraction grating **1500** can be formed by nanoimprint lithography, laser scribing, or the like.

[0175] Note that a space X may be provided between the diffraction grating **1500** and the microlens array **2540**. The space X can be less than or equal to 1 mm, preferably less than or equal to 100 μm. The space may be an empty space or may be a sealing layer or an adhesion layer formed using a light-transmitting material. For example, an inert gas such as nitrogen or a rare gas can be sealed in the space. Alternatively, an acrylic resin, an epoxy resin, a polyimide resin, or the like may be provided in the space. Alternatively, a liquid such as silicone oil may be provided. Even in the case where the microlens array **2540** is not provided, the space X may be provided between the color filter **2530** and the diffraction grating **1500**.

[0176] As illustrated in FIGS. **23A1** and **23B1**, the imaging device may be bent. FIG. **23A1** illustrates a state in which the imaging device is bent in the direction of dashed-two dotted line **X1-X2**. FIG. **23A2** is a cross-sectional view illustrating a portion indicated by dashed-two dotted line **X1-X2** in FIG. **23A1**. FIG. **23A3** is a cross-sectional view illustrating a portion indicated by dashed-two dotted line **Y1-Y2** in FIG. **23A1**.

[0177] FIG. **23B1** illustrates a state where the imaging device is bent in the direction of dashed-two dotted line **X3-X4** and the direction of dashed-two dotted line **Y3-Y4**. FIG. **23B2** is a cross-sectional view illustrating a portion indicated by dashed-two dotted line **X3-X4** in FIG. **23B1**. FIG. **23B3** is a cross-sectional view illustrating a portion indicated by dashed-two dotted line **Y3-Y4** in FIG. **23B1**.

[0178] Bending the imaging device can reduce field curvature and astigmatism. Thus, the optical design of the lens and the like, which are used in combination of the imaging device, can be facilitated. For example, the number of lenses used for aberration correction can be reduced; accordingly, the size or weight of semiconductor devices including the imaging device can be easily reduced. In addition, the quality of captured images can be improved.

[0179] In this embodiment, one embodiment of the present invention has been described. Other embodiments of the present invention are described in the other embodiments. Note that one embodiment of the present invention is not limited thereto. In other words, various embodiments of the invention are described in this embodiment and the other embodiments, and one embodiment of the present invention is not limited to a particular embodiment. Although an example in which one embodiment of the present invention is applied to an imaging device is described, one embodiment of the present invention is not limited thereto. Depending on circumstances or conditions, one embodiment of the present invention is not necessarily applied to an imaging device. One embodiment of the present invention may be applied to a semiconductor device with another function, for example. Although an example in which a channel formation region, a source region, a drain region, or the like of a transistor includes an oxide semiconductor is described as one embodiment of the present invention, one embodiment of the present invention is not limited thereto. Depending on circumstances or conditions, various transistors or a channel formation region, a source region, a drain region, or the like of a transistor in one embodiment of the present invention may include various semiconductors. Depending on circumstances or conditions, various transistors or a channel formation region, a source region, a drain region, or the like of a transistor in one embodiment of the present invention may include, for example, at least one of silicon, germanium, silicon germanium, silicon carbide, gallium arsenide, aluminum gallium arsenide, indium phosphide, gallium nitride, and an organic semiconductor. Alternatively, for example, depending on circumstances or conditions, various transistors or a channel formation region, a source region, a drain region, or the like of a transistor in one embodiment of the present invention does not necessarily include an oxide semiconductor. For example, depending on circumstances or conditions, either one or both the transistors **51** and **53** do not necessarily include an oxide semiconductor in the active layer.

[0180] This embodiment can be combined with any of the structures described in the other embodiments as appropriate.

Embodiment 2

[0181] In this embodiment, a transistor including an oxide semiconductor that can be used in one embodiment of the present invention is described with reference to drawings. In the drawings in this embodiment, some components are enlarged, reduced in size, or omitted for easy understanding.

[0182] FIGS. **24**A and **24**B are a top view and a cross-sectional view illustrating a transistor **101** in one embodiment of the present invention. FIG. **24**A is a top view, and a cross section in the direction of dashed-dotted line B**1**-B**2** in FIG. **24**A is illustrated in FIG. **24**B. A cross section in the direction of dashed-dotted line B**3**-B**4** in FIG. **24**A is illustrated in FIG. **26**A. The direction of dashed-dotted line B**1**-B**2** is referred to as a channel length direction, and the direction of dashed-dotted line B**3**-B**4** is referred to as a channel width direction.

[0183] The transistor **101** includes an insulating layer **120** in contact with a substrate **115**; an oxide semiconductor layer **130** in contact with the insulating layer **120**; conductive layers **140** and **150** electrically connected to the oxide semiconductor layer **130**; an insulating layer **160** in contact with the oxide semiconductor layer **130** and the conductive layers **140** and **150**; a conductive layer **170** in contact with the insulating layer **160**; an insulating layer **175** in contact with the conductive layers **140** and **150**, the insulating layer **160**, and the conductive layer **170**; and an insulating layer **180** in contact with the insulating layer **175**. The insulating layer **180** may function as a planarization film as necessary.

[0184] The conductive layer **140**, the conductive layer **150**, the insulating layer **160**, and the conductive layer **170** can function as a source electrode layer, a drain electrode layer, a gate insulating film, and a gate electrode layer, respectively.

[0185] A region **231**, a region **232**, and a region **233** in FIG. **24**B can function as a source region, a drain region, and a channel formation region, respectively. The region **231** and the region **232** are in contact with the conductive layer **140** and the conductive layer **150**, respectively. When a conductive material that is easily bonded to oxygen is used for the conductive layers **140** and **150**, the resistance of the regions **231** and **232** can be reduced.

[0186] Specifically, since the oxide semiconductor layer **130** is in contact with the conductive layers **140** and **150**, an oxygen vacancy is generated in the oxide semiconductor layer **130**, and interaction between the oxygen vacancy and hydrogen that remains in the oxide semiconductor layer **130** or diffuses into the oxide semiconductor layer **130** from the outside changes the regions **231** and **232** to n-type regions with low resistance.

[0187] Note that functions of a "source" and a "drain" of a transistor are sometimes interchanged with each other when a transistor of an opposite conductivity type is used or when the direction of current flow is changed in circuit operation, for example. Therefore, the terms "source" and "drain" can be interchanged with each other in this specification. In addition, the term "electrode layer" can be changed into the term "wiring".

[0188] The conductive layer **170** includes two layers, conductive layers **171** and **172**, but also may be a single layer or a stack of three or more layers. The same applies to other transistors described in this embodiment.

[0189] Each of the conductive layers **140** and **150** is a single layer, but also may be a stack of two or more layers. The same applies to other transistors described in this embodiment.

[0190] The transistor in one embodiment of the present invention may have a structure illustrated in FIGS. **24**C and **24**D. FIG. **24**C is a top view of a transistor **102**. A cross section in the direction of dashed-dotted line C**1**-C**2** in FIG. **24**C is illustrated in FIG. **24**D. A cross section in the direction of dashed-dotted line C**3**-C**4** in FIG. **24**C is illustrated in FIG. **26**B. The direction of dashed-dotted line C**1**-C**2** is referred to as a channel length direction, and the direction of dashed-dotted line C**3**-C**4** is referred to as a channel width direction.

[0191] The transistor **102** has the same structure as the transistor **101** except that an end portion of the insulating layer **160** functioning as a gate insulating film is not aligned with an end portion of the conductive layer **170** functioning as a gate electrode layer. In the transistor **102**, wide areas of the conductive layers **140** and **150** are covered with the insulating layer **160** and accordingly the resistance between the conductive layer **170** and the conductive layers **140** and **150** is high; therefore, the transistor **102** has low gate leakage current.

[0192] The transistors **101** and **102** each have a top-gate structure including a region where the conductive layer **170** overlaps with the conductive layers **140** and **150**. To reduce parasitic capacitance, the width of the region in the channel length direction is preferably greater than or equal to 3 nm and less than 300 nm. Since an offset region is not formed in the oxide semiconductor layer **130** in this structure, a transistor with high on-state current can be easily formed.

[0193] The transistor in one embodiment of the present invention may have a structure illustrated in FIGS. **24**E and **24**F. FIG. **24**E is a top view of a transistor **103**. A cross section in the direction of dashed-dotted line D**1**-D**2** in FIG. **24**E is illustrated in FIG. **24**F. A cross section in the direction of dashed-dotted line D**3**-D**4** in FIG. **24**E is illustrated in FIG. **26**A. The direction of dashed-dotted line D**1**-D**2** is referred to as a channel length direction, and the direction of dashed-dotted line D**3**-D**4** is referred to as a channel width direction.

[0194] The transistor **103** includes the insulating layer **120** in contact with the substrate **115**; the oxide semiconductor layer **130** in contact with the insulating layer **120**; the insulating layer **160** in contact with the oxide semiconductor layer **130**; the conductive layer **170** in contact with the insulating layer **160**; the insulating layer **175** covering the oxide semiconductor layer **130**, the insulating layer **160**, and the conductive layer **170**; the insulating layer **180** in contact with the insulating layer **175**; and the conductive layers **140** and **150** electrically connected to the oxide semiconductor layer **130** through openings provided in the insulating layers **175** and **180**. The transistor **103** may further include, for example, an insulating layer (planarization film) in contact with the insulating layer **180** and the conductive layers **140** and **150** as necessary.

[0195] The conductive layer **140**, the conductive layer **150**, the insulating layer **160**, and the conductive layer **170** can function as a source electrode layer, a drain electrode layer, a gate insulating film, and a gate electrode layer, respectively.

[0196] The region **231**, the region **232**, and the region **233** in FIG. **24**F can function as a source region, a drain region, and a channel formation region, respectively. The regions **231** and **232** are in contact with the insulating layer **175**. When an insulating material containing hydrogen is used for the insulating layer **175**, for example, the resistance of the regions **231** and **232** can be reduced.

[0197] Specifically, interaction between an oxygen vacancy generated in the regions **231** and **232** by the steps up to formation of the insulating layer **175** and hydrogen that diffuses into the regions **231** and **232** from the insulating layer **175** changes the regions **231** and **232** to n-type regions with low resistance. As the insulating material containing hydrogen, for example, silicon nitride, aluminum nitride, or the like can be used.

[0198] The transistor in one embodiment of the present invention may have a structure illustrated in FIGS. **25**A and **25**B. FIG. **25**A is a top view of a transistor **104**. A cross section in the direction of dashed-dotted line E**1**-E**2** in FIG. **25**A is illustrated in FIG. **25**B. A cross section in the direction of dashed-dotted line E**3**-E**4** in FIG. **25**A is illustrated in FIG. **26**A. The direction of dashed-dotted line E**1**-E**2** is referred to as a channel length direction, and the direction of dashed-dotted line E**3**-E**4** is referred to as a channel width direction.

[0199] The transistor **104** has the same structure as the transistor **103** except that the conductive layers **140** and **150** in contact with the oxide semiconductor layer **130** cover end portions of the oxide semiconductor layer **130**.

[0200] In FIG. **25**B, regions **331** and **334** can function as a source region, regions **332** and **335** can function as a drain region, and a region **333** can function as a channel formation region.

[0201] The resistance of the regions **331** and **332** can be reduced in a manner similar to that of the regions **231** and **232** in the transistor **101**.

[0202] The resistance of the regions **334** and **335** can be reduced in a manner similar to that of the regions **231** and **232** in the transistor **103**. In the case where the length of the regions **334** and **335** in the channel length direction is less than or equal to 100 nm, preferably less than or equal to 50 nm, a gate electric field prevents a significant decrease in on-state current. Therefore, a reduction in resistance of the regions **334** and **335** is not performed in some cases.

[0203] The transistors **103** and **104** each have a self-aligned structure that does not include a region where the conductive layer **170** overlaps with the conductive layers **140** and **150**. A transistor with a self-aligned structure, which has extremely low parasitic capacitance between a gate electrode layer and source and drain electrode layers, is suitable for applications that require high-speed operation.

[0204] The transistor in one embodiment of the present invention may have a structure illustrated in FIGS. **25**C and **25**D. FIG. **25**C is a top view of a transistor **105**. A cross section in the direction of dashed-dotted line F**1**-F**2** in FIG. **25**C is illustrated in FIG. **25**D. A cross section in the direction of dashed-dotted line F**3**-F**4** in FIG. **25**C is illustrated in FIG. **26**A. The direction of dashed-dotted line F**1**-F**2** is referred to as a channel length direction, and the direction of dashed-dotted line F**3**-F**4** is referred to as a channel width direction.

[0205] The transistor **105** includes the insulating layer **120** in contact with the substrate **115**; the oxide semiconductor layer **130** in contact with the insulating layer **120**; conductive layers **141** and **151** electrically connected to the oxide semiconductor layer **130**; the insulating layer **160** in contact with the oxide semiconductor layer **130** and the conductive layers **141** and **151**; the conductive layer **170** in contact with the insulating layer **160**; the insulating layer **175** in contact with the oxide semiconductor layer **130**, the conductive layers **141** and **151**, the insulating layer **160**, and the conductive layer **170**; the insulating layer **180** in contact with the insulating layer **175**; and conductive layers **142** and **152** electrically connected to the conductive layers **141** and **151**, respectively, through openings provided in the insulating layers **175** and **180**. The transistor **105** may further include, for example, an insulating layer in contact with the insulating layer **180** and the conductive layers **142** and **152** as necessary.

[0206] Here, the conductive layers **141** and **151** are in contact with the top surface of the oxide semiconductor layer **130** and are not in contact with side surfaces of the oxide semiconductor layer **130**.

[0207] The transistor **105** has the same structure as the transistor **101** except that the conductive layers **141** and **151** are provided, that openings are provided in the insulating layers **175** and **180**, and that the conductive layers **142** and **152** electrically connected to the conductive layers **141** and **151**, respectively, through the openings are provided. The conductive layer **140** (the conductive layers **141** and **142**) can function as a source electrode layer, and the conductive layer **150** (the conductive layers **151** and **152**) can function as a drain electrode layer.

[0208] The transistor in one embodiment of the present invention may have a structure illustrated in FIGS. **25**E and **25**F. FIG. **25**E is a top view of a transistor **106**. A cross section in the direction of dashed-dotted line G**1**-G**2** in FIG. **25**E is illustrated in FIG. **25**F. A cross section in the direction of dashed-dotted line G**3**-G**4** in FIG. **25**E is illustrated in FIG. **26**A. The direction of dashed-dotted line G**1**-G**2** is referred to as a channel length direction, and the direction of dashed-dotted line G**3**-G**4** is referred to as a channel width direction.

[0209] The transistor **106** includes the insulating layer **120** in contact with the substrate **115**; the oxide semiconductor layer **130** in contact with the insulating layer **120**; the conductive layers **141** and **151** electrically connected to the oxide semiconductor layer **130**; the insulating layer **160** in contact with the oxide semiconductor layer **130**; the conductive layer **170** in contact with the insulating layer **160**; the insulating layer **175** in contact with the insulating layer **120**, the oxide semiconductor layer **130**, the conductive layers **141** and **151**, the insulating layer **160**, and the conductive layer **170**; the insulating layer **180** in contact with the insulating layer **175**; and the conductive layers **142** and **152** electrically connected to the conductive layers **141** and **151**, respectively, through openings provided in the insulating layers **175** and **180**. The transistor **106** may further include, for example, an insulating layer (planarization film) in contact with the insulating layer **180** and the conductive layers **142** and **152** as necessary.

[0210] The conductive layers **141** and **151** are in contact with the top surface of the oxide semiconductor layer **130** and are not in contact with side surfaces of the oxide semiconductor layer **130**.

[0211] The transistor **106** has the same structure as the transistor **103** except that the conductive layers **141** and **151** are provided. The conductive layer **140** (the conductive layers **141** and **142**) can function as a source electrode layer, and the conductive layer **150** (the conductive layers **151** and **152**) can function as a drain electrode layer.

[0212] In the structures of the transistors **105** and **106**, the conductive layers **140** and **150** are not in contact with the insulating layer **120**. These structures make the insulating layer **120** less likely to be deprived of oxygen by the conductive layers **140** and **150** and facilitate oxygen supply from the insulating layer **120** to the oxide semiconductor layer **130**.

[0213] An impurity for forming an oxygen vacancy to increase conductivity may be added to the regions **231** and **232** in the transistor **103** and the regions **334** and **335** in the transistors **104** and **106**. As an impurity for forming an oxygen vacancy in an oxide semiconductor layer, for example, one or more of the following can be used: phosphorus, arsenic, antimony, boron, aluminum, silicon, nitrogen, helium, neon, argon, krypton, xenon, indium, fluorine, chlorine, titanium, zinc, and carbon. As a method for adding the impurity, plasma treatment, ion implantation, ion doping, plasma immersion ion implantation, or the like can be used.

[0214] When the above element is added as an impurity element to the oxide semiconductor layer, a bond between a metal element and oxygen in the oxide semiconductor layer is cut, so that an oxygen vacancy is formed. Interaction between an oxygen vacancy in the oxide semiconductor layer and hydrogen that remains in the oxide semiconductor layer or is added to the oxide semiconductor layer later can increase the conductivity of the oxide semiconductor layer.

[0215] When hydrogen is added to an oxide semiconductor in which an oxygen vacancy is formed by addition of an impurity element, hydrogen enters an oxygen vacant site and forms a donor level in the vicinity of the conduction band. Consequently, an oxide conductor can be formed. Here, an oxide conductor refers to an oxide semiconductor having become a conductor. Note that the oxide conductor has a light-transmitting property in a manner similar to the oxide semiconductor.

[0216] The oxide conductor is a degenerated semiconductor and it is suggested that the conduction band edge equals or substantially equals the Fermi level. For that reason, an ohmic contact is made between an oxide conductor layer and conductive layers functioning as a source electrode layer and a drain electrode layer; thus, contact resistance between the oxide conductor layer and the conductive layers functioning as a source electrode layer and a drain electrode layer can be reduced.

[0217] The transistor in one embodiment of the present invention may include a conductive layer **173** between the oxide semiconductor layer **130** and the substrate **115** as illustrated in cross-sectional views in the channel length direction in FIGS. **27**A to **27**F and cross-sectional views in the channel width direction in FIGS. **26**C and **26**D. When the conductive layer **173** is used as a second gate electrode layer (back gate), the on-state current can be increased or the threshold voltage can be controlled. In the cross-sectional views in FIGS. **27**A to **27**F, the width of the conductive layer **173** may be shorter than that of the oxide semiconductor layer **130**. Moreover, the width of the conductive layer **173** may be shorter than that of the conductive layer **170**.

[0218] In order to increase the on-state current, for example, the conductive layers **170** and **173** are made to have the same potential, and the transistor is driven as a double-gate transistor. Furthermore, in order to control the threshold voltage, a fixed potential that is different from the potential of the conductive layer **170** is applied to the conductive layer **173**. To set the conductive layers **170** and **173** at the same potential, for example, as illustrated in FIG. **26**D, the conductive layers **170** and **173** may be electrically connected to each other through a contact hole.

[0219] Although the transistors **101** to **106** in FIGS. **24**A to **24**F and FIGS. **25**A to **25**F are examples in which the oxide semiconductor layer **130** is a single layer, the oxide semiconductor layer **130** may be a stacked layer. The oxide semiconductor layer **130** in the transistors **101** to **106** can be replaced with the oxide semiconductor layer **130** in FIG. **28**B, **28**C, **28**D, or **28**E.

[0220] FIG. **28**A is a top view of the oxide semiconductor layer **130**, and FIGS. **28**B and **28**C are cross-sectional views of the oxide semiconductor layer **130** with a two-layer structure. FIGS. **28**D and **28**E are cross-sectional views of the oxide semiconductor layer **130** with a three-layer structure.

[0221] Oxide semiconductor layers with different compositions, for example, can be used as an oxide semiconductor layer **130***a*, an oxide semiconductor layer **130***b*, and an oxide semiconductor layer **130***c*.

[0222] The transistor in one embodiment of the present invention may have a structure illustrated in FIGS. **29**A and **29**B. FIG. **29**A is a top view of a transistor **107**. A cross section in the direction of dashed-dotted line H**1**-H**2** in FIG. **29**A is illustrated in FIG. **29**B. A cross section in the direction of dashed-dotted line H**3**-H**4** in FIG. **29**A is illustrated in FIG. **31**A. The direction of dashed-dotted line H**1**-H**2** is referred to as a channel length direction, and the direction of dashed-dotted line H**3**-H**4** is referred to as a channel width direction.

[0223] The transistor **107** includes the insulating layer **120** in contact with the substrate **115**; a stack of the oxide semiconductor layers **130***a* and **130***b* in contact with the insulating layer **120**; the conductive layers **140** and **150** electrically connected to the stack; the oxide semiconductor layer **130***c* in contact with the stack and the conductive layers **140** and **150**; the insulating layer **160** in contact with the oxide semiconductor layer **130***c*; the conductive layer **170** in contact with the insulating layer **160**; the insulating layer **175** in contact with the conductive layers **140** and **150**, the oxide semiconductor layer **130***c*, the insulating layer **160**, and the conductive layer **170**; and the insulating layer **180** in contact with the insulating layer **175**. The insulating layer **180** may function as a planarization film as necessary.

[0224] The transistor **107** has the same structure as the transistor **101** except that the oxide semiconductor layer **130** includes two layers (the oxide semiconductor layers **130***a* and **130***b*) in the regions **231** and **232**, that the oxide semiconductor layer **130** includes three layers (the oxide semiconductor layers **130***a* to **130***c*) in the region **233**, and that part of the oxide semiconductor layer (the oxide semiconductor layer **130***c*) exists between the insulating layer **160** and the conductive layers **140** and **150**.

[0225] The transistor in one embodiment of the present invention may have a structure illustrated in FIGS. **29**C and **29**D. FIG. **29**C is a top view of a transistor **108**. A cross section in the direction of dashed-dotted line **11-12** in FIG. **29**C is illustrated in FIG. **29**D. A cross section in the direction of dashed-dotted line **13-14** in FIG. **29**C is illustrated in FIG. **31**B. The direction of dashed-dotted line **11-12** is referred to as a channel length direction, and the direction of dashed-dotted line **13-14** is referred to as a channel width direction.

[0226] The transistor **108** differs from the transistor **107** in that end portions of the insulating layer **160** and the oxide semiconductor layer **130***c* are not aligned with the end portion of the conductive layer **170**.

[0227] The transistor in one embodiment of the present invention may have a structure illustrated in FIGS. **29**E and **29**F. FIG. **29**E is a top view of a transistor **109**. A cross section in the direction of dashed-dotted line J1-J2 in FIG. **29**E is illustrated in FIG. **29**F. A cross section in the direction of dashed-dotted line J3-J4 in FIG. **29**E is illustrated in FIG. **31**A. The direction of dashed-dotted line J1-J2 is referred to as a channel length direction, and the direction of dashed-dotted line J3-J4 is referred to as a channel width direction.

[0228] The transistor **109** includes the insulating layer **120** in contact with the substrate **115**; a stack of the oxide semiconductor layers **130***a* and **130***b* in contact with the insulating layer **120**; the oxide semiconductor layer **130***c* in contact with the stack; the insulating layer **160** in contact with the oxide semiconductor layer **130***c*; the conductive layer **170** in contact with the insulating layer **160**; the insulating layer **175** covering the stack, the oxide semiconductor layer **130***c*, the insulating layer **160**, and the conductive layer **170**; the insulating layer **180** in contact with the insulating layer **175**; and the conductive layers **140** and **150** electrically connected to the stack through openings provided in the insulating layers **175** and **180**. The transistor **109** may further include, for example, an insulating layer (planarization film) in contact with the insulating layer **180** and the conductive layers **140** and **150** as necessary.

[0229] The transistor **109** has the same structure as the transistor **103** except that the oxide semiconductor layer **130** includes two layers (the oxide semiconductor layers **130***a* and **130***b*) in the regions **231** and **232** and that the oxide semiconductor layer **130** includes three layers (the oxide semiconductor layers **130***a* to **130***c*) in the region **233**.

[0230] The transistor in one embodiment of the present invention may have a structure illustrated in FIGS. **30**A and **30**B. FIG. **30**A is a top view of a transistor **110**. A cross section in the direction of dashed-dotted line K**1**-K**2** in FIG. **30**A is illustrated in FIG. **30**B. A cross section in the direction of dashed-dotted line K**3**-K**4** in FIG. **30**A is illustrated in FIG. **31**A. The direction of dashed-dotted line K**1**-K**2** is referred to as a channel length direction, and the direction of dashed-dotted line K**3**-K**4** is referred to as a channel width direction.

[0231] The transistor **110** has the same structure as the transistor **104** except that the oxide semiconductor layer **130** includes two layers (the oxide semiconductor layers **130***a* and **130***b*) in the regions **331** and **332** and that the oxide semiconductor layer **130** includes three layers (the oxide semiconductor layers **130***a* to **130***c*) in the region **333**.

[0232] The transistor in one embodiment of the present invention may have a structure illustrated in FIGS. **30**C and **30**D. FIG. **30**C is a top view of a transistor **111**. A cross section in the direction of dashed-dotted line L**1**-L**2** in FIG. **30**C is illustrated in FIG. **30**D. A cross section in the direction of dashed-dotted line L**3**-L**4** in FIG. **30**C is illustrated in FIG. **31**A. The direction of dashed-dotted line L**1**-L**2** is referred to as a channel length direction, and the direction of dashed-dotted line L**3**-L**4** is referred to as a channel width direction.

[0233] The transistor **111** includes the insulating layer **120** in contact with the substrate **115**; a stack of the oxide semiconductor layers **130***a* and **130***b* in contact with the insulating layer **120**; the conductive layers **141** and **151** electrically connected to the stack; the oxide semiconductor layer **130***c* in contact with the stack and the conductive layers **141** and **151**; the insulating layer **160** in contact with the oxide semiconductor layer **130***c*; the conductive layer **170** in contact with the insulating layer **160**; the insulating layer **175** in contact with the stack, the conductive layers **141** and **151**, the oxide semiconductor layer **130***c*, the insulating layer **160**, and the conductive layer **170**; the insulating layer **180** in contact with the insulating layer **175**; and the conductive layers **142** and **152** electrically connected to the conductive layers **141** and **151**, respectively, through openings provided in the insulating layers **175** and **180**. The transistor **111** may further include, for example, an insulating layer (planarization film) in contact with the insulating layer **180** and the conductive layers **142** and **152** as necessary.

[0234] The transistor **111** has the same structure as the transistor **105** except that the oxide semiconductor layer **130** includes two layers (the oxide semiconductor layers **130***a* and **130***b*) in the regions **231** and **232**, that the oxide semiconductor layer **130** includes three layers (the oxide semiconductor layers **130***a* to **130***c*) in the region **233**, and that part of the oxide semiconductor layer (the oxide semiconductor layer **130***c*) exists between the insulating layer **160** and the conductive layers **141** and **151**.

[0235] The transistor in one embodiment of the present invention may have a structure illustrated in FIGS. **30**E and **30**F. FIG. **30**E is a top view of a transistor **112**. A cross section in the direction of dashed-dotted line **M1**-**M2** in FIG. **30**E is illustrated in FIG. **30**F. A cross section in the direction of dashed-dotted line **M3**-**M4** in FIG. **30**E is illustrated in FIG. **31**A. The direction of dashed-dotted line **M1**-**M2** is referred to as a channel length direction, and the direction of dashed-dotted line **M3**-**M4** is referred to as a channel width direction.

[0236] The transistor **112** has the same structure as the transistor **106** except that the oxide semiconductor layer **130** includes two layers (the oxide semiconductor layers **130***a* and **130***b*) in the regions **331**, **332**, **334**, and **335** and that the oxide semiconductor layer **130** includes three layers (the oxide semiconductor layers **130***a* to **130***c*) in the region **333**.

[0237] The transistor in one embodiment of the present invention may include the conductive layer **173** between the oxide semiconductor layer **130** and the substrate **115** as illustrated in cross-sectional views in the channel length direction in FIGS. **32**A to **32**F and cross-sectional views in the channel width direction in FIGS. **31**C and **31**D. When the conductive layer is used as a second gate electrode layer (back gate), the on-state current can be increased or the threshold voltage can be controlled. In the cross-sectional views in FIGS. **32**A to **32**F, the width of the conductive layer **173** may be shorter than that of the oxide semiconductor layer **130**. Moreover, the width of the conductive layer **173** may be shorter than that of the conductive layer **170**.

[0238] As illustrated in FIGS. **33**A and **33**B (illustrating only the oxide semiconductor layer **130**, the conductive layer **140**, and the conductive layer **150**), the width (WSD) of the conductive layer **140** (source electrode layer) and the conductive layer **150** (drain electrode layer) in the transistor of one embodiment of the present invention may be either longer than or shorter than the width (W_{OS}) of the oxide semiconductor layer **130**. When $W_{OS} \geq W_{SD}$ (W_{SD} is less than or equal to W_{OS}) is satisfied, a gate electric field is easily applied to the entire oxide semiconductor layer **130**, so that electrical characteristics of the transistor can be improved. As illustrated in FIG. **33**C, the conductive layers **140** and **150** may be formed only in a region that overlaps with the oxide semiconductor layer **130**.

[0239] In the transistor in one embodiment of the present invention (any of the transistors **101** to **112**), the conductive layer **170** functioning as a gate electrode layer electrically surrounds the oxide semiconductor layer **130** in the channel width direction with the insulating layer **160** functioning as a gate insulating film positioned therebetween. This structure increases the on-state current. Such a transistor structure is referred to as a surrounded channel (s-channel) structure.

[0240] In the transistor including the oxide semiconductor layers **130***a* and **130***b* and the transistor including the oxide semiconductor layers **130***a* to **130***c*, selecting appropriate materials for the two or three layers forming the oxide semiconductor layer **130** makes current flow to the oxide semiconductor layer **130***b*. Since current flows to the oxide semiconductor layer **130***b*, the current is hardly influenced by interface scattering, leading to high on-state current. Therefore, increasing the thickness of the oxide semiconductor layer **130***b* might increase the on-state current.

[0241] A semiconductor device including a transistor with any of the above structures can have favorable electrical characteristics.

[0242] The structure described above in this embodiment can be combined with any of the structures described in the other embodiments as appropriate.

Embodiment 3

[0243] In this embodiment, components of the transistors described in Embodiment 2 are described in detail.

[0244] As the substrate **115**, a glass substrate, a quartz substrate, a semiconductor substrate, a ceramic substrate, a metal substrate having a surface subjected to insulation treatment, or the like can be used. The substrate **115** can be a silicon substrate provided with a transistor and/or a photodiode; and an insulating layer, a wiring, a conductor functioning as a contact plug, and the like that are provided over the silicon substrate. Note that when p-channel transistors are formed using the silicon substrate, a silicon substrate with n^--type conductivity is preferably used. Alternatively, an SOI substrate including an n^--type or i-type silicon layer may be used. In the case where a p-channel transistor is formed using the silicon substrate, a surface of the silicon substrate where the transistor is formed preferably has a (**110**) plane orientation. Forming a p-channel transistor with the (110) plane can increase mobility.

[0245] The insulating layer **120** can have a function of supplying oxygen to the oxide semiconductor layer **130** as well as a function of preventing diffusion of impurities from a component included in the substrate **115**. For this reason, the insulating layer **120** is preferably an insulating film containing oxygen and more preferably, the insulating layer **120** is an insulating film containing oxygen in which the oxygen content is higher than that in the stoichiometric composition. The insulating layer **120** is a film in which the amount of released oxygen when converted into oxygen atoms is preferably greater than or equal to 1.0×10^{19} atoms/cm^3 in TDS analysis. In the TDS analysis, the film surface temperature is higher than or equal to 100° C. and lower than or equal to 700° C., or higher than or equal to 100° C. and lower than or equal to 500° C. In the case where the substrate **115** is provided with another device, the insulating layer **120** also functions as an interlayer insulating film. In that case, the insulating layer **120** is preferably subjected to planarization treatment such as CMP so as to have a flat surface.

[0246] For example, the insulating layer **120** can be formed using an oxide insulating film including aluminum oxide, magnesium oxide, silicon oxide, silicon oxynitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, tantalum oxide, or the like; a nitride insulating film including silicon nitride, silicon nitride oxide, aluminum nitride, aluminum nitride oxide, or the like; or a mixed material of any of these. The insulating layer **120** may be a stack of any of the above materials.

[0247] In this embodiment, detailed description is given mainly on the case where the oxide semiconductor layer **130** of the transistor has a three-layer structure in which the oxide semiconductor layers **130***a* to **130***c* are sequentially stacked from the insulating layer **120** side.

[0248] Note that in the case where the oxide semiconductor layer **130** is a single layer, a layer corresponding to the oxide semiconductor layer **130***b* described in this embodiment is used.

[0249] In the case where the oxide semiconductor layer **130** has a two-layer structure, a stack in which a layer corresponding to the oxide semiconductor layer **130***a* and a layer corresponding to the oxide semiconductor layer **130***b* are sequentially stacked from the insulating layer **120** side described in this embodiment is used. In such a case, the oxide semiconductor layers **130***a* and **130***b* can be replaced with each other.

[0250] In the case where the oxide semiconductor layer **130** has a layered structure of four or more layers, for example, a structure in which another oxide semiconductor layer is added to the three-layer stack of the oxide semiconductor layer **130** described in this embodiment can be employed.

[0251] For the oxide semiconductor layer **130***b*, for example, an oxide semiconductor whose electron affinity (an energy difference between a vacuum level and the conduction band minimum) is higher than those of the oxide semiconductor layers **130***a* and **130***c* is used. The electron affinity can be obtained by subtracting an energy difference between the conduction band minimum and the valence band maximum (what is called an energy gap) from an energy difference between the vacuum level and the valence band maximum (what is called an ionization potential).

[0252] The oxide semiconductor layers **130***a* and **130***c* each contain one or more kinds of metal elements contained in the oxide semiconductor layer **130***b*. For example, the oxide semiconductor layers **130***a* and **130***c* are preferably formed using an oxide semiconductor whose conduction band minimum is closer to a vacuum level than that of the oxide semiconductor layer **130***b* by 0.05 eV or more, 0.07 eV or more, 0.1 eV or more, or 0.15 eV or more and 2 eV or less, 1 eV or less, 0.5 eV or less, or 0.4 eV or less.

[0253] In such a structure, when an electric field is applied to the conductive layer **170**, a channel is formed in the oxide semiconductor layer **130***b* whose conduction band minimum is the lowest in the oxide semiconductor layer **130**.

[0254] Furthermore, since the oxide semiconductor layer **130***a* contains one or more kinds of metal elements contained in the oxide semiconductor layer **130***b*, an interface state is unlikely to be formed at the interface between the oxide semiconductor layers **130***a* and **130***b*, compared with the interface between the oxide semiconductor layer **130***b* and the insulating layer **120** on the assumption that the oxide semiconductor layer **130***b* is in contact with the insulating layer **120**. The interface state sometimes forms a channel; therefore, the threshold voltage of the transistor is changed in some cases. Thus, with the oxide semiconductor layer **130***a*, variations in electrical characteristics of the transistor, such as a threshold voltage, can be reduced. Moreover, the reliability of the transistor can be improved.

[0255] Furthermore, since the oxide semiconductor layer **130***c* contains one or more kinds of metal elements contained in the oxide semiconductor layer **130***b*, scattering of carriers is unlikely to occur at the interface between the oxide semiconductor layers **130***b* and **130***c*, compared with the interface between the oxide semiconductor layer **130***b* and the gate insulating film (the insulating layer **160**) on the assumption that the oxide semiconductor layer **130***b* is in contact with the gate insulating film. Thus, with the oxide semiconductor layer **130***c*, the field-effect mobility of the transistor can be increased.

[0256] For the oxide semiconductor layers **130***a* and **130***c*, for example, a material containing Al, Ti, Ga, Ge, Y, Zr, Sn, La, Ce, or Hf with a higher atomic ratio than that used for the oxide semiconductor layer **130***b* can be used. Specifically, the atomic ratio of any of the above metal elements in the oxide semiconductor layers **130***a* and **130***c* is 1.5 times or more, preferably 2 times or more, more preferably 3 times or more as large as that in the oxide semiconductor layer **130***b*. Any of the above metal elements is strongly bonded to oxygen and thus has a function of suppressing generation of an oxygen vacancy in the oxide semiconductor layers **130***a* and **130***c*. That is, an oxygen vacancy is less likely to be generated in the oxide semiconductor layers **130***a* and **130***c* than in the oxide semiconductor layer **130***b*.

[0257] An oxide semiconductor that can be used for each of the oxide semiconductor layers **130***a* to **130***c* preferably contains at least In or Zn. Both In and Zn are preferably contained. In order to reduce variations in electrical characteristics of the transistor including the oxide semiconductor, the oxide semiconductor preferably contains a stabilizer in addition to In and Zn.

[0258] Examples of a stabilizer include Ga, Sn, Hf, Al, and Zr. Other examples of the stabilizer include lanthanoids such as La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and Lu.

[0259] As the oxide semiconductor, for example, any of the following can be used: indium oxide, tin oxide, gallium oxide, zinc oxide, an In—Zn oxide, a Sn—Zn oxide, an Al—Zn oxide, a Zn—Mg oxide, a Sn—Mg oxide, an In—Mg oxide, an In—Ga oxide, an In—Ga—Zn oxide, an In—Al—Zn oxide, an In—Sn—Zn oxide, a Sn—Ga—Zn oxide, an Al—Ga—Zn oxide, a Sn—Al—Zn oxide, an In—Hf—Zn oxide, an In—La—Zn oxide, an In—Ce—Zn oxide, an In—Pr—Zn oxide, an In—Nd—Zn oxide, an In—Sm—Zn oxide, an In—Eu—Zn oxide, an In—Gd—Zn oxide, an In—Tb—Zn oxide, an In—Dy—Zn oxide, an In—Ho—Zn oxide, an In—Er—Zn oxide, an In—Tm—Zn oxide, an In—Yb—Zn oxide, an In—Lu—Zn oxide, an In—Sn—Ga—Zn oxide, an In—Hf—Ga—Zn oxide, an In—Al—Ga—Zn oxide, an In—Sn—Al—Zn oxide, an In—Sn—Hf—Zn oxide, and an In—Hf—Al—Zn oxide.

[0260] For example, an In—Ga—Zn oxide means an oxide containing In, Ga, and Zn as its main components. The In—Ga—Zn oxide may contain another metal element in addition to In, Ga, and Zn. In this specification, a film containing the In—Ga—Zn oxide is also referred to as an IGZO film.

[0261] A material represented by $InMO_3(ZnO)_m$ ($m>0$, where m is not an integer) may be used. Note that M represents one or more metal elements selected from Ga, Y, Zr, La, Ce, and Nd. Alternatively, a material represented by $In_2SnO_5(ZnO)_n$ ($n>0$, where n is an integer) may be used.

[0262] Note that when each of the oxide semiconductor layers **130***a* to **130***c* is an InM-Zn oxide containing at least indium, zinc, and M (M is a metal such as Al, Ti, Ga, Ge, Y, Zr, Sn, La, Ce, or Hf), in the case where the oxide semiconductor layer **130***a* has an atomic ratio of In to M and Zn which is $x_1:y_1:z_1$, the oxide semiconductor layer **130***b* has an atomic ratio of In to M and Zn which is $x_2:y_2:z_2$, and the oxide semiconductor layer **130***c* has an atomic ratio of In to M and Zn which is $x_3:y_3:z_3$, each of y_1/x_1 and y_3/x_3 is preferably larger than y_2/x_2. Each of y_1/x_1 and y_3/x_3 is 1.5 times or more, preferably 2 times or more, more preferably 3 times or more as large as y_2/x_2. At this time, when y_2 is greater than or equal to x_2 in the oxide semiconductor layer **130***b*, the transistor can have stable electrical characteristics. However, when y_2 is 3 times or more as large as x_2, the field-effect mobility of the transistor is reduced; accordingly, y_2 is preferably smaller than 3 times x_2.

[0263] In the case where Zn and O are not taken into consideration, the proportion of In and the proportion of M in each of the oxide semiconductor layers **130***a* and **130***c* are preferably less than 50 atomic % and greater than or equal to 50 atomic %, respectively, more preferably less than 25 atomic % and greater than or equal to 75 atomic %, respectively. Furthermore, in the case where Zn and O are not taken into consideration, the proportion of In and the proportion of M in the oxide semiconductor layer **130***b* are preferably greater than or equal to 25 atomic % and less than 75 atomic %, respectively, more preferably greater than or equal to 34 atomic % and less than 66 atomic %, respectively.

[0264] The indium content in the oxide semiconductor layer **130***b* is preferably higher than those in the oxide semiconductor layers **130***a* and **130***c*. In an oxide semiconductor, the s orbital of heavy metal mainly contributes to carrier transfer, and when the proportion of In in the oxide semiconductor is increased, overlap of the s orbitals is likely to be increased. Therefore, an oxide in which the proportion of In is higher than that of M has higher mobility than an oxide in which the proportion of In is equal to or lower than that of M. Thus, with the use of an oxide having a high content of indium for the oxide semiconductor layer **130***b*, a transistor having high field-effect mobility can be obtained.

[0265] The thickness of the oxide semiconductor layer **130***a* is greater than or equal to 3 nm and less than or equal to 100 nm, preferably greater than or equal to 5 nm and less than or equal to 50 nm, more preferably greater than or equal to 5 nm and less than or equal to 25 nm. The thickness of the oxide semiconductor layer **130***b* is greater than or equal to 3 nm and less than or equal to 200 nm, preferably greater than or equal to 5 nm and less than or equal to 150 nm, more preferably greater than or equal to 10 nm and less than or equal to 100 nm. The thickness of the oxide semiconductor layer **130***c* is greater than or equal to 1 nm and less than or equal to 50 nm, preferably greater than or equal to 2 nm and less than or equal to 30 nm, more preferably greater than or equal to 3 nm and less than or equal to 15 nm. In addition, the oxide semiconductor layer **130***b* is preferably thicker than the oxide semiconductor layer **130***c*.

[0266] Note that in order that a transistor in which a channel is formed in an oxide semiconductor layer have stable electrical characteristics, it is effective to make the oxide semiconductor layer intrinsic or substantially intrinsic by reducing the concentration of impurities in the oxide semiconductor layer. The term "substantially intrinsic" refers to a state where an oxide semiconductor layer has a carrier density lower than $1\times10^{15}/\text{cm}^3$, preferably lower than $1\times10^{13}/\text{cm}^3$, more preferably lower than $8\times10^{11}/\text{cm}^3$, still more preferably higher than or equal to $1\times10^{-9}/\text{cm}^3$ and lower than $1\times10^{8}/\text{cm}^3$.

[0267] In the oxide semiconductor layer, hydrogen, nitrogen, carbon, silicon, and a metal element other than main components of the oxide semiconductor layer are impurities. For example, hydrogen and nitrogen form donor levels to increase the carrier density, and silicon forms impurity levels in the oxide semiconductor layer. The impurity levels serve as traps and might cause deterioration of electrical characteristics of the transistor. Therefore, it is preferable to reduce the concentration of the impurities in the oxide semiconductor layers **130***a* to **130***c* and at interfaces between the oxide semiconductor layers.

[0268] In order to make the oxide semiconductor layer intrinsic or substantially intrinsic, the oxide semiconductor layer is controlled to have a region in which the concentration of hydrogen estimated by secondary ion mass spectrometry (SIMS) is lower than or equal to 2×10^{20} atoms/cm^3, preferably lower than or equal to 5×10^{19} atoms/cm^3, more preferably lower than or equal to 1×10^{19} atoms/cm^3, still more preferably higher than or equal to 1×10^{17} atoms/cm^3 and lower than or equal to 5×10^{18} atoms/cm^3. Furthermore, the oxide semiconductor layer is controlled to have a region in which the concentration of nitrogen is lower than 5×10^{19} atoms/cm^3, preferably lower than or equal to 5×10^{18} atoms/cm^3, more preferably lower than or equal to 1×10^{18} atoms/cm^3, still more preferably higher than or equal to 5×10^{16} atoms/cm^3 and lower than or equal to 5×10^{17} atoms/cm^3.

[0269] The high concentration of silicon or carbon might reduce the crystallinity of the oxide semiconductor layer. In order not to lower the crystallinity of the oxide semiconductor layer, the oxide semiconductor layer is controlled to have a region in which the concentration of silicon is lower than 1×10^{19} atoms/cm^3, preferably higher than or equal to 1×10^{18} atoms/cm^3 and lower than 5×10^{18} atoms/cm^3. Furthermore, the oxide semiconductor layer is controlled to have a region in which the concentration of carbon is lower than 1×10^{19} atoms/cm^3, preferably lower than or equal to 5×10^{18} atoms/cm^3, more preferably higher than or equal to 6×10^{17} atoms/cm^3 and lower than 1×10^{18} atoms/cm^3.

[0270] A transistor in which a highly purified oxide semiconductor film is used for a channel formation region exhibits extremely low off-state current. When voltage between a source and a drain is set at about 0.1 V, 5 V, or 10 V, for example, the off-state current per channel width of the transistor can be as low as several yoctoamperes per micrometer to several zeptoamperes per micrometer.

[0271] As the gate insulating film of the transistor, an insulating film containing silicon is used in many cases; thus, it is preferable that, as in the transistor in one embodiment of the present invention, a region of the oxide semiconductor layer that serves as a channel not be in contact with the gate insulating film for the above reason. In the case where a channel is formed at the interface between the gate insulating film and the oxide semiconductor layer, scattering of carriers occurs at the interface, so that the field-effect mobility of the transistor is reduced in some cases. Also from the view of the above, it is preferable that the region of the oxide semiconductor layer that serves as a channel be separated from the gate insulating film.

[0272] Accordingly, with the oxide semiconductor layer **130** having a layered structure including the oxide semiconductor layers **130***a* to **130***c*, a channel can be formed in the oxide semiconductor layer **130***b*; thus, the transistor can have high field-effect mobility and stable electrical characteristics.

[0273] In a band structure, the conduction band minimums of the oxide semiconductor layers **130***a* to **130***c* are continuous. This can be understood also from the fact that the compositions of the oxide semiconductor layers **130***a* to **130***c* are close to one another and oxygen is easily diffused among the oxide semiconductor layers **130***a* to **130***c*. Thus, the oxide semiconductor layers **130***a* to **130***c* have a continuous physical property though they have different compositions and form a stack. In the drawings, interfaces between the oxide semiconductor layers of the stack are indicated by dotted lines.

[0274] The oxide semiconductor layer **130** in which layers containing the same main components are stacked is formed to have not only a simple layered structure of the layers but also a continuous energy band (here, in particular, a well structure having a U shape in which the conduction band minimums are continuous (U-shape well)). In other words, the layered structure is formed such that there exists no impurity that forms a defect level such as a trap center or a recombination center at each interface. If impurities exist between the stacked oxide semiconductor layers, the continuity of the energy band is lost and carriers disappear by a trap or recombination at the interface.

[0275] For example, an In—Ga—Zn oxide whose atomic ratio of In to Ga and Zn is 1:3:2, 1:3:3, 1:3:4, 1:3:6, 1:4:5, 1:6:4, or 1:9:6 can be used for the oxide semiconductor layers **130***a* and **130***c*, and an In—Ga—Zn oxide whose atomic ratio of In to Ga and Zn is 1:1:1, 2:1:3, 5:5:6, or 3:1:2 can be used for the oxide semiconductor layer **130***b*. In the case where each of the oxide semiconductor layers **130***a*, **130***b*, and **130***c* is formed using the above oxide as a sputtering target, the atomic ratio of each sputtering target and that of each formed oxide semiconductor layer are not necessarily consistent with each other.

[0276] The oxide semiconductor layer **130***b* of the oxide semiconductor layer **130** serves as a well, so that a channel is formed in the oxide semiconductor layer **130***b*. Since the conduction band minimums are continuous, the oxide semiconductor layer **130** can also be referred to as a U-shaped well. Furthermore, a channel formed to have such a structure can also be referred to as a buried channel.

[0277] Trap levels due to impurities or defects might be formed in the vicinity of the interface between an insulating layer such as a silicon oxide film and each of the oxide semiconductor layers **130***a* and **130***c*. The oxide semiconductor layer **130***b* can be distanced away from the trap levels owing to existence of the oxide semiconductor layers **130***a* and **130***c*.

[0278] However, when the energy differences between the conduction band minimum of the oxide semiconductor layer **130***b* and the conduction band minimum of each of the oxide semiconductor layers **130***a* and **130***c* are small, an electron in the oxide semiconductor layer **130***b* might reach the trap level by passing over the energy differences. When the electron is trapped in the trap level, negative charge is generated at the interface with the insulating layer, so that the threshold voltage of the transistor is shifted in a positive direction.

[0279] The oxide semiconductor layers **130***a* to **130***c* preferably include crystal parts. In particular, when crystals with c-axis alignment are used, the transistor can have stable electrical characteristics. Moreover, crystals with c-axis alignment are resistant to bending; therefore, using such crystals can improve the reliability of a semiconductor device using a flexible substrate.

[0280] As the conductive layer **140** functioning as a source electrode layer and the conductive layer **150** functioning as a drain electrode layer, for example, a single layer or a stacked layer formed using a material selected from Al, Cr, Cu, Ta, Ti, Mo, W, Ni, Mn, Nd, and Sc and alloys of any of these metal materials can be used. Typically, it is preferable to use Ti, which is particularly easily bonded to oxygen, or W, which has a high melting point and thus makes subsequent process temperatures comparatively high. It is also possible to use a stack of any of the above materials and Cu or an alloy such as Cu—Mn, which has low resistance. In the transistors **105**, **106**, **111**, and **112**, for example, it is possible to use W for the conductive layers **141** and **151** and use a stack of Ti and Al for the conductive layers **142** and **152**.

[0281] The above materials are capable of extracting oxygen from an oxide semiconductor film. Therefore, in a region of the oxide semiconductor film that is in contact with any of the above materials, oxygen is released from the oxide semiconductor layer and an oxygen vacancy is formed. Hydrogen slightly contained in the film and the oxygen vacancy are bonded to each other, so that the region is markedly changed to an n-type region. Accordingly, the n-type region can serve as a source or a drain of the transistor.

[0282] In the case where W is used for the conductive layers **140** and **150**, the conductive layers **140** and **150** may be doped with nitrogen. Doping with nitrogen can appropriately lower the capability of extracting oxygen and prevent the n-type region from spreading to a channel region. It is possible to prevent the n-type region from spreading to a channel region also by using a stack of W and an n-type semiconductor layer as the conductive layers **140** and **150** and putting the n-type semiconductor layer in contact with the oxide semiconductor layer. As the n-type semiconductor layer, an In—Ga—Zn oxide, zinc oxide, indium oxide, tin oxide, indium tin oxide, or the like to which nitrogen is added can be used.

[0283] The insulating layer **160** functioning as a gate insulating film can be formed using an insulating film containing one or more of aluminum oxide, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, and tantalum oxide. The insulating layer **160** may be a stack including any of the above materials. The insulating layer **160** may contain La, N, Zr, or the like as an impurity.

[0284] An example of a layered structure of the insulating layer **160** is described. The insulating layer **160** includes, for example, oxygen, nitrogen, silicon, or hafnium. Specifically, the insulating layer **160** preferably includes hafnium oxide and silicon oxide or silicon oxynitride.

[0285] Hafnium oxide and aluminum oxide have higher dielectric constants than silicon oxide and silicon oxynitride. Therefore, the insulating layer **160** using hafnium oxide or aluminum oxide can have larger thickness than the insulating layer **160** using silicon oxide, so that leakage current due to tunnel current can be reduced. That is, a transistor with low off-state current can be provided. Moreover, hafnium oxide with a crystalline structure has a higher dielectric constant than hafnium oxide with an amorphous structure. Therefore, it is preferable to use hafnium oxide with a crystalline structure in order to provide a transistor with low off-state current. Examples of the crystal structure include a monoclinic crystal structure and a cubic crystal structure. Note that one embodiment of the present invention is not limited to the above examples.

[0286] For the insulating layers **120** and **160** in contact with the oxide semiconductor layer **130**, a film that releases less nitrogen oxide is preferably used. In the case where the oxide semiconductor is in contact with an insulating layer that releases a large amount of nitrogen oxide, the density of states due to nitrogen oxide becomes high in some cases. For the insulating layers **120** and **160**, for example, an oxide insulating layer such as a silicon oxynitride film or an aluminum oxynitride film that releases less nitrogen oxide can be used.

[0287] A silicon oxynitride film that releases less nitrogen oxide is a film of which the amount of released ammonia is larger than the amount of released nitrogen oxide in TDS; the amount of released ammonia is typically greater than or equal to 1×10^{18} molecules/cm^3 and less than or equal to 5×10^{19} molecules/cm^3. Note that the amount of released ammonia is the amount of ammonia released by heat treatment with which the surface temperature of the film becomes higher than or equal to 50° C. and lower than or equal to 650° C., preferably higher than or equal to 50° C. and lower than or equal to 550° C.

[0288] By using the above oxide insulating layer for the insulating layers **120** and **160**, a shift in the threshold voltage of the transistor can be reduced, which leads to reduced fluctuations in the electrical characteristics of the transistor.

[0289] For the conductive layer **170** functioning as a gate electrode layer, for example, a conductive film formed using Al, Ti, Cr, Co, Ni, Cu, Y, Zr, Mo, Ru, Ag, Mn, Nd, Sc, Ta, W, or the like can be used. Alternatively, an alloy or a conductive nitride of any of these materials may be used. Alternatively, a stack of a plurality of materials selected from these materials, alloys of these materials, and conductive nitrides of these materials may be used. Typically, tungsten, a stack of tungsten and titanium nitride, a stack of tungsten and tantalum nitride, or the like can be used. Alternatively, Cu or an alloy such as Cu—Mn, which has low resistance, or a stack of any of the above materials and Cu or an alloy such as Cu—Mn may be used. In this embodiment, tantalum nitride is used for the conductive layer **171** and tungsten is used for the conductive layer **172** to form the conductive layer **170**.

[0290] As the insulating layer **175**, a silicon nitride film, an aluminum nitride film, or the like containing hydrogen can be used. In the transistors **103**, **104**, **106**, **109**, **110**, and **112** described in Embodiment 2, when an insulating film containing hydrogen is used as the insulating layer **175**, part of the oxide semiconductor layer can have n-type conductivity. In addition, a nitride insulating film functions as a blocking film against moisture and the like and can improve the reliability of the transistor.

[0291] An aluminum oxide film can also be used as the insulating layer **175**. It is particularly preferable to use an aluminum oxide film as the insulating layer **175** in the transistors **101**, **102**, **105**, **107**, **108**, and **111** described in Embodiment 2. The aluminum oxide film has a high blocking effect of preventing penetration of both oxygen and impurities such as hydrogen and moisture. Accordingly, during and after the manufacturing process of the transistor, the aluminum oxide film can suitably function as a protective film that has effects of preventing entry of impurities such as hydrogen and moisture into the oxide semiconductor layer **130**, preventing release of oxygen from the oxide semiconductor layer, and preventing unnecessary release of oxygen from the insulating layer **120**. Furthermore, oxygen contained in the aluminum oxide film can be diffused into the oxide semiconductor layer.

[0292] Furthermore, the insulating layer **180** is preferably formed over the insulating layer **175**. The insulating layer **180** can be formed using an insulating film containing one or more of magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, and tantalum oxide. The insulating layer **180** may be a stack of any of the above materials.

[0293] Here, like the insulating layer **120**, the insulating layer **180** preferably contains oxygen more than that in the stoichiometric composition. Oxygen released from the insulating layer **180** can be diffused into the channel formation region in the oxide semiconductor layer **130** through the insulating layer **160**, so that oxygen vacancies formed in the channel formation region can be filled with oxygen. In this manner, stable electrical characteristics of the transistor can be achieved.

[0294] High integration of a semiconductor device requires miniaturization of a transistor. However, it is known that miniaturization of a transistor causes deterioration of electrical characteristics of the transistor. In particular, a decrease in channel width causes a reduction in on-state current.

[0295] In the transistors **107** to **112** in one embodiment of the present invention, the oxide semiconductor layer **130***c* is formed to cover the oxide semiconductor layer **130***b* where a channel is formed; thus, a channel formation layer is not in contact with the gate insulating film. Accordingly, scattering of carriers at the interface between the channel formation layer and the gate insulating film can be reduced and the on-state current of the transistor can be increased.

[0296] In the transistor in one embodiment of the present invention, as described above, the gate electrode layer (the conductive layer **170**) is formed to electrically surround the oxide semiconductor layer **130** in the channel width direction; accordingly, a gate electric field is applied to the oxide semiconductor layer **130** in a direction perpendicular to its side surface in addition to a direction perpendicular to its top surface. In other words, a gate electric field is applied to the entire channel formation layer and effective channel width is increased, leading to a further increase in the on-state current.

[0297] Furthermore, in the transistor in one embodiment of the present invention in which the oxide semiconductor layer **130** has a two-layer structure or a three-layer structure, since the oxide semiconductor layer **130***b* where a channel is formed is provided over the oxide semiconductor layer **130***a*, an effect of making an interface state less likely to be formed is obtained. In the transistor in one embodiment of the present invention in which the oxide semiconductor layer **130** has a three-layer structure, since the oxide semiconductor layer **130***b* is positioned at the middle of the three-layer structure, an effect of eliminating the influence of an impurity that enters from upper and lower layers on the oxide semiconductor layer **130***b* is obtained as well. Therefore, the transistor can achieve not only the increase in the on-state current of the transistor but also stabilization of the threshold voltage and a reduction in the S value (subthreshold value). Thus, current when gate voltage VG is 0 V can be reduced and power consumption can be reduced. In addition, since the threshold voltage of the transistor becomes stable, long-term reliability of the semiconductor device can be improved. Furthermore, the transistor in one embodiment of the present invention is suitable for a highly integrated semiconductor device because deterioration of electrical characteristics due to miniaturization is reduced.

[0298] Although the variety of films such as the metal films, the semiconductor films, and the inorganic insulating films that are described in this embodiment typically can be formed by sputtering or plasma-enhanced CVD, such films may be formed by another method such as thermal CVD. Examples of thermal CVD include metal organic chemical vapor deposition (MOCVD) and atomic layer deposition (ALD).

[0299] Since plasma is not used for deposition, thermal CVD has an advantage that no defect due to plasma damage is generated.

[0300] Deposition by thermal CVD may be performed in such a manner that a source gas and an oxidizer are supplied to the chamber at the same time, the pressure in the chamber is set to an atmospheric pressure or a reduced pressure, and reaction is caused in the vicinity of the substrate or over the substrate.

[0301] Deposition by ALD is performed in such a manner that the pressure in a chamber is set to an atmospheric pressure or a reduced pressure, source gases for reaction are introduced into the chamber and reacted, and then the sequence of gas introduction is repeated. An inert gas (e.g., argon or nitrogen) may be introduced as a carrier gas with the source gases. For example, two or more kinds of source gases may be sequentially supplied to the chamber. In that case, after reaction of a first source gas, an inert gas is introduced, and then a second source gas is introduced so that the source gases are not mixed. Alternatively, the first source gas may be exhausted by vacuum evacuation instead of introduction of the inert gas, and then the second source gas may be introduced. The first source gas is adsorbed on the surface of the substrate and reacted to form a first layer, and then, the second source gas introduced is absorbed and reacted. As a result, a second layer is stacked over the first layer, so that a thin film is formed. The sequence of gas introduction is controlled and repeated more than once until desired thickness is obtained, so that a thin film with excellent step coverage can be formed. The thickness of the thin film can be adjusted by the number of repetition times of the sequence of gas introduction; therefore, ALD makes it possible to accurately adjust thickness and thus is suitable for manufacturing a minute FET.

[0302] The variety of films such as the metal film, the semiconductor film, and the inorganic insulating film that have been disclosed in the embodiments can be formed by thermal CVD such as MOCVD or ALD. For example, in the case where an In—Ga—Zn—O film is formed, trimethylindium ($In(CH_3)_3$), trimethylgallium ($Ga(CH_3)_3$), and dimethylzinc ($Zn(CH_3)_2$) can be used. Without limitation to the above combination, triethylgallium ($Ga(C_2H_5)_3$) can be used instead of trimethylgallium and diethylzinc ($Zn(C_2H_5)_2$) can be used instead of dimethylzinc.

[0303] For example, in the case where a hafnium oxide film is formed by a deposition apparatus using ALD, two kinds of gases, i.e., ozone (O_3) as an oxidizer and a source material gas which is obtained by vaporizing liquid containing a solvent and a hafnium precursor (hafnium alkoxide and a hafnium amide such as tetrakis(dimethylamide)hafnium (TDMAH, $Hf[N(CH_3)_2]_4$) and tetrakis(ethylmethylamide)hafnium) are used.

[0304] For example, in the case where an aluminum oxide film is formed by a deposition apparatus using ALD, two kinds of gases, i.e., H_2O as an oxidizer and a source gas which is obtained by vaporizing liquid containing a solvent and an aluminum precursor (e.g., trimethylaluminum (TMA, $Al(CH_3)_3$)) are used. Examples of another material include tris(dimethylamide)aluminum, triisobutylaluminum, and aluminum tris(2,2,6,6-tetramethyl-3,5-heptanedionate).

[0305] For example, in the case where a silicon oxide film is formed by a deposition apparatus using ALD, hexachlorodisilane is adsorbed on a surface where a film is to be formed, and radicals of an oxidizing gas (e.g., O_2 or dinitrogen monoxide) are supplied to react with an adsorbate.

[0306] For example, in the case where a tungsten film is formed by a deposition apparatus using ALD, a WF_6 gas and a B_2H_6 gas are sequentially introduced to form an initial tungsten film, and then a WF_6 gas and an H_2 gas are sequentially introduced to form a tungsten film. Note that an SiH_4 gas may be used instead of a B_2H_6 gas.

[0307] For example, in the case where an oxide semiconductor film, e.g., an In—Ga—Zn—O film is formed by a deposition apparatus using ALD, an $In(CH_3)_3$ gas and an O_3 gas are sequentially introduced to form an In—O layer, a $Ga(CH_3)_3$ gas and an O_3 gas are sequentially introduced to form a Ga—O layer, and then a $Zn(CH_3)_2$ gas and an O_3 gas are sequentially introduced to form a Zn—O layer. Note that the order of these layers is not limited to this example. A mixed compound layer such as an In—Ga—O layer, an In—Zn—O layer, or a Ga—Zn—O layer may be formed by using these gases. Although an H_2O gas which is obtained by bubbling with an inert gas such as Ar may be used instead of an O_3 gas, it is preferable to use an O_3 gas, which does not contain H.

[0308] A facing-target-type sputtering apparatus can be used for deposition of an oxide semiconductor layer. Deposition using the facing-target-type sputtering apparatus can also be referred to as vapor deposition SP (VDSP).

[0309] When an oxide semiconductor layer is deposited using a facing-target-type sputtering apparatus, plasma damage to the oxide semiconductor layer at the time of deposition can be reduced. Thus, oxygen vacancies in a film can be reduced. In addition, the use of the facing-target-type sputtering apparatus enables low-pressure deposition. Accordingly, the concentration of impurities (e.g., hydrogen, a rare gas (e.g., argon), or water) in a deposited oxide semiconductor layer can be lowered.

[0310] The structure described above in this embodiment can be combined with any of the structures described in the other embodiments as appropriate.

Embodiment 4

[0311] The structure of an oxide semiconductor film that can be used for one embodiment of the present invention is described below.

[0312] In this specification, the term "parallel" indicates that the angle formed between two straight lines is greater than or equal to −10° and less than or equal to 10°, and accordingly includes the case where the angle is greater than or equal to −5° and less than or equal to 5°. The term "perpendicular" indicates that an angle formed between two straight lines is greater than or equal to 80° and less than or equal to 100°, and accordingly includes the case where the angle is greater than or equal to 85° and less than or equal to 95°.

[0313] In this specification, the trigonal and rhombohedral crystal systems are included in the hexagonal crystal system.

[0314] An oxide semiconductor film is roughly classified into a non-single-crystal oxide semiconductor film and a single-crystal oxide semiconductor film. The non-single-crystal oxide semiconductor film means any of a c-axis aligned crystalline oxide semiconductor (CAAC-OS) film, a polycrystalline oxide semiconductor film, a microcrystalline oxide semiconductor film, an amorphous oxide semiconductor film, and the like.

[0315] First, a CAAC-OS film is described.

[0316] The CAAC-OS film is one of oxide semiconductor films having a plurality of c-axis aligned crystal parts.

[0317] With a transmission electron microscope (TEM), a combined analysis image (also referred to as a high-resolution TEM image) of a bright-field image and a diffraction pattern of the CAAC-OS film is observed. Consequently, a plurality of crystal parts are observed clearly. However, in the high-resolution TEM image, a boundary between crystal parts, i.e., a grain boundary is not observed clearly. Thus, in the CAAC-OS film, a reduction in electron mobility due to the grain boundary is less likely to occur.

[0318] According to the high-resolution cross-sectional TEM image of the CAAC-OS film observed in a direction substantially parallel to a sample surface (cross-sectional TEM image), metal atoms are arranged in a layered manner in the crystal parts. Each metal atom layer has a morphology that reflects a surface over which the CAAC-OS film is formed (also referred to as a formation surface) or a top surface of the CAAC-OS film, and is provided parallel to the formation surface or the top surface of the CAAC-OS film.

[0319] On the other hand, according to the high-resolution planar TEM image of the CAAC-OS film observed in a direction substantially perpendicular to the sample surface (planar TEM image), metal atoms are arranged in a triangular or hexagonal configuration in the crystal parts. However, there is no regularity of arrangement of metal atoms between different crystal parts.

[0320] The CAAC-OS film is subjected to structural analysis with an X-ray diffraction (XRD) apparatus. For example, when the CAAC-OS film including an $InGaZnO_4$ crystal is analyzed by an out-of-plane method, a peak appears frequently when the diffraction angle (2θ) is around 31°. This peak is derived from the (009) plane of the $InGaZnO_4$ crystal, which indicates that crystals in the CAAC-OS film have c-axis alignment, and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS film.

[0321] Note that when the CAAC-OS film with an $InGaZnO_4$ crystal is analyzed by an out-of-plane method, a peak of 2θ may also be observed at around 36°, in addition to the peak of 2θ at around 31°. The peak of 2θ at around 36° indicates that a crystal having no c-axis alignment is included in part of the CAAC-OS film. It is preferable that in the CAAC-OS film, a peak of 2θ appear at around 31° and a peak of 2θ not appear at around 36°.

[0322] The CAAC-OS film is an oxide semiconductor film having low impurity concentration. The impurity is an element other than the main components of the oxide semiconductor film, such as hydrogen, carbon, silicon, or a transition metal element. In particular, an element that has higher bonding strength to oxygen than a metal element included in the oxide semiconductor film, such as silicon, disturbs the atomic order of the oxide semiconductor film by depriving the oxide semiconductor film of oxygen and causes a decrease in crystallinity. Furthermore, a heavy metal such as iron or nickel, argon, carbon dioxide, or the like has a large atomic radius (molecular radius), and thus disturbs the atomic order of the oxide semiconductor film and causes a decrease in crystallinity when it is contained in the oxide semiconductor film. Note that the impurity contained in the oxide semiconductor film might serve as a carrier trap or a carrier generation source.

[0323] The CAAC-OS film is an oxide semiconductor film having low density of defect states. In some cases, oxygen vacancies in the oxide semiconductor film serve as carrier traps or serve as carrier generation sources when hydrogen is captured therein.

[0324] The state in which impurity concentration is low and density of defect states is low (the number of oxygen vacancies is small) is referred to as “highly purified intrinsic” or “substantially highly purified intrinsic.” A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has few carrier generation sources, and thus can have low carrier density. Thus, a transistor including the oxide semiconductor film rarely has negative threshold voltage (is rarely normally on). The highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has few carrier traps. Accordingly, the transistor including the oxide semiconductor film has few variations in electrical characteristics and high reliability. Charge trapped by the carrier traps in the oxide semiconductor film takes a long time to be released and may behave like fixed charge. Thus, the transistor that includes the oxide semiconductor film having high impurity concentration and high density of defect states has unstable electrical characteristics in some cases.

[0325] In a transistor including the CAAC-OS film, changes in electrical characteristics of the transistor due to irradiation with visible light or ultraviolet light are small.

[0326] Next, a microcrystalline oxide semiconductor film is described.

[0327] A microcrystalline oxide semiconductor film has a region where a crystal part is observed in a high-resolution TEM image and a region where a crystal part is not clearly observed in a high-resolution TEM image. In most cases, a crystal part in the microcrystalline oxide semiconductor film is greater than or equal to 1 nm and less than or equal to 100 nm, or greater than or equal to 1 nm and less than or equal to 10 nm. A microcrystal with a size greater than or equal to 1 nm and less than or equal to 10 nm, or a size greater than or equal to 1 nm and less than or equal to 3 nm is specifically referred to as nanocrystal (nc). An oxide semiconductor film including nanocrystal is referred to as a nanocrystalline oxide semiconductor (nc-OS) film. In a high-resolution TEM image, a grain boundary cannot be found clearly in the nc-OS film in some cases.

[0328] In the nc-OS film, a microscopic region (e.g., a region with a size greater than or equal to 1 nm and less than or equal to 10 nm, in particular, a region with a size greater than or equal to 1 nm and less than or equal to 3 nm) has periodic atomic order. There is no regularity of crystal orientation between different crystal parts in the nc-OS film. Thus, the orientation of the whole film is not observed. Accordingly, in some cases, the nc-OS film cannot be distinguished from an amorphous oxide semiconductor film depending on an analysis method. For example, when the nc-OS film is subjected to structural analysis by an out-of-plane method with an XRD apparatus using an X-ray having a diameter larger than that of a crystal part, a peak that shows a crystal plane does not appear. Furthermore, a halo pattern is shown in a selected-area electron diffraction pattern of the nc-OS film obtained by using an electron beam having a probe diameter larger than the diameter of a crystal part (e.g., larger than or equal to 50 nm). Meanwhile, spots are shown in a nanobeam electron diffraction pattern of the nc-OS film obtained by using an electron beam having a probe diameter close to or smaller than the diameter of a crystal part. Furthermore, in a nanobeam electron diffraction pattern of the nc-OS film, regions with high luminance in a circular (ring) pattern are observed in some cases. Also in a nanobeam electron diffraction pattern of the nc-OS film, a plurality of spots are shown in a ring-like region in some cases.

[0329] The nc-OS film is an oxide semiconductor film that has high regularity than an amorphous oxide semiconductor film. Thus, the nc-OS film has a lower density of defect states than the amorphous oxide semiconductor film. Note that there is no regularity of crystal orientation between different crystal parts in the nc-OS film; thus, the nc-OS film has a higher density of defect states than the CAAC-OS film.

[0330] Next, an amorphous oxide semiconductor film is described.

[0331] The amorphous oxide semiconductor film has disordered atomic arrangement and no crystal part. For example, the amorphous oxide semiconductor film does not have a specific state as in quartz.

[0332] In a high-resolution TEM image of the amorphous oxide semiconductor film, crystal parts cannot be found.

[0333] When the amorphous oxide semiconductor film is subjected to structural analysis by an out-of-plane method with an XRD apparatus, a peak which shows a crystal plane does not appear. A halo pattern is shown in an electron diffraction pattern of the amorphous oxide semiconductor film. Furthermore, a halo pattern is shown but a spot is not shown in a nanobeam electron diffraction pattern of the amorphous oxide semiconductor film.

[0334] Note that an oxide semiconductor film may have a structure having physical properties between the nc-OS film and the amorphous oxide semiconductor film. The oxide semiconductor film having such a structure is specifically referred to as an amorphous-like oxide semiconductor (amorphous-like OS) film.

[0335] In a high-resolution TEM image of the amorphous-like OS film, a void may be seen. Furthermore, in the high-resolution TEM image, there are a region where a crystal part is clearly observed and a region where a crystal part is not observed. In the amorphous-like OS film, crystallization by a slight amount of electron beam used for TEM observation occurs and growth of the crystal part is found sometimes. In contrast, crystallization by a slight amount of electron beam used for TEM observation is less observed in the nc-OS film having good quality.

[0336] Note that the crystal part size in the amorphous-like OS film and the nc-OS film can be measured using high-resolution TEM images. For example, an $InGaZnO_4$ crystal has a layered structure in which two Ga—Zn—O layers are included between In—O layers. A unit cell of the $InGaZnO_4$ crystal has a structure in which nine layers of three In—O layers and six Ga—Zn—O layers are layered in the c-axis direction. Accordingly, the spacing between these adjacent layers is equivalent to the lattice spacing on the (009) plane (also referred to as a d value). The value is calculated to be 0.29 nm from crystal structure analysis. Thus, each of the lattice fringes in which the spacing therebetween is from 0.28 nm to 0.30 nm corresponds to the a-b plane of the $InGaZnO_4$ crystal, focusing on the lattice fringes in the high-resolution TEM image.

[0337] Note that an oxide semiconductor film may be a stacked film including two or more films of an amorphous oxide semiconductor film, an amorphous-like OS film, a microcrystalline oxide semiconductor film, and a CAAC-OS film, for example.

[0338] The structure described above in this embodiment can be combined with any of the structures described in the Other Embodiments as Appropriate.

Embodiment 5

[0339] An imaging device in one embodiment of the present invention and a semiconductor device including the imaging device can be used for display devices, personal computers, or image reproducing devices provided with recording media (typically, devices that reproduce the content of recording media such as digital versatile discs (DVD) and have displays for displaying the reproduced images). Furthermore, as electronic devices that can include the imaging device in one embodiment of the present invention and the semiconductor device including the imaging device, cellular phones, game machines (including portable game machines), portable information terminals, e-book readers, cameras such as video cameras and digital still cameras, goggle-type displays (head mounted displays), navigation systems, audio reproducing devices (e.g., car audio systems and digital audio players), copiers, facsimiles, printers, multifunction printers, automated teller machines (ATM), vending machines, and the like can be given. FIGS. **34**A to **34**F illustrate specific examples of these electronic devices.

[0340] FIG. **34**A illustrates a portable game machine, which includes housings **901** and **902**, display portions **903** and **904**, a microphone **905**, speakers **906**, an operation key **907**, a stylus **908**, a camera **909**, and the like. Although the portable game machine in FIG. **34**A includes the two display portions **903** and **904**, the number of display portions included in the portable game machine is not limited to this. The imaging device in one embodiment of the present invention can be used for the camera **909**.

[0341] FIG. **34**B illustrates a portable data terminal, which includes a first housing **911**, a display portion **912**, a camera **919**, and the like. The touch panel function of the display portion **912** enables input and output of information. The imaging device in one embodiment of the present invention can be used for the camera **919**.

[0342] FIG. **34**C illustrates a wrist-watch-type information terminal, which includes a housing **931**, a display portion **932**, a wristband **933**, a camera **939**, and the like. The display portion **932** may be a touch panel. The imaging device in one embodiment of the present invention can be used for the camera **939**.

[0343] FIG. **34**D illustrates a cellular phone, which includes a display portion **952**, a microphone **957**, a speaker **954**, a camera **959**, an input/output terminal **956**, an operation button **955**, and the like in a housing **951**. The imaging device in one embodiment of the present invention can be used for the camera **959**.

[0344] FIG. **34**E illustrates a digital camera, which includes a housing **961**, a shutter button **962**, a microphone **963**, a light-emitting portion **967**, a lens **965**, and the like. The imaging device in one embodiment of the present invention can be used provided in a focus of the lens **965**.

[0345] FIG. **34**F illustrates a video camera, which includes a first housing **971**, a second housing **972**, a display portion **973**, operation keys **974**, a lens **975**, a joint **976**, and the like. The operation keys **974** and the lens **975** are provided in the first housing **971**, and the display portion **973** is provided in the second housing **972**. The first housing **971** and the second housing **972** are connected to each other with the joint **976**, and an angle between the first housing **971** and the second housing **972** can be changed with the joint **976**. An image displayed on the display portion **973** may be switched in accordance with the angle between the first housing **971** and the second housing **972** at the joint **976**. The imaging device in one embodiment of the present invention can be provided in a focus of the lens **975**.

[0346] This embodiment can be combined with any of the other embodiments described in this specification as appropriate.

[0347] This application is based on Japanese Patent Application serial No. 2015-016743 filed with Japan Patent Office on Jan. 30, 2015, the entire contents of which are hereby incorporated by reference.

What is claimed is:

1. An imaging device comprising:

a first transistor;

a second transistor;

a third transistor;

a fourth transistor; and

a photoelectric conversion element,

wherein one electrode of the photoelectric conversion element is electrically connected to one of a source electrode and a drain electrode of the first transistor,

wherein the one electrode of the photoelectric conversion element is electrically connected to one of a source electrode and a drain electrode of the third transistor,

wherein the other of the source electrode and the drain electrode of the first transistor is electrically connected to a gate electrode of the second transistor,

wherein one of a source electrode and a drain electrode of the second transistor is electrically connected to one of a source electrode and a drain electrode of the fourth transistor,

wherein the other electrode of the photoelectric conversion element is electrically connected to a first wiring,
wherein a gate electrode of the first transistor is electrically connected to a second wiring, and
wherein when a potential supplied to the first wiring is HVDD, the highest value of a potential supplied to the second wiring is lower than HVDD.

2. The imaging device according to claim **1**,
wherein the other of the source electrode and the drain electrode of the second transistor is electrically connected to a third wiring, and
wherein when the potential supplied to the first wiring is HVDD, a potential supplied to the third wiring is VDD, and HVDD is higher than VDD, the highest value of the potential supplied to the second wiring is VDD.

3. The imaging device according to claim **1**,
wherein the first transistor and the third transistor each include an oxide semiconductor in an active layer,
wherein the oxide semiconductor includes In, Zn, and M, and
wherein M is Al, Ti, Ga, Sn, Y, Zr, La, Ce, Nd, or Hf.

4. The imaging device according to claim **1**,
wherein the second transistor and the fourth transistor each include silicon in an active layer or an active region.

5. An electronic device comprising:
the imaging device according to claim **1**; and
a display device.

6. An imaging device comprising:
a first transistor;
a second transistor;
a third transistor;
a fourth transistor; and
a photoelectric conversion element,
wherein one electrode of the photoelectric conversion element is electrically connected to one of a source electrode and a drain electrode of the first transistor,
wherein the one electrode of the photoelectric conversion element is electrically connected to one of a source electrode and a drain electrode of the third transistor,
wherein the other of the source electrode and the drain electrode of the first transistor is electrically connected to a gate electrode of the second transistor,
wherein one of a source electrode and a drain electrode of the second transistor is electrically connected to one of a source electrode and a drain electrode of the fourth transistor,
wherein the other electrode of the photoelectric conversion element is electrically connected to a first wiring,
wherein a gate electrode of the first transistor is electrically connected to a second wiring,
wherein when a potential supplied to the first wiring is HVDD, the highest value of a potential supplied to the second wiring is lower than HVDD, and
wherein the first transistor and the third transistor are provided over the second transistor and the fourth transistor.

7. The imaging device according to claim **6**,
wherein the other of the source electrode and the drain electrode of the second transistor is electrically connected to a third wiring, and
wherein when the potential supplied to the first wiring is HVDD, a potential supplied to the third wiring is VDD, and HVDD is higher than VDD, the highest value of the potential supplied to the second wiring is VDD.

8. The imaging device according to claim **6**,
wherein the first transistor and the third transistor each include an oxide semiconductor in an active layer,
wherein the oxide semiconductor includes In, Zn, and M, and
wherein M is Al, Ti, Ga, Sn, Y, Zr, La, Ce, Nd, or Hf.

9. The imaging device according to claim **6**,
wherein the second transistor and the fourth transistor each include silicon in an active layer or an active region.

10. An electronic device comprising:
the imaging device according to claim **6**; and
a display device.

11. An imaging device comprising:
a first transistor;
a second transistor;
a third transistor;
a fourth transistor; and
a photoelectric conversion element,
wherein one electrode of the photoelectric conversion element is electrically connected to one of a source electrode and a drain electrode of the first transistor,
wherein the one electrode of the photoelectric conversion element is electrically connected to one of a source electrode and a drain electrode of the third transistor,
wherein the other of the source electrode and the drain electrode of the first transistor is electrically connected to a gate electrode of the second transistor,
wherein one of a source electrode and a drain electrode of the second transistor is electrically connected to one of a source electrode and a drain electrode of the fourth transistor,
wherein the other electrode of the photoelectric conversion element is electrically connected to a first wiring,
wherein a gate electrode of the first transistor is electrically connected to a second wiring,
wherein when a potential supplied to the first wiring is HVDD, the highest value of a potential supplied to the second wiring is lower than HVDD,
wherein the first transistor and the third transistor are provided over the second transistor and the fourth transistor, and
wherein the photoelectric conversion element is provided over the first transistor and the third transistor.

12. The imaging device according to claim **11**,
wherein the other of the source electrode and the drain electrode of the second transistor is electrically connected to a third wiring, and
wherein when the potential supplied to the first wiring is HVDD, a potential supplied to the third wiring is VDD, and HVDD is higher than VDD, the highest value of the potential supplied to the second wiring is VDD.

13. The imaging device according to claim **11**,
wherein the first transistor and the third transistor each include an oxide semiconductor in an active layer,
wherein the oxide semiconductor includes In, Zn, and M, and
wherein M is Al, Ti, Ga, Sn, Y, Zr, La, Ce, Nd, or Hf.

14. The imaging device according to claim **11**,
wherein the second transistor and the fourth transistor each include silicon in an active layer or an active region.

15. An electronic device comprising:
the imaging device according to claim **11**; and
a display device.

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