United States Patent

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[54] **CONFLICTING PHASE ERROR DETECTOR**
10 Claims, 5 Drawing Figs.

[52] U.S. Cl. 340/46
[51] Int. Cl. G08g 1/097
[50] Field of Search 340/46; 307/218

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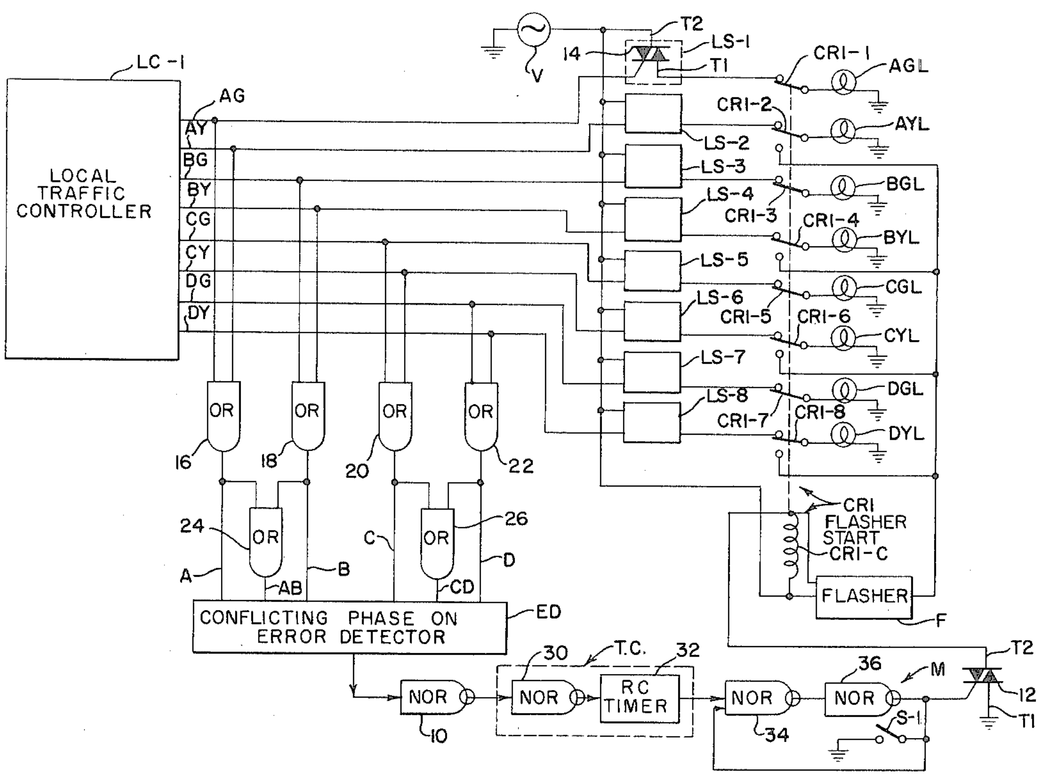
ABSTRACT: A system for traffic signal controllers is provided to detect the occurrence of coincident command signals that would cause right-of-way signals to be displayed for conflicting or intersecting traffic lanes or traffic paths or courses. For such detection NOR logic means are provided with input connections to controller command signal output lines to produce an output when different right-of-way command signals are coincident. The output from the NOR logic means is employed to disconnect all right-of-way traffic lamps and to connect all caution lamps to an energy source through a flasher.



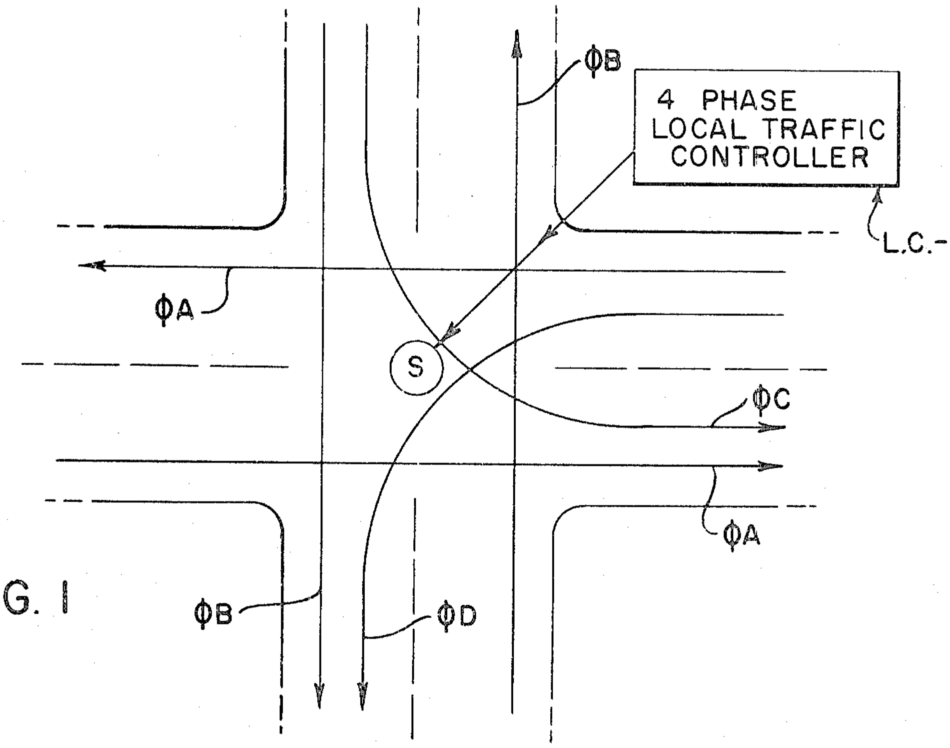


FIG. 1

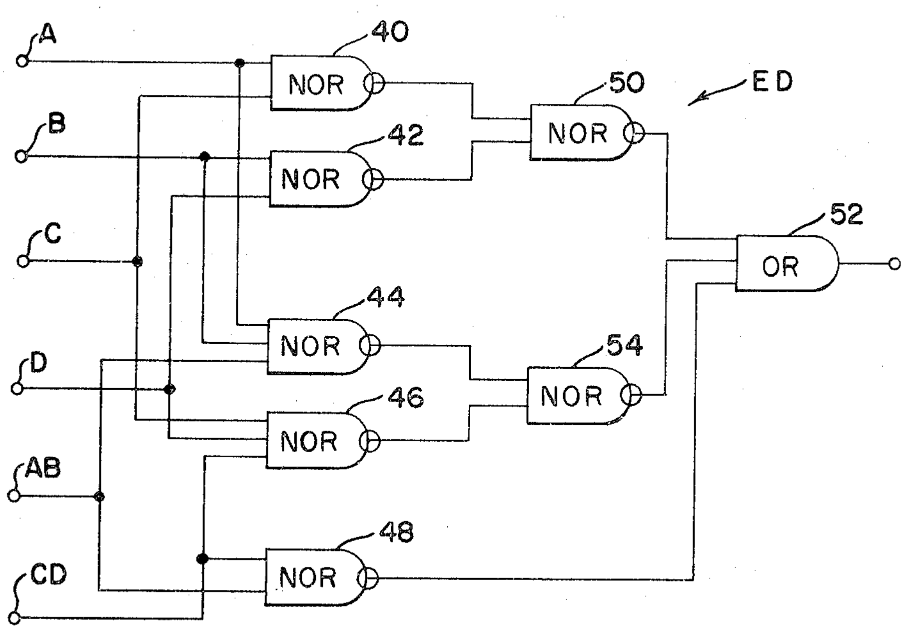


FIG. 3

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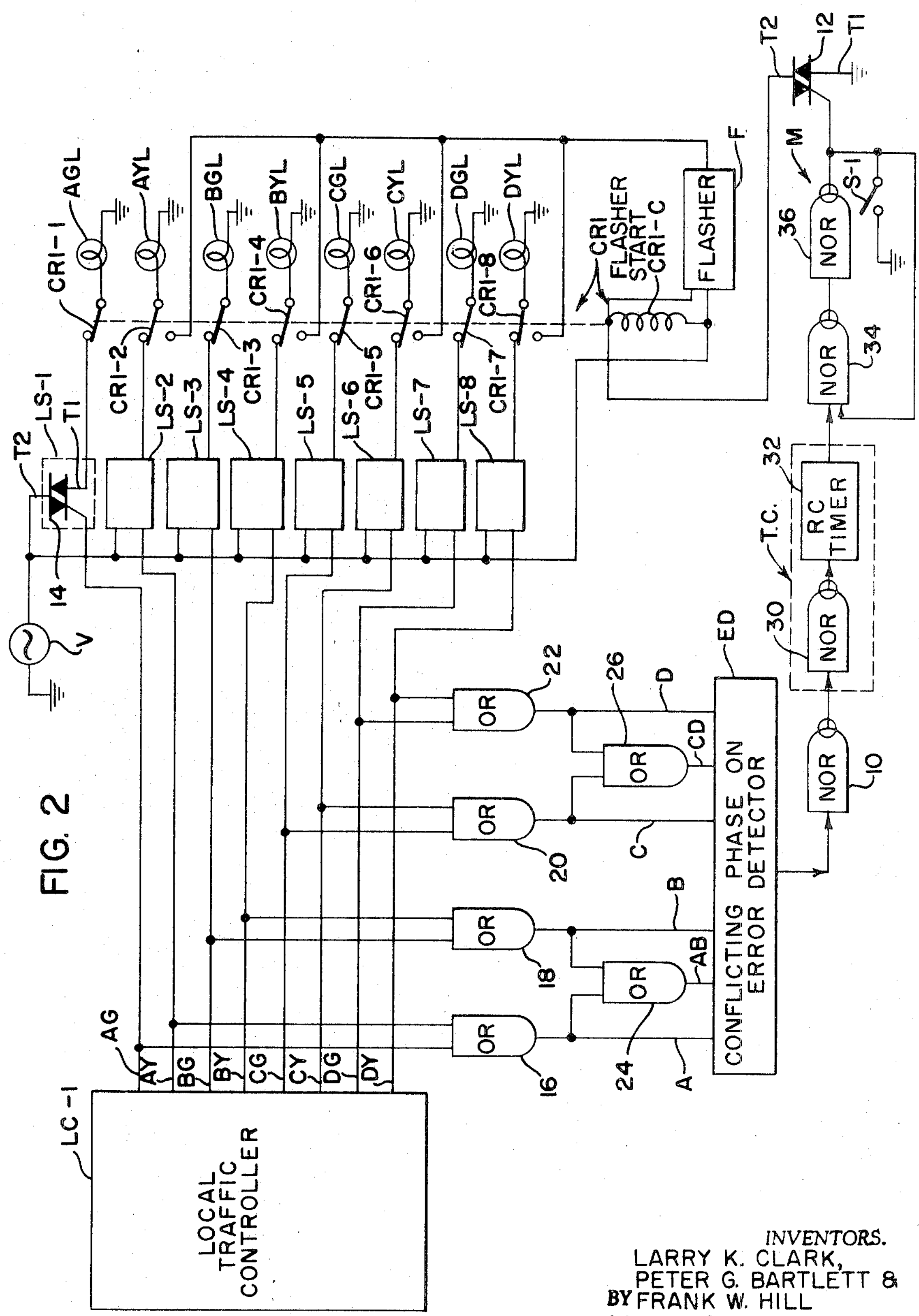

FIG. 2

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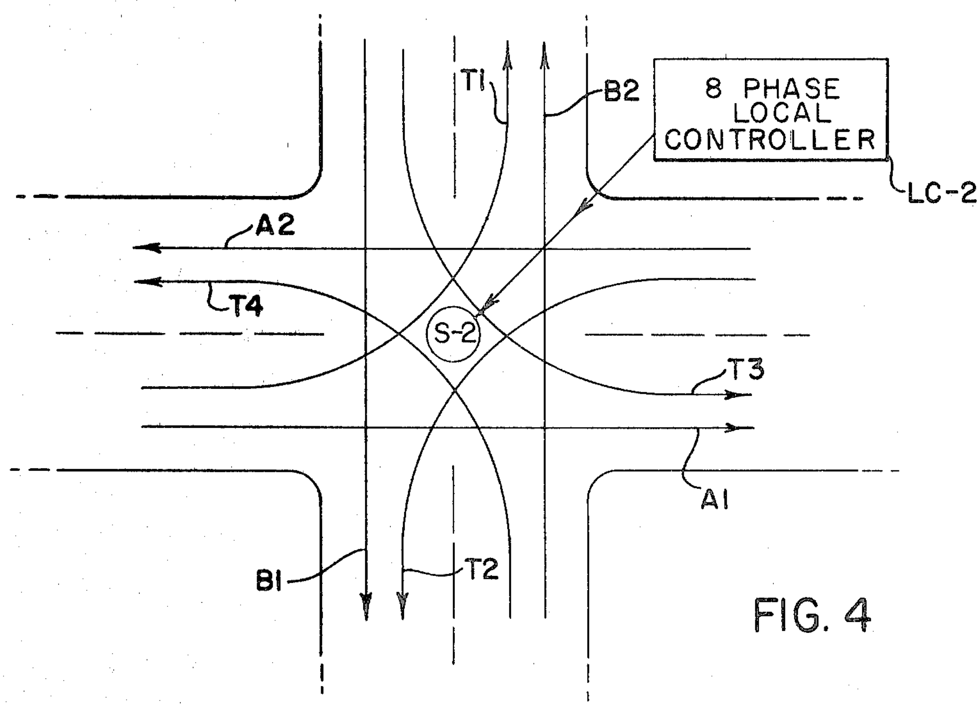

FIG. 4

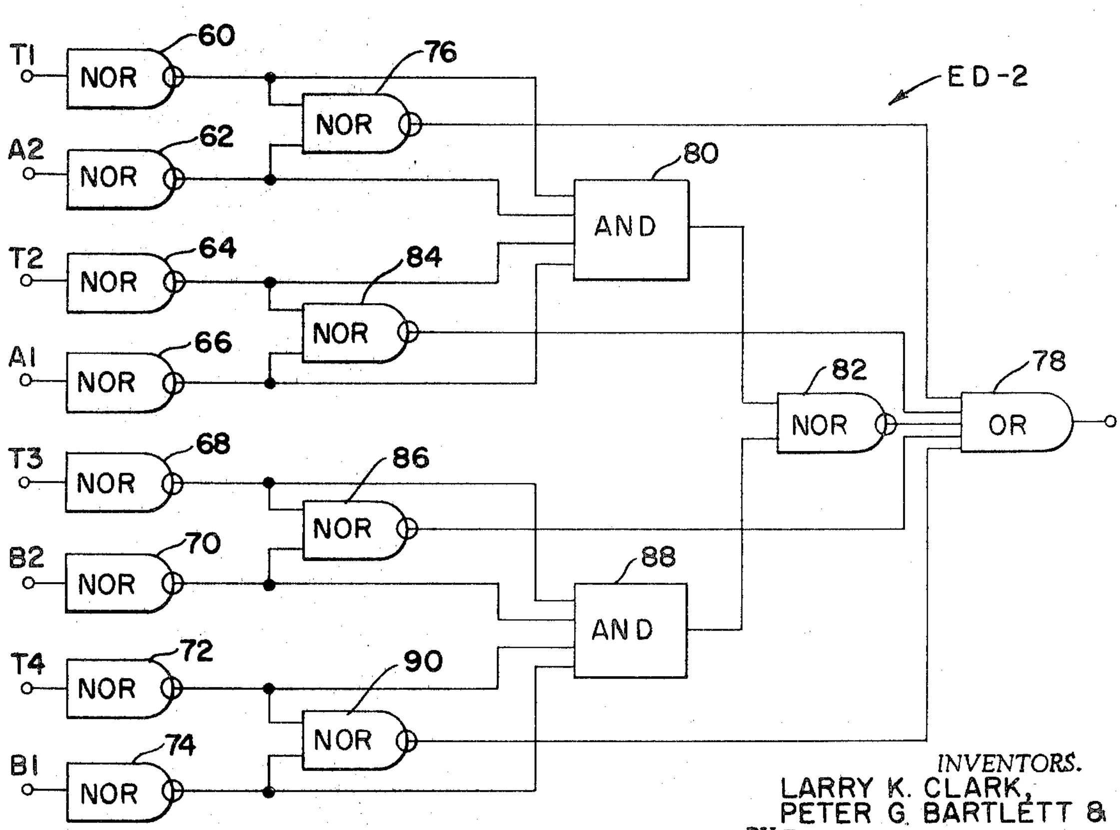

FIG. 5

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CONFLICTING PHASE ERROR DETECTOR

This invention relates to the art of traffic control and, more particularly, to means for detecting whether two or more conflicting traffic movements, are concurrently being awarded right-of-way signals.

The invention is particularly applicable for energizing a flashing warning signal, such as a yellow light of a traffic signal, to all traffic approaching an intersection where an error has occurred, although the invention is not limited thereto and may be used wherever it is desired to prevent conflicting traffic movements from concurrently receiving right-of-way signals.

In a traffic control system a traffic signal light serves to provide right-of-way (green), caution (yellow), and stop (red) visual displays to traffic approaching the intersection. A traffic controller serves to energize the traffic light to sequentially provide the green, yellow and red displays in conflicting or intersecting traffic lanes, such as in a main street and in an intersecting cross street. The traffic controller normally operates in successive phases, each corresponding to traffic movement in one of the intersecting lanes or streets or traffic courses in the case of left-turn passage of vehicles. Obviously, in the event that both the main street and cross street green lights are concurrently energized, there would result a disruption in traffic flow. This may result, for example, due to a malfunction in the traffic controller or the associated circuitry used for energizing the traffic signal lights. Accordingly, it is desirable in the event the traffic signal lights are commanded to display green signals in intersecting streets for conflicting traffic movements, such as main street and cross street in the example given above, that some means be provided for detecting this condition and in response thereto providing an error signal, which may be used, for example, to energize a warning signal.

Error detection circuitry known heretofore for use with traffic controllers has taken the form of interlocks or interconnecting contacts on various relays to prevent the conflicting signals from appearing. With such apparatus should a relay fail to function, or a contact on a relay weld, the conflicting signals will still result. These relays are normally the same relays that are used for switching the AC line voltage directly to the traffic signals. Hence, such relay mechanisms were not a true error detection circuit, since they do not serve a separate function with the single purpose of providing an output indication of an error.

The present invention is directed toward an error detection circuit which serves the independent function of monitoring traffic signal commands obtained from a traffic signal controller and then providing an error signal when the commands are such to concurrently display right-of-way signals for conflicting traffic movements.

The present invention contemplates that a traffic control system serve to control traffic flow through an intersection of at least two conflicting traffic lanes, and having signal light means for, upon command by the control signal, displaying a right-of-way signal in one of the lanes. It is further contemplated that a traffic signal control means serve to provide the control signal for each of the traffic lanes.

In accordance with the present invention, the improvement incorporates solid-state error detector means which is coupled to the traffic signal control means for developing an error signal in response to coinciding command signals, commanding the signal means to display right-of-way signals in conflicting traffic lanes.

In accordance with a more limited aspect of the present invention, the error signal is used to operate an error indicating means, such as a flashing yellow light, to provide a warning signal in each of the conflicting traffic lanes for the duration of the error signal.

In accordance with a further aspect of the present invention, a timing means serves to time a predetermined period of time before the error signal causes a warning signal to be displayed.

The primary object of the present invention is to provide a conflicting error detection system which is relatively inexpensive to manufacture and economical to operate.

It is a still further object of the present invention to provide an error detection system using solid-state logic circuitry to minimize power requirements, as well as to minimize maintenance normally attributed to electromechanical systems.

It is a still further object of the present invention to provide a conflicting error detection circuit which has as its sole purpose to monitor the command signals from a traffic controller, and then provide an error signal in the event that conflicting traffic movements are to receive right-of-way signals.

It is a still further object of the present invention to provide an error detection system which may be used for both conflicting and compatible traffic movement, such as in an eight-phase, quad left-turn traffic control system.

The foregoing objects and advantages of the invention will become apparent from the following description of the preferred embodiments of the invention as read in connection with the accompanying drawings in which:

FIG. 1 illustrates one application of the invention in conjunction with four conflicting traffic lanes;

FIG. 2 is a combined schematic block diagram illustration of the preferred embodiment of the invention;

FIG. 3 is a schematic illustration of the error detector circuit used in FIG. 2;

FIG. 4 is a schematic illustration of another application of the invention to an eight-phase, quad left-turn traffic control system; and,

FIG. 5 is a schematic illustration of the error detector circuit to be used for the eight-phase, quad left-turn traffic control system.

GENERAL DESCRIPTION

Referring now to the drawings, which are presented for illustrating preferred embodiments of the invention only and not for limiting same, FIG. 1 illustrates an intersection of four conflicting traffic movements; to wit, in traffic paths or courses designated by reference characters ΦA, ΦB, ΦC and ΦD. Phases A and B may be respectively considered as in the main street and cross street directions of traffic flow. Traffic movement D is a left-turn from main street A into cross street B and, similarly, traffic movement C is a left turn from cross street B into main street A. All of these traffic movements are conflicting. That is, if any pair of these traffic movements receive right-of-way signals at the same time, the traffic movements will conflict with each other, resulting in a disruption of traffic flow through the intersection. A traffic signal S is provided to display green, yellow and red signals for each of the traffic movements under control of command signals received from a four-phase local controller LC-1.

Reference is now made to FIG. 2 which illustrates a local traffic controller LC-1 having eight output circuits AG, AY, BG, BY, CG, CY, DG, and DY, each for carrying a command signal for respectively actuating load switches LS-1, LS-2, LS-3, LS-4, LS-5, LS-6, LS-7 and LS-8. These load switches serve, when actuated, to respectively connect an associated load AGL, AYL, BGL, BYL, CGL, CYL, DGL and DYL, with an alternating current voltage source V. The outputs of the local traffic controller are applied through a plurality of OR gates to conflicting traffic error detector circuit ED, which has its output coupled through a NOR-gate 10 to a timer control circuit TC. Timer control circuit TC, in turn, is coupled through a memory circuit M to a triac 12 which, when biased into conduction, serves to apply alternating current voltage from source V across coil CR1-C of a relay CR1. Briefly, during operation, the local controller LC-1 serves to sequentially apply a direct current control signal on its output terminals for purposes of sequentially energizing the associated load switches LS-1 through LS-8. The error detector ED serves to monitor the operation of the output circuits AG through DY for purposes of detecting whether conflicting loads are being energized. In the event, for example, that green light AGL and green light BGL are concurrently energized due to command signals being present on output terminals AG and BG of local controller LC-1, the error detector circuit ED applies a binary "1" signal into the input of NOR-gate **10**. This triggers an operation, as will be described in detail hereinafter, wherein relay CR1 becomes energized to couple flasher F to each of the yellow lights AYL, BYL, CYL and DYL so that these lights alternately flash on and off, providing a warning signal to each of the conflicting traffic movements.

TRAFFIC CONTROL SYSTEM

In the embodiment illustrated in FIG. 2, the traffic control system includes traffic signal lights AGL through DYL for traffic movements A through D. Thus, for example, lights AGL and AYL respectively serve as the green light for lane A and the yellow light for lane A. The traffic controller LC-1 provides positive direct current voltage signals on its output circuits AG through DY in a sequential fashion so that the associated signal lights AGL through DYL become sequentially energized. Typically, such traffic controllers incorporate direct current logic circuitry for determining when the green and yellow terminals for each of the traffic courses A, B, C and D are to be energized, and for what duration. An example of such a traffic controller is found in the U.S. Pat. to G. D. Hendricks, No. 3,344,398, which is assigned to the same assignee as the present invention. Load switches LS-1 through LS-8 each incorporate a triac. Thus, switch LS-1 includes a triac **14** having its gate connected to terminal AG of local controller LC-1 and its terminal T2 connected through alternating current voltage source V to ground. Terminal T1 of triac **14** is connected through normally closed relay contacts CR1-1 of relay CR1 to the traffic course A green light AGL. The remaining load switches LS-2 to LS-8 are connected in a similar fashion to source V, as well as to output terminals AY through DY. Also, the outputs of load switches LS-2 through LS-8 are respectively coupled through normally closed relay contacts CR1-2 through CR1-8 and then to the associated signal lights AYL through DYL, as shown in FIG. 2.

Controller output terminals AG and AY are coupled through an OR-gate **16** having its output connected to input terminal A of the conflicting traffic detector ED. Similarly, output terminals BG and BY are coupled through an OR-gate **18** having its output connected to input terminal B or error detector ED. Also, output terminals CG and CY are coupled through an OR-gate **20** having its output coupled to input terminal C of error detector ED. Also, output terminals DG and DY are coupled through an OR-gate **22** having its output connected to input terminal D of error detector ED. The outputs of OR-gates **16** and **18** are also coupled through an OR-gate **24** having its output connected to input terminal AB of error detector ED. Similarly, the outputs of OR-gates **20** and **22** are coupled through an OR-gate **26** having its output connected to input terminal CD of error detector ED. The output of error detector ED, which is illustrated in greater detail in FIG. 3, is coupled to the input of NOR-gate **10** having its output coupled to the timer control circuit TC. NOR-gate **10**, as well as the remaining NOR gates disclosed herein, preferably take the form of the resistor-transistor logic RTL NOR gate illustrated in Figure 7.5, at page 178, of General Electric's Transistor Manual, 7th Edition. The timer control circuit TC includes a NOR-gate **30**, used as a signal inverter, together with an RC timing circuit **32**. This timing circuit may take various forms, such as a unijunction relaxation oscillator circuit, as illustrated in Figure 13.18, at page 313, of General Electric's Transistor Manual, 7th Edition. Briefly, that oscillator circuit includes a capacitor which is normally short circuited by a binary "1" signal from NOR-gate **30**. However, whenever the output binary signal of NOR-gate **30** becomes a binary "0" signal this short circuit is removed whereupon the capacitor charges toward the value of a direct current voltage source. When the level of the voltage stored reaches the peak point voltage of the unijunction transistor, the capacitor discharges through the emitter to base B1 of the transistor and a positive voltage pulse appears across a load resistor. This positive pulse may be considered as a "1" signal. Whenever the capacitor has not discharged through the transistor unijunction, the output of timer control circuit TC is at a ground or binary "0" level.

The output of the timer control circuit TC is applied to a NOR-gate **34** in memory circuit M. This memory circuit includes an additional NOR-gate **36** which is coupled to the output of NOR-gate **34** and has a feedback path for defining a bistable multivibrator circuit. The output of NOR-gate **36** is also coupled through a normally open switch S-1 to ground potential. Closure of this switch serves to reset memory M, as will be described in detail with respect to the operation of the circuitry.

The output of memory M is coupled to the gate of triac **12** having its terminal T1 connected to ground and its terminal T2 connected through relay coil CR1-C to voltage source V, as well as to flasher F. The other side of flasher F is coupled through the normally open side of relay contacts CR1-2, CR1-4, CR1-6 and CR1-8. The flasher F may take any suitable form, such as a motor controlled circuit interrupter, for alternately opening and closing the circuit between source V and the above-mentioned normally open relay contacts. Such a flasher commences operation upon closure of these relay contacts.

CONFLICTING TRAFFIC ERROR DETECTOR

Reference is now made to FIG. 3 which illustrates the circuitry within error detector ED of FIG. 2. This error detector includes six inputs; to wit, terminals A, B, C, D, AB and CD. These input terminals are connected to various combinations of NOR-gates **40, 42, 44, 46** and **48**. Thus, terminal A is connected to one input each of NOR-gates **40** and **44**. Terminal B is connected to one input each of NOR-gates **42** and **44**. Terminal C is connected to one input each of NOR-gates **40** and **46**. Terminal D is connected to one input each of NOR-gates **42** and **46**. Terminal AB is connected to one input each of NOR-gates **44** and **48**. Lastly, terminal CD is connected to one input each of NOR-gates **46** and **48**. The outputs of NOR-gates **40** and **42** are coupled to the input of a NOR-gate **50** having its output connected to the input of an OR-gate **52**. Similarly, the outputs of NOR-gates **44** and **46** are coupled to the input of a NOR-gate **54** having its output connected to the input of OR-gate **52**. Lastly, the output of NOR-gate **48** is connected to one input of OR-gate **52**. The output of OR-gate **52** is connected to the input of NOR-gate**1 0** in FIG. 2.

OPERATION

During the operation of the circuitry illustrated in FIGS. **1**, **2** and **3**, it may be assumed that initially the local controller LC-1 has energized its main street A green terminal AG with a positive direct current signal. This signal is coupled to the gate of triac **14** in load switch LS-1 so as to gate this triac into conduction. Accordingly, alternating current voltage from source V is applied through the triac and normally closed relay contacts CR1-1, to energize the main street A green lamp AGL. The positive signal on terminal AG is applied through OR-gate **16** to input terminal A of the error detector ED. This signal is also applied from the output of OR-gate **16** through OR-gate **24** to the input terminal AB of error detector ED. Accordingly, binary "1" signals are applied to the input terminals A and AB of the error detector circuitry shown in FIG. 3. The binary "1" signal on input terminal A is inverted by NOR-circuit **40** to apply a binary "0" signal to one input of NOR-circuit **50**. Since, however, the input on terminal B is a binary "0" signal, which is the normal signal when traffic in cross street B is not receiving a right-of-way signal, NOR-gate **42** applies a binary "1" signal to the input of NOR-gate **50**. Accordingly, the output of NOR-gate **50** carries a binary "0" signal which is reflected to OR-gate **52**. Terminals C, D and CD also carry binary "0" signals and hence the output of

NOR-gate 46 carries a binary "1" signal and the output of NOR-gate 54 carries a binary "0" signal. Since input terminal AB carries a binary "1" signal, then the output of NOR-gate 48 carries a binary "0" signal. Since all of the inputs to OR-gate 52 are binary "0" signals, the output of this gate is also a binary "0" signal which is the correct indication for a situation wherein conflicting traffic movements are not receiving right-of-way signals from the traffic signal S.

With reference to FIG. 1, it can be seen that traffic movements A and B conflict and accordingly should not be awarded right-of-way intervals at the same time. Assume now that output terminals AG and BG are concurrently energized by local controller LC-1. In such case, input terminals A, B and AB will all carry binary "1" input signals. Since terminals A and B both carry binary "1" signals, the outputs of NOR-gates 40 and 42 carry binary "0" signals. Accordingly, the output of NOR-circuit 50 carries a binary "1" signal which is reflected through OR-gate 52 and is applied to the input of NOR-gate 10 in FIG. 2. This is indicative of an error condition of conflicting traffic movements receiving right-of-way signal displays.

Since a binary "1" signal has been applied to its input, NOR-gate 10 applies a binary "0" signal to the input of NOR-gate 30, which in turn, applies a binary "1" signal to the input of the RC timer 32 in the timer control circuit TC. The timing circuit 32 now times a predetermined period of time and then provides a binary "1" signal pulse which is applied to the input of NOR-gate 34 in memory M. This causes the output of NOR-gate 36 to become a binary "1" signal and this state of the memory M is retained due to the feedback circuit until switch S-1 is momentarily closed to return the memory to its normal condition. The binary "1" signal obtained from the output of NOR-gate 36 serves to gate triac 12 into conduction to thereby energize relay coil CR1-C and apply power to start flasher F. This causes all the movable contacts of relay CR1 to move in a downward direction, as viewed in FIG. 2, so that the previously open side of relay contacts CR1-2, CR1-4, CR1-6 and CR1-8 become closed so that flasher F can then alternately energize and deenergize yellow lamps AYL, BYL, CYL and DYL. These yellow lamps will stay in this flashing condition displaying warning signals to all conflicting traffic movements A, B, C and D until switch S-2 is momentarily closed to restore the memory circuit to the condition where it applies a binary "0" signal to the gate of triac 12. As the alternating current voltage obtained from source V crosses through a zero level, the triac will cease to conduct, deenergizing relay CR1. The operation in conjunction with detecting conflicting go signal conditions for any of the combinations of conflicting traffic movements A, B, C and D is the same as that discussed above with respect to traffic lanes A and B, and no further description is deemed necessary for a complete understanding of this invention.

SECOND EMBODIMENT

Reference is now made to FIGS. 4 and 5 which illustrate a second embodiment of the invention. FIG. 4 schematically illustrates an eight-phase, quad left-turn traffic control system wherein signal light S2 is controlled by an eight-phase local controller LC-2. From an inspection of FIG. 4, it will be noted that there are both conflicting traffic movements and compatible traffic movements. Conflicting movements, of course, are movements which, if given right-of-way signals, will result in a disruption of traffic flow. Compatible traffic movements are those which may receive right-of-way signals at the same time without disruption in traffic flow. Thus, for example, with reference to FIG. 4, traffic courses A1 and A3 are compatible, traffic courses B1 and B2 are compatible; left-turn courses T3 and T4 are compatible; left-turn courses T1 and T2 are compatible; course A2 and course T2 are compatible; phase A1 and phase T1 are compatible; phase B2 and course T4 are compatible; and, course B1 and course T3 are compatible. Also, with reference to FIG. 4, it will be noted that the following traffic courses are conflicting. A1 with T2, A2 with T1, B1 with T4 and B2 with T3. It will further be noted that the group of traffic courses consisting of A1, A2, T1 and T2 are conflicting with the group of courses consisting of B1, B2, T3 and T4.

Conflicting traffic course error detector ED-2 serves essentially the same purpose for an eight-phase, quad left-turn system as the error detector circuit ED serves for a four-phase conflicting traffic control system. However, since, as discussed above, an eight-phase, quad left-turn system has both conflicting phases and compatible phases, the error detector circuit should recognize right-of-way signals being displayed to compatible traffic movements as being proper, but right-of-way signals being displayed to conflicting traffic movements as being an error condition. This function is performed by error detector ED-2.

Error detector ED-2, like error detector ED, illustrated in FIG. 3, has a plurality of input terminals which are energized by local controller LC-2 by a positive direct current signal, i.e., a binary "1" signal, when an associated traffic movement is to receive a right-of-way signal. As shown in FIG. 5, these input terminals are labeled T1, A2, T2, A1, T3, B2, T4 and B1, each representative of the like numbered traffic courses shown in FIG. 4. The input terminals representative of conflicting courses are grouped together; to wit, terminals T1 and A2, terminals T2 and A1, terminals T3 and B3, and terminals T4 and B1. These terminals are coupled to the inputs of NOR-gates 60 through 74 which serve as signal inverters. More particularly, the inputs of NOR-gates 60 through 74 are coupled to terminals T1, A2, T2, A1, T3, B2, T4 and B1, respectively. The outputs of NOR-gates 60 and 62 are coupled to the inputs of a NOR-gate 76 having its output coupled to the input of an OR-gate 78, the output of which is coupled to the input of a NOR gate such as NOR-gate 10, of the circuitry shown in FIG. 2.

The outputs of NOR-gates 60 and 62 are also connected to inputs of an AND-gate 80 having its output connected through a NOR-gate 82 to the input of OR-gate 78. The outputs of NOR-gates 64 and 66 are coupled to the inputs of a NOR-gate 84 having its output connected to one input of OR-gate 78. The outputs of NOR-gates 64 and 66 are also connected to inputs of AND-gate 80.

The outputs of NOR-gates 68 and 70 are connected to the inputs of NOR-gate 86 having its output connected to one input of OR-gate 78. The outputs of NOR-gate 68 and 70 are also connected to two inputs of AND-gate 88. The outputs of NOR-gates 72 and 74 are applied to the inputs of NOR-gate 90 having its output connected to one input of OR-gate 78. The outputs of NOR-gates 72 and 74 are also connected to inputs of AND-gate 88.

Preferably, the error detector ED-2 is coupled to a traffic controller in a manner similar to that of error-detector ED in FIG. 2. Thus, the local controller LC-2 may take the form of four, two-phase controllers or two, four-phase controllers or a single, eight-phase controller. In any case, the controller circuitry should have the capability of providing outputs similar to those of the eight outputs with reference to local controller LC-1 of FIG. 2. Each of these outputs are connected through load switches, similar to load switches LS-1 through LS-8, to energize traffic signal lamps as in the case of lamps AGL through DYL of FIG. 2. This circuitry is not shown with reference to FIG. 5 for purposes of simplifying the description of the invention.

The operation of error detector ED-2 is substantially similar to that of error detector ED of FIG. 2. Thus, for example, if input terminals T1 and A2 receive binary "1" signals representative that conflicting traffic courses T1 and T2 are being awarded right-of-way signals, then NOR-gate 76 provides a binary "1" signal which is reflected through OR-gate 78 as an error signal. As in the case of FIG. 2, this will cause the operation of triac 12 to energize a relay CR1, whereupon switches are actuated to display flashing yellow signals to all approaches to the intersection shown in FIG. 4. However, in the event compatible traffic courses, such as turns T1 and T2, are being awarded right-of-way signals, then NOR-gate **76** and NOR-gate **84** have binary "0" signals on their outputs which are reflected through OR-gate **78** and no error signal is provided. Thus, in this case, all terminals carry binary "1" signals with the exception of terminals T1 and T2. Accordingly, the outputs of NOR-gates **60** and **64** carry binary "0" signals and the outputs of NOR-gate **62** and **66** through **74** carry binary "1" signals. Since one of its inputs has a binary "1" signal, the outputs of NOR-gate **76** and **84** each carry "0" signals for application to the input of OR-gate **78**. Since the outputs of NOR-gate **60** and **64** carry binary "0" signals and the outputs of NOR-gates **62** and **66** carry binary "1" signals, only two of the four inputs of AND-gate **80** carry binary "1" signals and, accordingly, the output of AND-gate **80** carries a binary "0" signal for application to one input of NOR-gate **82**. However, since each of the outputs of NOR-gates **68** through **74** carry binary "1" signals, AND-gate **88** applies a binary "1" signal to the other input of NOR-gate **82**, whereupon all inputs to OR-gate **78** are binary "0" signals, which is the correct condition for no error with compatible traffic courses T1 and T2 being awarded right-of-way signals.

The operation that results with another combination of compatible traffic courses being awarded right-of-way signals and/or conflicting traffic courses being awarded right-of-way signals is substantially the same as discussed above and, accordingly, no further description is deemed necessary for a complete understanding of the invention.

Although the invention has been shown in connection with preferred embodiments, it will be readily apparent to those skilled in the art that various changes in form and arrangements of parts may be made to suit requirements without departing from the spirit and scope of the invention as defined by the appended claims.

We claim:

1. In a traffic control system for controlling traffic flow through an intersection of at least two conflicting traffic courses and having signal light means for, upon command by a command signal, displaying a right-of-way signal in one of said traffic courses and traffic signal control means for providing a said command signal for each traffic course for which a right-of-way signal is to be received; the improvement comprising:

NOR logic means associated with conflicting traffic courses for providing an output signal indicative that said controller means has provided coincident command signals for causing right-of-way signals to be displayed for such conflicting traffic courses; and,

means associated with the output of said NOR logic means for providing an error signal whenever said NOR logic means provides such an output signal.

2. In a traffic control system the improvement as set forth in claim **1** including error indicating means responsive to a said error signal for providing an indication thereof.

3. In a traffic control system the improvement as set forth in claim **2** wherein said error indicating means includes a visual display means, and means for alternately, energizing and deenergizing said visual display means for the duration of said error signal.

4. In a traffic control system the improvement as set forth in claim **3** wherein said visual display means includes traffic signal light means for displaying a warning signal for each of said conflicting traffic courses for the duration of said error signal.

5. In a traffic control system the improvement as set forth in claim **2** wherein said error indicating means includes timing means responsive to a said error signal for timing a predetermined period of time and then providing a control signal.

6. In a traffic control system the improvement as set forth in claim **5** including bistable means having a normal first condition and a second condition in response to a said control signal, and

error warning signal means responsive to said second condition for providing a warning signal.

7. In a traffic control system the improvement as set forth in claim **6** wherein said error warning signal means includes traffic signal light means for providing a said warning signal in each of said conflicting traffic courses.

8. In a traffic control system the improvement as set forth in claim **7** including reset means for resetting said bistable means to its normal first condition.

9. In a traffic control system for controlling traffic flow through an intersection of a plurality of pairs of conflicting traffic courses, each having signal light means associated therewith for, upon actuation by a command signal, displaying a right-of-way signal to the associated traffic course, and traffic signal control means for providing a said command signal for each of said traffic courses; the improvement comprising:

solid-state NOR logic means associated with each pair of conflicting traffic courses for providing an output signal indicative that said controller means has provided coincident command signals for causing right-of-way signals to be displayed in both of said conflicting traffic courses; and,

solid state logic means associated with the outputs of each of said NOR logic means for providing an error signal when any of said NOR logic means provides a said output signal.

10. In a traffic control system the improvement as set forth in claim **1**, having output logic means adapted activate an indicator, wherein the NOR logic means comprises a plurality of NOR gates, each having inputs from controller output lines for causing conflicting go signals, and NOR gate means having inputs from said first-mentioned NOR gates with output means to said output logic means.

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