Methods of forming integrated circuit chips include forming a plurality of criss-crossing grooves in a semiconductor wafer having a plurality of contact pads thereon and filling the criss-crossing grooves with an electrically insulating layer. The electrically insulating layer is then patterned to define at least first and second through-holes therein that extend in a first one of the criss-crossing grooves. The first and second through-holes are then filled with first and second through-chip connection electrodes, respectively. The semiconductor wafer is then diced into a plurality of integrated circuit chips by cutting through the electrically insulating layer in a criss-crossing pattern that overlaps with the locations of the criss-crossing grooves.
FIG. 1
(Prior Art)
METHODS OF FABRICATING INTEGRATED CIRCUIT CHIPS FOR MULTI-CHIP PACKAGING AND WAFERS AND CHIPS FORMED THEREBY

REFERENCE TO PRIORITY APPLICATION

[0001] This application claims priority to Korean Application Serial No. 2004-58689, filed Jul. 23, 2004, the disclosure of which is hereby incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to methods of fabricating integrated circuit chips and, more particularly, to methods of fabricating integrated circuit chips suitable for multi-chip packaging.

BACKGROUND OF THE INVENTION

[0003] Multi-chip package (MCP) technologies typically include methods of fabricating integrated circuit chips that may be combined side-by-side or stacked together within a single integrated circuit package or module. The use of MCP technologies can significantly increase the integration density of integrated circuits, including those that are used in hand-held and other small devices (e.g., cellular phones). An example of an MCP technology that uses wiring plugs within penetrant apertures that extend through an integrated circuit chip is disclosed in U.S. Pat. No. 6,429,096 to Yanagida. These wiring plugs support the electrical interconnection of a plurality of chips that can be stacked vertically within a single integrated circuit package. Another example of an MCP technology that uses through-holes is disclosed in U.S. Pat. No. 6,566,232 to Hara et al.

[0004] Other packaging technologies that seek to increase the integration densities of integrated circuits on a substrate (e.g., printed circuit board (PCB)) include chip scale packaging (CSP) technologies. These CSP technologies seek to increase integration levels using packages that have very small form factors and are nearly the same size as the integrated circuit chip(s) they enclose. One commonly accepted requirement of a CSP package requires that it have a lateral footprint that is no greater than about 1.2 times the size of the semiconductor chip it encloses. An example of a CSP packaging technology is disclosed in U.S. Pat. No. 6,774,475 to Blakesheer et al. One type of CSP technology includes wafer-level chip-scale packaging (WL CSP), which enables an integrated circuit chip to be mounted face-down to a printed circuit board (PCB), with the chip's pads connected to the board's pads through individual solder balls without needing any underfill material. This technology differs from other ball-grid array (BGA) technologies because there is typically no bond wires or interposer connections. The principle advantage of WL CSP is that the IC-to-PC board inductance is minimized and the secondary advantages are the reduction in package size and manufacturing cycle time and the enhanced thermal conduction characteristics. Another type of CSP technology, which describes initially forming partial through-holes in a semiconductor substrate and then removing an underside surface of the substrate to expose the through-holes, is disclosed in Korean Laid Open Patent Application No. 2003-0023040.

[0005] FIG. 1 illustrates a cross-sectional view of a vertical stack 20 of first and second integrated circuit chips 10a and 10b that are electrically connected together. This vertical stack 20 has some similarities to the vertical stack of chips illustrated at FIG. 12 of the aforementioned Korean Laid Open Patent Application No. 2003-0023040. The first chip 10a is illustrated as including a first semiconductor substrate 12a having a first through-hole 17a therein. The first through-hole 17a extends from an upper surface of the substrate 12a to a lower surface of the substrate 12a. A first passivation layer 13a is provided on the upper surface of the substrate 12a. This first passivation layer 13a has an opening therein that exposes a first chip pad 11a. A first insulating layer 18a is also provided. This first insulating layer 18a extends on the first passivation layer 13a and directly on sidewalls of the first through-hole 17a. A first metal layer 21a is provided directly on the first chip pad 11a and forms an electrical connection therewith. As illustrated, this first metal layer 21a also extends on the first insulating layer 18a and into the first through-hole 17a. The first through-hole 17a is filled with a first electrode metal layer 22a, which is electrically coupled to the first chip pad 11a by the first metal layer 21a.

[0006] Similarly, the second chip 10b is illustrated as including a second semiconductor substrate 12b having a second through-hole 17b therein. The second through-hole 17b extends from an upper surface of the substrate 12b to a lower surface of the substrate 12b. A second passivation layer 13b is provided on the upper surface of the substrate 12b. This second passivation layer 13b has an opening therein that exposes a second chip pad 11b. A second insulating layer 18b is also provided. This second insulating layer 18b extends on the second passivation layer 13b and directly on sidewalls of the second through-hole 17b. A second metal layer 21b is provided directly on the second chip pad 11b. This second metal layer 21b also extends on the second insulating layer 18b and into the second through-hole 17b. The second through-hole 17b is filled by a second electrode metal layer 22b, which is electrically coupled to the second chip pad 11b by the second metal layer 21b.

[0007] An electrical interconnection is provided between the first and second integrated circuit chips 10a and 10b and the first and second chip pads 11a and 11b. This electrical interconnection is provided by a first metal bump 24a (e.g., solder ball), which electrically connects the first electrode metal layer 22a to the second electrode metal layer 22b. A second metal bump 24b is also provided to electrically connect the second electrode metal layer 22b to an underlying chip, package or printed circuit board (not shown).

[0008] As will be understood by those skilled in the art, the first and second integrated circuit chips 10a and 10b may be formed from a common semiconductor wafer (not shown) containing integrated circuits therein and a plurality of chip pads thereon, which are partially covered by a passivation layer (shown as 13a and 13b in FIG. 1). The first and second through-holes 17a and 17b may be formed in the semiconductor wafer using a laser drilling technique. After formation of the through-holes, an insulating layer (shown as 18a and 18b in FIG. 1) is formed on the passivation layer and along sidewalls of the through-holes. This insulating layer may then be patterned to expose the chip pads. A metal layer (shown as 21a and 21b in FIG. 1) and an electrode metal layer (shown as 22a and 22b in FIG. 1) are then deposited in sequence on the insulating layer. The electrode metal layer is deposited to a thickness sufficient to fill the
through-holes. Following these steps, the semiconductor wafer may be thinned by removing a portion of a bottom surface of the semiconductor wafer. This thinning operation may include conventional grinding, polishing and wet etching techniques that result in an exposure of the electrode metal layer within the through-holes.

[0009] Unfortunately, the conventional fabrication step of laser drilling to form through-holes in a semiconductor wafer is a relatively lengthy process step that may require each hole to be formed one-at-a-time in sequence. Moreover, the drilling of holes may damage the semiconductor wafer and result in through-holes with tapered sidewall profiles. The formation of tapered sidewall profiles may lead to the formation of electrode metal layers that are susceptible to defects (e.g., electrical disconnection). Thus, notwithstanding these conventional techniques for forming integrated circuit chips that may be stacked together to provide high levels of integration, there continues to be a need for improved methods of forming through-holes in semiconductor wafers and chips.

SUMMARY OF THE INVENTION

[0010] Semiconductor chips according to embodiments of the present invention use outer edge insulating layers with through-holes therein that provide reliable interconnection vias when the chips are used in stacked multi-chip packaging applications. In some of these embodiments, a semiconductor substrate is provided having upper and lower faces thereof that extend to an outer edge thereof. At least a first contact pad is provided on a portion of the upper face extending adjacent the outer edge. An electrically insulating region is provided on the outer edge of the semiconductor substrate. This electrically insulating region, which may surround an entire periphery of the semiconductor substrate, includes at least one through-hole that extends vertically through an entire thickness of the electrically insulating region and has a longitudinal axis that is substantially parallel to the outer edge of the semiconductor substrate. A connection electrode is also provided. This connection electrode extends through the through-hole and is electrically connected to the first contact pad. The electrically insulating layer may have a lower surface that is coplanar with the lower face of the semiconductor substrate and an upper surface that is above the upper face of the semiconductor substrate, which results in a length of the through-hole being greater than a thickness of the semiconductor substrate. In particular, the electrically insulating layer may wrap around the outer edge and extend onto a passivation layer covering the semiconductor substrate.

[0011] Additional embodiments of the invention include a semiconductor chip having a peripheral edge defined by an electrically insulating region having interconnect through-holes therein. The semiconductor chip includes a semiconductor substrate having upper and lower faces thereof that extend to an outer edge thereof. An electrically insulating region is provided on the outer edge of the semiconductor substrate. The electrically insulating region has a through-hole therein that is filled within a connection electrode. A solder bump is also provided. The solder bump is electrically connected to a portion of the connection electrode extending adjacent a bottom of the through-hole.

[0012] Still further embodiments of the invention include methods of fabricating a plurality of integrated circuit chips from a semiconductor wafer. These methods include forming a plurality of crisscrossing grooves in a semiconductor wafer having a plurality of contact pads thereon. The crisscrossing grooves are then filled with an electrically insulating layer. The electrically insulating layer is patterned to define at least first and second through-holes therein, which extend into a first one of the criss-crossing grooves. The first and second through-holes are filled with first and second through-chip connection electrodes, respectively. The semiconductor wafer is then diced into a plurality of integrated circuit chips. This dicing step may be performed by cutting through the electrically insulating layer in a criss-crossing pattern that overlaps with the locations of the crisscrossing grooves.

[0013] In additional embodiments of the invention, the dicing step is preceded by the step of removing an underside of the semiconductor wafer to thereby expose the first and second through-chip connection electrodes and the electrically insulating layer. The step of filling the first and second through-holes may also include depositing a base metal layer that extends on the electrically insulating layer and lines the first and second through-holes and then electroplating the first and second through-chip connection electrodes into the first and second through-holes using the base metal layer as an electroplating electrode. The base metal layer may then be etched back using the first and second through-chip connection electrodes as an etching mask.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. 1 is a cross-sectional view of a stack of integrated circuit chips that is compatible with chip scale packaging technologies, according to the prior art.

[0015] FIG. 2 is a plan view of a semiconductor wafer that may be processed in accordance with the methods of FIGS. 3-14 herein.

[0016] FIGS. 3-14 are cross-sectional views of intermediate structures that illustrate methods of forming integrated circuit chips according to embodiments of the present invention.

[0017] FIG. 15 is a cross-sectional view of a stack of integrated circuit chips formed in accordance with the methods of FIGS. 3-14.

DESCRIPTION OF PREFERRED EMBODIMENTS

[0018] The present invention now will be described more fully herein with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity of description. It will also be understood that when a layer is referred to as being “on” another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. Like reference numerals refer to like elements throughout.

[0019] Methods of forming integrated circuit chips according to embodiments of the present invention will now
be described with reference to FIGS. 2-14. In FIG. 2, a semiconductor wafer 30 is illustrated. This semiconductor wafer 30 includes a semiconductor substrate 32 (e.g., silicon substrate) having a primary surface 35 thereon, which is also described herein as an upper face of the substrate 32. As described more fully hereinbelow with respect to FIGS. 3-14, a plurality of semiconductor chips 34 may be formed from the semiconductor wafer 30 by dicing the semiconductor wafer 30 along crisscrossing scribe lanes 36 (a/k/a dicing streams) to thereby form a plurality of separate semiconductor chips 34.

[0020] FIG. 3 is a plan view of a portion of the semiconductor wafer 30 of FIG. 2 and FIG. 4 is a cross-sectional view of the portion of FIG. 3, taken along line 4-4'. In particular, FIG. 3 illustrates peripheral portions of adjacent integrated circuit devices that are separated from each other by a scribe lane 36. Each integrated circuit device includes respective contact pads 31 on the primary surface 35. These pads 31 are illustrated as extending adjacent one side of each of the illustrated integrated circuit devices. In other embodiments of the present invention, other pads (not shown) may also be provided adjacent other sides of the integrated circuit devices. In FIG. 4, a surface passivation layer 33 is also illustrated as extending across the primary surface 35 of the semiconductor wafer 30. The pads 31 may be made of aluminum or copper, for example, and the passivation layer 33 may be made of electrically insulating materials such as silicon oxide, silicon nitride and silicon oxynitride. This passivation layer 33 may be formed as a relatively thick electrically insulating layer that covers multiple underlying layers of metallization, interconnects, interlayer insulating layers and active devices (not shown), for example. FIG. 4 also illustrates the position of a scribe lane 36, which extends between two portions of the substrate 32 that will ultimately constitute separate semiconductor chips 34 after a final wafer dicing step is performed.

[0021] As illustrated by FIGS. 5-6, a series of deep criss-crossing grooves 37 are formed along the scribe lanes 36. These grooves 37 may have a width equal to about the width of the scribe lanes 36. As illustrated more fully by FIG. 12, the depth of these grooves 37 may be a function of the amount of the underside surface 39 of the semiconductor wafer 30 that is to be removed prior to wafer dicing. In some embodiments of the invention, the depth of the grooves 37 may be in the range from about 30 microns to about 300 microns. These grooves 37 may be formed using a wafer sawing technique and/or a wafer etching technique. A relatively thick electrically insulating layer 38 is then formed as a blanket layer on the primary surface of the semiconductor wafer 30. This electrically insulating layer 38 is of sufficient thickness to completely fill the grooves 37 and cover adjacent portions of the substrate 32, as illustrated by FIG. 6. The electrically insulating layer 38 may be formed as a silicon oxide layer or as a polyimide layer, for example.

[0022] Referring now to FIG. 7, the electrically insulating layer 38 is selectively removed to define a plurality of through-holes 41 therein (i.e., connection holes), which are located in the scribe lanes 36 and sufficiently deep to expose the bottoms of the grooves 37, and expose the contact pads 31. This removal step may be performed as a photolithographically-defined etching step, which results in through-holes 41 having substantially vertical sidewalls and uniform diameters. These through-holes 41 may have diameters in a range from about 10 microns to about 50 microns. The electrically insulating layer 38 is also formed of a material that has good adhesive strength to the substrate 32, which inhibits detachment and/or delamination of the insulating layer 38 during subsequent processing and packaging. Moreover, by using a selective etching step that processes the entire wafer 30 at the same time, significant process time savings can be achieved because all of the through-holes 41 may be formed at the same time and all of the contact pads 31 may be exposed at the same time.

[0023] After the through-holes 41 have been formed, a blanket base metal layer 42 may be deposited on the wafer 30. As illustrated by FIG. 8, this base metal layer 42 is illustrated as contacting upper surfaces of the exposed contact pads 31 and lining the bottoms and sidewalls of the through-holes 41. The base metal layer 42, which should be chosen to have good adhesive properties with the underlying electrically insulating layer 38, may be formed using a sputtering technique, and may have a thickness in a range from about 0.05 microns to about 1 micron. In some embodiments of the present invention, the base metal layer 42 may be a composite of two or more metal layers. The first of these metal layers within the composite may be chromium, titanium or other metal layer having good adhesive properties with the electrically insulating layer 38 and the second of these metal layers may be silver, gold, copper, nickel, palladium, platinum or other metal layer having good adhesive properties with a subsequently formed connection electrode.

[0024] Referring now to FIGS. 9-11, a blanket layer of photosist material is deposited and patterned to define a photosist mask 51 having a plurality of openings 52 therein. These openings 52 expose portions of the base metal layer 42 extending over each contact pad 31 and its corresponding through-hole 41. Then, as illustrated best by FIG. 10, electrode metal layers 43 are formed to completely fill respective openings 52 in the photosist mask 51. These electrode metal layers 43 may be formed using an electroplating technique, which includes using the base metal layer 42 as a plating electrode, or another selective deposition technique. These electrode metal layers 43, which represent respective connection electrodes, may be formed of silver, gold, copper, nickel, palladium, platinum and alloys thereof or other suitable high conductivity materials. As illustrated by FIG. 11, the photosist mask 51 is then removed to thereby expose portions of the base metal layer 42. These exposed portions of the base metal layer 42 are then selectively removed using an etching step and the electrode metal layers 43 as etching masks. This etching step causes portions of the electrically insulating layer 38 to be exposed and the electrode metal layers 43 to become electrically disconnected from each other.

[0025] Referring now to FIG. 12, a wafer thinning step is performed to expose portions of the electrode metal layers 43 extending to the bottoms of the through-holes 41. This wafer thinning step may be performed using a grinding wheel 53 to remove a portion of the underside surface 39 of the semiconductor wafer 30. In addition to grinding, wet etching may be used to remove portions of the underside surface 39 of the semiconductor wafer 30. The portion of the underside surface 39 of the semiconductor wafer 30 that is removed may be substantial. For example, if the semiconductor wafer 30 has a thickness of about 700 microns prior
to wafer thinning, it may only have a thickness of about 100 microns (or less) after wafer thinning. Accordingly, the depth of the through-holes 41 and the grooves 37 should be greater than about 100 microns to guarantee, exposure of the electrode metal layers 43. When this relationship is present, each electrode metal layer 43 and corresponding base metal layer 42 provide a high conductivity electrical path from a corresponding contact pad 31 to an underside of the semiconductor wafer 30.

As illustrated by FIGS. 13-14, the wafer thinning step may be followed by the step of applying an adhesive tape 54 (e.g., ultraviolet adhesive tape) to the entire underside surface 39 of the thinned semiconductor wafer 30. This tape 54 preserves the integrity of the semiconductor wafer 30 during subsequent processing steps (e.g., wafer dicing). The semiconductor wafer 30 is then diced into a plurality of separate integrated circuit chips 60 by sawing the wafer along the center of the scribe lanes 36 using a cutting tool 55.

Referring now to FIG. 15, a cross-sectional view of a stack 70 of integrated circuit chips 60a and 60b formed in accordance with the methods of FIGS. 3-14 uses a first metallic (e.g., solder) bump 45a to electrically connect an upper connection electrode 43a associated with an upper chip 60a to a lower connection electrode 43b associated with a lower chip 60b. A second metallic bump 45b may also be provided to support mounting and electrical connection of the stack 70 to a printed circuit board (PCB) (not shown). In this manner, the second metallic bump 45b operates as a terminal to the stack 70. These first and second metallic bumps 45a and 45b may be formed using an electroplating or other metal bump forming technique.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

That which is claimed is:

1. A semiconductor chip, comprising:
   - a semiconductor substrate having upper and lower faces thereon that extend to an outer edge thereof and at least a first contact pad on a portion of the upper face extending adjacent the outer edge;
   - an electrically insulating region on the outer edge of said semiconductor substrate, said electrically insulating region having through-hole therein; and
   - a connection electrode that extends through said through-hole and is electrically connected to the first contact pad.

2. The semiconductor chip of claim 1, wherein said electrically insulating layer has a lower surface that is coplanar with the lower face of said semiconductor substrate.

3. The semiconductor chip of claim 1, wherein a length of the through-hole is greater than a thickness of said semiconductor substrate.

4. The semiconductor chip of claim 3, wherein a longitudinal axis of the through-hole is substantially parallel to the outer edge of said semiconductor substrate.

5. The semiconductor chip of claim 1, further comprising a passivation layer extending on the upper face and having an opening therein that exposes the first contact pad; and wherein said electrically insulating region wraps around the outer edge and extends onto the passivation layer.

6. The semiconductor chip of claim 5, wherein said electrically insulating region extends between the upper face and said connection electrode.

7. The semiconductor chip of claim 1, wherein an outer edge of said electrically insulating region represents an outer edge of the semiconductor chip.

8. A semiconductor chip, comprising:
   - a semiconductor substrate having upper and lower faces thereon that extend to an outer edge thereof;
   - an electrically insulating region on the outer edge of said semiconductor substrate, said electrically insulating region having through-hole therein with a length greater than a thickness of said semiconductor substrate;
   - a connection electrode extending through the through-hole; and
   - a solder bump electrically connected to a portion of said connection electrode extending adjacent a bottom of the through-hole.

9. The semiconductor chip of claim 8, wherein an outer edge of said electrically insulating region represents an outer edge of the semiconductor chip.

10. A method of fabricating a plurality of integrated circuit chips, comprising the steps of:
   - forming a plurality of criss-crossing grooves in a semiconductor wafer having a plurality of contact pads thereon;
   - filling the criss-crossing grooves with an electrically insulating layer;
   - patterning the electrically insulating layer to define at least first and second through-holes therein that extend in a first one of the criss-crossing grooves;
   - filling the first and second through-holes with first and second through-chip connection electrodes, respectively; and
   - dicing the semiconductor wafer into a plurality of integrated circuit chips by cutting through the electrically insulating layer in a crisscrossing pattern that overlaps with the locations of the criss-crossing grooves.

11. The method of claim 10, wherein said dicing step is preceded by the step of removing an underside of said semiconductor wafer to thereby expose the first and second through-chip connection electrodes and the electrically insulating layer.

12. The method of claim 11, wherein said step of filling the first and second through-holes comprises the steps of:
   - depositing a base metal layer that extends on the electrically insulating layer and lines the first and second through-holes;
   - electroplating the first and second through-chip connection electrodes into the first and second through-holes; and
   - etching back the base metal layer using the first and second through-chip connection electrodes as an etching mask.
13. The method of claim 10, wherein said step of filling the first and second through-holes comprises the steps of:
   - depositing a base metal layer that extends on the electrically insulating layer and lines the first and second through-holes;
   - electroplating the first and second through-chip connection electrodes into the first and second through-holes; and
   - etching back the base metal layer using the first and second through-chip connection electrodes as an etching mask.

14. The method of claim 13, wherein said electroplating step comprises electroplating the first and second through-chip connection electrodes into the first and second through-holes using the base metal layer as an electroplating electrode.

15. The method of claim 14, wherein said electroplating step is preceded by the step of patterning an electroplating mask on the base metal layer.

16. A method of fabricating an integrated circuit chip, comprising the steps of:
   - forming a groove in a semiconductor substrate;
   - filling the groove with an electrically insulating region;
   - forming first and second through-holes in the electrically insulating region;
   - filling the first and second through-holes with first and second connection electrodes, respectively;
   - removing an underside of the semiconductor substrate to thereby expose the electrically insulating region and the first and second connection electrodes; and
   - dicing the semiconductor substrate into first and second semiconductor chips by cutting through the electrically insulating region at a location extending between the first and second connection electrodes.

17. The method of claim 16, wherein said step of filling the first and second through-holes comprises electroplating first and second connection electrodes into the first and second through-holes.

18. A method of processing a semiconductor wafer, comprising the steps of:
   - forming a plurality of criss-crossing grooves in a semiconductor wafer;
   - filling the criss-crossing grooves with an electrically insulating layer;
   - removing an underside of the semiconductor wafer to thereby expose a surface of the electrically insulating layer having a criss-crossing pattern; and
   - dicing the semiconductor wafer into a plurality of integrated circuit chips having electrically insulating edges by cutting through the electrically insulating region at locations defined by the criss-crossing pattern.

19. The method of claim 18, wherein said removing step is preceded by the steps of:
   - forming a plurality of through-holes in the electrically insulating layer; and
   - filling the plurality of through-holes with a corresponding plurality of connection electrodes.

20. The method of claim 19, wherein said removing step comprises removing an underside of the semiconductor wafer to thereby expose a surface of the electrically insulating layer and the plurality of connection electrodes.

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