A circuit arrangement for driving a plasma display panel comprises PNP and NPN transistors respectively coupled to first and second electrodes of the panel. Responsive to control signals selected PNP transistors are turned on to deliver high frequency pulses from a D.C. power source to the first electrodes thus selected to vary the electric potential of the electrodes from a low level to a high level, similarly selected NPN transistors vary the electric potential of the coupled second electrodes from a high level to a low level coincident with the potential variation at the selected first electrodes.

5 Claims, 8 Drawing Figures
FIG. 2

FIG. 3
FIG. 5
FIG. 6
DRIVING CIRCUIT FOR A PLASMA DISPLAY PANEL COMPRISING PNP AND NPN TRANSISTORS

BACKGROUND OF THE INVENTION

This invention relates to a driving circuit for a plasma display panel and, more particularly, to a circuit arrangement responsive to control signals for driving a plasma display panel from an electric power source in accordance with time division principles.

A plasma display panel generally comprises a thin glass plate having a plurality of bores at predetermined places and two thin glass plates closely disposed on both sides of the perforated glass plate. The three stacked glass plates are sealed together around the periphery thereof. The inside of the bores is evacuated and then filled with neon or a like inert gas or gases. Line (column) and row electrodes, called an electrode matrix in their ensemble, are arranged on the respective sides of the stacked glass plates in a manner such that the line and row electrodes cross each other at the locations of the bores. With application of a sufficiently high high-frequency voltage to a selected pair of the line and row electrodes, a gas discharge occurs in a bore in registry with the location where the selected electrodes cross i.e., at their crosspoint location. As an improvement in such plasma display panels, a panel in practical use may comprise a relatively thick glass plate instead of each of the outside two of the abovemen tioned three glass plates; line and row electrodes disposed on the inside surfaces of the respective relatively thick glass plates; and thin glass or other dielectric films coated on the exposed faces of the line and row electrodes. The central glass plate may be dispensed with. Alternatively, a plasma display panel may comprise a plurality of paired segment electrodes instead of the matrix type electrode. In any case, such a plasma display panel comprises a plurality of opposing electrodes arranged to define a coplanar array of plasma discharge cells on both sides of the array at the outside of the cells, with each pair of the opposing electrodes arranged in registration either with a cell or with several preselected cells.

It is possible to initiate the discharge through a plasma discharge cell by applying across the cell a D.C. voltage higher than the firing voltage (with the voltage drop due to the dielectric films neglected). The discharge so started produces charged particles within the cell, which charge up the dielectric films in a reverse direction, i.e., a direction to weaken the electric field provided by the applied D.C. voltage within the cell. As a result, the discharge ceases when the algebraic sum of the applied D.C. voltage and the reversed voltage resulting from the charged dielectric films goes below the discharge sustaining voltage. It is possible to restart the discharge by applying a reversed D.C. voltage that is at least as high as the firing voltage minus the reversely directed voltage produced by the charged dielectric films. In this manner it is possible to make the cell glow with sufficient brightness by successively instantaneously applying a D.C. voltage across the cell with the polarity varied alternatingly at a high rate, such as ten thousand times per second, and consequently to display a desired figure or letter by selecting those paired electrodes which intersect at the cells arranged within the array in the form of the desired display.

A plasma present panel may be driven to display a desired display in a time division fashion. For convenience of description, the panel may be assumed to have matrix type electrodes. In this case, the cell electrodes or the row electrodes are line-scanned by a group of several successive pulses of a predetermined height. During the time the group of pulses is applied to a desired one of the electrodes, namely, during the period of a desired time slot, a similar group of pulses is applied with the reversed polarity to the selected one of the opposing electrodes. Discharge occurs thereby through the cell or cells sandwiched between the selected electrodes.

It is to be noted here that the wave form of the discharge current flowing through the plasma discharge cell depends on the output impedance of the driving circuit for the plasma display panel and that the luminance of the discharge depends on the form of the discharge current. If the output impedance is sufficiently small compared with the impedance of the cell in the state of discharge, the form of the discharge current is determined only by the characters of the cell. For example, the discharge current is of the form of a pulse having a peak and a pulse width of about 0.1 microsecond. In a case where the output impedance of the driving circuit is relatively large, the discharge current is suppressed by the voltage drop introduced by the output impedance to lower the peak value of the discharge current and to widen the pulse width. The current wave form further depends on that slope of the pulse voltage which appears at the start of the discharge. If the slope is steeper, the peak value of the current becomes higher. On the other hand, the luminance of the discharge is almost proportional to the peak value of the discharge current. Accordingly, it is desirable that the driving circuit for applying the pulse voltage to the cells be of low output impedance and that the slope of the discharge starting pulse be as great as possible.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a circuit arrangement capable of driving a plasma display panel with sufficient luminance. It is a further object of this invention to provide a circuit arrangement whose output impedance is rendered negligible supplying a plasma discharge cell of a plasma display panel with voltage to fire the cell.

According to the instant invention, a circuit arrangement for driving a plasma display panel having first electrodes and opposing second electrodes from an electric power source and control signal generating means comprises a plurality of PNP transistors and a like number of NPN transistors. The collector electrodes of the PNP transistors are coupled to the respective first electrodes. The collector electrodes of the NPN transistors are coupled to the respective second electrodes. The control signal generating means generates control signals having high frequency components which are selectively applied to a pair of the PNP and NPN transistors to make the pair turn on (i.e., conduct). The selected pair of PNP and NPN transistors cooperates to deliver high frequency pulse voltage from the power source means to the first and second electrodes coupled to their collector electrodes.

While supplying the high frequency pulses across a selected plasma discharge cell of the plasma display
3 panel, the driving circuit presents only negligible output impedance because of the conduction of the selected NPN and PNP transistors.

**BRIEF DESCRIPTION OF THE DRAWINGS**

FIGS. 1a, 1b, and 1c are timing diagrams depicting high frequency pulses used to start and sustain gas discharge through a plasma discharge cell of a plasma display panel;

FIG. 2 graphically illustrates a typical relation between the peak discharge current flowing through a plasma discharge cell and the luminance of the cell;

FIG. 3 graphically illustrates the luminance of a plasma discharge cell versus the output impedance of typical driving circuits therefor; and

FIGS. 4 through 6 depict several embodiments of the present invention.

**DESCRIPTION OF THE PREFERRED EMBODIMENTS**

Referring to FIGS. 1a, 1b, and 1c, the wave forms of pulses to be applied to a selected one of the electrodes of a plasma display panel will be discussed in greater detail before describing several preferred embodiments of the instant invention. A train of pulses shown in FIG. 1a consists of pulses that rise from zero potential to a predetermined positive level \( V_p \). Another train depicted in FIG. 1b consists of pulses that go negative from the predetermined level \( V_p \) to zero potential. When such pulse trains are coincidently applied to a pair of opposing electrodes of a plasma display panel, the plasma discharge cell interposed between the electrode pair is supplied with a train of pulses having an effective absolute value of \( 2V_p \) as shown in FIG. 1c. In this case, gas discharge occurs through the cell and is sustained if the value \( V_p \) is higher than the firing voltage of the cell. When one of the pulse train is removed, the discharge ceases if the value \( V_p \) is lower than two times the discharge sustaining voltage of the cell. This is because the sum of the pulse voltage \( V_p \) applied to only one of the electrodes and the reversed voltage resulting from the charges produced by the previous gas discharge on the dielectric films is then lower than the firing voltage. It is thus possible by reducing the difference between the firing voltage and the discharge sustaining voltage of the cells and minimizing the depolarizations in the electric characteristics of the cells to widen the range of that pulse height \( V_p \) which provides the display when coincidently applied to a pair of the line and row electrodes but does not when applied only to either one of the pair.

Referring to FIG. 2, it may be observed that the luminance of the display is substantially linearly proportional to the peak value of the discharge current flowing through the cells, as has already been described.

Referring to FIG. 3, a curve (a) represents the relationship between the luminance of the display and the output impedance of the driving circuit in case both levels, namely, the pulse output level and a pulse interval level, are derived by the driving circuit with the same impedance. Another curve (b) is for the case where the output impedance for one of the levels is similar to that for the curve (a) and the output impedance for the other level approaches zero. It is thus preferable that the output impedance for at least one of the pulse trains be as low as possible to obtain sufficient display luminance.

Referring to FIG. 4, a circuit arrangement according to a first embodiment of the present invention, connected to a D.C. power source \( x \) and a control signal generator \( y \), drives a plasma display panel having opposing electrodes, such as, for example, row electrodes \( 13 \) and line electrodes \( 14 \). The D.C. power source \( x \) supplies a D.C. voltage of the above-mentioned voltage \( V_p \) to a first conductor \( 16 \) with respect to a second conductor \( 17 \) which is grounded as shown. The control signal generator \( y \) produces a continuous train of positive-going pulses \( \phi_a \), a similar train of negative-going pulses \( \phi_b \), a time division pulse train of cyclical positive-going pulses \( \phi_a \), and \( \phi_b \), and a negative-going cell selection pulses, such as \( \phi_a \) and \( \phi_b \). Description will later appear in more detail as to the control pulses produced by the control signal generator \( y \).

The first embodiment comprises a plurality of PNP switching transistors \( Q_1 \), . . . , and \( Q_n \) coupled to the respective row electrodes \( 13 \) and an equal number of NPN switching transistors \( Q_1 \), . . . , and \( Q_n \) coupled to the respective line electrodes \( 14 \). Each of the switching transistors \( Q_1 \), . . . , and \( Q_n \) is adapted to switch a relatively high D.C. voltage and has an emitter, a collector, and a base electrode. The emitter electrodes of the PNP transistors \( Q_1 \), . . . , and \( Q_n \) are connected directly to the first conductor \( 16 \). The collector electrodes of the PNP transistors \( Q_1 \), . . . , and \( Q_n \) are connected direct to the associated row electrodes \( 13 \) and to the second conductor \( 17 \) through resistors \( 21 \), respectively. The emitter electrodes of the NPN transistors \( Q_1 \), . . . , and \( Q_n \) are connected directly to the second conductor \( 17 \). The collector electrodes of the NPN transistors \( Q_1 \), . . . , and \( Q_n \) are connected directly to the associated line electrodes \( 14 \) and to the first conductor \( 16 \) through resistors \( 22 \), respectively. The first embodiment further comprises a plurality of NPN auxiliary transistors \( Q'_1 \), . . . , and \( Q'_n \) and a like number of PNP auxiliary transistors \( Q''_1 \), . . . , and \( Q''_n \), each having an emitter, a collector, and a base electrode. The emitter electrodes of the NPN auxiliary transistors \( Q'_1 \), . . . , and \( Q'_n \) are connected directly to the second conductor \( 17 \). The collector electrodes of these transistors are connected to a third conductor \( 23 \) of the collector voltage \( V_c \) through resistors \( 24 \), respectively. The emitter electrodes of the PNP auxiliary transistors \( Q''_1 \), . . . , and \( Q''_n \) are connected directly to the third conductor \( 23 \). The collector electrodes of these transistors are connected to the second conductor \( 17 \) through resistors \( 25 \), respectively. The base electrodes of the PNP switching transistors \( Q_1 \) through \( Q_n \) are connected to the first conductor \( 16 \) through resistors \( 26 \), respectively, and to the respective collector electrodes of the NPN auxiliary transistors \( Q'_1 \) through \( Q'_n \) through capacitors \( 27 \), respectively. The base electrodes of the NPN switching transistors \( Q_1 \) through \( Q_n \) are connected to the collector electrodes of the PNP auxiliary transistors \( Q''_1 \) through \( Q''_n \) through resistor and capacitor parallel circuits \( 28 \), respectively. Further referring to FIG. 4, the first embodiment still further comprises a plurality of positive logic AND circuits \( A_1 \), . . . , and \( A_n \), each comprising a first diode \( 31 \), a second diode \( 32 \), and a resistor \( 33 \) connected to the third conductor \( 23 \), and a similar number of negative logic AND circuits \( \bar{A}_1 \), . . . , and \( \bar{A}_n \), each comprising a first diode \( 36 \), a second diode \( 37 \), and a resistor \( 38 \) connected to the second conductor \( 17 \). Each of the AND circuits \( A_1 \) through \( A_n \) and \( \bar{A}_1 \) through \( \bar{A}_n \) thus
serves in effect as a two-input AND circuit having a first and a second input terminal. The first input termin-
als of the positive and negative logic AND circuits A1 through An and A1 through An provided by the first
diodes 31 and 36 are simultaneously supplied with the positive and negative going pulses $\phi$ and $\bar{\phi}$, re-
spectively. The second input terminals of the positive logic AND circuits provided by the second diodes 32 are cy-
clically supplied with the time division pulses $t_i$ through $t_n$. The second input terminals of the negative logic
AND circuits A1 through An similarly provided by the second diodes 36 are selectively supplied with the cell
selection pulses, such as $a$ and $b$. It will now be under-
stood that the positive going pulses $\phi$ and the time divi-
sion pulses $t_i$ through $t_n$ should rise from zero voltage
up to the collector voltage $V_{cc}$ and that the negative
going pulses $\bar{\phi}$ and the cell selection pulses $a$, $b$, and so
forth should fall from the collector voltage $V_{cc}$ down to
the zero level.

The base electrodes of the NPN auxiliary transistors
$\bar{Q}^1$ through $\bar{Q}^n$ are coupled to the output terminals of the positive logic AND circuits A1 through An through resistor and capacitor parallel circuits 39, respectively. The base electrodes of the PNP auxiliary transistors $Q^1$ through $Q^n$ are connected directly to the output terminals of the respective negative logic AND circuits
$\bar{A}1$ through $\bar{A}n$.

In operation of the first embodiment of the present
invention depicted in FIG. 4, the positive logic AND
circuits A1 through An are responsive to the positive
group of high frequency pulses $\phi$ and the time division
pulses $t_i$ through $t_n$ for producing cyclically appearing
groups of high frequency pulses. These pulses are cur-
rent-amplified by the respective NPN auxiliary transis-
tors $\bar{Q}^1$ through $\bar{Q}^n$ to be supplied to the base elec-
 trodes of the corresponding PNP switching transistors
$Q1$ through $Qn$. Supplied with the capacitively coupled
negatively going high frequency components, the PNP
switching transistors $Q1$ through $Qn$ are turned on in a
time division fashion (by the $t_1, \ldots, t_n$ pulses) to inter-
mittently deliver the voltage $V_a$ from the D.C. power
source 11 to the coupled row electrodes 13.

Responsive to the negative going high frequency
pulses appearing in coincidence with the group of
high frequency pulses supplied to one of the PNP switching transistors $Q1$ through $Qn$, at least one of the PNP
switching transistors $Q1$ through $Qn$ is turned on to lower the voltage supplied to the line electrodes 14 asso-
ciated therewith approximately to ground. The
high frequency voltage of the value $V_a$ is applied across a plasma discharge cell or cells (not shown) placed between at least one of the line conductors 14 that is intermittently grounded in response to the address pulse, and one of the row con-
ductors 13 that is intermittently supplied with the volt-
age $V_a$ in response to one of the time division pulses $t_i$
through $t_n$, in coincidence with which the address pulse
is supplied to the selected at least one of the negative
logic AND circuits $\bar{A}1$ through $\bar{A}n$. It should be noted
here that the output impedance of the row drive circuit
for the high frequency pulses supplied cyclically in
groups to the row electrodes 13 and 14 of the line drive
for the intermittent grounding of the select-
ed line electrode(s) 14 are extremely low, being al-
most zero, because the participant ones of the switching
transistors $Q1$ through $Qn$ and $Q1$ through $Qn$ are
turned on. It should also be noted that positive going
address pulses may be supplied to the selected one(s)
of the positive logic AND circuits $A1$ through $An$ in
stead of the time division pulses $t_i$ through $t_n$ so that
desired cell or cells may be supplied with the high fre-
quency pulses in combination with the negative going
address pulses $a$, $b$, and others. In any event, the first
embodiment provides sufficient luminance of the dis-
play by virtue of the low output impedance.

Still further referring to FIG. 4, it is necessary that
the capacitors 27 should be capable of withstanding a
voltage greater than the voltage $V_a$ because the capaci-
tors 27 are supplied with the voltage $V_a$ when the asso-
ciated PNP switching transistor $Q1$ through $Qn$ turns
on. The time constant dependent on the resistor 26 and
the capacitor 27 should be sufficiently greater than the
width of the high frequency pulse $\phi$. It is necessary,
moreover, that the resistance of the collector resistors
21 be selected in such a manner that the time constant
dependent on the resistance of each of the resistors 21
and the capacitance that exists between the associated
one of the row electrodes 13 and other electrodes be
smaller than the interval of the high frequency pulses
$\phi$. This is because, when each of the PNP switching
transistors $Q1$ through $Qn$ turns off, the potential of the
associated row electrode 13, which in principle is
clamp by its collector resistor to the ground potential
and in fact decreases exponentially to ground should
substantially attain the zero potential before the PNP
switching transistor is turned on by the next subsequent
one of the high frequency pulses $\phi$. In this regard, it
should be noted that the resistance of the collector res-
istors 21 should be appreciably large to reduce the
power consumed in the resistors 21 when the transis-
tors $Q1$ through $Qn$ are cyclically turned on. By way of
example, it may be assumed that the capacitance that is
present between each of the row electrodes 13 and the
others of the electrodes 13 and 14 is 30 pF and that the
frequency and the pulse width of the high fre-
quency pulses $\phi$ are 50 kHz and 5 microseconds, re-
spectively. Under the circumstances, the resistance of
each of the collector resistors 21 may be 100 kilohms.
The time constant in question is then 3 microseconds,
which is sufficiently smaller than the interval of 15 mi-
croseconds of the high frequency pulses $\phi$.

Referring to FIG. 5, a circuit arrangement according
to a second embodiment of the present invention com-
prises NPN switching transistors $Q1, \ldots, Qn$ and $Qn$
and PNP switching transistors $Q1, \ldots, Qn$ and $Qn$. The emitter
electrodes of the NPN switching transistors $Q1$ through $Qn$ and $Q1$ through $Qn$ are connected direct to the second conductor 17. The col-
lector electrodes of these transistors are connected di-
rect to the respective row electrodes 13 and to the first
conductor 16 through resistors 41, respectively. The
emitter electrodes of the PNP transistors $Q1$ through
$Qn$ are directly connected to the first conductor 16.
The collector electrodes of these transistors are con-
ected directly to the respective line electrodes 14 and
to the second conductor 17 through resistors 42, re-
spectively.
The second embodiment further comprises positive logic AND circuits A1, . . . , and An, each comprising diodes 44 and 45 and a resistor 46 connected to the third conductor 23. Negative logic AND circuits A1, . . . , and An, each comprises diodes 47 and 48, and a resistor 49 connected to the second conductor 17. The first input terminals of the positive logic AND circuits A1 through An are simultaneously supplied with the positive going high frequency pulses $\phi$. The second input terminals of these AND circuits are supplied with the positive going time division pulses $t_1$ through $t_n$ in a time division fashion. The first input terminals of the negative logic AND circuits A1 through An are supplied with the negative going high frequency pulses $\phi$ that appear in coincidence with the positive going ones $\phi$. The second input terminals of these latter AND circuits are selectively supplied with positive-going cell selection or address pulses $a$, $b$, and so forth that appear in coincidence with the desired ones of the time division pulses $t_1$ through $t_n$. The base electrodes of the PNP transistors Q1 through Qn are connected to the output terminals of the positive logic AND circuits A1 through An through resistor and capacitor parallel circuits 51, respectively. The base electrodes of the PNP transistors Q1 through Qn are connected to the output terminals of the negative logic AND circuits A1 through An through capacitors 52, respectively.

In operation of the second embodiment illustrated in FIG. 5, the positive going high frequency pulses $\phi$ appearing within the positive cycle of one of the time division pulses $t_1$ through $t_n$, intermittently turn the corresponding one of the NPN transistors O1 through On on to apply ground to the associated one of the row electrodes 13 at the frequency of the high frequency pulses $\phi$. Similarly, the negative going high frequency pulses $\phi$ appearing within the negative cycle of one of the address pulses $a$, $b$, and others intermittently turn the related at least one of the PNP transistors Q1 through Qn on to apply the voltage $V_4$ to the associated at least one of the line electrodes 14 at the frequency of the high frequency pulses $\phi$ or $\phi$. In this manner, the cyclically selected one of the NPN transistors and at least one of the PNP transistors selected in coincidence with the cycle selected NPN transistor cooperate to apply high frequency component of the control signals across the selected cell or cells. It is thus possible to drive the switching transistors Q1 through Qn and O1 through On without the auxiliary transistors Q'1 through Q'n and O'1 through O'n for current amplifying the output signals of the AND circuits A1 through An and A1 through An if the output impedance of the control signal generator 12 is sufficiently small.

Referring finally to FIG. 6, a circuit arrangement according to a third embodiment of the present invention comprises NPN switching transistors Q1, . . . , and On, PNP switching transistors Q1, . . . , and Qn, and NPN auxiliary transistors O'1, . . . , and O'n. The emitter electrodes of the NPN switching transistors are simultaneously supplied with the negative going high frequency pulses $\phi$. The collector electrodes of these NPN transistors are connected directly to the respective row electrodes 13 and to the first conductor 16 through resistors 41, respectively. The base electrodes of these NPN transistors, connected to the second conductor 17 through resistors 55, are cyclically supplied with the positive going time division pulses $t_1$ through $t_n$ through resistors 56, respectively. The emitter electrodes of the PNP transistors are connected directly to the first conductor 16. The collector electrodes of the PNP transistors are connected directly to the respective line electrodes 14 and to the second conductor 17 through resistors 42, respectively. The base electrodes of the PNP transistors are connected through capacitors 52 to those collector electrodes of the NPN auxiliary transistors, respectively, which are connected in common to the third conductor 23 through resistors 61, respectively. The emitter electrodes of the NPN auxiliary transistors are simultaneously supplied with the negative going high frequency pulses $\phi$. The base electrodes of these NPN transistors are connected to the second conductor 17 through resistors 62, respectively, and selectively supplied with the positive going cell selection or address pulses $a$, $b$, and the like through resistors 63, respectively.

It will be appreciated that the NPN switching transistors Q1 through Qn concurrently serve as AND circuits conditioned by the negative going high frequency pulses $\phi$ and the positive going time division pulses $t_1$ through $t_n$. More particularly, the negative going high frequency pulses $\phi$ intermittently reduce the emitter potential of these NPN transistors substantially to the zero level. Also, the positive going time division pulses $t_1$ through $t_n$ raise the base potential of these NPN transistors to cyclically apply forward voltage to the base-emitter junctions of the NPN transistors. In this manner, the NPN switching transistors cyclically and intermittently turn on to supply the voltage $V_4$ to the associated one of the row electrodes 13 at the frequency of the high frequency component of the control signals.

It will also be seen that the NPN auxiliary transistors O'1 through O'n serve as AND circuits are operative in response to the negative going high frequency pulses $\phi$ and the positive going address pulses $a$, $b$, and so forth. These NPN transistors further effect the current amplifying function. When the base and emitter electrodes of these NPN transistors are selectively supplied with the high frequency pulses $\phi$ and the address pulse, respectively, the NPN transistors turn on, amplify the high frequency pulses $\phi$, and apply the current amplified pulses to the base electrode of the associated PNP transistor to intermittently turn the selected PNP transistor on. In this manner, each of the NPN switching transistors Q1 through Qn and the concurrently selected one or ones of the PNP transistors Q1 through Qn cooperate to apply the voltage $V_4$ to the associated pair or pairs of the electrodes 13 and 14 at the frequency of the high frequency component of the control signals. The circuit shown in FIG. 6 is advantageous in applications where the output impedances of the control signal generator 12 supplying the positive going time division pulses $t_1$ through $t_n$ and the positive going address pulses $a$, $b$ and so on are relatively large.

While several embodiments and modifications thereof have been described above, it will be understood that the instant invention is applicable to a plasma display panel having opposing segment electrodes and that various combinations of the embodiments and their modifications are possible; and that the circuit arrangement according to the present invention may be provided by an integrated circuit with the pairs of PNP and NPN transistors implemented by sets of complementary transistors.

What is claimed is:
1. A circuit arrangement for making electric power source means and control signal generating means cooperate to drive a plasma display panel including a coplanar array of plasma discharge cells, a plurality of first electrodes, and a plurality of second electrodes, said first and second electrodes being disposed on both sides of said PNP and NPN transistors of said cells, wherein the improvement comprises a plurality of PNP transistors coupled to the respective ones of said first electrodes and a like number of NPN transistors coupled to the respective ones of said second electrodes, said PNP and NPN transistors being further coupled to said power source means and said control signal generating means and cooperatively producing a high frequency voltage to apply said voltage to a pair of the electrodes selected one each from said first and second electrodes in response to control signals generated by said control signal generating means, said power source means including a first and a second conductor between which a D.C. power is developed, each of said PNP and NPN transistors including an emitter, a collector, and a base electrode, wherein said control signal generating means comprises high frequency pulse generating means and address pulse generating means, the emitter electrodes of said PNP transistors are connected directly to said first conductor, the collector electrodes of said PNP transistors are connected to the respective ones of said first electrodes directly and to said second conductor through resistors, respectively, the emitter electrodes of said NPN transistors are connected directly to said second conductors, the collector electrodes of said NPN transistors are connected to the respective ones of said second electrodes directly and to said first conductor through resistors, respectively, and the base electrodes of said PNP and NPN transistors are coupled to said high frequency pulse generating means and said address pulse generating means whereby one of said PNP transistors and one of said NPN transistors selected by an address pulse generated by said address pulse generating means cooperatively amplify high frequency pulses generated by said high frequency pulse generating means to deliver the amplified high frequency pulses to a pair of the electrodes connected direct to the collector electrodes of the selected PNP and NPN transistors, wherein:
said high frequency pulse generating means comprises first and second high frequency pulse generating means for successively simultaneously producing first and second high frequency pulses, respectively,
said address pulse generating means comprises first and second address pulse generating means for successively simultaneously producing first and second address pulses, respectively, and
said arrangement further comprises AND circuits, each comprising a first input terminal, a second input terminal, and an output terminal, the output terminals being coupled to the respective base electrodes of said PNP and NPN transistors, the first input terminals of the AND circuits being coupled to said PNP and NPN transistors being connected to said first and second high frequency pulse generating means to be simultaneously supplied with said first and second high frequency pulses, respectively, the second input terminals of the AND circuits coupled to said PNP and NPN transistors being connected to said first and second address pulse generating means to be selectively supplied with said first and second address pulses, respectively.

2. A circuit arrangement as claimed in claim 1, wherein each of the base electrodes of said PNP transistors is connected to said first conductor through a resistor and to the output terminal of the AND circuit through a capacitor, the time constant dependent on the last-mentioned resistor and said capacitor being greater than the width of the first high frequency pulse.

3. A circuit arrangement as claimed in claim 1, wherein the AND circuits coupled to said PNP and NPN transistors are positive logic AND circuits and negative logic AND circuits, respectively, each of the output terminals of said positive logic AND circuits being coupled to the base electrode of the PNP transistor through an inverter circuit for inverting the signal produced at the output terminal of the positive logic AND circuit, each of the output terminals of said negative logic AND circuits being coupled to the base electrode of the NPN transistor through an inverter circuit for inverting the signal produced at the output terminal of the negative logic AND circuit.

4. A circuit arrangement for making electric power source means and control signal generating means cooperate to drive a plasma display panel including a coplanar array of plasma discharge cells, a plurality of first electrodes, and a plurality of second electrodes, said first and second electrodes being disposed on both sides of said array at the outside of said cells, wherein the improvement comprises a plurality of PNP transistors coupled to the respective ones of said first electrodes, and a like number of NPN transistors coupled to the respective ones of said second electrodes, said PNP and NPN transistors being further coupled to said power source means and said control signal generating means and cooperatively producing a high frequency voltage to apply said voltage to a pair of the electrodes selected one each from said first and second electrodes in response to control signals generated by said control signal generating means, said power source means including a first and a second conductor between which a D.C. power is developed, each of said PNP and NPN transistors including an emitter, a collector, and a base electrode, wherein:
said control signal generating means comprises high frequency pulse generating means for producing high frequency pulses, first address pulse generating means, and second address pulse generating means, said first and second address pulse generating means successively and simultaneously producing first and second address pulses, respectively, said arrangement further comprises AND circuits, each comprising a first input terminal, a second input terminal, and an output terminal, the emitter electrodes of said PNP transistors being connected direct to said first conductor, the collector electrodes of said PNP transistors being connected to the respective ones of said first electrodes directly and to said second conductor through resistors, respectively, the base electrodes of said PNP transistors being coupled to the respective terminal of said AND circuits, the collector electrodes of said NPN transistors being connected to the respective ones of second
electrodes directly and to said first conductor through resistors, respectively, the emitter electrodes of said NPN transistors and the first input terminals of said AND circuits being connected to said high frequency pulse generating means to be simultaneously supplied with said high frequency pulses, the base electrodes of said NPN transistors and the second input terminals of said AND circuits being connected to said first and second address pulse generating means to be selectively supplied with said first and second address pulses, respectively.

5. A circuit arrangement as claimed in claim 4, wherein each of said AND circuits comprises an NPN transistor including an emitter, a collector, and a base electrode, the emitter electrode serving as said first input terminal, the collector electrode serving as said output terminal, the base electrode serving as said second input terminal.

* * * * *