(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 288 832 B1**

(12) # EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification : **28.12.94 Bulletin 94/52**

(51) Int. Cl.[5] : **G11C 16/06,** G11C 7/00

(21) Application number : **88105979.4**

(22) Date of filing : **14.04.88**

(54) **Data writing system for EEPROM.**

(30) Priority : **30.04.87 JP 104506/87**

(43) Date of publication of application : **02.11.88 Bulletin 88/44**

(45) Publication of the grant of the patent : **28.12.94 Bulletin 94/52**

(84) Designated Contracting States : **DE FR**

(56) References cited :
WO-A-80/02881
WO-A-86/04727

(73) Proprietor : **KABUSHIKI KAISHA TOSHIBA**
72, Horikawa-cho
Saiwai-ku
Kawasaki-shi Kanagawa-ken 210 (JP)

(72) Inventor : **Iijima, Yasuo c/o Patent Division**
Kabushiki Kaisha Toshiba
1-1 Shibaura 1-chome
Minato-ku Tokyo 105 (JP)

(74) Representative : **Henkel, Feiler, Hänzel & Partner**
Möhlstrasse 37
D-81675 München (DE)

EP 0 288 832 B1

Description

The present invention relates to a data writing system for a semiconductor memory used as a data memory in, for example, an IC card, and, in particular, to an auto page writing system for an EEPROM.

EEPROMs, which permit electrical data erasing and rewriting, have recently become the object of considerable attention as a semiconductor memory for replacing EPROMs. Due to the EEPROMs requiring longer data writing time than EPROMS, however, various improvements have been made to the EEPROMs.

Of the improved EEPROMs, what is receiving attention is the type which has a buffer constituted by, for example, a RAM of several bytes such that data writing is done in the buffer within a specified time period and the contents of the buffer are then internally written in the EEPROM. The data writing time in this memory is about the same as what is required of an EPROM, so that the data writing time appears to be shortened. This EEPROM utilizes a system in which the memory is divided on the basis of the paging concept and some lower significant bits of an address data sent to the memory indicate the number of bytes in a page and the remaining higher significant bits indicate the number of pages. From that concept, this system is called a so-called page writing function.

A conventional page writing system functions as follows. Data for the page to be written is all transferred in advance in the buffer from the memory and data externally input replaces the data in the buffer. After a specified time, all the contents of the buffer are stored again in the specified page of the memory.

According to this system, for example, with an EEPROM of 8192 words × 8 bits, each page having a 16 byte area, address "0000_H" and address "$000F_H$" exist in the same page. If only the data at address "0000_H" is rewritten, data from address "0000_H" to address "$000F_H$" is temporarily stored in the buffer where the data corresponding to address "0000_H" alone is rewritten. Then, all the data in the buffer is written in the memory area from address "0000_H" to address "$000F_H$." That is, even if the data at address "0000_H" alone is rewritten, data writing is actually done to address "$000F_H$." Provided that the maxim rewritable number for an EEPROM is 10000, when data rewriting is done only to "0000_H" 10000 times, there would not be any guarantee for proper data writing for "$000F_H$." In other words, the writing times for the memory cells is too much in this case, thus reducing the life of the memory cells.

Conventionally, the write data reception time is fixed so that, when data input time is half the write data reception time in order to rewrite all the contents of a given page, the conventional EEPROM does not start the internal data writing unless the remaining half of the write data reception time is elapsed. From a global point of view, this results in a time loss in executing page writing, thus making it impossible to provide a higher data writing.

Further, according to the prior art, in order to cancel the page writing operation after data access is done within a given time for page writing, it is necessary to power off the EEPROM, for example, by shutting off the power supplied thereto.

In addition, the time specified for data writing in the buffer is only described in the specification. Therefore, the page writing operation for an EEPROM serving as an external unit is designed on the basis of the value given in the specification. Depending on EEPROMs, however, when the specified writing time becomes short due to some factors such as data writing environment, the external unit may erroneously recognize as if all the accessed data has been written. In this respect, therefore, there is a demand for a system which permits such an external unit to easily recognize whether or not an EEPROM is in the data reception state.

Prior art document WO-A-8 604 727 discloses a page mode writing system for writing data into the EEPROM comprising memory cells. During a loading cycle, latches are loaded with externally supplied data from bit lines. In addition, a program gate line is latched to a selected state to control whether its associated byte in the EEPROM will have data written into it during a page mode write cycle. Every eight bit line latches has one program gate latch which indicates whether or not the data in the eight latches should be transferred to the EEPROM cells during a write cycle. The writing cycle starts a fixed time period after the last leading edge of a word enable signal. During the writing cycle only data latched by the latches on the bit lines in selected bytes defined by line latches are stored in the EEPROM.

It is an object of this invention to provide a data writing system which reduces the writing times of memory cells so as to prevent reduction in the life of the memory cells, which can reduce a total write-in loss at the time of page writing operation and implement a high-speed writing process, which can cancel a page writing operation upon reception of an external request, without shutting off power, etc. and which ensures easy external recognition of the data reception time at the time the page writing is carried out.

To solve this object the present invention provides a data writing system as specified in the claims.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a circuit block diagram of an EEPROM;

Fig. 2 is a timing chart illustrating the timing for data writing; and

Fig. 3 is a flowchart for explaining an internal writing process.

An embodiment of this invention will now be ex-

plained with reference to the accompanying drawings.

Fig. 1 illustrates the circuit structure of an EEPROM of, for example, 64 kilobits (8192 words x 8 bits). A row address latch 1 latches the upper 8 bit data A_{12}-A_5 of address data A_{12}-A_0 in response to a signal d from a control circuit 10, which will be described later. A row address decoder 2 decodes the address data A_{12}-A_5 latched by row address latch 1 to produce a row select signal a and sends the signal a to a memory cell array 3 of 8192 words x 8 bits. A column address buffer 4 stores the lower 5 bit data A_4-A_0 of address data A_{12}-A_0. A column address decoder 5 decodes the address data A_4-A_0 from column address buffer 4 in response to a signal e (to be described later) from control circuit 10 to produce column select signals b and c.

An access identification (ID) latch 6 latches access ID data in response to signal c from column address decoder 5, An input data latch 7 latches 8 bit data from an input/output buffer 8, which will be described later, in response to signal c from column address decoder 5. The input/output buffer 8 stores 8-bit input/output data D_7-D_0 in response to a signal h from control circuit 10, which will be described later. A write controller 9 executes an internal writing operation in response to a signal f from control circuit 10, which will be described later.

Control circuit 10 controls the data writing and reading done to the present EEPROM. This control circuit 10 externally receives an $\overline{RST}$ signal (signal for cancelling the internal writing operation), a $\overline{WE}$ signal (write enable signal), and an $\overline{OE}$ signal (output enable signal), and outputs a WRB signal and an RRB signal as write status signals to the outside, the latter two signals being described later.

Fig. 2 illustrates the external writing timing for thus constituted EEPROM. In the normal state, both of the WRB and RRB signals are at an "H" level. The WRB signal becomes "L" level when the first byte of write bytes is accessed and again becomes "H" level when the subsequent internal writing operation is completed.

Control circuit 10 includes a timer 11 and a counter 12. Timer 11 is for determining a data reception time for the next write bytes after the present write bytes have been input. Counter 12 counts how many times the write bytes are received. According to this embodiment, the data reception ends upon reception of, for example, 32 bytes. Timer 11 is designed to overflow upon elapse of 50 μs after being reset. In other words, the reception operation for the write bytes will end either when 50 μs has elapsed between accessing of one byte and the next byte or when accessing between bytes falls within 50 μs but 32 bytes are accessed. The count-up operation of counter 12 and the reset operation for timer 11 are executed by an input reception timer reset signal (pulse) that is produced by a data writing operation. It is the RRB signal which informs to the outside whether or not the data reception operation is in process, and this signal becomes "L" level upon completion of the data reception and becomes "H" level upon completion of the subsequent internal writing operation.

When both the WRB and RRB signals are "H" level, it means that the EEPROM is ready for the first byte of write bytes. When the WRB signal is "L" level and the RRB signal is "H" level, the first byte has already been received and the reception of the subsequent bytes is being carried out. When both of the WRB and RRB signals are "L" level, the write byte reception is inhibited and the internal writing operation is in process. This permits an external unit to easily discriminate the above three states.

When data writing is performed with both of the WRB and RRB signals being at "H" level, address data A_{12}-A_0 is latched as a row address in row address latch 1 by the signal (signal d in Fig. 1) resulting from a logical product of the $\overline{CE}$ and $\overline{WE}$ signals. At this time, the WRB signal is set to "L" level. At the same time, column address decoder 5 decodes address data A_4-A_0 from column address buffer 4 based on the signal (signal e in Fig. 1) which is a logical product of the $\overline{CE}$ and $\overline{WE}$ signals, thereby producing the signal c.

Access ID latch 6 is constituted by 32 1-bit latches and is normally reset; only that constituent latch which is selected by the signal c is set. Input data latch 7 is constituted by latches of 8 bits × 32 words; each 8-bit latch is selected by the signal c and the latch selected at this time latches data coming through input/output buffer 8. In other words, when data values of A_4-A_0 are input at random, they are stored in their associated 8-bit latches and access ID latch 6 stores data that indicates which latches the data is stored.

In the case of Fig. 2, upon elapse of the data reception time, data "xx" is latched in row address latch 1. In input data latch 7, data "a" is latched in the first 8-bit latch, and data "d", "c", and "b" are latched in the third, fourth and seventh 8-bit latches, respectively. In access ID latch 6, the first-bit, third-bit, fourth-bit and seventh-bit latches are set with the remaining ones being reset.

The internal writing operation will now be explained, referring to the flowchart of Fig. 3. First, upon elapse of the data reception time, the column address for the internal writing operation is set to "0" (step S31). This column address is generated by a column address generator (not shown) included in write controller 9 and is a value between "00" to "1F." The output of the column address generator is decoded to thereby produce the row select signal i and the signals j and k.

Based on the generated signal j, write controller 9 selects the associated latch in access ID latch 6, i.e., controller 9 refers to the access ID data corre-

sponding to the column address (step S32) and discriminates whether or not the selected latch is set (step S33). If the latch is not set (or at "0"), no data writing to memory cell array 3 is performed and the address is incremented by one by the column address generator (step S34).

If the selected latch is in the set state (or at "0"), based on the generated signal k write controller 9 selects the associated 8-bit latch in input data latch 7 or selects the 8-bit latch of input data latch 7 which corresponds to the column address. The data in the selected latch is sent to memory cell array 3, and at the same time, the memory cell to be accessed for data writing is designated by the column select signal i (column address) and row select signal a (row address) and a write permit signal l is supplied to memory cell array 3. Upon reception of the write permit signal l, memory cell array 3 stores data received in advance into the memory cell (of 8 bits) designated by the address data (step S35). Write controller 9 discriminates that the data has been written in memory cell array 3 and causes its column address generator to increment the column address by one (step S34).

Prior to step S34 where the column address is incremented by one, however, it is determined whether or not the address is "$1F_H$" (step S36). If the decision is affirmative, write controller 9 sends a signal m to control circuit 10 to inform that the writing operation is completed. When acknowledging the end of the writing operation through the signal m, control circuit 10 sets both the WRB and RRB signals at "H" level and resets all the latches of access ID latch 6 using a signal g, setting latch 6 back to the normal memory state.

During the internal writing operation in Fig. 2, the $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ signals are ineffective.

An read operation is performed in response to the $\overline{CE}$ and $\overline{OE}$ signals that are input during a read permit time (the period other than the internal writing period in Fig. 2). If control circuit 10 discriminates at this time that the read operation is being performed, address data A_{12}-A_5 is converted into the row select signal a by row address decoder 2 through row address latch 1. Address data A_4-A_0 is converted into the column select signal b by column address decoder 5 through column address buffer 4. Data in the memory cell (of 8 bits) specified by the row select signal a and column select signal b is read out and stored in input/output buffer 8 by signal h.

When the $\overline{RST}$ signal is set to "L" level during the data reception period in Fig. 2, control circuit 10 sets both of the WRB and RRB signals to "H" level, and, at the same time, resets all the latches of access ID latch 6, thus setting the latch 6 back to the normal memory state.

According to a preferred embodiment of the present data writing system, there is provided means (access ID latch 6) for storing access ID data for the buffers for one page so that those buffers accessed within a specified time can be discriminated and only the contents of the buffers accessed during the internal writing operation are written in the memory cells. This can ensure that only the data received during the data reception time is accurately written in the target memory cells. Therefore, the writing times of the memory cells can be reduced, thus preventing the life of the memory cells from being shortened.

In addition, counter 12 for counting the quantity of data received at the time of the data reception is provided so that when the quantity of the counted data reaches a predetermined value (for example, 32 bytes), the write data reception is ended and the internal writing operation is performed immediately thereafter. This reduces an overall write time loss at the time of the page writing operation, thus ensuring a higher writing operation.

Further, control circuit 10 is designed to receive the internal writing cancel signal ($\overline{RST}$ signal), which is externally generated, so that upon reception of this signal during the write data reception time, the present system resets the internal circuits to cancel the page writing operation and returns to the normal state. With this design, therefore, even when the memory cells are accessed for a page writing operation at some timing, the page writing operation can be canceled by an external request.

Furthermore, at the time of the page writing operation, the write status signals (WRB and RRB signals) are output to the outside and the levels of these write status signals are changed at the time when the first byte is received for the page writing operation, at the time when a predetermined time has elapsed (the data reception operation is ended) and at the time when the internal writing operation is ended. This ensures an easy external detection of the data reception time for the page writing operation, thus providing an effective writing sequence as an external unit.

Claims

1. A data writing system comprising:

memory means (3) having pages, each page including a plurality of word areas;

means (7) for receiving and holding externally supplied data to be stored in the memory means (3); and

write control means (9, 10) for writing the data held in the receiving and holding means (7) into a designated word area of a specific page in the memory means (3); wherein

said write control means (9, 10) includes a timer (11) for counting the time interval from a first time point at which a unit of said externally supplied data is received to a second time point at which the next unit of said externally supplied

data is received, and means (9, 10) for terminating the reception of the externally supplied data when the next unit of data is not received within a predetermined period of time counted by the timer (11), thereby enabling the data transfer from the data receiving and holding means (7) to the memory means (3) immediately after the reception of the externally supplied data is terminated,

characterized by further comprising:

output means (10) for outputting to an external device first data (RRB) representing whether or not the writing operation by the write control means (9, 10) is being performed.

2. A data writing system according to claim 1, characterized in that said output means (10) further output to the external device second data (WRB, RRB) representing a period during which the data to be renewed can be received.

3. A data writing system according to claim 1 or 2, characterized in that said data receiving and holding means (7) includes first storing means (7) having the same number of words and bits as the page in the memory means (3) for receiving and holding the data to be renewed, and a second storing means (6) for storing identification data representing the locations of words in said first storing means which are to be renewed in the memory means (3); and that said write control means (9, 10) includes means (9, 10) for reading out only the data words stored in the first storing means (7) which are designated for renewal by said second storing means so as to store the read data words into the memory means (3).

4. A data writing system according to claim 1 or 2, characterized in that said write control means (9, 10) includes means for cancelling the writing operation of the data held in the data receiving and holding means (7) into the memory means (3) in response to an external signal ($\overline{RST}$), when the data receiving and holding means (7) receives the new data to be stored in the memory means (3).

5. The data writing system according to claim 4, characterized in that said write control means (9, 10) outputs to an outside a signal (WRB, RRB) indicating a data reception period for said receiving and holding means (7).

6. The data writing system according to any one of claims 1 to 5 characterized in that said memory means (3) is included in an EEPROM.

Patentansprüche

1. Datenschreibsystem, welches folgendes umfaßt:
eine Speichereinrichtung (3) mit Seiten, wobei jede Seite eine Vielzahl von Wortbereichen enthält;
eine Einrichtung (7) zum Empfangen und Halten extern gelieferter in der Speichereinrichtung (3) zu speichernder Daten; und
eine Schreibsteuereinrichtung (9, 10) zum Schreiben der in der Empfangs- und Halteeinrichtung (7) gehaltenen Daten in einen vorgegebenen Wortbereich einer bestimmten Seite in der Speichereinrichtung (3);
wobei die Schreibsteuereinrichtung (9, 10) einen Zeitgeber (11) zum Zählen des Zeitintervalls ab einem ersten Zeitpunkt, in dem eine Einheit der extern gelieferten Daten empfangen wird, bis zu einem zweiten Zeitpunkt, in dem die nächste Einheit der extern gelieferten Daten empfangen wird, und eine Einrichtung (9, 10) zum Beenden des Empfangs der extern gelieferten Daten, wenn die nächste Dateneinheit nicht innerhalb einer vorgegebenen vom Zeitgeber (11) gezählten Zeitspanne empfangen wird, womit die Datenübertragung von der Empfangs- und Halteeinrichtung (7) an die Speichereinrichtung (3) unmittelbar nach der Beendigung des Empfangs der extern gelieferten Daten freigegeben wird, enthält,
dadurch gekennzeichnet, daß es weiterhin umfaßt: eine Ausgabeeinrichtung (10) zur Ausgabe eines ersten Datums (RRB) an eine externe Einrichtung, welches angibt, ob die Schreiboperation durch die Schreibsteuereinrichtung (9, 10) durchgeführt wird oder nicht.

2. Datenschreibsystem gemäß Anspruch 1, dadurch gekennzeichnet, daß die Ausgabeeinrichtung (10) des weiteren ein zweites Datum (WRB, RRB) an die externe Einrichtung ausgibt, welches eine Zeitspanne repräsentiert, während der das zu erneuernde Datum empfangen werden kann.

3. Datenschreibsystem gemäß Anspruch 1 oder 2, dadurch gekennzeichnet, daß die Datenempfangs- und Halteeinrichtung (7) eine erste Speichereinrichtung (7) mit derselben Anzahl von Wörtern und Bits wie die Seite in der Speichereinrichtung (3) zum Empfang und zum Halten der zu erneuernden Daten und eine zweite Speichereinrichtung (6) zum Speichern von Identifikationsdaten, welche die Plätze von Wörtern in der ersten Speichereinrichtung repräsentieren, die in der Speichereinrichtung (3) zu erneuern sind, enthält; und daß die Schreibsteuereinrichtung (9, 10) eine Einrichtung (9, 10) zum Auslesen nur der in der ersten Speichereinrichtung (7) gespeicher-

ten Datenwörter, welche zur Erneuerung durch die zweite Speichereinrichtung vorgegeben sind, um die gelesenen Datenwörter in der Speichereinrichtung (3) zu speichern, enthält.

4. Datenschreibsystem gemäß Anspruch 1 oder 2, dadurch gekennzeichnet, daß die Schreibsteuereinrichtung (9, 10) eine Einrichtung zum Annullieren der Schreiboperation der in der Datenempfangs- und Halteeinrichtung (7) gehaltenen Daten in die Speichereinrichtung (3) als Reaktion auf ein externes Signal ($\overline{RST}$), wenn die Datenempfangs- und Halteeinrichtung (7) die neuen in der Speichereinrichtung (3) zu speichernden Daten empfängt.

5. Datenschreibsystem gemäß Anspruch 4, dadurch gekennzeichnet, daß die Schreibsteuereinrichtung (9, 10) nach außen ein Signal (WRB, RRB) absetzt, welches einen Datenempfangszeitraum für die Empfangs- und Halteeinrichtung (7) angibt.

6. Datenschreibsystem gemäß einem der Ansprüche 1 bis 5, dadurch gekennzeichnet, daß die Speichereinrichtung (3) in einem EEPROM enthalten ist.

Revendications

1. Système d'écriture de données comprenant :
un dispositif de mémoire (3) ayant des pages, chaque page comprenant une pluralité de zones de mots ;
un dispositif (7) pour recevoir et maintenir de façon externe des données appliquées à stocker dans le dispositif de mémoire (3) ; et
un dispositif de commande d'écriture (9, 10) pour écrire les données maintenues dans le dispositif de réception et de maintien (7) dans une zone de mots désignée d'une page spécifique dans le dispositif de mémoire (3) ; dans lequel
ledit dispositif de commande d'écriture (9, 10) comprend un temporisateur (11) pour compter l'intervalle de temps à partir d'un premier instant auquel une unité desdites données fournies de façon externe est reçue jusqu'à un second instant auquel l'unité suivante desdites données fournies de façon externe est reçue, et un dispositif (9, 10) pour terminer la réception des données fournies de façon externe lorsque l'unité suivante de données n'est pas reçue dans une période de temps prédéterminée comptée par le temporisateur (11), validant ainsi le transfert des données du dispositif de réception et de maintien de données (7) au dispositif de mémoire (3) immédiatement après que soit terminée la réception des données fournies de façon externe,
caractérisé en outre en ce qu'il comprend :
un dispositif de sortie (10) pour fournir à un dispositif externe des premières données (RRB) représentant si l'opération d'écriture par le dispositif de commande d'écriture (9, 10) est ou non en cours de réalisation.

2. Système d'écriture de données selon la revendication 1, caractérisé en ce que ledit dispositif de sortie (10) fournit en outre au dispositif externe des secondes données (WRB, RRB) représentant une période pendant laquelle les données à renouveler peuvent être reçues.

3. Système d'écriture de données selon la revendication 1 ou 2, caractérisé en ce que ledit dispositif de réception et de maintien de données (7) comprend un premier dispositif de stockage (7) ayant le même nombre de mots et de bits que la page dans le dispositif de mémoire (3) pour recevoir et maintenir les données à renouveler, et un second dispositif de stockage (6) pour stocker des données d'identification représentant les emplacements de mots dans ledit premier dispositif de stockage qui sont à renouveler dans le dispositif de mémoire (3) ; et en ce que ledit dispositif de commande d'écriture (9, 10) comprend un dispositif (9, 10) pour extraire seulement les mots de données stockés dans le premier dispositif de stockage (7) qui sont désignés pour le renouvellement par ledit second dispositif de stockage afin de stocker les mots de données lus dans le dispositif de mémoire (3).

4. Système d'écriture de données selon la revendication 1 ou 2, caractérisé en ce que ledit dispositif de commande d'écriture (9, 10) comprend ùn dispositif pour annuler l'opération d'écriture des données maintenues dans le dispositif de réception et de maintien de données (7) dans le dispositif de mémoire (3) en réponse à un signal externe ($\overline{RST}$), lorsque le dispositif de réception et de maintien de données (7) reçoit les nouvelles données à stocker dans le dispositif de mémoire (3).

5. Système d'écriture de données selon la revendication 4, caractérisé en ce que ledit dispositif de commande d'écriture (9, 10) fournit à l'extérieur un signal (WRB, RRB) indiquant une période de réception de données pour ledit dispositif de réception et de maintien (7).

6. Système d'écriture de données selon l'une quelconque des revendications 1 à 5, caractérisé en ce que ledit dispositif de mémoire (3) est compris dans une EEPROM.

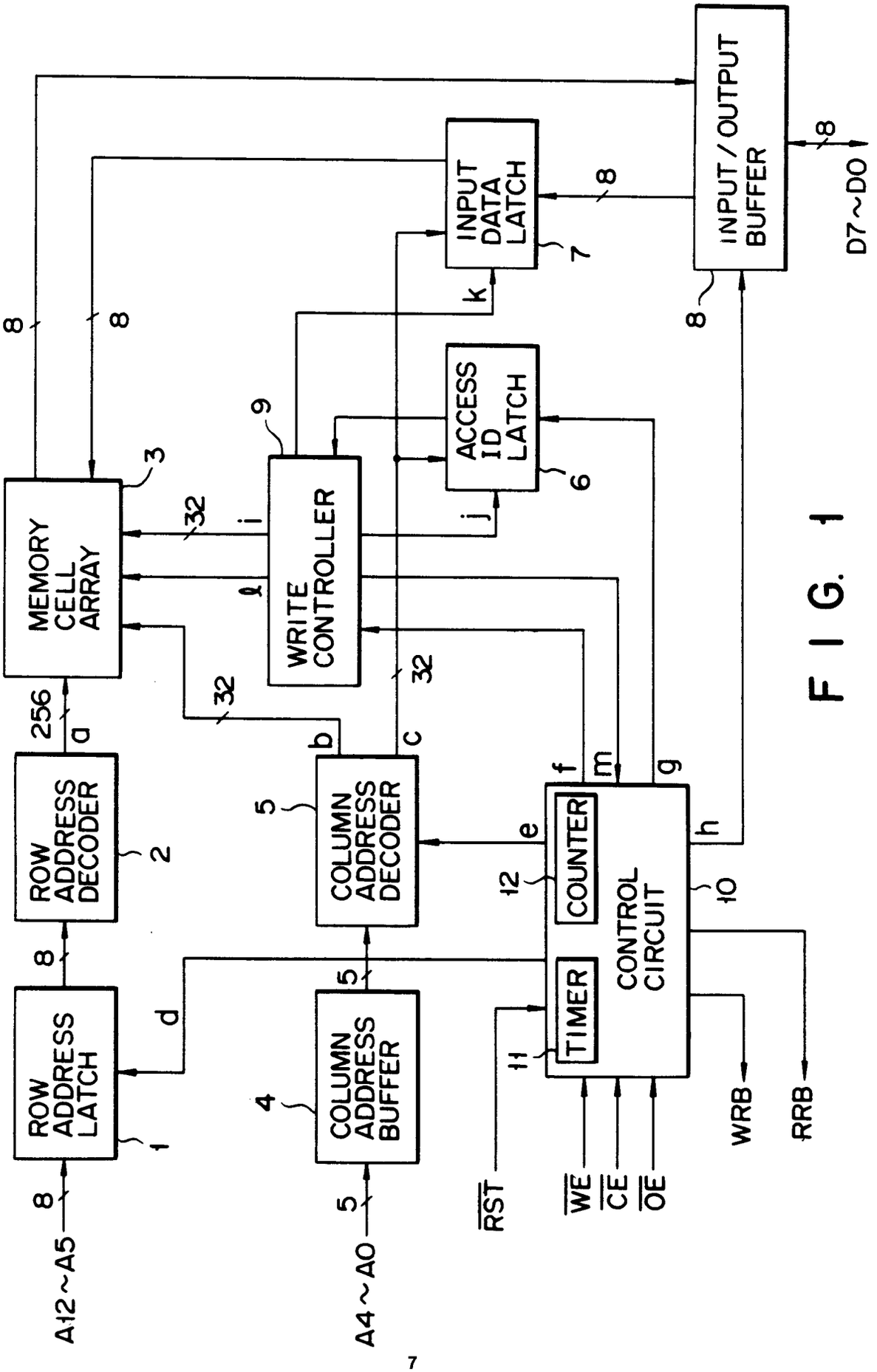
MEMORY CELL ARRAY
3
ROW ADDRESS DECODER
2
ROW ADDRESS LATCH
1
COLUMN ADDRESS DECODER
5
COLUMN ADDRESS BUFFER
4
WRITE CONTROLLER
9
ACCESS ID LATCH
6
INPUT DATA LATCH
7
INPUT / OUTPUT BUFFER
CONTROL CIRCUIT
10
COUNTER
12
TIMER
11
A12~A5
A4~A0
D7~D0
RST
WE
CE
OE
WRB
RRB
256
32
8
a
b
c
d
e
f
g
h
i
j
k
l
m

FIG. 1

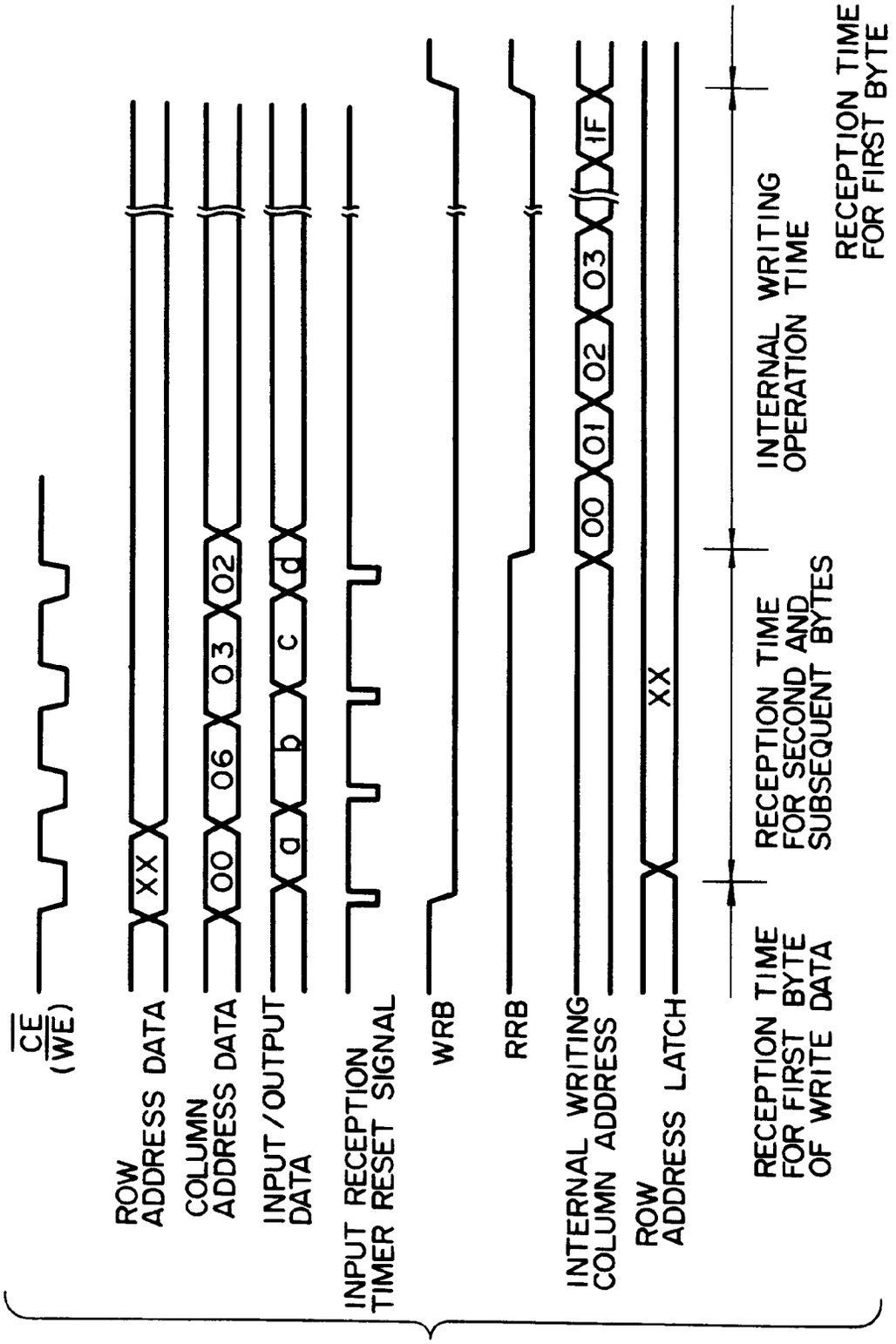
CE
(WE)
ROW ADDRESS DATA
XX
COLUMN ADDRESS DATA
00
06
03
02
INPUT / OUTPUT DATA
a
b
c
d
INPUT RECEPTION TIMER RESET SIGNAL
WRB
RRB
INTERNAL WRITING COLUMN ADDRESS
00
01
02
03
1F
ROW ADDRESS LATCH
XX
RECEPTION TIME FOR FIRST BYTE OF WRITE DATA
RECEPTION TIME FOR SECOND AND SUBSEQUENT BYTES
INTERNAL WRITING OPERATION TIME
RECEPTION TIME FOR FIRST BYTE

FIG. 2

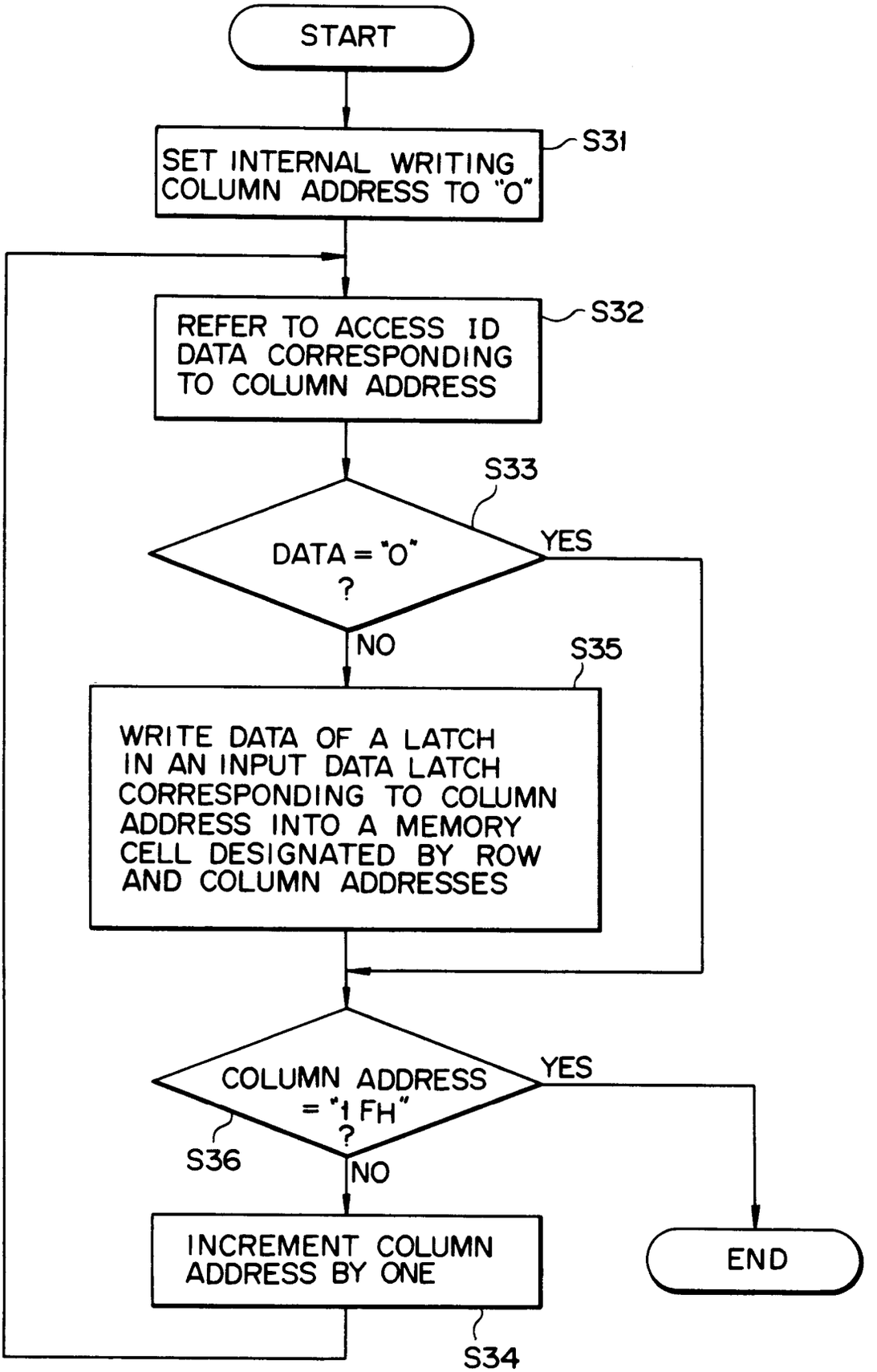
START
SET INTERNAL WRITING COLUMN ADDRESS TO "0"
S31
REFER TO ACCESS ID DATA CORRESPONDING TO COLUMN ADDRESS
S32
S33
DATA = "0" ?
YES
NO
S35
WRITE DATA OF A LATCH IN AN INPUT DATA LATCH CORRESPONDING TO COLUMN ADDRESS INTO A MEMORY CELL DESIGNATED BY ROW AND COLUMN ADDRESSES
COLUMN ADDRESS = "1FH" ?
YES
S36
NO
INCREMENT COLUMN ADDRESS BY ONE
S34
END

FIG. 3