(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 January 2003 (09.01.2003)

(10) International Publication Number
WO 03/003576 A2

(51) International Patent Classification:
H03K

(21) International Application Number:
PCT/IB02/02526

(22) International Filing Date:
20 June 2002 (20.06.2002)

(25) Filing Language:
English

(26) Publication Language:
English

(30) Priority Data:
09/894,390 28 June 2001 (28.06.2001) US

(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors: SINGH, Balwinder; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). DE LANGEN, Klaas-Jan; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: VON LAUE, Hans-Ulrich; Internationaal Octroibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(54) Title: LEVEL SHIFTER WITH INDEPENDENT GROUNDS AND IMPROVED EME-ISOLATION

(57) Abstract: A driving circuit provides a symmetric differential driving signal relative to one set of voltage potentials to a driver circuit that drives an output node to another set of voltage potentials. The differential driving signals from the driving system are equal and opposite to each other, thereby avoiding stray current flow between the driving system and the driven current mirrors. The transistors that provide the driving signal are continuously biased, using a weak bias in one logic state and stronger bias in the other state, to avoid hard-switching transients.
Level shifter with independent grounds and improved eme-isolation

This invention relates to the field of electronic circuits, and in particular to a level shifter with independent ground potentials, and reduced electro-magnetic emissions (EME).

Level shifters are commonly used to provide communication of signals from a system having a first range of voltage potential to another system having a different range of voltage potential. For example, level shifters are commonly used in automotive applications, because typical automobile systems operate at 0-18 volts, whereas common integrated circuits typically operate at 0-3 volts, or 0-5 volts. An asserted "logic-high" three or five volt output from an integrated circuit may be insufficient to be interpreted as a logic-high in a twelve volt system. A level shifter provides the appropriate mapping of voltage levels from one system to another, to ensure the proper communication of logic values.

Figure 1 illustrates an example schematic of a conventional level shifter 100 that is configured to provide a logic-high voltage level of Vd2 at its output (Out) corresponding to a logic-high voltage level of Vd1 at its input (In). The logic-low levels of both signal (In, Out) is zero volts. Each of these voltage potentials are referenced with regard to a common ground potential.

When a logic-high (Vd1) input signal is received at the In node, the transistor N1 is turned on. At the same time, the inverter 110 turns transistor N2 off. With transistor N1 turned on, and N2 turned off, transistor P2 is turned on, thereby pulling the Out node to Vd2. In this manner, an input voltage level of Vd1 is converted to an output voltage level of Vd2.

When a logic-low (ground potential) input signal is received, transistor N1 is turned off, and the inverter 110 turns transistor N2 on. With transistor N1 turned off, transistor P2 is turned off, and transistor N2 pulls the Out node to ground potential. In this manner, an input signal at ground potential provides an output signal that is also at ground potential.

Note that the level shifter of Figure 1 relies on a common ground potential for proper operation. If the ground of the input system (inverter 110) differs from the ground
potential of the output system (N1, P1, N2, P2), ground currents will flow. If the difference between ground potentials is significant, the level shifter 100 may fail to operate, or may operate intermittently.

Figure 2 illustrates an example schematic of a level shifter 200 that is configured to convert signals from floating sources 210, 220 into signals for driving a bus between two potentials, V+, V-, as presented in US Patent 6,154,061, "CAN BUS DRIVER WITH SYMMETRICAL DIFFERENTIAL OUTPUT SIGNALS", issued 28 November 2000 to Hendrik Boezen et al, and incorporated by reference herein. Transistor P2 and diode D1 are configured to drive a bus load Lb to a potential of V+, and transistors N2 and diode D2 are configured to drive a bus load La to a potential of V- and therefore substantially independent of potentials V+ and V- for both logic-high and logic-low signal levels. The level shifter 200 provides equal and opposite currents to the loads La, Lb, thereby avoiding ground currents, and ground bounce as the bus switches state. The output transistors P2 and N2, however, are hard-driven to each corresponding rail voltage, V+ and V-, at each bus state transition, causing substantial electro-magnetic emissions (EME).

It is an object of this invention to provide a level shifter that allows for two substantially independent ground voltage potentials. It is a further object of this invention to provide a level shifter that has reduced electromagnetic emissions (EME), compared to the conventional level shifters of Figures 1 and 2.

These objects, and others, are achieved by providing a symmetric differential driving signal relative to one set of voltage potentials to a pair of current sources that drive an output node to another set of voltage potentials. The differential driving signals from the driving system are equal and opposite to each other, thereby avoiding stray current flow between the driving system and the driven current mirrors. The transistors that provide the driving signal are continuously biased, using a weak bias in one logic state and stronger bias in the other state, to avoid hard-switching transients.

The invention is explained in further detail, and by way of example, with reference to the accompanying drawings wherein:

Figure 1 illustrates an example schematic of a prior art level shifter.
Figure 2 illustrates an example schematic of a prior art symmetric differential bus driver.

Figure 3 illustrates an example schematic of a level shifter in accordance with this invention.

Figure 3 illustrates an example schematic of a level shifter 300 in accordance with this invention. For convenience, the level shifter 300 is hereinafter referred to as comprising a transmitting (driving) section 310, and a receiving (driven) section 320. Consistent with this terminology and the prior art, the level shifter 300 may also be referred to as a transceiver. The transmit section 310 is configured to operate with power supply potentials of Vdd1 and G1, and the receive section 320 is configured to operate with power supply potentials of Vdd2 and G2. These two sets of voltage potentials are substantially independent, the relationship between them being symbolized by a virtual resistance $R_{\text{gnd}}$ between the two ground potentials G1 and G2. Note that as used herein, the term ground potential is used merely to identify a potential that a particular system uses as a reference potential, which may or may not be tied to an earth-ground potential, and may in fact be floating relative to any other reference potential.

The transmit section 310 includes transistors Pt1, Pt2, Nt1, and Nt2 that are configured in a current mirror configuration. A current source I_{\text{bias}} is provided to weakly bias the transistors Pt1, Pt2, Nt1, and Nt2. The input signal, I_{\text{in}}, controls whether or not an additional current source, I_{\text{drive}}, is applied in parallel to the bias current I_{\text{bias}}. The diodes D1 and D2 protect the supplies Vdd1 and Vdd2 from being shorted to ground potentials G2 and G1, respectively.

The receive section 320 includes transistors Pr1 and Pr2 that act as current sources, and transistors Nr1 and Nr2 that are configured as a resistor-rationed current mirror. The voltage B biases the gates of transistors Pr1 and Pr2.

In the absence of the I_{\text{drive}} current, when the I_{\text{in}} signal is not asserted (logic-low), the I_{\text{bias}} current is mirrored by the transistors Pt2 and Nt2 to cause current flow through resistors R4 and R1, respectively. The resultant voltage across the resistors R4 and R1 biases Pr1 and Nr2 away from conduction, causing a weak pull-up of the output signal Out toward Vdd2. The current source I_{\text{weak}} is provided to counteract this weak pull-up, and pulls the output signal Out to ground potential G2. Thus, with a non-asserted input signal, the
output signal is pulled to a ground potential G2, independent of the reference potentials Vdd1, G1 associated with the input signal.

When the In signal is asserted (logic-high), the Idrive current augments the Ibias current, and this additive current is mirrored by the transistors Pt2 and Nt2, causing more current to flow through resistors R4 and R1, thereby turning transistor Pr2 on, and transistors Pr1, Nr1, and Nr2 off. Because the Iweak current source is weak, the conduction of transistor Pr2 pulls the Out signal to Vdd2. Thus, with an asserted input signal, the output signal is pulled to a source potential Vdd2, independent of the reference potentials Vdd1, G1 associated with the input signal. Because the transistors Pt2 and Nt2 are initially biased by the Ibias current source, the application of the Idrive current source does not introduce a hard switching of the transistors Pt2 and Nt2, thereby reducing EME, relative to the hard-switching EME of the bus driving circuit 200 of Figure 2.

The current mirror configuration of the transmit section 310 assures that equal currents flow through transistors Pt2 and Nt2. The current flow through Pt2 flows into the receiver 320, and the current flow through Nt2 flows from the receiver 320. This equal and opposite current flow avoids current flow through the ground path Rgnd, thereby minimizing ground bounce and hence minimizing EME.

Note that, if the potential difference between G1 and G2 is very large, some pull-up or pull-down current through Rgnd will occur. In such cases, the level-shifting function of the level shifter 300 will continue to operate properly, albeit with some ground-bounce induced EME. The level shifter 300 can operate at high speeds, can tolerate large ground offsets, and has a large common-mode range.

The foregoing merely illustrates the principles of the invention. It will thus be appreciated that those skilled in the art will be able to devise various arrangements which, although not explicitly described or shown herein, embody the principles of the invention and are thus within the spirit and scope of the following claims.
CLAIMS:

1. A level shifter (300) comprising:
   - a driver circuit (310) that is configured to provide a first current and an equal
     and opposite second current from a first set of supply voltage potentials (Vdd1, G1), and
   - a driven circuit (320), operably coupled to the driver circuit (310), that is
     configured to provide an output signal (Out) corresponding to a second set of supply voltage
     potentials (Vdd2, G2),

5 wherein the first set of supply voltage potentials (Vdd1, G1) are substantially independent of
the second set of supply voltage potentials (Vdd2, G2).

10 2. The level shifter (300) of claim 1, wherein the driver circuit (310) includes a
pair of current mirrors (Pt1-Pt2, Nt1-Nt2) for providing the first and second equal and
opposite currents.

3. The level shifter (300) of claim 2, further including

15 - a voltage controlled current source (Idrive) that provides a controlled input
current to the pair of current mirrors (Pt1-Pt2, Nt1-Nt2).

4. The level shifter (300) of claim 3, further including
   - a bias current source (Ibias) that provides a bias input current to the pair of
   current mirrors (Pt1-Pt2, Nt1-Nt2).

20 5. The level shifter (300) of claim 2, further including
   - a bias current source (Ibias) that provides a bias input current to the pair of
   current mirrors (Pt1-Pt2, Nt1-Nt2).

25 6. The level shifter (300) of claim 1, wherein the driver circuit (310) provides the
first and second currents in dependence upon a state of an input signal (In).

7. The level shifter (300) of claim 6, wherein the driver circuit (310) provides
- a bias current during a first state of the input signal (In), and
- a drive current that is substantially larger than the bias current during a second state of the input signal (In).

8. The level shifter (300) of claim 1, wherein the driven circuit (320) includes:
- a first resistor (R1) through which the first current flows between a first voltage source (Vdd2) of the second set of supply voltage potentials (Vdd2, G2) and the driver circuit (310), and
- a second resistor (R4) through which the second current flows between a second voltage source (G2) of the second set of supply voltage potentials (Vdd2, G2) and the driver circuit (310);
wherein a state of the output signal (Out) is dependent upon voltage drops across the first (R1) and second (R4) resistors.

9. The level shifter (300) of claim 8, further including
- a weak current source (Iweak) that is configured to control the state of the output signal (Out) when the voltage drops are below a given threshold level.

10. The level shifter (300) of claim 1, wherein the driven circuit (320) includes:
- a current mirror (Nr1-Nr2) and
- at least one current source (Pr2);
wherein a state of the output signal (Out) is dependent upon current flows through the current mirror (Nr1-Nr2) and the at least one current source (Pr2).

11. A level shifter circuit (300) for coupling a first system having a first pair of voltage supply potentials (Vdd1, G1) with a second system having a second pair of voltage supply potentials (Vdd2, G2), comprising:
- a driver circuit (310) comprising:
  a first current mirror (Pt1-Pt2) that provides a first current to the second system, and
  a second current mirror (Nt1-Nt2) that draws a second current from the second system,
the second current being substantially equal in magnitude to the first current; and
- a driven circuit (320) comprising:
  one or more current sources (Pr2) that are configured to selectively
couple an output signal (Out) to either voltage supply of the second pair of voltage supply
potentials (Vdd2, G2) in dependence upon the magnitude of the first and second currents.

12. The level shifter circuit (300) of claim 11, wherein
the first current mirror (Pt1-Pt2) includes
- a first p-channel device (Pt1) having
  a source that is coupled to a first voltage supply (Vdd1) of the first
pair of voltage supply potentials (Vdd1, G1),
  a drain that is coupled to a first terminal of a controllable current
source (Idrive, Ibias), and
  a gate that is coupled to the drain of the first p-channel device (Pt1);
- a second p-channel device (Pt2) having
  a source that is coupled to the first voltage supply (Vdd1) of the first
pair of voltage supply potentials (Vdd1, G1),
  a drain that is configured to provide the first current, and
  a gate that is coupled to the gate of the first p-channel device (Pt1);
the second current mirror (Nt1-Nt2) includes
- a first n-channel device (Nt1) having
  a source that is coupled to a second voltage supply (G1) of the first
pair of voltage supply potentials (Vdd1, G1),
  a drain that is coupled to a second terminal of the controllable current
source (Idrive, Ibias), and
  a gate that is coupled to the drain of the first n-channel device (Nt1);
- a second n-channel device (Nt2) having
  a source that is coupled to the second voltage supply (G1) of the first
pair of voltage supply potentials (Vdd1, G1),
  a drain that is configured to draw the second current, and
  a gate that is coupled to the gate of the first n-channel device (Nt1).

13. The level shifter circuit (300) of claim 12, further including
- the controllable current source (Idrive, Ibias), and
wherein
- the controllable current source (I_{drive}, I_{bias}) includes:
  - a bias current source (I_{bias}), and
  - a drive current source (I_{drive}) that is controllably coupled to the bias current source (I_{bias}) based on an input signal (I_{in}).

14. The level shifter circuit (300) of claim 12, further including:
- a first diode that is coupled to the drain of the second p-channel device (P_{T2}), and
- a second diode that is coupled to the drain of the second n-channel device (N_{T2}).

15. The level shifter circuit (300) of claim 12, wherein the driven circuit (320) includes
- a first resistor (R_{1}) that is coupled between a first voltage supply (V_{dd2}) of the second pair of voltage supply potentials (V_{dd2}, G_{2}) and a first node,
- a third p-channel device (P_{R1}) having
  - a source that is coupled to the first node,
  - a drain that is coupled to a second node, and
  - a gate that is coupled to a third node;
- a second resistor (R_{2}) that is coupled between the first voltage supply (V_{dd2}) of the second pair of voltage supply potentials (V_{dd2}, G_{2}) and a fourth node,
- a fourth p-channel device (P_{R2}) having
  - a source that is coupled to the fourth node,
  - a drain that is coupled to a fifth node, and
  - a gate that is coupled to the third node;
- a third resistor (R_{3}) that is coupled between a second voltage supply (G_{2}) of the second pair of voltage supply potentials (V_{dd2}, G_{2}) and a sixth node,
- a third n-channel device (N_{R1}) having
  - a source that is coupled to the sixth node,
  - a drain that is coupled to the second node, and
  - a gate that is coupled to the second node;
- a fourth resistor (R_{4}) that is coupled between the second voltage supply (G_{2}) of the second pair of voltage supply potentials (V_{dd2}, G_{2}) and a seventh node,
- a fourth n-channel device (N_{R2}) having
a source that is coupled to the seventh node,
a drain that is coupled to the fifth node, and
a gate that is coupled to the second node; and

wherein:

the first current is provided to the seventh node,
the second current is drawn from the first node, and
the fifth node corresponds to the output signal (Out).

The level shifter circuit (300) of claim 15, wherein the driven circuit (320) further includes

- a bias potential source (B) that is configured to bias the gates of the third (Pr1) and fourth (Pr2) p-channel devices.

The level shifter circuit (300) of claim 15, wherein the driven circuit (320) further includes

- a weak current source (Iweak) having
  a first terminal that is connected to the fifth node, and
  a second terminal that is connected to the second voltage supply (G2)
of the second pair of voltage supply potentials (Vdd2, G2).
FIG. 1

[Prior Art]

FIG. 2

[Prior Art]