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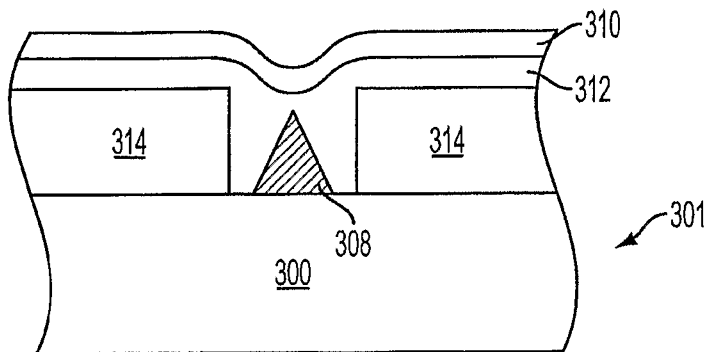
(54) **Title:** REPRODUCIBLE RESISTANCE VARIABLE INSULATING MEMORY DEVICES AND METHODS FOR FORMING SAME



(57) Abstract: The present invention relates to the use of a shaped bottom electrode in a resistance variable memory device (301) . The preferably cone-like shaped bottom electrode (308) ensures that the thickness of the insulating material (312) at the tip of the bottom electrode is thinnest, creating the largest electric field at the tip of the bottom electrode. The arrangement of electrodes (308, 310) and the structure of the memory element makes it possible to create conduction paths with stable, σonsistend and reproducible switching and memory properties in the memory device .

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REPRODUCIBLE RESISTANCE VARIABLE INSULATING MEMORY DEVICES AND METHODS FOR FORMING SAME

FIELD OF THE INVENTION

[0001] The invention relates to the field of random access memory (RAM) devices formed using a resistance variable material, and in particular to an improved structure for, and a method of manufacturing, a resistance variable memory element.

BACKGROUND OF THE INVENTION

[0002] Resistance variable memory is a RAM that has electrical resistance characteristics that can be changed by external influences. The basic component of a resistance variable memory cell is a variable resistor. The variable resistor can be programmed to have high resistance or low resistance (in two-state memory circuits), or any intermediate resistance value (in multi-state memory circuits). The different resistance values of the resistance variable memory cell represent the information stored in the resistance variable memory circuit. The advantages of resistance variable memory are the simplicity of the circuit, leading to smaller devices, the non-volatile characteristic of the memory cell, and the stability of the memory states.

[0003] FIG. 1 shows a cross-section of a conventional resistance variable memory device. This resistance variable memory device is a Type GRAD (one resistor, one diode) memory device. It includes a word line (N type region) 102 in substrate 100, a plurality of P+ regions 104 and N+ regions 106, wherein word line 102 and P+ region 104 constitute a diode. A dielectric layer 114 is formed over substrate 100. A plurality of memory units 107 are set in dielectric layer 114, wherein each memory unit 107 includes a flat plate bottom electrode 108, a flat plate

top electrode 110, and a resistive film 112, which may be formed of one or more layers, between the flat plate bottom electrode 108 and the flat plate top electrode 110. Word line contact via 116 is formed in dielectric layer 114. One end of word line contact via 116 is electrically connected to N+ region 106; the other end is electrically connected to a conducting line 120 on the surface of dielectric layer 114 so that the word line 102 can electrically connect with external circuits. Furthermore, there is a bit line 118 formed on dielectric layer 114 for electrically connecting with top electrode 110 of the memory unit 107.

[0004] A second example of a conventional resistance variable memory device is a Type 1R1T (one resistor one transistor) memory device illustrated in FIG. 2. This device includes a plurality of N+ regions 202 and 204 in substrate 200. A dielectric layer 220 is formed over substrate 200. Dielectric layer 220 includes a plurality of memory units 207, a plurality of gate structures (word lines) 212 and a plurality of contact vias 214 and 216. Each memory unit includes a flat plate bottom electrode 206, a flat plate top electrode 208 and a resistive film 210; which may be formed of one or more material layers, each memory unit is set on the surface of a respective N+ region. Gate structure 212 and N+ regions 202 and 204 constitute a transistor. Contact vias 214 and 216 are electrically connected to the gate structure 212 and the common line 204, respectively, so that the gate structure 212 and the common line 204 can connect with the external circuits. Furthermore, there is a bit line 218 formed on dielectric layer 220 for electrically connecting with the flat plate top electrode 208 of the memory unit 207.

[0005] Unfortunately, the metal-insulator-metal (MIM) structure with a resistive film or insulting oxide sandwiched between two flat metallic electrode plates as disclosed in FIGS. 1 and 2 does not provide stable and reproducible switching and does not provide memory properties in a controlled manner, as the

conduction path between the elements can occur anywhere in the resistive film or insulating oxide between the top and bottom electrodes. The random and unpredictable conduction path between the elements is believed to be created by random and unpredictable defect sites in the deposited film.

[0006] There is needed, therefore, an alternative apparatus for improving and controlling the conduction path between the electrodes in a resistance variable memory device to form large arrays of memory devices based on the resistance switching phenomenon.

BRIEF SUMMARY OF THE INVENTION

[0007] The present invention relates to the use of a shaped bottom electrode in a resistance variable memory device. The shaped bottom electrode ensures that the thickness of the insulating material at the tip of the bottom electrode is thinnest, therefore creating the largest electric field at the tip of the bottom electrode. The small curvature of the electrode tip also enhances the local electric field. The arrangement of electrodes and the structure of the memory element makes it possible to create conduction paths with stable, consistent and reproducible switching and memory properties in the memory device.

[0008] Additional advantages and features of the present invention will be apparent from the following detailed description and drawings which illustrate preferred embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1 shows a cross-section of a conventional resistance random access memory device.

[0010] FIG. 2 shows a cross-section of another conventional resistance random access memory device.

[0011] FIG. 3 illustrates a partial cross-section of a memory device in accordance with an exemplary embodiment of the present invention.

[0012] FIG. 4 illustrates a partial cross-section of a memory device in accordance with an second exemplary embodiment of the present invention.

[0013] FIG. 5 illustrates a partial cross-section of a memory device in accordance with a third exemplary embodiment of the present invention.

[0014] FIG. 6 illustrates a cross-sectional view of a semiconductor wafer undergoing the process of forming a memory device according to an exemplary embodiment of the present invention.

[0015] FIG. 7 illustrates the semiconductor of FIG. 6 at a stage of processing subsequent to that shown in FIG. 6.

[0016] FIG. 8 illustrates the semiconductor of FIG. 6 at a stage of processing subsequent to that shown in FIG. 7.

[0017] FIG. 9 illustrates the semiconductor wafer of FIG. 6 at a stage of processing subsequent to that shown in FIG. 8.

[0018] FIG. 10 illustrates the semiconductor wafer of FIG. 6 at a stage of processing subsequent to that shown in FIG. 9.

[0019] FIG. 11 illustrates the semiconductor wafer of FIG. 6 at a stage of processing subsequent to that shown in FIG. 10.

[0020] FIG. 12 illustrates a cross-sectional view of a semiconductor wafer undergoing a second process for forming a memory device according to an exemplary embodiment of the present invention.

[0021] FIG. 13 illustrates the semiconductor of FIG. 12 at a stage of processing subsequent to that shown in FIG. 12.

[0022] FIG. 14 illustrates a cross-sectional view of a semiconductor wafer undergoing the process of forming a memory device according to an exemplary embodiment of a second embodiment of the present invention.

[0023] FIG. 15 illustrates the semiconductor of FIG. 14 at a stage of processing subsequent to that shown in FIG. 14.

[0024] FIG. 16 illustrates the semiconductor of FIG. 14 at a stage of processing subsequent to that shown in FIG. 15.

[0025] FIG. 17 illustrates a processor-based system having a memory element formed according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0026] In the following detailed description, reference is made to the accompanying drawings, which form a part hereof and show by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and that structural, logical, and electrical changes may be made without departing from the spirit and scope of the present invention. The progression of processing steps described is exemplary of embodiments of the invention; however, the sequence of

steps is not limited to that set forth herein and may be changed as is known in the art, with the exception of steps necessarily occurring in a certain order.

[0027] The term "substrate" used in the following description may include any supporting structure including, but not limited to, a plastic, ceramic, semiconductor, or other substrate that has an exposed substrate surface. A semiconductor substrate should be understood to include silicon, silicon-on-insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor material structures. When reference is made to a semiconductor substrate or wafer in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation.

[0028] The invention will now be explained with reference to the figures, which illustrate exemplary embodiments and where like reference numbers indicate like features.

[0029] A memory device 301 according to an embodiment of the invention is schematically illustrated in FIG. 3. The device 301 includes a shaped bottom electrode 308, a top electrode 310, a dielectric layer 314, and a resistance variable insulating material 312 between the shaped bottom electrode 308 and the top electrode 310. In a preferred embodiment of the invention, the resistance variable insulating material 312 is formed from resistance-reversible materials such as colossal magnet resistive thin films, such as, for example a PCMO thin film (*i.e.*, $Pr_{0.7}Cr_{0.3}MoO_3$); oxidation films having Perovskite structure, such as, for example, doped or undoped $BaTiO_3$, $SrTiO_3$ or $SrZrO_3$; or an oxidation film such as, for example, Nb_2O_5, TiO_2, TaO_5, and NiO. Preferably the resistance variable insulating material 312 is $SrTiO_3$. The shaped bottom electrode 308 and the top electrode 310

may be formed from a metal such as, for example, platinum, titanium or gold, or other suitable materials such as, for example, $SrRuO_3$.

[0030] Reference is now made to FIG. 4. FIG. 4 is similar to FIG. 3 and illustrates a memory device 303 where the resistance variable insulating material 312 has been planarized before the top electrode 310 has been formed over the substrate 300.

[0031] Reference is now made to FIG. 5. FIG. 5 is similar to FIGS. 3 and 4 and illustrates a memory device 304 according to a third embodiment of the present invention where the bottom electrode 308 is formed over a conductive plug 322. As discussed above with FIG. 3, resistance variable insulating material 312 has been planarized before the top electrode 310 has been formed over the substrate 300. It should be understood that the resistance variable insulating material 312 may simply deposited and then have the top electrode 310 formed over the resistance variable insulating material 312, as discussed above with reference to FIG. 3.

[0032] FIGS. 6-11 depict the formation of the memory device 301 according to an exemplary embodiment of the invention. No particular order is required for any of the actions described herein, except for those logically requiring the results of prior actions. Accordingly, while the actions below are described as being performed in a general order, the order is exemplary only and can be altered if desired.

[0033] FIG. 6 illustrates a dielectric layer 314 formed over the substrate 300. The dielectric layer 314 may be formed by any known deposition methods, such as sputtering by chemical vapor deposition (CVD), plasma enhanced CVD (PECVD) or physical vapor deposition (PVD). The dielectric layer 314 may be

formed of a conventional insulating oxide, such as silicon oxide (SiO_2), a silicon nitride (Si_3N_4); a low dielectric constant material; among others.

[0034] A mask 316 is formed over the dielectric layer 314. In the illustrated embodiment, the mask 316 is a photoresist mask; the mask 316, however, could instead be any other suitable material such as, for example, a metal. An opening 313 extending to the substrate 300 is formed in the dielectric layer 314 and mask 316. The opening 313 may be formed by known methods in the art, for example, by a conventional patterning and etching process. Preferably, the opening 313 is formed by a dry etch via process to have substantially vertical sidewalls.

[0035] As shown in FIG. 7, a portion of the opening 313 is widened to form an opening 315 within the dielectric layer 314. The opening 315 extends under the mask 316, such that the opening 313 through the mask 316 is smaller than the opening 315 through the dielectric layer 314. Preferably, the opening 315 is formed using a wet etch process.

[0036] FIG. 8 depicts the formation of the shaped bottom electrode 308. A conductive material is deposited on the mask 316 and through the openings 313, 315 onto the substrate 300 to form a cone-like shaped bottom electrode 308 and a conductive layer 341 over the mask 316. The shaped bottom electrode 308 may comprise any conductive material, for example, platinum, titanium or gold, or other suitable materials such as, for example, $SrRuO_3$. The conductive material is deposited by a physical vapor deposition (PVD) process, such as evaporation or collimated sputtering, but any suitable technique may be used. As indicated by arrow 351, the substrate 300 is rotated during deposition of the conductive material. Additionally, as indicated by arrows 350, the conductive material is deposited in a single direction. Preferably, as shown in FIG. 8 by the angle of the arrows 350, the conductive material is deposited at an angle less than approximately 75 degrees

with respect to the top surface of the substrate 300, but the conductive material can also deposited at an angle of approximately 75 degrees if desired.

[0037] By forming the shaped bottom electrode 308 using a PVD process, the seams or gaps that occur when an electrode is formed in the conventional chemical vapor deposition (CVD) plug process can be avoided. Additionally, PVD deposited material tends to have a smoother surface than CVD deposited material. Accordingly the shaped bottom electrode 308 may have a smoother surface than conventional electrodes.

[0038] The conductive layer 341 and the mask 316 are removed, as illustrated in FIG. 9. This can be accomplished by any suitable technique. For example, a chemical mechanical polish (CMP) step can be conducted or a solvent lift-off process may be used according to known techniques.

[0039] Referring to FIG. 10, a resistance variable insulating material layer 312 is formed within the opening 315 and surrounding the shaped bottom electrode 308. The resistance variable insulating material layer 312 is formed from resistance-reversible materials such as colossal magnet resistive thin films, such as, for example a PCMO thin film (*i.e.*, $Pr_{0.7}Cr_{0.3}MoO_3$); oxidation films having Perovskite structure, such as, for example, doped or undoped $BaTiO_3$, $SrTiO_3$ or $SrZrO_3$; or an oxidation film such as, for example, Nb_2O_5, TiO_2, TaO_5, and NiO. Preferably the resistance variable insulating material 312 is $SrTiO_3$. The resistance variable insulating material 312 is formed by known methods, such as, for example, pulsed laser deposition (PLD), PVD, sputtering, or CVD.

[0040] Referring to FIG. 11, a second electrode 310 is formed over the resistance variable insulating material layer 312. The second electrode 310 may

comprise any electrically conductive material, for example, platinum, titanium or gold, or other suitable materials such as, for example, $SrRuO_3$.

[0041] Conventional processing steps can then be carried out to electrically couple the memory device 301 to various circuits of a memory array.

[0042] FIGS. 12-13 illustrate another exemplary embodiment for forming the memory element 301 according to the invention. The embodiment illustrated in FIGS. 12-13 is similar to that described in FIGS. 6-11, except that the second opening 315 (FIG. 7) need not be formed.

[0043] As shown in FIG. 12, a mask 316, which may be a photoresist mask, is applied over dielectric layer 314 and substrate 300. An opening 313 extending to the substrate 300 is formed in the dielectric layer 314 and mask 316.

[0044] The shaped bottom electrode 308 can be formed as described above in connection with FIG. 8. A conductive material is deposited over the mask 316 and through the opening 313 onto the substrate 300 to form the shaped bottom electrode 308 and a conductive layer 341 over the mask 316 as illustrated in FIG. 13. As indicated by arrow 351, the substrate 300 is rotated during deposition of the conductive material. Additionally, as indicated by arrows 350, the conductive material is deposited in a single direction. Preferably, as shown in FIG. 13 by the angle of arrows 50, the conductive material is deposited at an angle less than approximately 75 degrees with respect to the top surface of the substrate 300, but the conductive material can also deposited at an angle less of approximately 75 degrees.

[0045] The memory device 301 is then processed as discussed above with reference to FIGS. 9-11. Conventional processing steps can then be carried out to electrically couple the memory device 301 to various circuits of a memory array.

[0046] FIGS. 14-16 depict the formation of the memory device 303 according to a second exemplary embodiment of the invention. FIG. 14 illustrates memory device which is processed as set forth above with reference to FIGS. 6-10 or 12-13.

[0047] A CMP step is conducted to planarize the resistance variable insulating material layer 312 to achieve the structure shown in FIG. 15. A second electrode 310 is formed over the resistance variable insulating material layer 312 as illustrated in FIG. 16. As set forth above, the second electrode 310 may comprise any electrically conductive material, for example, platinum, titanium or gold, or other suitable materials such as, for example, $SrRuO_3$. Conventional processing steps can then be carried out to electrically couple the memory device 301 to various circuits of a memory array.

[0048] The embodiments described above refer to the formation of only a few possible resistance variable memory element structures (e.g., resistance variable memory devices) in accordance with the invention, which may be part of a memory array. It must be understood, however, that the invention contemplates the formation of other memory structures within the spirit of the invention, which can be fabricated as a memory array and operated with memory element access circuits.

[0049] FIG. 17 illustrates a processor system 700 which includes a memory circuit 748, e.g., a memory device, which employs resistance variable memory elements (e.g., elements 301 and/or 303 (FIGS. 3 and 4, respectively)) according to the invention. The processor system 700, which can be, for example, a computer system, generally comprises a central processing unit (CPU) 744, such as a microprocessor, a digital signal processor, or other programmable digital logic devices, which communicates with an input/output (I/O) device 746 over a bus 752.

The memory circuit 748 communicates with the CPU 744 over bus 752 typically through a memory controller.

[0050] In the case of a computer system, the processor system 700 may include peripheral devices such as a floppy disk drive 754 and a compact disc (CD) ROM drive 756, which also communicate with CPU 744 over the bus 752. Memory circuit 748 is preferably constructed as an integrated circuit, which includes one or more resistance variable memory elements, e.g., elements 200 and/or 600. If desired, the memory circuit 748 may be combined with the processor, for example CPU 744, in a single integrated circuit.

[0051] While the invention has been described in detail in connection with exemplary embodiments known at the time, it should be readily understood that the invention is not limited to such disclosed embodiments. Rather, the invention can be modified to incorporate any number of variations, alterations, substitutions or equivalent arrangements not heretofore described, but which are commensurate with the spirit and scope of the invention. Accordingly, the invention is not to be seen as limited by the foregoing description, but is only limited by the scope of the appended claims.

CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A memory element comprising:

a substrate;

a first electrode formed over said substrate, a first end of the first electrode being larger than a second end of the first electrode;

a second electrode; and

a resistance variable insulating layer between said first and second electrodes.

2. The memory element according to claim 1, wherein said resistance variable insulating layer is an oxide layer.

3. The memory element according to claim 1, wherein said first electrode has a cone-like shape.

4. The memory element according to claim 1, wherein said first electrode is selected from the group consisting of platinum, titanium, gold, and $SrRuO_3$.

5. The memory element according to claim 3, wherein said first electrode is $SrRuO_3$.

6. The memory element according to claim 1, wherein said second electrode is selected from the group consisting of platinum, titanium gold, and $SrRuO_3$.

7. The memory element according to claim 1, wherein said resistance variable insulating layer is selected from the group consisting of PCMO thin films, Perovskite structures and oxidation films.

8. The memory element according to claim 6, wherein said resistance variable insulating layer is selected from the group consisting of $Pr_{0.7}Cr_{0.3}MoO_3$, Nb_2O_5, TiO_2, TaO_5, and NiO.

9. The memory element according to claim 1, wherein said resistance variable insulating layer is doped or undoped $BaTiO_3$, $SrTiO_3$ or $SrZrO_3$.

10. The memory element according to claim 1, wherein said memory element is a resistance variable memory device.

11. The memory element according to claim 1, wherein the resistance variable insulating layer between said first and second electrodes is planarized before the second electrode is formed.

12. The memory element according to claim 1, wherein the second electrode is formed over the as deposited resistance variable insulating layer.

13. The memory element according to claim 1, further comprising a conductive plug formed between said substrate and said first electrode.

14. A memory element comprising:

a substrate;

a dielectric layer formed over said substrate, said dielectric layer having an opening formed therein from an upper surface of said dielectric layer to said substrate;

a first electrode formed over said substrate and in said hole in said dielectric layer, said first electrode having a cone-like structure;

a resistance variable insulating layer formed over said first electrode in said opening in said dielectric layer; and

a second electrode formed over said resistance variable insulating layer.

15. The memory element according to claim 14, wherein said first electrode is selected from the group consisting of platinum, titanium, gold, and $SrRuO_3$.

16. The memory element according to claim 15, wherein said first electrode is $SrRuO_3$.

17. The memory element according to claim 15, wherein said second electrode is selected from the group consisting of platinum, titanium gold, and $SrRuO_3$.

18. The memory element according to claim 15, wherein said resistance variable insulating layer is selected from the group consisting of PCMO thin films, Perovskite structures and oxidation films.

19. The memory element according to claim 15, wherein said resistance variable insulating layer is doped or undoped $BaTiO_3$, $SrTiO_3$ or $SrZrO_3$.

20. The memory element according to claim 15, wherein said resistance variable insulating layer is selected from the group consisting of $Pr_{0.7}Cr_{0.3}MoO_3$, Nb_2O_5, TiO_2, TaO_5, and NiO.

21. The memory element according to claim 15, wherein said resistance variable insulating layer is formed over said dielectric layer.

22. The memory element according to claim 14, wherein the resistance variable insulating layer between said first and second electrodes is planarized before the second electrode is formed.

23. The memory element according to claim 14, wherein the second electrode is formed over the as deposited resistance variable insulating layer.

24. The memory element according to claim 14, wherein said memory element is a resistance variable memory element.

25. The memory element according to claim 14, further comprising a conductive plug formed between said substrate and said first electrode.

26. A processor system, comprising:

a processor; and

a substrate;

a first electrode formed over said substrate, a first end of the first electrode being larger than a second end of the first electrode;

a second electrode; and

a resistance variable insulating layer between said first and second electrodes.

27. The processor system according to claim 26, wherein said first electrode has a cone-like shape.

28. The processor system according to claim 26, wherein said first electrode is selected from the group consisting of platinum, titanium, gold, and $SrRuO_3$.

29. The processor system according to claim 28, wherein said first electrode is $SrRuO_3$.

30. The processor system according to claim 26, wherein said second electrode is selected from the group consisting of platinum, titanium gold, and $SrRuO_3$.

31. The processor system according to claim 26, wherein said resistance variable insulating layer is doped or undoped $BaTiO_3$, $SrTiO_3$ or $SrZrO_3$.

32. The processor system according to claim 26, wherein said resistance variable insulating layer is selected from the group consisting of $Pr_{0.7}Cr_{0.3}MoO_3$, Nb_2O_5, TiO_2, TaO_5, and NiO.

33. The processor system according to claim 26, wherein said memory element is a resistance variable memory element.

34. A method of forming a memory element, the method comprising:

forming a first electrode such that a first end of the first electrode is larger than a second end of the first electrode;

forming a resistance variable insulating layer over said first electrode; and

forming a second electrode, wherein said resistance variable insulating layer is formed between said first and second electrodes.

35. The method according to claim 34, wherein forming the first electrode comprises forming the first electrode having a cone-like shape.

36. The method according to claim 34, wherein forming the first electrode comprises depositing a conductive material and rotating the substrate while depositing the conductive material an angle less than 75 degrees with respect to the top surface of the substrate.

37. The method according to claim 36, wherein the conductive material is deposited in a single direction, such that the conductive material forms a cone-like structure on the substrate.

38. The method according to claim 34, wherein said first electrode is formed from a material selected from the group consisting of platinum, titanium, gold, and $SrRuO_3$.

39. The method according to claim 34, wherein said resistance variable insulating layer is formed from doped or undoped $BaTiO_3$, $SrTiO_3$ or $SrZrO_3$.

40. The method according to claim 34, wherein said resistance variable insulating layer is selected from the group consisting of $Pr_{0.7}Cr_{0.3}MoO_3$, Nb_2O_5, TiO_2, TaO_5, and NiO.

41. The method according to claim 39, wherein said resistance variable insulating layer is formed by pulsed laser deposition, physical vapor deposition, sputtering, or chemical vapor deposition.

42. The method of claim 34, further comprising:

forming a first material layer over a substrate;

forming a second material layer over the substrate;

forming a first opening within the first and second material layers, wherein forming the first electrode comprises depositing a conductive material through the first opening, and rotating the substrate while depositing the conductive material, the conductive material being deposited in a single direction, such that the conductive material forms a cone-like structure on the substrate, wherein the conductive material is deposited at an angle less than 75 degrees with respect to the top surface of the substrate.

43. A method of forming a memory element, the method comprising:

forming a dielectric layer over a substrate;

forming an opening within said dielectric layer;

depositing a conductive material in said opening by rotating the substrate while depositing the conductive material, the conductive material being deposited in

a single angled direction, such that the conductive material forms a cone-like structure on the substrate, the cone-like structure being a first electrode;

forming a resistance variable insulating layer in the opening; and

forming a second electrode over the resistance variable insulating layer.

44. The method according to claim 43, wherein the conductive material is deposited at an angle less than 75 degrees with respect to the top surface of the substrate.

45. The method according to claim 43, wherein said first electrode is formed from a material selected from the group consisting of platinum, titanium, gold, and $SrRuO_3$.

46. The method according to claim 43, wherein said resistance variable insulating layer is formed from doped or undoped $BaTiO_3$, $SrTiO_3$ or $SrZrO_3$.

47. The method according to claim 46, wherein said resistance variable insulating layer is formed by pulsed laser deposition, physical vapor deposition, sputtering, or chemical vapor deposition.

48. The method according to claim 43, wherein said resistance variable insulating layer is selected from the group consisting of $Pr_{0.7}Cr_{0.3}MoO_3$, Nb_2O_5, TiO_2, TaO_5, and NiO.

49. The method according to claim 43, further comprising planarizing said resistance variable insulating layer prior to forming said second electrode.

50. A method of forming a memory element, the method comprising:

forming a dielectric layer over a substrate;

forming a first opening within said dielectric layer;

widening a portion of said first opening within said dielectric layer to form a second opening;

depositing a conductive material through the first and second openings;

rotating the substrate while depositing the conductive material, the conductive material being deposited in a single angled direction, such that the conductive material forms a cone-like structure on the substrate, the cone-like structure being a first electrode;

forming a resistance variable insulating layer in the first and second openings; and

forming a second electrode over resistance variable insulating layer.

51. The method according to claim 50, wherein the conductive material is deposited at an angle less than 75 degrees with respect to the top surface of the substrate.

52. The method according to claim 50, wherein said first electrode is formed from a material selected from the group consisting of platinum, titanium, gold, and $SrRuO_3$.

53. The method according to claim 50, wherein said resistance variable insulating layer is formed from doped or undoped $BaTiO_3$, $SrTiO_3$ or $SrZrO_3$.

54. The method according to claim 53, wherein said resistance variable insulating layer is formed by pulsed laser deposition, physical vapor deposition, sputtering, or chemical vapor deposition.

55. The method according to claim 50, wherein said resistance variable insulating layer is selected from the group consisting of $Pr_{0.7}Cr_{0.3}MoO_3$, Nb_2O_5, TiO_2, TaO_5, and NiO.

56. The method according to claim 50, further comprising planarizing said resistance variable insulating layer prior to forming said second electrode.

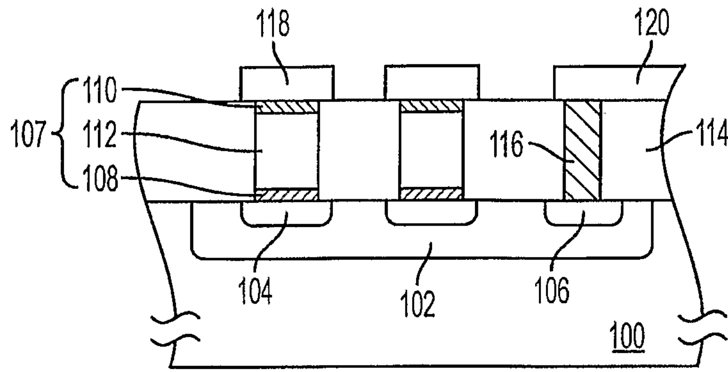

FIG. 1
PRIOR ART

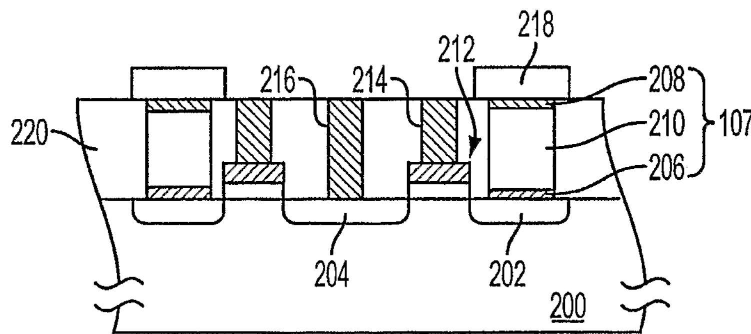

FIG. 2
PRIOR ART

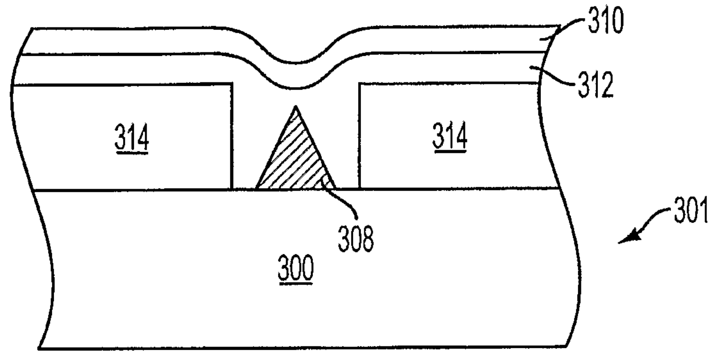

FIG. 3

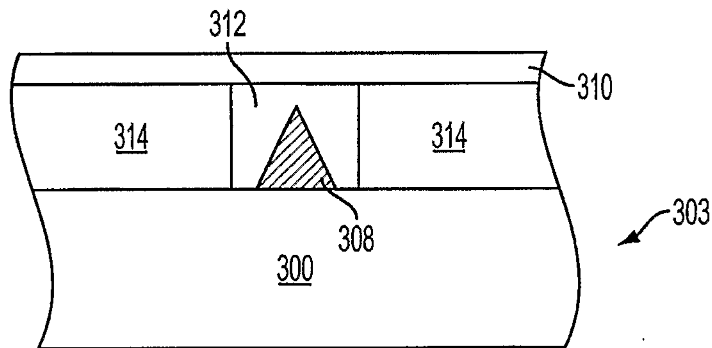

FIG. 4

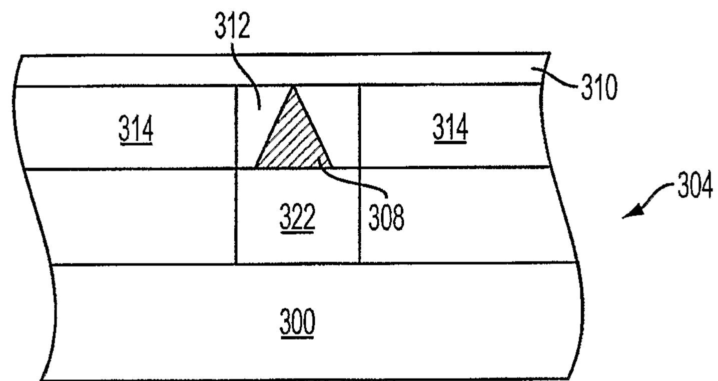

FIG. 5

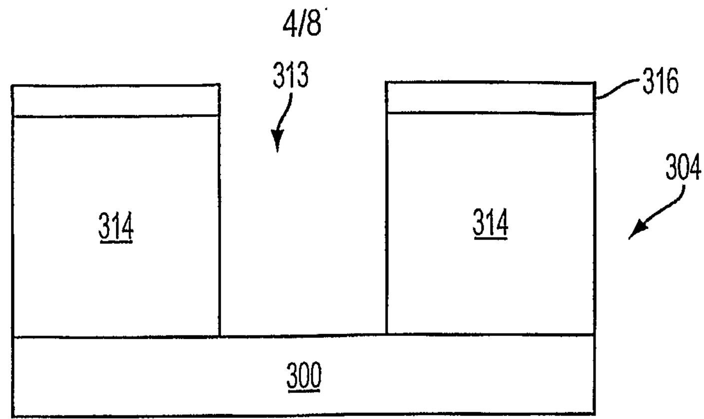

FIG. 6

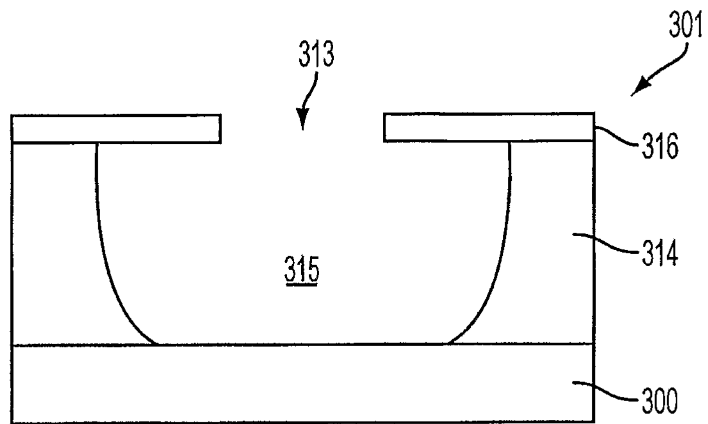

FIG. 7

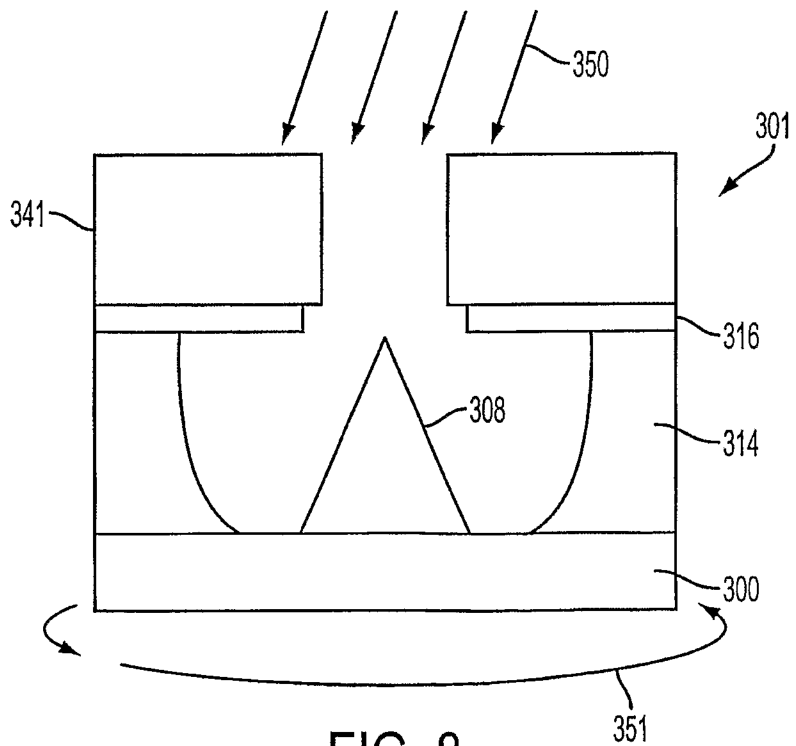

FIG. 8

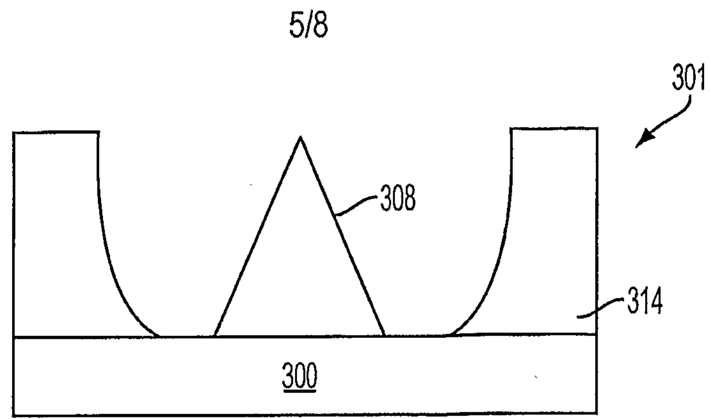

FIG. 9

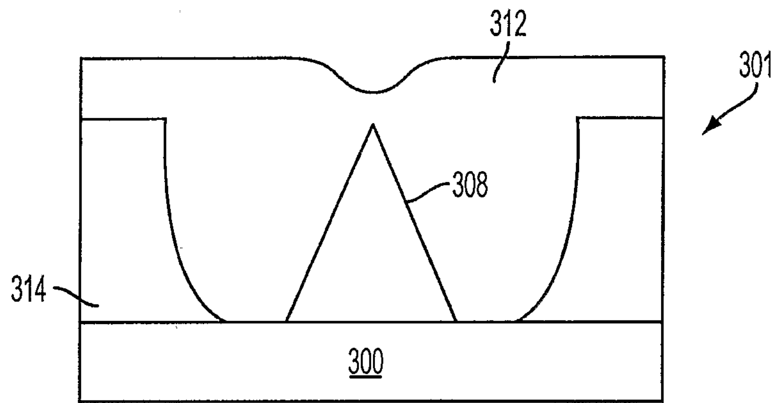

FIG. 10

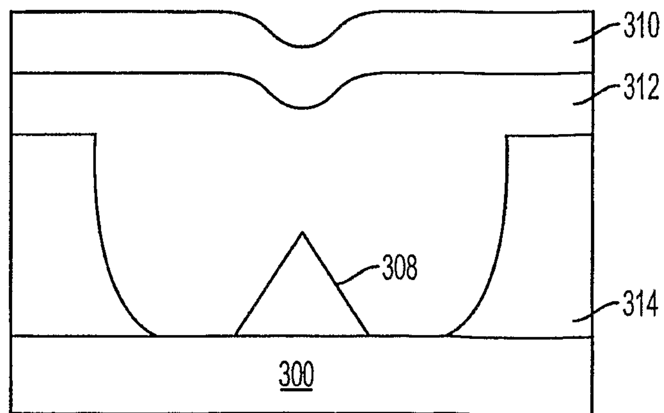

FIG. 11

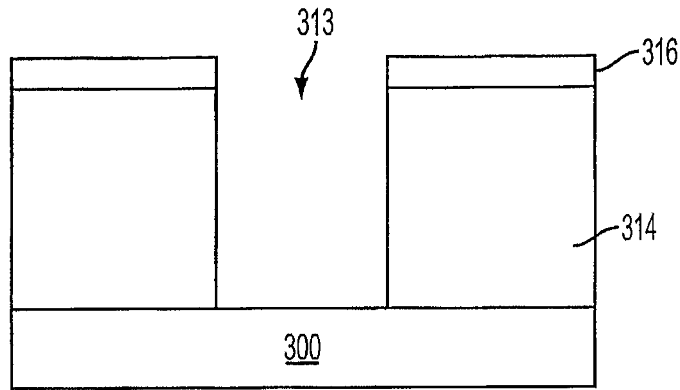

FIG. 12

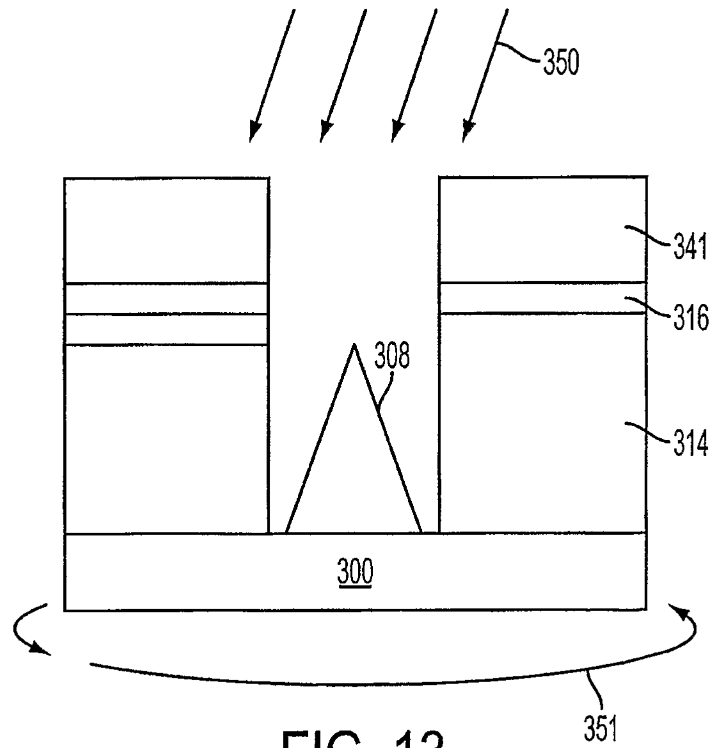

FIG. 13

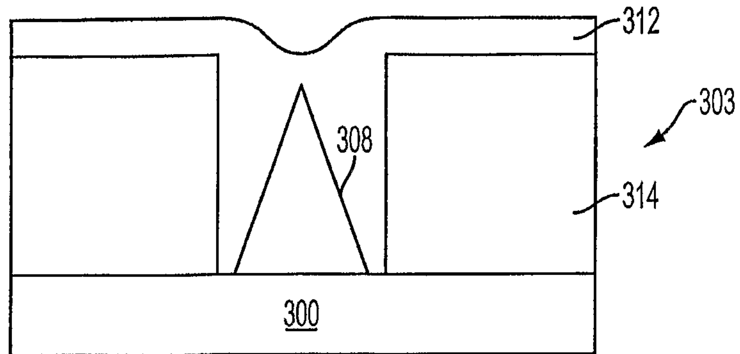

FIG. 14

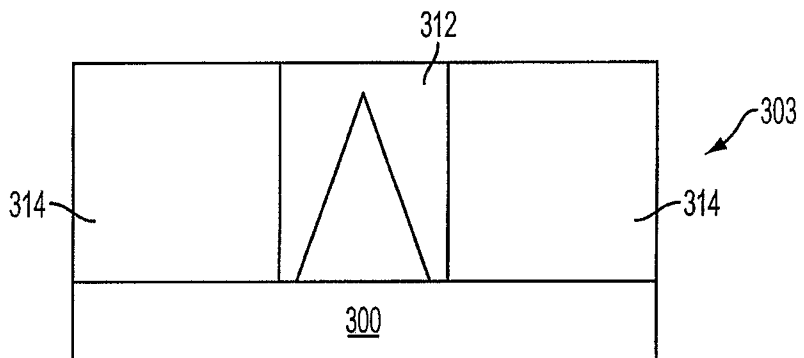

FIG. 15

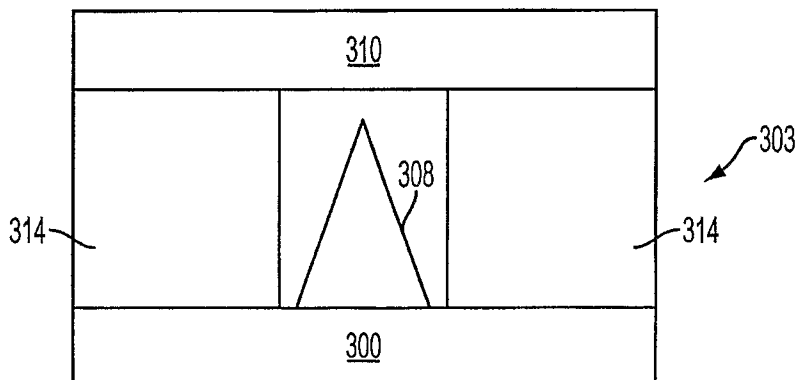

FIG. 16

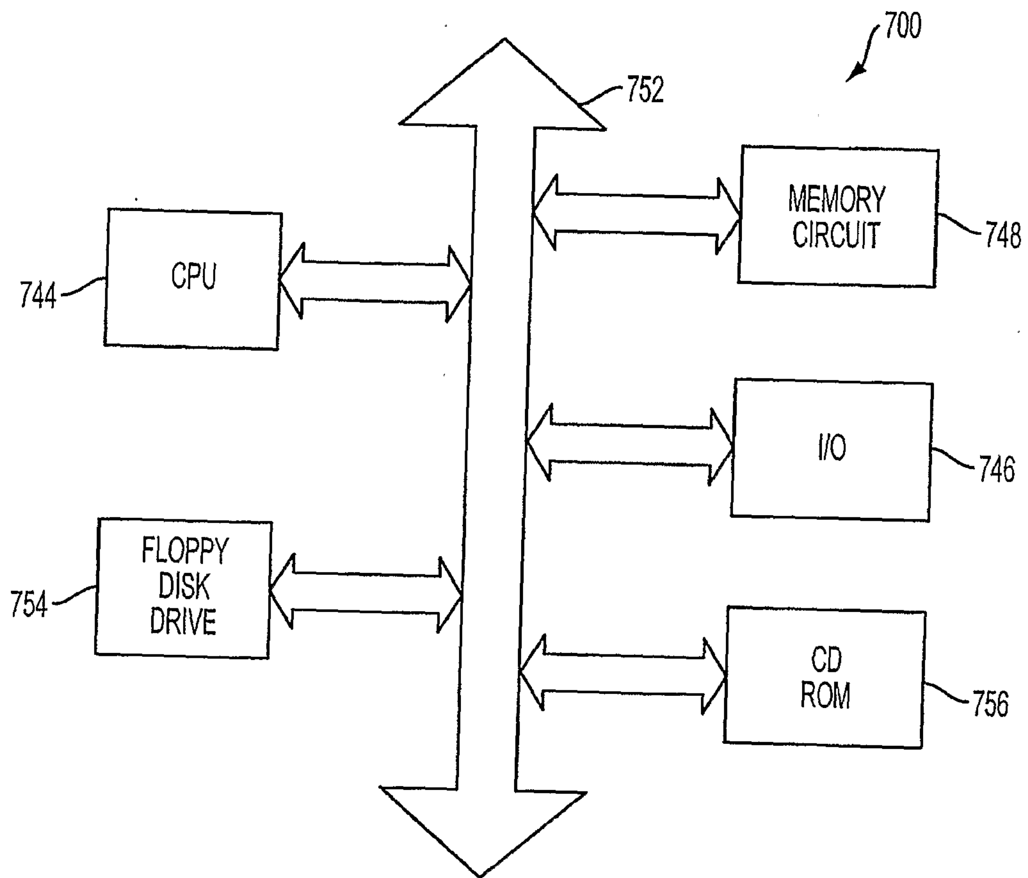

FIG. 17

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/031345

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L45/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/167699 A1 (SUGITA YASUNARI ET AL) 4 August 2005 (2005-08-04)	1,2,4-7, 10-12, 26, 28-30, 33,34,38
Y		3,8,9, 13-18, 21-24, 27,31, 32,35, 39-41
A	paragraphs [0026] - [0034]; figure 1 paragraphs [0078] - [0087]; figures 9,10 -----	43,45,47

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 January 2007	22/01/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Köpf, Christian

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/031345

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	WO 2004/017436 A2 (INFINEON TECHNOLOGIES AG; IMEC VZW; BREUIL LAURENT ET AL) 26 February 2004 (2004-02-26) page 8, last paragraph - page 10, paragraph 2; figure 3A page 13 - page 15, paragraph 4; figure 5 -----	3,14-18, 21-24, 27,35 36,37, 42,43,50
Y	US 2004/160804 A1 (RINERSON DARRELL ET AL) 19 August 2004 (2004-08-19) paragraphs [0030] - [0032]; figure 1A paragraphs [0069] - [0075]; figures 6-9 -----	8,9,13, 31,32, 39-41
Y	BECK A ET AL: "Reproducible switching effect in thin oxide films for memory applications" APPLIED PHYSICS LETTERS, vol. 77, no. 1, 3 July 2000 (2000-07-03), pages 139-141, XP000958527 ISSN: 0003-6951 page 139 -----	8,9,31, 32,39-41
P,X	US 2006/006471 A1 (ROSSEL CHRISTOPHE P ET AL) 12 January 2006 (2006-01-12) paragraphs [0072] - [0079]; figure 1 paragraphs [0089] - [0092]; figure 2 paragraphs [0103], [0104]; figure 5 paragraphs [0123] - [0125]; figures 9-14 -----	1-7,9, 10, 12-14, 23,24, 34,35, 38,39,41
P,X	US 2006/027893 A1 (MEIJER GERHARD I ET AL) 9 February 2006 (2006-02-09) paragraphs [0027] - [0029]; figure 1 paragraphs [0039] - [0045]; figures 2-9 -----	1-3, 7-14, 22-25, 34,35, 39-41
P,X	US 2006/160304 A1 (HSU SHENG T ET AL) 20 July 2006 (2006-07-20) paragraphs [0030] - [0037]; figures 1,2 paragraphs [0039] - [0043]; figures 6,7 ----- -/--	1-3,6,7, 10,11, 14,17, 18,22, 24,34,35

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/031345

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	US 2005/180189 A1 (HAPP THOMAS ET AL) 18 August 2005 (2005-08-18) paragraphs [0036] - [0042], [0049]; figure 2 paragraphs [0057] - [0068]; figures 3-6 -----	1-3,7, 10-12, 34,35

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2006/031345

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