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[54] DIGITAL DRYER CONTROL CIRCUIT

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[52] **U.S. Cl.** **34/33,** 34/45, 34/48

[51] **Int. Cl.**.....**F26b 3/00**

[58] **Field of Search**.....34/23, 31, 33, 45, 48

[56] **References Cited**

UNITED STATES PATENTS

3,471,938	10/1969	Elders	34/45
3,474,545	10/1969	Klinkmuller et al.	34/45

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[57] **ABSTRACT**

A fabric treating apparatus, such as a domestic clothes dryer, is provided with a digital control circuit and a sensor system which cooperate to terminate a fabric treatment operation when the fabric has reached a desired condition. A digital counter receives and accumulates pulses from a reference source and is repetitively reset by signals from a sensor circuit which provides reset pulses at a rate dependent upon the dryness condition of the fabric load. As the fabric load approaches the desired dryness condition the interval between reset pulses increases, thus allowing the counter to accumulate successively greater counts before being reset, until eventually a preselected count is accumulated which triggers circuitry to terminate the fabric drying operation. After termination of the drying operation the counter serves as a clock and operates in conjunction with an indexable digital memory and associated logic circuitry to control a program of subsequent fabric treatment operations.

11 Claims, 3 Drawing Figures

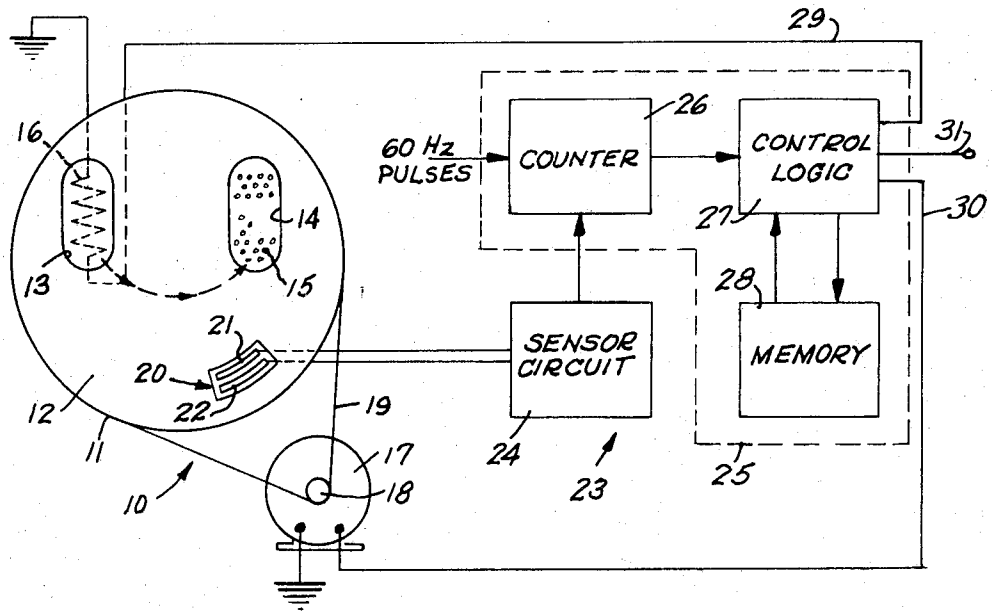


Fig. 1

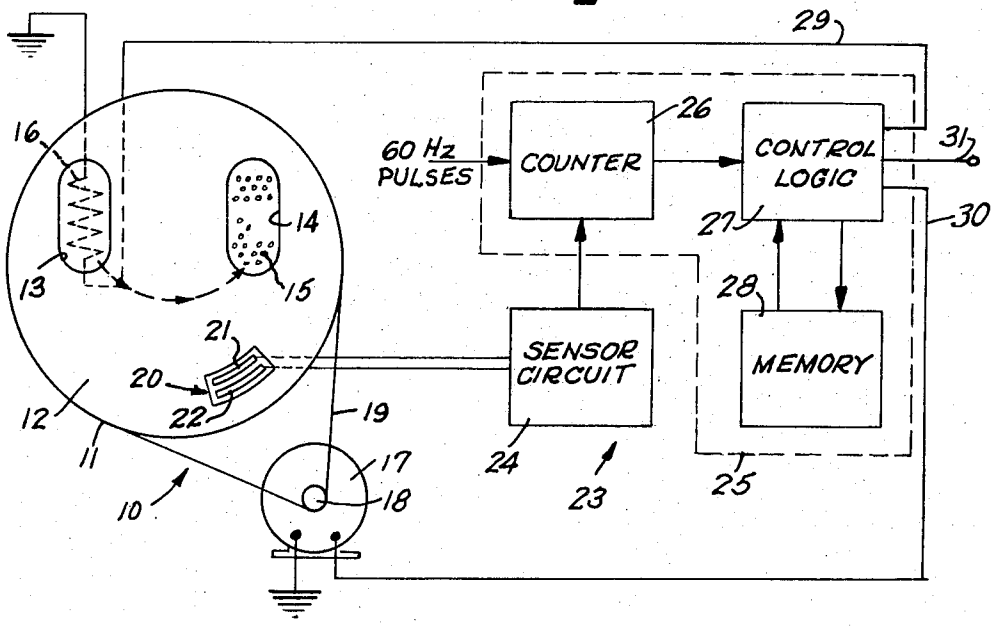
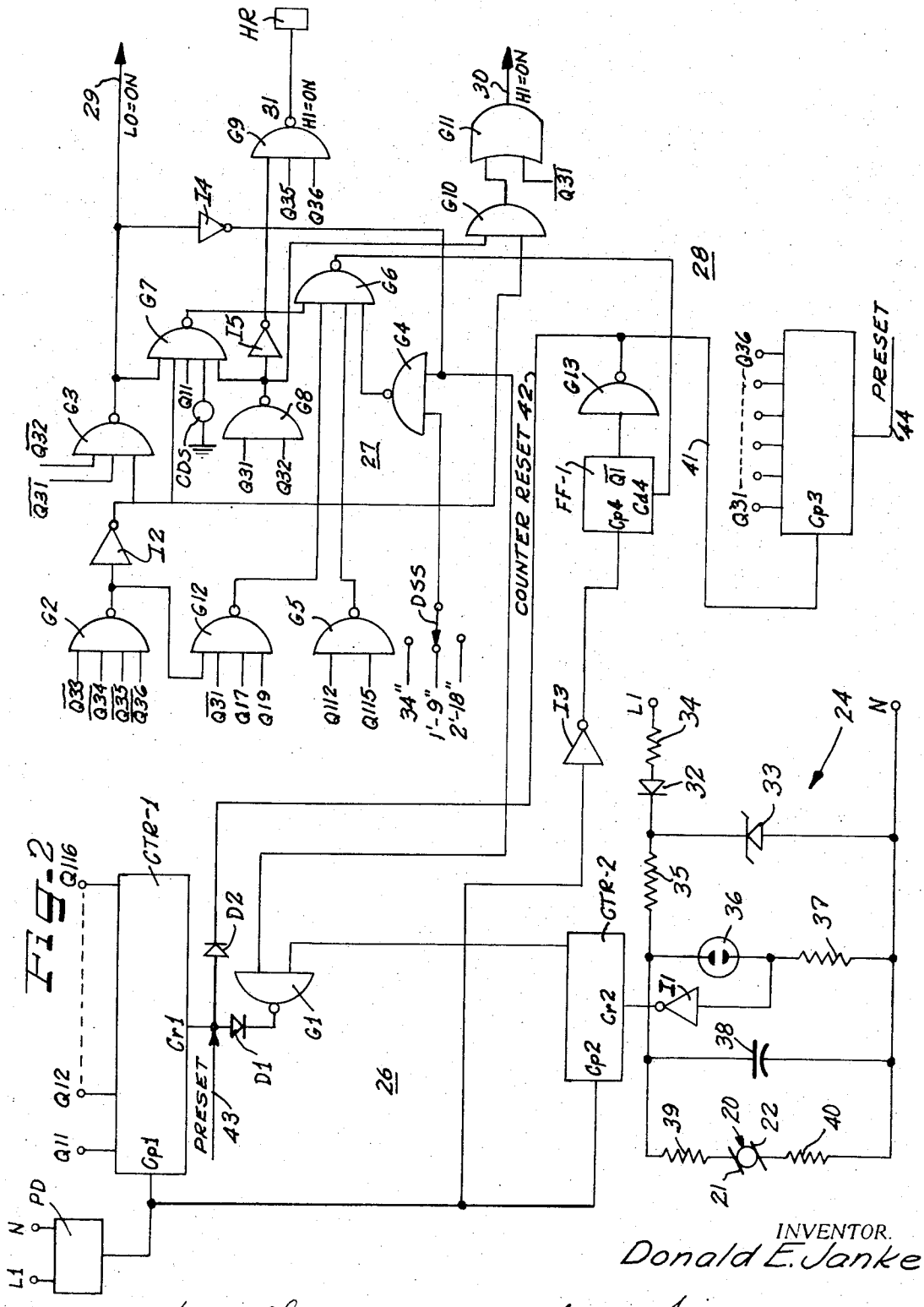


Fig. 3

STEP	MEMORY STATE						FUNCTION
	Q31	Q32	Q33	Q34	Q35	Q36	
0	0	0	0	0	0	0	DRY
1	1	0	0	0	0	0	TUMBLE - NO HEAT
2	0	1	0	0	0	0	TUMBLE - NO HEAT
3	1	1	0	0	0	0	PAUSE - 5 MIN.
4	0	0	1	0	0	0	TUMBLE - 5 SEC.
5	1	0	1	0	0	0	PAUSE - 5 MIN.
51	1	1	0	0	1	1	STOP

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DIGITAL DRYER CONTROL CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

this invention relates to control techniques for laundry apparatus, and is particularly concerned with methods and apparatus for controlling the operation of a clothes dryer on a digital basis.

2. Description of the Prior Art

Heretofore, a motor-driven timer having sequentially operated contacts has served as the basic control component of a clothes dryer. The timer allocates time intervals, or cycles, within a drying program to various functions of dryer operation, such as heating a flow of air and tumbling with or without the flow of air being heated. As new fabrics and laundry features and corresponding dryer functions were developed, and as demand for these features and various combinations of features increased, various techniques were employed to provide an increase in the capacity of the timer. In addition to adding timer contacts and modifying the sequence of contact operation, additional timers were connected in circuit with a main timer to provide as a cycle of the main timer a plurality of sub-cycles of an added timer as a secondary drying program within the main drying program. Also, other techniques have been utilized to produce timer stall and re-energization of the timer upon sensing of the occurrence of some condition of the laundry or its treatment zone. It is therefore readily apparent that a motor-driven timer circuit, in connection with auxiliary timing devices, may become complex as the demand for combinations of drying features increases, and inasmuch as the design of such timers and circuits becomes exceedingly difficult and as the space available to accommodate timers and their circuits is somewhat limited, it is clearly evident that the addition of more time intervals to accommodate new features may become technically and economically unjustified.

SUMMARY OF THE INVENTION

An object of the invention is to provide an appliance control circuit having a basic circuit concept which can be expanded as necessary or as desired to accommodate additional features within the fabric treating program.

Another object of the invention is to eliminate the need for the conventional electromechanical timing mechanism in a clothes dryer.

It is a further object of the invention to provide a dryer control circuit which exhibits improved repeatability for a given dryness setting by virtue of the precise nature of the digital control circuit and ciruitry included to eliminate erroneous sensor signals.

Still another object of the invention is to provide a dryer control circuit which, with the exception of a few components, may be fabricated as a single integrated circuit to advantageously provide compatible interfacing with sensor control elements which generally provide low level signals.

The invention comprises a control circuit and operating method for use with a fabric treating apparatus which effects at least one fabric treating operation and which includes means for sensing a parameter or variable quantity related to the condition of the fabric during the treatment operation. A digital control

circuit utilizes information received from the fabric sensing means to terminate a fabric treating operation when the fabric reaches a predetermined desired condition. Additional digital circuit means are provided for advancing the treating apparatus through a preselected program of subsequent fabric treating operations.

In its broad aspect, the invention may be applied to various types of fabric treating apparatus; however, a particularly advantageous application of the inventive concept is depicted by the preferred embodiment of the present application, wherein a domestic clothes dryer is operated and controlled in accordance with the principles of the invention.

In the preferred embodiment of the invention, a clothes dryer is provided with a moisture sensing circuit, a digital counter, a memory circuit, and control logic circuitry.

The memory comprises a chain of sold state flip-flop circuits which may be sequenced or indexed to provide the dryer program as a sequence of these unique binary states. The binary states of the memory are read by the control logic circuit which includes a plurality of gating circuits which are connected by means of appropriate interfacing circuitry to respective controlled components, such as the dryer motor and the dryer heater. In the particular embodiment illustrated herein, the gating circuits are provided primarily as NAND gates.

Inasmuch as the memory is to be indexed to provide the sequence of unique binary states, indexing means are provided which comprise, in part, a portion of the aforementioned control logic circuit which reads, in addition to memory state, the time position of a digital counter in a logical binary format.

The digital counter receives and accumulates a pulse count corresponding to pulses which may be derived from the conventional alternating voltage wave, hereinafter referred to as "line pulses." The digital counter comprises a chain of solid state flip-flop circuits which provide the pulse count accumulation in the binary format to be read by the control logic circuit.

The drying portion of the program during which a flow of heated air is supplied to the laundry treatment zone is ordinarily the initial portion of the drying program. Since the moisture content of laundry will vary from load to load, the drying portion of the program is provided an indefinite time interval and is terminated under the control of a moisture sensor which effects cyclic resetting of the digital counter and thereby prevents indexing of the memory from its first state until a desired degree of dryness is attained.

Inasmuch as the moisture content of a single load is usually nonuniform and as the clothes of a tumbling load provide random contact with moisture sensors and thereby effect random moisture indication signals ranging from infinite to almost zero ohms, means are provided to effect a slow response to occasional infinite signals to allow for tumbling and permit the sensor to search for damp fabrics within a load, and to respond to some preset resistance level. This means comprises a moisture sensing circuit including an oscillator for generating repetitive pulses in response to detection of a predetermined dryness level by an associated sensor. These pulses are applied to a reset input of a second digital counter which is, like the first-mentioned digital

counter, driven by the line pulses. The output of the second digital counter is employed to reset the first digital counter and the number of stages of the second counter and the repetition rate of the pulses from the sensor circuit are such that the first digital counter is repetitively reset by the second digital counter for moisture conditions above a predetermined level and permitted to cyclically accumulate line pulse count upon the sensing of the predetermined moisture level. By selectively adjusting the count which must be accumulated by the first counter to terminate the drying operation, the final moisture content of the clothes load can be selectively varied.

When the clothes load is dry, metallic objects occasionally fall across the sensor and briefly disable the oscillator thereby producing a momentary signal which is indicative of wet clothes. Also, static produced by the tumbling of a clothes load across the sensor can temporarily disable the oscillator. The second digital counter is employed specifically to prevent such false indications of a damp load from resetting the first digital counter. Inasmuch as the output pulses from the oscillator must disappear for a sufficient period to enable the second digital counter to accumulate several line pulses before a reset pulse will be produced to reset the first digital counter, the absence of an occasional pulse or two from the oscillator will not provide sufficient time for the second digital counter to generate a reset pulse. Therefore, after a correct sensing of the predetermined moisture content (dryness level) by the sensor, the first digital counter is permitted to cyclically accumulate the line pulse count and function as a system clock.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features and advantages of the invention, its organization, construction, and operation will be best understood by reference to the following detailed description of an exemplary embodiment thereof taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a schematic diagram of a dryer including a dryer control circuit according to the present invention;

FIG. 2 is a schematic logic circuit diagram of a control circuit constructed in accordance with the principles of the present invention; and

FIG. 3 is a truth table example of the unique binary states of the memory of FIGS. 1 and 2.

DESCRIPTION OF THE PREFERRED EMBODIMENT

In FIG. 1 a clothes dryer and its associated driving apparatus is generally referenced **10**. A drum **11** having a bulkhead **12** in which there is an inlet aperture **13** and an outlet aperture **14** through which air is circulated as indicated by the arrows. A screen or perforate plate **15** is positioned within each of these apertures (shown only for the aperture **13**) and a heating element **16** is disposed behind the aperture **13**. A fan (not shown) is connected in an air flow relationship with the apertures so that air is drawn into the drum by way of the aperture **13** after first passing the heating element **16** and is withdrawn from the drum through the aperture **14**. A drive motor **17**, which may also be employed to drive the fan, is connected in a driving relationship with drum **11** by way of a pulley **18** and a belt **19**.

A dryness sensor assembly **20** is fixed to the bulkhead **12** within the drum **11** and includes a pair of sensor elements **21** and **22** for connection to the dryer control circuit.

The digital control circuit is generally referenced **23** and includes a sensor circuit **24** connected to the electrodes **21** and **22** of the sensor, a digital counter circuit **26** which may be driven by 60 Hz pulses, a memory **28** and a control logic circuit **27** for reading the states of the counter **26** and the memory **28** for indexing the memory **28**.

The control logic circuit **27** includes a plurality of outputs for controlling various machine functions and, accordingly, for controlling the program of the dryer. A first output is indicated by the electrical connection **29** which extends from the control circuit **27** to the heating element **16** for controlling the application of heat to the interior of the drum **11**. A second output is indicated by means of an electrical connection **30** which extends from the control logic circuit to the drive motor **17** for controlling rotation of the drum **11** and the fan. Another output is evidenced by the electrical connection **31** which may be employed, for example, as a master power control lead for disconnecting the circuits from the electrical supply at the termination of the drying program. As will be appreciated by those skilled in the art, the electrical connections **29**, **30** and **31** are of schematic form only, and in practice appropriate interface circuitry such as is well known in the art will be necessary to enable the relatively low level signals developed by the logic circuitry to be used to control the power supplied to the machine components.

The sensor circuit **24** of the digital dryer control circuit may be of the type described in U. S. Pat. No. 3,471,938 issued to Alvin J. Elders on Oct. 14, 1969 and assigned to Whirlpool Corporation. This type of sensing circuit and the associated sensor assembly are well known and commonly employed in modern clothes dryers. In the present control, the sensor operates to supply pulses to the counter **26** whenever the moisture condition of the clothes in the drum **11** provides a resistance which is above some predetermined level.

The counter **26** is driven by and accumulates the pulse count of 60 cycle pulses derived from the conventional alternating voltage wave. When a predetermined number of such pulses is counted, an output signal is produced by a first section CTR–1 of the counter **26** which may be employed to terminate the drying portion of the program by means of the control logic circuit **27**. A second section CTR–2 of the counter circuit **26** operates in conjunction with the moisture sensing circuit **24** to supply reset pulses to the section CTR–1 of the counter **26** whenever a predetermined interval passes during which no pulses are received from the sensor circuit **24**. Therefore, as long as the clothes load is damp and its resistance is low, the first section CTR–1 of the counter **26** will be continually reset by the second section CTR–2 of the counter **26**, and the predetermined number of pulses necessary to initiate an output signal will not be accumulated. As the clothes load becomes dryer, the reset signals from the

second section of the counter **26** will be spaced by greater time intervals, and once the spacing becomes sufficiently long to permit the first section CTR–1 to accumulate the predetermined pulse count, a signal will be initiated which terminates the drying portion of the program. The control logic circuit **27** receives the signal from the section CTR–2 of the counter **26** which indicates termination of the drying portion of the program and communicates with the memory **28** to control the various operating elements of the dryer as indicated schematically in FIG. **1**. For example, the control logic circuit **27** controls the power supplied to the heating element **16**, the power supplied to the drive motor **17**, and provides, by way of the output conductor **31**, a master power supply control to remove power from the machine at the termination of the drying program.

The memory **28** is a digital circuit which can be sequentially advanced through a plurality of states and which provides a unique combination of binary signals for each of its memory states. The state of the memory **28** determines the condition of the outputs **29**, **30** and **31** from the control logic circuit **27** and therefore the energization and de-energization of the corresponding controlled elements. Referring to FIG. **3**, the memory **28** may be realized by a plurality of bistable circuits, six being here illustrated, and capable of advancing through a plurality of unique binary state to provide corresponding machine functions. In FIG. **3** the first six binary states are illustrated as steps 0–5 which correspond to a dry interval, two successive 5 minute cool down intervals, a 5 minute pause, a 5 second tumble interval and a 5 minute pause. The 51st memory state of 110011 corresponds to a stop order to the control logic circuit **27**. The steps 6–50 may be utilized to control any desired machine function and the memory itself may be increased stage by stage, as desired, to provide a greater number of unique binary states, as is well known in the art. It will be recognized by those skilled in the art that the cool-down intervals and tumbling intervals provide for wrinkle protection. It should also be clearly evident that additional steps may be utilized or interposed in this exemplary program. For example, an anti-static additive may be dispensed by assigning a memory state to this function and providing appropriate portions of the logic control circuit to control dispensing, or dispensing and tumbling.

After the sensor circuit **24** indicates that the clothes are dry and the section CTR–1 of the counter **26** has provided an output signal indicative of this condition, the section CTR–1 then functions in a different role and serves as a clock for the control logic circuit. The connection between the counter **26** and the control logic circuit **27** illustrated in FIG. **1** is actually a plurality of connections through which the counter communicates with the control logic circuit. The same is true for the connections between the control logic circuit **27** and the memory **28**. The control logic circuit **27** therefore operates to read or sense the time and state of the memory and to index the memory in accordance with a predetermined program on the basis of the logical inputs from the counter **26** and from the memory **28**.

Referring to FIG. **2**, the digital control circuit **23** of FIG. **1** is illustrated in greater detail. In this illustrative embodiment the sensor circuit **24** comprises a pair of input terminals L1 and N for connection to a conventional 60 Hz voltage supply. A diode **32**, a Zener diode **33**, and a resistor **34** are connected across the input terminals to supply approximately 100 volts DC across the diode **33**. Connected across the diode **33** is a resistor **35**, a neon lamp **36** and a resistor **37**. A capacitor **38** is connected across the neon lamp **36** and the resistor **37**. A resistor **39** and a resistor **40** are connected in series with the sensor assembly **20** and the series combination is connected in parallel with the capacitor **38**. For a detailed description of the operation of the sensor circuit, reference is invited to the aforementioned Elders U.S. Pat. No. 3,471,938; however, it is here sufficient to state that when the clothes load is wet, the sensor circuit produces only occasional, randomly spaced output pulses at the junction between the neon lamp **36** and the resistor **37**, and when the clothes reach a predetermined dryness, regular, periodic pulses are produced at this junction by the neon oscillator of the sensor system. The presence or absence of these pulses during an interval of time determines whether the section CTR–1 of the counter **26** is repetitively reset or permitted to count pulses during that interval.

The counter **26** comprises a first digital counter CTR–1 having a clock input Cp1 which is connected to a pulse derivation circuit PD which is in turn connected to the line terminals L1 and N. The pulse derivation circuit PD is responsive to the applied alternating wave to provide a corresponding series of pulses Cp at the frequency of the applied wave. The timing pulses for the present control circuit can, if desired, be produced by means of an internal oscillator or other timing source rather than derived from the AC line voltage. The first digital counter CTR–1 may be realized by a chain of solid-state bistable flip-flop circuits, 16 of such circuits being here illustrated by output terminals Q11, Q12, ... Q116. Counter CTR–1 is responsive to the derived or line pulses Cp to accumulate a count of these pulses and provide such count in a binary format at the aforementioned output terminals Q11–Q116. A cursory inspection of the gating circuits on the right hand portion of FIG. **2** will indicate that various ones of these output terminals are read by the control logic circuit **27**.

A second digital counter section CTR–2 of the counter **26** has its clock input Cp2 connected in common with the clock input of the first digital counter CTR–1. The second digital counter CTR–2 is constructed in a manner similar to that of the first digital counter CTR–1 and has an output connection from its last stage to a reset input Cr1 of the first digital counter CTR–1 by way of a NAND gate G1 and a diode D1. THerefore, since the counters CTR–1 and CTR–2 are toggled by the same clock pulses and have substantially the same configuration, the first digital counter CTR–1 will be reset upon a full pulse count accumulation by the second digital counter CTR–2 before it has had a chance to count many pulses, assuming that the second digital counter CTR–2 comprises only a few stages compared to the number of stages of the first digital counter CTR–1.

The second digital counter CTR–2 includes a reset input Cr2 which is connected to the sensor circuit **24** by means of an inverter I1. Therefore, with no pulses being generated by the sensor circuit **24** to reset the second digital counter CTR–2, the first digital counter

CTR–1 is repetitively reset in response to cyclic full pulse count accumulations by the second digital counter CTR–2 after counting only a few of the line pulses Cp. The first digital counter CTR–1 is therefore prevented from accumulating a sufficient pulse count to affect the control logic circuit 27. When the sensor circuit 24 generates pulses, however, to repetitively reset the second digital counter CTR–2, cyclic resetting of the first digital counter CTR–1 is prevented and pulse count accumulation by counter CTR–1 is permitted.

As mentioned above, when the clothes load is dry, metallic objects occasionally fall across the sensor electrodes 21 and 22 to disable the neon oscillator thereby producing a momentary signal which is indicative of a wet clothes load. Also, static produced by the tumbling of a dry clothes load will produce pulses across the sensor electrodes 21 and 22 which temporarily disable the oscillator. The second digital counter CTR–2 is employed specifically to prevent such erroneous moisture indications from resetting the first digital counter CTR–1. Inasmuch as the output pulses from the oscillator must be disabled for a period sufficient to enable the second digital counter CTR–2 to accumulate several line pulses before an output from this counter will be produced, the absence of an occasional pulse or two from the oscillator does not provide a sufficient time for the generation of a reset pulse by the second digital counter CTR–2. By adjusting the number of pulses which counter CTR–2 must accumulate before producing a reset pulse for counter cTR–1, the duration of the moisture signal necessary at the sensor electrodes and the sensitivity of the system to static can be adjusted as desired.

The memory 28 comprises a chain of six bistable flip-flop circuits and may have a construction that is similar to that of the first and second digital counters CTR–1 and CTR–2. The memory 28 includes a clock or indexing input Cp3 by which the memory may be indexed to provide the sequence of unique binary states at the output terminals shown at Q31, ... Q36.

The control logic circuit 27 includes a plurality of interconnected NAND gates G2–G9, G12 and G13, and AND gate G10, and an OR gate G11. The control logic circuit 27 also includes a bistable flip-flop FF-1 which aids in indexing the memory 28.

The NAnD gate G2 senses several of the memory outputs and produces a low signal for the steps 0, 1, 2 and 3 of the truth table illustrated in FIG. 3.

The NAND gate G3 receives the output from the NAND gate G2 by way of an inverter I2 and senses the first two stages of the memory 28. The gate G3 operates to disable the heating element 16 by way of the electrical connection 29 for all steps after the step 0 of the truth table. In this particular circuit, a low output signal from the gate G3 indicates that the heater is energized.

In order to advance or index the memory from one state to another, an indexing signal must be produced by the flip-flop FF–1. The NAND gate G13 is connected to the output of the flip-flop FF–1 and serves as a buffer and an inverter and supplies the indexing signals to the clock input Cp3 of the memory 28 over a memory index conductor 41 and supplies a reset signal to the first digital counter CTR–1 by way of a counter reset conductor 42 and a diode D2. Therefore, each time that the memory is indexed, the first digital counter CTR–1 is reset to start timing for each function from time zero. The flip-flop FF–1 receives the line pulses from the pulse derivation circuit PD at trigger input Cp4 by way of an inverted I3, and receives state or data signals from the NAND gate G6 at data input Cd4. the gate G6 receives a timing signal every 5 seconds from the NAND gate G12 during even numbered memory state and a timing signal every 5 minutes from the NAND gate G5. The gates G12 and G5 are connected to appropriate outputs (Q17, Q19, Q112 and Q115) of the first digital counter CTR–1 which, as mentioned above, serves as a clock for the system.

The inverted output of the gate G3 is supplied to an input of the gate G4 by way of the inverter I4 along with a timing signal which is derived from the first digital counter CTR–1 and a selector switch DSS. This timing signal represents the amount of time which must be accumulated by the first digital counter CTR–1 before the drying portion of a cycle will be terminated. The switch DSS symbolizes that an operator has the option of selecting several time periods which are derived from the outputs of the first digital counter CTR–1. In the present embodiment such selected times are referenced in seconds and minutes rather than by output terminal designation and includes as selected times or terminals 34'', 1'9'', 2'18'', which respectively correspond to damp dry, dry and bone dry.

If it is desirable, a temperature sensing element may be utilized to sense the temperature within the drum or within an air duct and terminate a cool down portion which follows the drying portion of the program. During this cool-down interval, the heating element 16 is deenergized and the motor is energized to tumble the load of clothes. The NAND gate G7 is designed to accept a signal from such a cool down sensor and this feature is symbolically illustrated in the drawings by the cool-down sensing device CDS. In this particular embodiment, a grounding signal is required from the temperature sensor to terminate the cool-down period. The NAND gate G8 disables the gate G7 during memory state 3, and the inverted output of gate G2 disables gate G7 thereafter (memory states 4 through 51). Gate G3 disables gate G7 during memory state 0. Thus, gate G7 is active only during the cool-down period corresponding to memory states 1 and 2. When a timed rather than a sensed cool-down period is adequate, the gate G7 may be removed from the circuit entirely or the sensed input to the gate may be grounded. In this case, the gate G5 will operate to ensure that the cool-down period comprises two memory steps with each producing 5 minutes of tumbling with no heat as indicated by the truth table of FIG. 3.

The NAND gate G9 provides the master signal for controlling the power supply to the machine. The output of this gate goes high as soon as the dryer is energized and remains high until the last step or state of the memory 28. When this output goes low, the change of state is employed to de-energize, for example, a holding relay HR or the like so as to completely remove power from the machine.

The OR gate G11 receives an output from the AND gate G10 and reads the inverted or complementary output Q31 of the first stage of the memory circuit. The

gates G2 and G8 provide inputs to the gate G10, the G2 input being inverted by the inverter 12, and assure that the drive motor 17 will be energized during the steps 0, 1 and 2 of the drying program. During all the subsequent steps, the motor 17 need only be energized on the even numbered steps, and since this condition is indicated by the first stage of the memory, this input is supplied to the gate G11. As indicated previously, the control outputs 29, 30 and 31 from the control logic circuit 27 are low level signals and must be properly processed by appropriate interface circuitry to effect control of the comparitively large amounts of power consumed by the dryer motor, heating means, and master relay or the like. Such interface circuitry is well known in the art, and may include for example, TRIACS (not shown) to control AC power to the motor, a heating element, and an AC master relay.

The digital counters are provided with appropriate preset circuitry indicated by the conductors 43 and 44 to insure that the counters are preset to some predetermined state, zero in this illustration (first state), upon initial energization of the dryer. It may not be necessary to preset these counters to zero or the first state in all cases but to some other suitable predetermined count, zero being chosen as most appropriate in this particular illustrated embodiment.

Although the present invention has been disclosed by reference to a specific embodiment, many changes and modifications may be made in the invention by one skilled in the art without departing from the spirit and scope thereof, and it is to be understood that I intend to include within the patent warranted heron all such changes and modifications as may reasonably and properly be included within the scope of contribution to the art.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A control circuit for a dryer, comprising:
   - a source of timing pulses;
   - a first resettable counter arranged to count said pulses;
   - moisture sensing means operative to sense the moisture content of the clothes load and reset said counter at a rate proportional to the sensed moisture content; and
   - control logic means for terminating the drying operation upon accumulation of a preselected count.

2. The control circuit of claim 1, wherein said moisture sensing means comprises:
   - an oscillator circuit operative to produce pulses at a predetermined frequency;
   - conductivity sensing means arranged to contact the fabric load and connected to said oscillator so as to prevent generation of oscillator pulses in response to contact with fabric having a conductivity greater than a predetermined amount; and,
   - circuit means for receiving said oscillator pulses and producing a reset pulse for said first counter whenever the time between pulses from said oscillator is greater than a predetermined interval.

3. The control circuit of claim 2, wherein said circuit means for producing a reset pulse comprises a second resettable counter connected to count pulses from said source of timing pulses, and having a reset input arranged to receive said oscillator pulses and an output arranged to reset said first counter upon accumulation of a predetermined number of said timing pulses.

4. The control circuit of claim 1, further including means for selectively adjusting said preselected count which must be accumulated to terminate said drying operation.

5. The control circuit of claim 1, wherein said source of timing pulses comprises pulse derivation circuit means for utilizing the AC power line voltage to generate pulses synchronized to said voltage.

6. The control circuit of claim 1, further including: an indexable memory circuit having a series of sequential states corresponding to a program of dryer operations; and logic circuit means connected to said memory circuit for indexing same and providing dryer control output signals in accordance with the state of said memory.

7. In fabric treatment apparatus having means defining a fabric treatment zone and means for treating fabric placed therein to a predetermined condition, a control for terminating said treatment operation comprising:
   - a source of timing signals;
   - a counter arranged to count pulses derived from said source of timing signals;
   - sensing means associated with said fabric treatment zone for sensing a parameter related to said predetermined fabric condition and operative to reset said counter at a rate dependent upon the level of said sensed parameter; AND
   - circuit means for terminating said fabric treatment operation in response to the accumulation of a preselected count.

8. A method of controlling a fabric treating apparatus having a treatment zone and means for effecting at least one fabric treating operation, comprising the steps of:
   - a. initiating a fabric treating operation;
   - b. sensing a parameter related to the condition of the fabric within the treatment zone;
   - c. counting pulses from a source of timing signals;
   - d. repeatedly terminating and restarting the count until said sensed parameter reaches a predetermined value; and,
   - e. terminating the fabric treating operation upon the accumulation of a preselected count.

9. A method of controlling a fabric drying apparatus having means for drying fabric placed therein, comprising the steps of:
   - a. initiating a fabric drying operation;
   - b. sensing the moisture content of the fabric load;
   - c. counting pulses from a source of timing signals;
   - d. repeatedly terminating and restarting the count in response to a sensed moisture content greater than a predetermined amount; and
   - e. terminating the fabric drying operation in response to the accumulation of a preselected count.

10. The method according to claim 9, wherein the step of counting pulses includes:
   - a. generating pulses which are derived from the AC power line voltage; and,
   - b. counting said pulses by means of a digital counter.

11. The method according to claim 9 further including the steps of:

f. providing a sequence of digital function signals corresponding to a program of fabric treating functions; and,

g. controlling the energization of said fabric drying means in accordance with said signals.

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