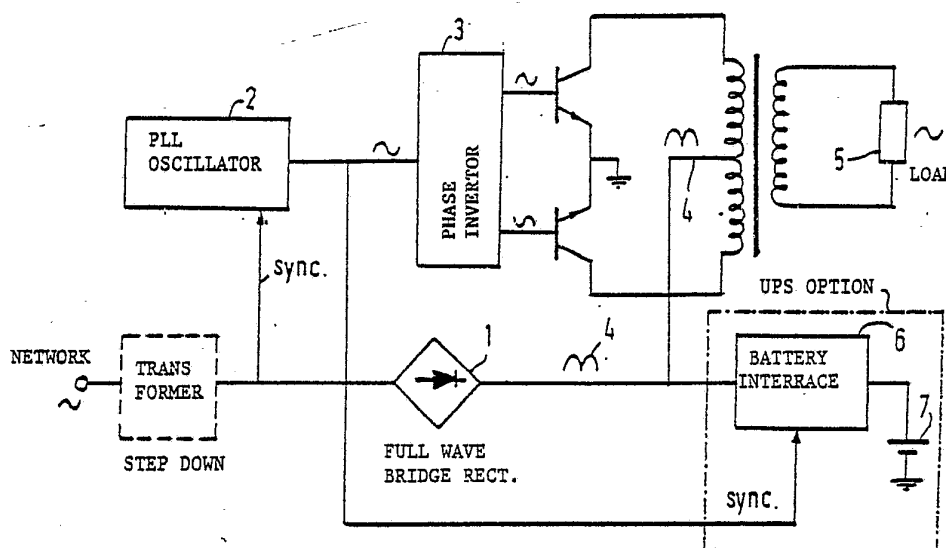




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(54) Title: AC VOLTAGE STABILIZER EASILY CONVERTIBLE INTO UNINTERRUPTIBLE POWER SUPPLY (UPS)



BLOCK DIAGRAM OF AC STABILIZER WITH UPS OPTION.

(57) Abstract

An electronic AC voltage stabilizer using a class B amplifier output stage which is fed by a full-wave rectified sine-wave voltage. The input voltage to (the phase inverter of) the class B amplifier output stage is kept in phase with the afore-said sine-wave voltage, which causes the power losses over the output stage to be very low. As compared to other electronic AC stabilizers the apparatus according to the invention offers high efficiency and simplicity. The AC stabilizer can easily be converted into a true UPS by adding a battery which by intermediary of a battery interface connects the conditioned battery voltage to the push pull amplifier output stage when the network fails.

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AC voltage stabilizer easily convertible into uninterruptible power supply (UPS)

Background of the invention.

Of all AC voltage stabilizers nowadays commercially available,
5 the pure electronic AC voltage stabilizer features the most precise and fastest regulation and has the lowest distortion on its output wave form. The conventional electronic AC stabilizer, however, tends to a certain complexity, which makes it the most expensive and often also the most inefficient stabilizing means because of the
10 substantial power losses inherent in the system. Even an overall efficiency as low as 50% is difficult to achieve in practice.

Summary of the invention.

In accordance with the present invention, an AC stabilizer is provided that supplies stable, "clean" AC power, even when the network
15 that is feeding it, is unstable and distorted. This type of stable, sinusoidal voltage is highly recommended for computers and other sorts of sensitive electronic equipment.

The basic part of the apparatus according to the invention is a conventional push pull power amplifier output stage. According to
20 the invention the power is applied to it in a special way. This will become apparent by comparing the conventional push pull output stage with that of the invention, supposing both have a sinusoidal signal applied to the input.

Fig. 1 shows a push pull power output stage receiving a filtered
25 low ripple DC supply voltage V_s . The voltage across either transistor T1 or T2 at a certain time will have the form of V_{ce} in Fig. 2, being the difference between the filtered DC voltage V_s and the voltage V_t

across the appropriate half of the output transformer. The other transistor does not conduct during this half cycle.

Assuming a resistive load R_L , which is transformed by the primary half of the transformer to $N^2 R_L$, the current through transistors T1 and T2 will have a half sinewave shape and will be proportional to V_t , so $I_C = \frac{V_t}{N^2 R_L}$. The power loss in the transistors during their half cycles is shown by the curve P_t in Fig. 2. $P_{t \text{ Max}}$, being the maximum loss over the half cycle, depends on the difference between V_s and V_t . This difference is called the voltage reserve. In practice the maximum dissipation will mostly occur somewhere in the slopes of the half sinewave, even when a non-resistive load is applied to the output stage. With non-resistive, or non-linear loads being applied, the transistor current will no longer be proportional to the transformer voltage, and efficiency will be reduced even more.

The present invention makes use of a totally different supply voltage to the output stage. This supply voltage is shown in Fig. 4 and has the shape of a series of half sinewaves, further to be called "bubble voltage". In Fig. 4 one full cycle of the bubble voltage is shown as V_s and the voltage across the transformer half is depicted as V_t . The voltage V_{ce} across the transistor is the difference between V_s and V_t and hence also a half sinewave. The value of V_{ce} is equal to or less than the voltage reserve and never exceeds this value during the cycle. This means that the power loss in the transistors, especially with non-linear or non-resistive loads, will be much less than that of the previously described conventional output stage. (see Fig. 1 and 2).

In theory the efficiency of the above output stage according to the invention can be 100% when $V_s = V_t$, but in practice it will be less than 100% for the following reasons.

The transistors T1 and T2 in Fig. 3 need the voltage reserve across their collector emitter junction in order to operate as amplifiers (see Fig. 5).

In case the bubble voltage is not an ideal half sinewave there

must be some reserve to ensure a clean voltage across the transformer primary and hence across the load. This means there is some dissipation in the transistors.

Furthermore it is recommended to maintain a certain voltage level at the zero crossing in order to prevent reactions of the load back-firing into the output transformer. Therefore a threshold voltage level is introduced which prevents the bubble voltage from becoming zero, thus ensuring a finite output impedance at the zero crossing (see Fig. 6). These precautions bring the practical efficiency of the output stage with bubble voltage supply down to approximately 85%, which is nevertheless substantially higher than that of the conventional DC-fed output stage of Fig. 1.

A major condition for the good operation of such an output stage is for the input signal to be equal in frequency and phase to the feeding bubble voltage, so the signal generator must be phase-locked to the bubble voltage frequency.

The simplest form of a circuit in accordance with the invention is shown in Fig. 7. The bubble voltage is simply created by full wave rectifying the network voltage (if necessary transformed down by a step-down transformer), by means of bridge 1, without the voltage being smoothed by a filter capacitor. The output signal of bridge 1 is called the network bubble voltage. The oscillator 2 is a phase locked loop oscillator which is locked to the network frequency so that the output signal of the phase inverter 3, being the input signal of the power stage fits snugly into the bubble voltage 4, resulting in a sinewave output voltage across resistive load 5, which is independent of the value of V_s , provided V_s is higher than V_t .

Below the level of V_t the amplifier output voltage will linearly follow the level of V_s . The system is then inoperative, the output signal showing same distortion as the bubble voltage V_s . The AC voltage stabilizer can be transferred into a true UPS - uninterruptible power supply - by adding a battery 7 via a battery interface 6. The battery interface is shown in Fig. 8. Although even a simple semiconductor element - like a transistor or SCR - can function as an interface to the output stage when the momentary value of the network bubble is too low,



the more elaborate way of using a PWM (pulse width modulated) converter is chosen because of the inherent smoother action when switching from network to battery operation and vice versa. The PWM converter receives a bubble voltage as a reference, obtained from rectification of the oscillator sinewave signal by means of a full wave bridge rectifier.

The output of the battery interface is changed into a battery bubble voltage, which is in phase with the network bubble voltage, and which is capable of supplying the necessary current to the amplifier output stage.

The peak value of the battery bubble voltage V_{DC} will be equal to the minimum value of the network bubble voltage (level at low network voltage). (See Fig. 9.) As soon as V_s becomes too low because of low network voltage and reaches the value of V_{DC} , the battery bubble V_{DC} will take over, not affecting V_t , which means that the output voltage of the power amplifier remains constant. The battery has taken over and delivers its current to the power amplifier through the battery interface. The difference in voltage between V_{DC} and V_t will be as small as possible ensuring maximum efficiency during battery operation. During network operation the value of V_s (=network bubble voltage) is relevant and the difference in voltage between V_s and V_t is a measure for the losses in the amplifier output stage. In case of high network voltage the efficiency of the power amplifier is lower, although still considerably higher than that of the conventional power amplifier earlier described. A limitation of the above described AC regulator/UPS which makes use of the network bubble voltage lies in the imperative synchronisation to the network frequency. Upon return from battery operation to network operation this will cause a slight output frequency deviation during the locking, which may disturb certain synchronous motor loads.

A configuration that does not suffer from above inconvenience is given in Fig. 10. There is no need for synchronisation to the network frequency, as the oscillator determines the frequency at which the system is operating. After an eventual step down, the network voltage is rectified by rectifier bridge 1 and buffered by a filter capacitor 8 in order to get a smooth DC voltage with low-ripple at point A



in Fig. 10. The battery voltage is connected through a diode to the same point A, which permits the battery to take over immediately when the DC voltage from the network is lower than the battery-voltage, creating an uninterruptible DC voltage at point A, which is supplied to the battery interface. This battery interface transforms the DC voltage into a bubble voltage under the control of the oscillator (see Fig. 8), which bubble voltage is supplied to the power amplifier output stage.

There is no imperative need for a synchronization to the network frequency, although it can be done if the load so requires. Due to the high efficiency of the PWM battery-interface - which can be 85% in practice - there is not much loss in overall efficiency in the system under normal network conditions. At high network voltage the battery bubble system has a better efficiency than the network bubble system previously described. A detailed circuit diagram is shown in Fig. 11. This is a complete AC-stabilizer with UPS facility, which functions in the network bubble operation mode. The network voltage is stepped down to a value of appr. 17V AC and full wave rectified to a bubble voltage with appr. 24Volts peak value ($V_s=24$). This network bubble voltage is fed to the class B output stage, consisting of two pairs of power transistors connected in Darlington configuration. The oscillator 2, consisting of a phase locked loop (IC 1) and a programmable oscillator (IC 2) which are connected in a feedback loop, generates the input signal for the entire embodiment. This sinusoidal signal is fed through optocoupler OC to the phase inverter which is of the floating paraphrase or seesaw type. The synchronization to the network is accomplished by taking a signal from the transformer secondary and connecting it to the phase locked loop IC 1 via resistor R4.

From the oscillator a signal is derived via voltage divider R17/R18 as an input for the battery interface. This signal is electronically full wave rectified by IC 5, IC 6 and diodes D3 and D4. and fed to the PWM converter as a reference. (Fig. 8). This reference voltage is amplified by operational amplifier IC 7 and applied to IC 8, which converts this signal into a pulse width modulated high frequency signal of about 20KHz, to be applied to the power transistor pair T5/T6, which receive their supply from the battery 7. The signal obtained is



integrated by choke coil Tr3 and capacitor C18. The resulting waveform is a bubble voltage (V_{DC} in Fig. 9) of stable amplitude, thanks to the feedback via R54/C16. This amplitude is equal to the "network low" value of the network bubble voltage (V_s in Fig. 9).

- 5 In the normal network condition the power to the class B output stage will come from network bubble V_s as this is higher than battery bubble V_{DC} and the latter will only be available as a shadow behind V_s .



C L A I M S .

1. An electronic AC power stabilizer for supplying stable and clean power to a load section comprising a push pull power amplifier output stage which is powered by a full wave rectified sinewave voltage - hereafter called network bubble voltage - said bubble
5 voltage being obtained by full wave rectification of the network voltage feeding said stabilizer, the signal input of the stabilizer being delivered by a phase locked loop oscillator which is synchronized to the frequency of said network voltage in such a way that the voltage over the transistors of said push pull power amplifier output
10 stage is synchronous with said bubble voltage resulting in a very low power loss over said power amplifier output stage.
2. The apparatus of claim 1 wherein a battery is connected to the said push pull power amplifier output stage by intermediary of a battery interface that consists of a semiconductor device, said
15 device being triggered to conduct when the said network voltage is below a certain level in such a way that said stabilizer is transformed into an uninterruptible power supply.
3. The apparatus of claim 1 wherein a battery is connected to the said push pull power amplifier output stage by intermediary of a
20 battery interface that consists of a pulse width modulated converter which converts the battery DC voltage into a waveshape that resembles a full wave rectified sinewave - the battery bubble voltage - that is in phase with said network bubble voltage but so much lower in amplitude that it will take over the voltage supply to said push pull amplifier
25 output stage when said network voltage is below a certain level, said stabilizer thus being transformed into a high efficiency uninterruptible power supply.
4. An electronic AC power stabilizer for supplying stable and clean power to a load section comprising a push pull power amplifier output
30 stage, which is powered by a voltage having a waveshape that resembles a full wave rectified sinewave - hereafter called feeding bubble voltage -



- said bubble voltage being obtained by full wave rectifying and filtering of the network voltage that is feeding said stabilizer and converting the smooth DC voltage into said feeding bubble voltage by a pulse width modulated converter, said converter
- 5 receiving a reference signal obtained by full wave rectifying a sine-wave signal from a sine-wave oscillator that is also connected to the signal input of the said push-pull power amplifier output stage, so ensuring a very low power loss over said power amplifier output stage.
- 10 5. The apparatus of claim 4 wherein a battery is connected to the said smooth DC voltage by intermediary of a diode in such a way that the battery takes over when said DC voltage is below the battery voltage, transforming said stabilizer into a high efficiency uninterruptible power supply.



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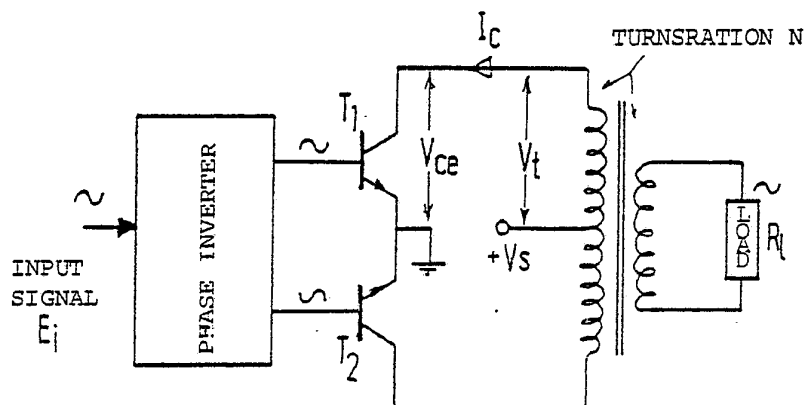


FIG.1

OUTPUT STAGE FED BY
FILTERED DC VOLTAGE

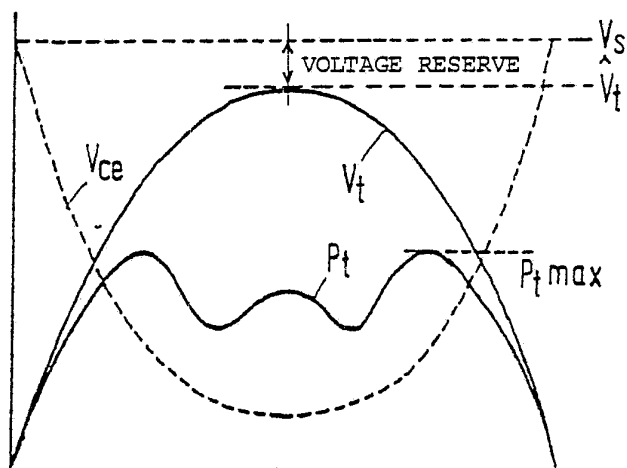


FIG.2

POWER LOSS P_t IN
TRANSISTOR DURING HALF CYCLE

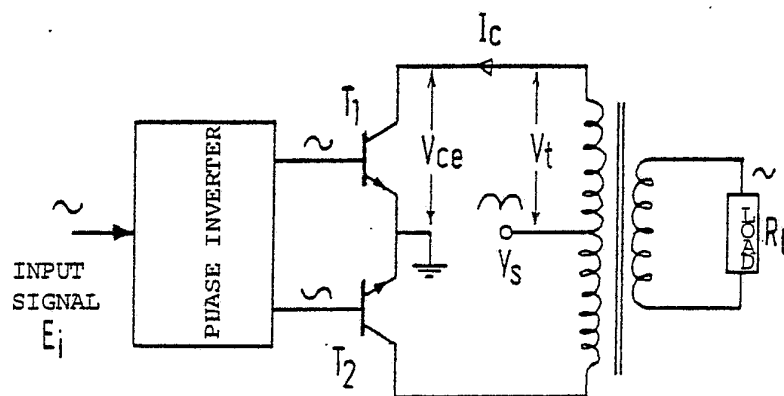


FIG.3

OUTPUTSTAGE FED BY
BUBBLEVOLTAGE

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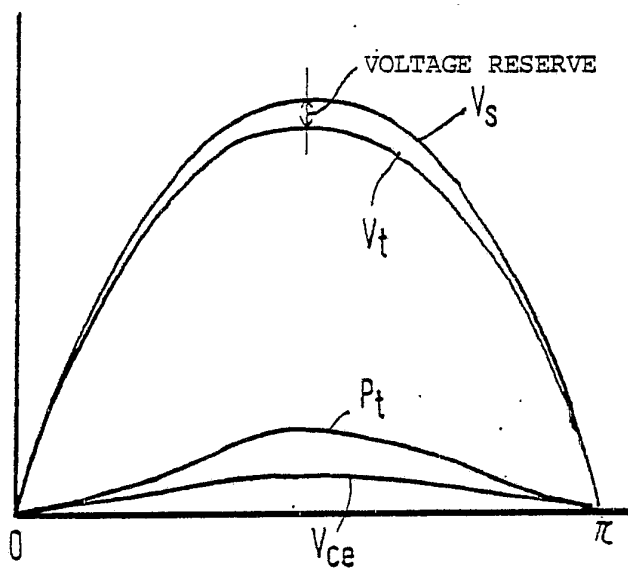


FIG. 4

POWER LOSS IN TRANSISTOR
 FED BY BUBBLE VOLTAGE

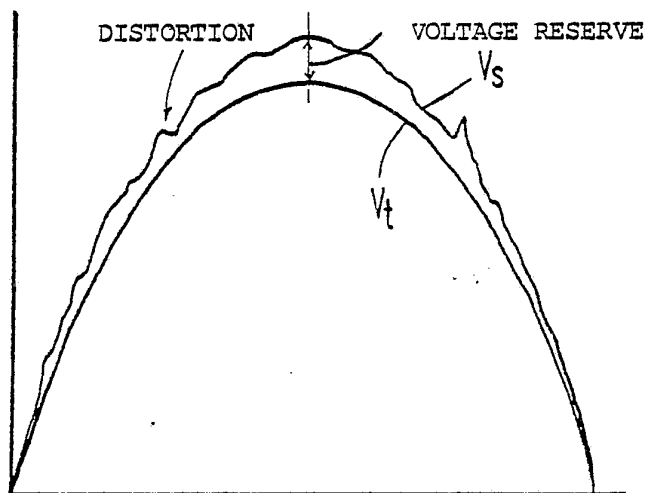


FIG. 5

DISTORTED BUBBLE VOLTAGE
 AND "CLEAN" TRANSFORMER-
 VOLTAGE.

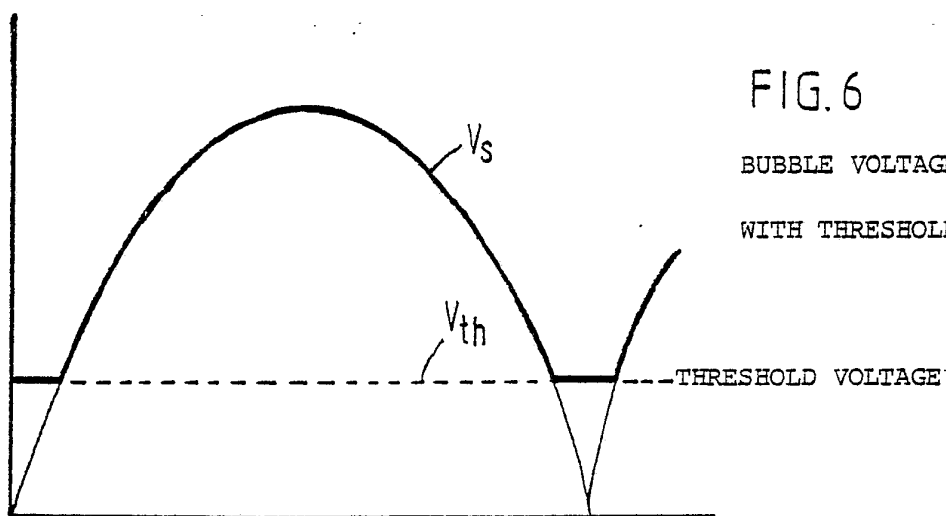


FIG. 6

BUBBLE VOLTAGE
 WITH THRESHOLD LEVEL

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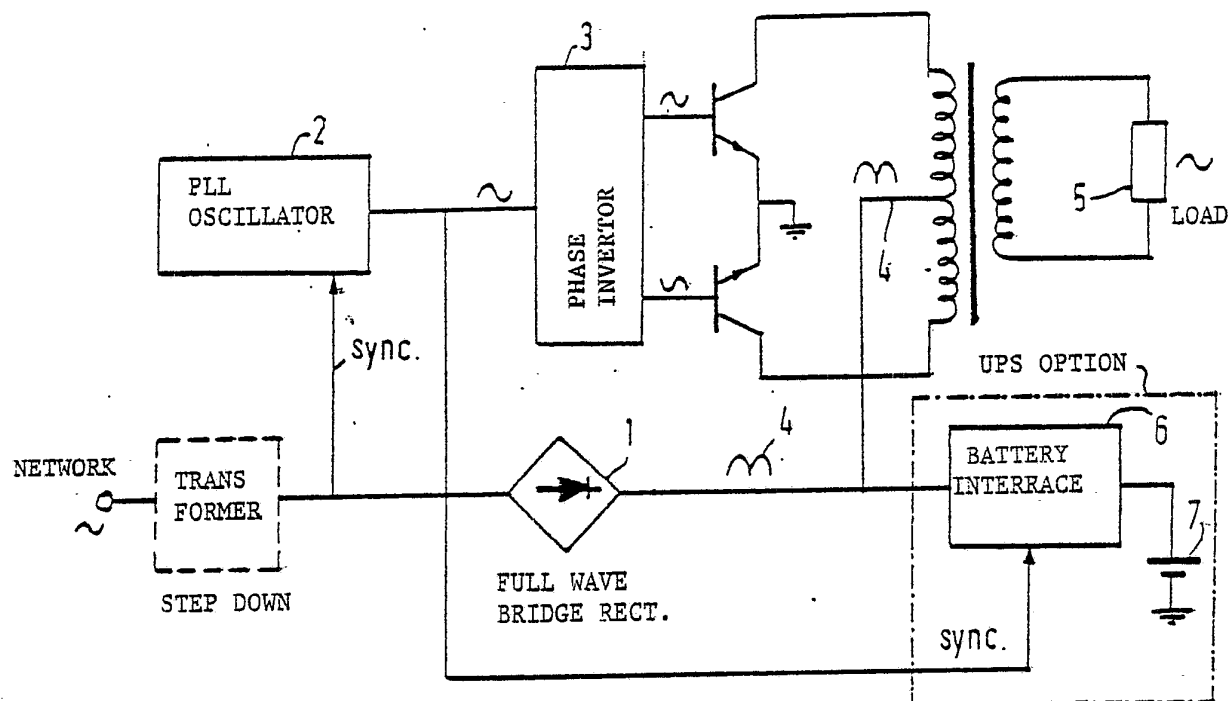


FIG. 7 BLOCK DIAGRAM OF AC STABILIZER WITH UPS OPTION.

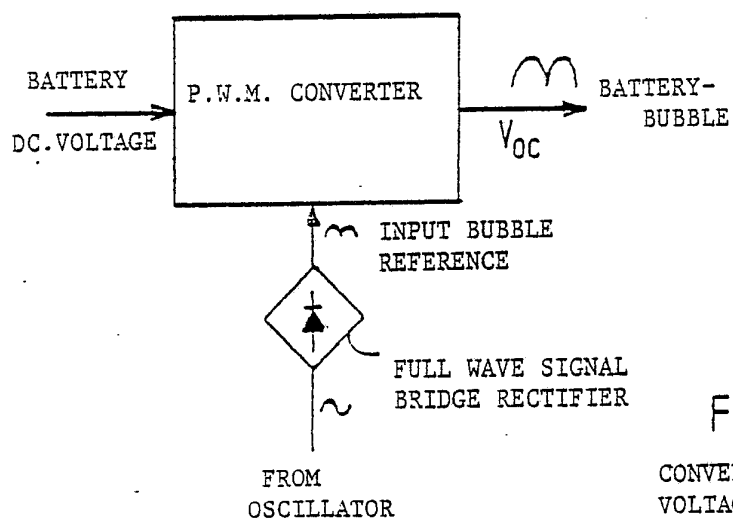


FIG. 8

CONVERSION OF BATTERY-VOLTAGE INTO BATTERY BUBBLE

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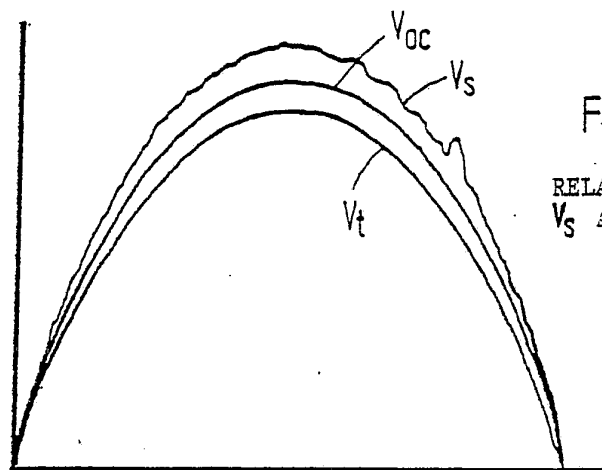


FIG. 9

RELATION BETWEEN NETWORKBUBBLE
 V_s AND BATTERY BUBBLE V_{oc}

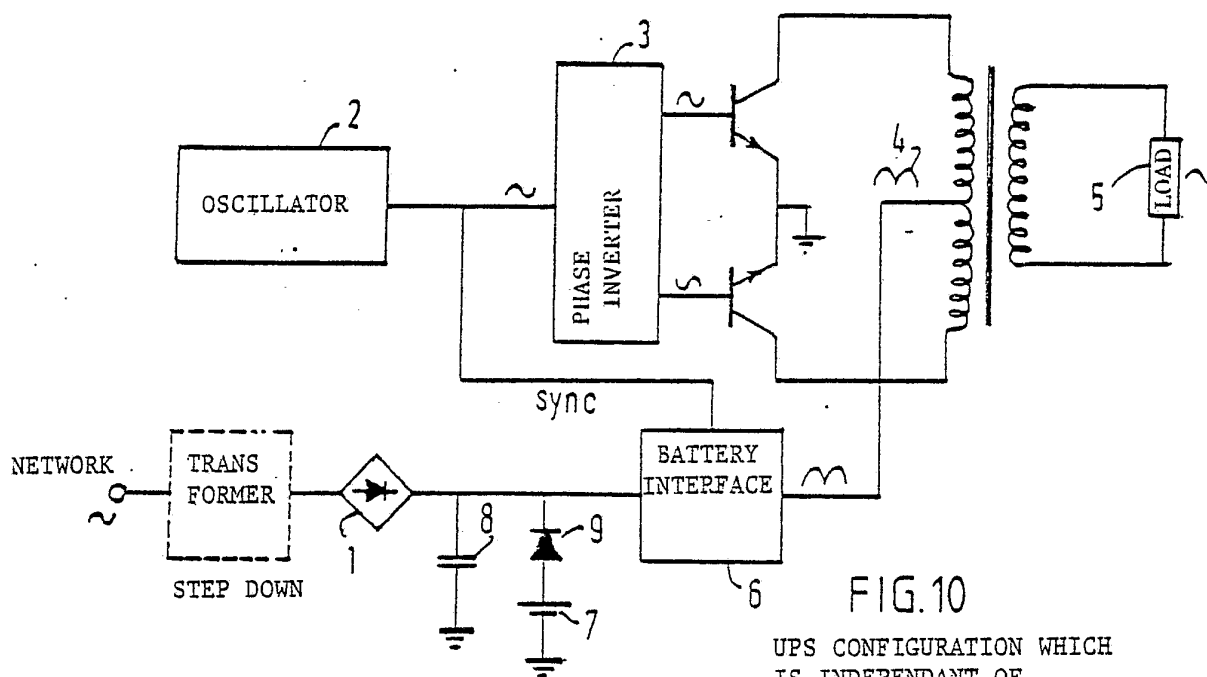


FIG. 10

UPS CONFIGURATION WHICH
IS INDEPENDANT OF
NETWORKFREQUENCY

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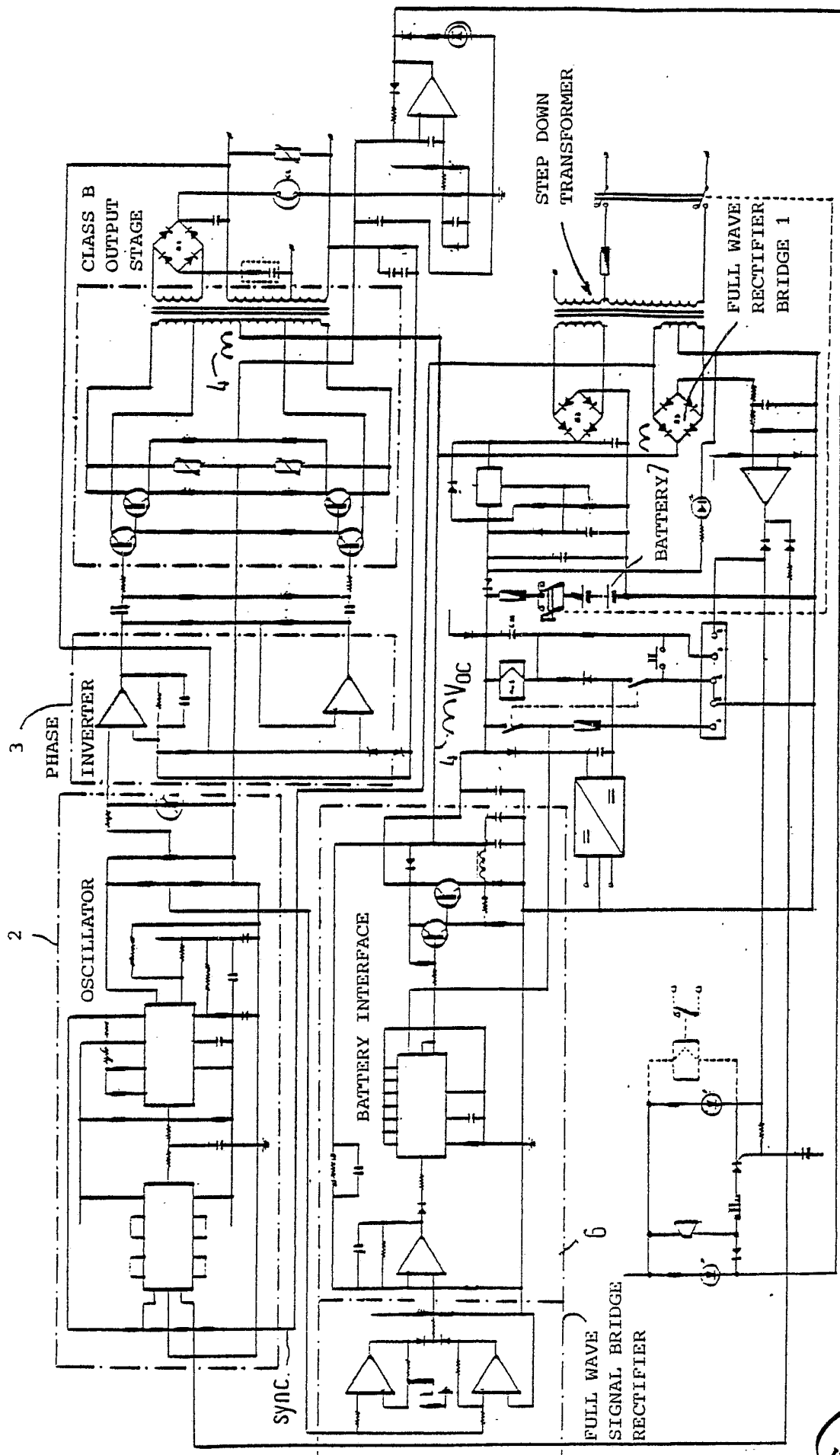
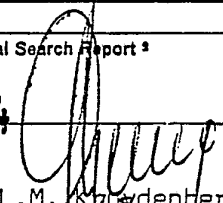


FIG.11 AC VOLTAGE STABILIZER COMPLETE WITH UPS OPTION

INTERNATIONAL SEARCH REPORT

International Application No PCT/NL 84/00012

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) ³		
According to International Patent Classification (IPC) or to both National Classification and IPC		
IPC ³ : H 02 M 5/257; H 02 M 7/538; H 02 J 9/06		
II. FIELDS SEARCHED		
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Classification System	Classification Symbols	
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Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁵		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ¹⁴		
Category [*]	Citation of Document, ¹⁶ with Indication, where appropriate, of the relevant passages ¹⁷	Relevant to Claim No. ¹⁸
A	DE, A, 2559333 (AMTENBRINK) 14 July 1977 see pages 5,6 --	1,2
A	EP, A1, 0061744 (TOSHIBA) 6 October 1982 see page 4, lines 8-29 --	1
A	DE, A, 3109750 (SIEMENS) 30 September 1982 see pages 5 and 6 --	3,4
A	US, A, 3825815 (GYUGYI et al.) 23 July 1974 -----	
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IV. CERTIFICATION		
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16th May 1984	27 JUN 1984	
International Searching Authority ¹	Signature of Authorized Officer ²⁰	
EUROPEAN PATENT OFFICE	 G.L.M. Koudenberg	

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/NL 84/00012 (SA 6775)

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DE-A- 2559333	14/07/77	None	
EP-A- 0061744	06/10/82	JP-A- 57160371	02/10/82
DE-A- 3109750	30/09/82	None	
US-A- 3825815	23/07/74	FR-A,B 2233752	10/01/75
		JP-A- 50036049	04/04/75

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