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- (54) **Title:** MICROELECTRONIC STRUCTURES HAVING MULTIPLE MICROELECTRONIC DEVICES CONNECTED WITH A MICROELECTRONIC BRIDGE EMBEDDED IN A MICROELECTRONIC SUBSTRATE

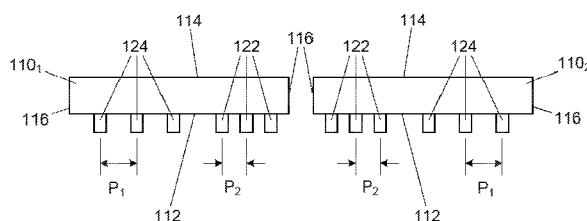


FIG. 1

- (57) **Abstract:** A microelectronic structure includes a microelectronic substrate having a first surface and a cavity extending into the substrate from the microelectronic substrate first surface, a first microelectronic device and a second microelectronic device attached to the microelectronic substrate first surface, and a microelectronic bridge disposed within the microelectronic substrate cavity and attached to the first microelectronic device and to the second microelectronic device. In one embodiment, the microelectronic structure may include a reconstituted wafer formed from the first microelectronic device and the second microelectronic device. In another embodiment, a flux material may extend between the first microelectronic device and the microelectronic bridge and between the second microelectronic device and the microelectronic bridge.



**MICROELECTRONIC STRUCTURES HAVING MULTIPLE
MICROELECTRONIC DEVICES CONNECTED WITH A MICROELECTRONIC
BRIDGE EMBEDDED IN A MICROELECTRONIC SUBSTRATE**

TECHNICAL FIELD

5 Embodiments of the present description generally relate to the field of microelectronic package fabrication, and, more particularly, to a microelectronic structure including a bridge embedded in a substrate for electrical signal connection between microelectronic devices and to methods of fabricating the same.

BACKGROUND

10 The microelectronic industry is continually striving to produce ever faster and smaller microelectronic packages for use in various electronic products. As part of this effort, microelectronic packages containing multiple devices, such a microelectronic dice, have been developed. These multiple microelectronic device packages are referred to in the art as multi-
15 device or multi-chip packages (MCPs) and offer the potential for increased architectural flexibility at reduced cost, but must do so such that appropriate microelectronic device-to-microelectronic device interconnect densities are provided. As will be understood to those skilled in the art, interconnect density is an important consideration because an insufficient number of microelectronic device connections would limit the bandwidth capability for the affected microelectronic device interface, and thus would reduce the communication efficiency
20 and capability between microelectronic devices.

BRIEF DESCRIPTION OF THE DRAWINGS

 The subject matter of the present disclosure is particularly pointed out and distinctly claimed in the concluding portion of the specification. The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended
25 claims, taken in conjunction with the accompanying drawings. It is understood that the accompanying drawings depict only several embodiments in accordance with the present disclosure and are, therefore, not to be considered limiting of its scope. The disclosure will be described with additional specificity and detail through use of the accompanying drawings, such that the advantages of the present disclosure can be more readily ascertained, in which:

30 FIG. 1-10 illustrate cross-sectional views of a method for fabricating a microelectronic structure including at least two microelectronic devices electrically connected with bridge, wherein the bridge resides within a cavity in a microelectronic substrate to which the microelectronic devices are electrically attached, according to an embodiment of the present description.

35 FIG. 11-16 illustrate cross-sectional views of another method for fabricating a

microelectronic structure including at least two microelectronic devices electrically connected with bridge, wherein the bridge resides within a cavity in a microelectronic substrate to which the microelectronic devices are electrically attached, according to an embodiment of the present description.

5 FIG. 17 is a flow chart of a process of fabricating a microelectronic structure according to an embodiment of the present description.

FIG. 18 illustrates a computing device in accordance with one implementation of the present description.

DESCRIPTION OF EMBODIMENTS

10 In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the claimed subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the subject matter. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within
15 other embodiments without departing from the spirit and scope of the claimed subject matter. References within this specification to “one embodiment” or “an embodiment” mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present description. Therefore,
20 the use of the phrase “one embodiment” or “in an embodiment” does not necessarily refer to the same embodiment. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the subject matter is defined only
25 by the appended claims, appropriately interpreted, along with the full range of equivalents to which the appended claims are entitled. In the drawings, like numerals refer to the same or similar elements or functionality throughout the several views, and that elements depicted therein are not necessarily to scale with one another, rather individual elements may be enlarged or reduced in order to more easily comprehend the elements in the context of the present
30 description.

The terms “over”, “to”, “between” and “on” as used herein may refer to a relative position of one layer with respect to other layers. One layer “over” or “on” another layer or bonded “to” another layer may be directly in contact with the other layer or may have one or more intervening layers. One layer “between” layers may be directly in contact with the layers or may
35 have one or more intervening layers.

Embodiments of the present description include fabricating a microelectronic structure comprising forming a first and a second microelectronic device, wherein each of the first and the second microelectronic device include a plurality of high density interconnect structures and a plurality of lower density interconnect structures on an active surface thereof, attaching a
5 microelectronic bridge to the plurality of high density interconnect structures of the first microelectronic device and to the plurality of high density interconnect structures of the second microelectronic device, forming a microelectronic substrate having a cavity extending into the microelectronic substrate from a first surface thereof, and electrically attaching the plurality of lower density interconnect structures of the first microelectronic device and the plurality of lower
10 density interconnect structures of the second microelectronic device to the first surface of the microelectronic substrate, wherein the microelectronic bridge extends into the microelectronic substrate cavity.

Embodiments of the present description may enable density scaling of structures within a microelectronic package that may represent a significant improvement over existing technology
15 generations by making use of microelectronic bridges that are embedded in the microelectronic substrate. These microelectronic bridges support dense microelectronic device-to-microelectronic device interconnection from a first microelectronic device to a second microelectronic device. Thus, a resulting microelectronic package may be considerably smaller than a microelectronic package that is only interconnected with conductive routes within the
20 microelectronic substrate.

FIGs. 1-11 illustrate a method of fabricating a microelectronic structure, according on one embodiment of the present description. As shown in FIG. 1, plurality of microelectronic devices, shown as a first microelectronic device 110₁ and a second microelectronic device 110₂, may be formed, wherein each microelectronic device 110₁, 110₂ may include an active
25 surface 112, an opposing back surface 114, and at least one side 116 extending between the microelectronic device active surface 112 and the microelectronic device back surface 114. Each microelectronic device 110₁, 110₂ may include a plurality of high density interconnect structures 122, such as bumps or pillars, and a plurality of lower density interconnect structures 124, such as bumps or pillars, on the microelectronic device active surface 112. It is
30 understood that the high density interconnect structures 122 and the lower density interconnect structures 124 may be in electrical communication with integrated circuitry (not shown) within the first microelectronic device 110₁ and the second microelectronic device 110₂. The first microelectronic device 110₁ and the second microelectronic device 110₂ may be any appropriate microelectronic device, such as microelectronic dice, including, but not limited to a
35 microprocessor, a chipset, a graphics device, a wireless device, a memory device, an application

specific integrated circuit device, and the like.

As defined for purposes of the present description, the term "lower density" in "lower density interconnect structures" is relative to the term "high density" in "high density interconnect structures" in that the lower density interconnect structures 124 have a greater
5 pitch/spacing P1 between the lower density interconnect structures 124 than a pitch/spacing P2 between the high density interconnect structures 122, and vice versa.

As shown in FIG. 2, the first microelectronic device 110₁ and the second microelectronic device 110₂ may be aligned on a carrier 132. In one embodiment, the first microelectronic device 110₁ and the second microelectronic device 110₂ may be aligned with their active
10 surfaces 112 facing the carrier 132 and secured in place with an adhesive layer 134 disposed between the carrier 132 and the active surfaces 112 of the first microelectronic device 110₁ and the second microelectronic device 110₂. In an embodiment, the first microelectronic device 110₁ and the second microelectronic device 110₂ may be aligned such that the plurality of high density interconnect structures 122 of the first microelectronic device 110₁ are directly adjacent the high
15 density interconnect structures 122 of the second microelectronic device 110₂. As will be understood to those skilled in the art, precision pick and place equipment may be utilized with pre-defined spacing and orientation to assure proper alignment.

As shown in FIG. 3, an encapsulant material 118 may be deposited over the first microelectronic device 110₁ and the second microelectronic device 110₂, such that the
20 encapsulant material 118 contacts the back surfaces 114 and sides 116 of the first microelectronic device 110₁ and the second microelectronic device 110₂. In one embodiment, wafer level compression molding with low coefficient of thermal expansion material may be used to deposit the encapsulant material 118. The encapsulant material 118 may be any appropriate material, including, but not limited to, polymer materials with or with appropriate
25 fillers.

As shown in FIG. 4, the encapsulant material 118 may be cured or partially cured and the structure may be thinned by removing a portion of the encapsulant material 118 adjacent to back surfaces 114 of the first microelectronic device 110₁ and the second microelectronic device 110₂ to expose the back surfaces 114 thereof. This removal leaves the encapsulant material 118
30 contacting the sides 116 of the first microelectronic device 110₁ and the second microelectronic device 110₂, thereby forming a structure which is referred to as a reconstituted wafer 120. It is understood that a portion of the first microelectronic device 110₁ and the second microelectronic device 110₂ may be removed during or after the removal of the portion of the encapsulant material 118 to reduce the thickness T of the reconstituted wafer 120. In one embodiment, the
35 removal of the portion of the encapsulant material 118 and the removal of the portion of the first

microelectronic device 110₁ and the second microelectronic device 110₂ may be performed before the carrier 132 (see FIG. 4) and adhesive layer 134 (see FIG. 4) are removed. In another embodiment, the removal of the portion of the encapsulant material 118 and the removal of the portion of the first microelectronic device 110₁ and the second microelectronic device 110₂ may be performed after the carrier 132 (see FIG. 4) and adhesive layer 134 (see FIG. 4) are removed, wherein the first microelectronic device 110₁ and the second microelectronic device 110₂ may be attached to a backgrinding tape (not shown) prior to the removal of the portion of the encapsulant material 118 and the removal of the portion of the first microelectronic device 110₁ and the second microelectronic device 110₂. The removal of the portion of the encapsulant material 118 and the removal of the portion of the first microelectronic device 110₁ and the second microelectronic device 110₂ may be achieved by any technique known in the art, including but not limited to mechanical grinder, etching, chemical mechanical planarization, and the like. As will be understood to those skilled in the art, the material removal may improve thermal performance and may planarize the reconstituted wafer 120.

As shown in FIG. 5, a microelectronic bridge 140 may be formed comprising a first surface 142, an opposing second surface 144, and at least one side 146 extending between the first surface 142 and the second surface 144. The microelectronic bridge 140 may include a plurality of interconnect structures 152, such as bumps or pillars, on the microelectronic bridge first surface 142. As illustrated, the microelectronic bridge 140 may include a plurality of conductive routes 148 formed therein to connect respective microelectronic bridge interconnect structures 152. As further illustrated, a solder material 154 may be applied on the interconnect structures 154 by any appropriate process known in the art, such as with a fine, but uniform pitch using a plating technique.

As shown in FIG. 6, the microelectronic bridge 140 may be attached to the high density interconnect structures 122 of the first microelectronic devices 110₁ and to the high density interconnect structures 122 of the second microelectronic device 110₂ to form an electrical connection therebetween. In one embodiment, the plurality of interconnect structures 152 of the microelectronic bridge 140 are in a mirror-image configuration to the plurality of high density interconnect structures 122 of the first microelectronic device 110₁ and the second microelectronic device 110₂, and are attached thereto with the solder material 154 by thermocompression bonding. In another embodiment, the microelectronic bridge 140 may be attached with a traditional chip attach module process despite the high density/fine pitch of the microelectronic bridge interconnect structures 152, when a low coefficient of the thermal expansion encapsulant material 118 is utilized, so the thermal expansion mismatch between the microelectronic bridge 140 and the reconstituted wafer 120 is minimal. The processes and

materials use for forming the microelectronic bridge 140 are well known in the art, and, for the sake of brevity and conciseness, will not be described or illustrated herein.

As shown in FIG. 7, a microelectronic substrate 160 may be formed having a cavity 170 therein that extends into the microelectronic substrate 160 from a first surface 162 thereof, wherein the microelectronic substrate cavity 170 is defined by at least one sidewall 174 and a bottom surface 172. The microelectronic substrate 160 may further include a plurality of bond pads 164 formed in or on the microelectronic substrate first surface 162. The microelectronic substrate cavity 170 may be formed by any known technique known in the art, including, but not limited to, laser ablation, controlled depth routing, etching, and the like.

The microelectronic substrate 160 may be any appropriate microelectronic substrate, including, but not limited to, an interposer, a motherboard, and the like. Further, the microelectronic substrate 160 may comprise a plurality of dielectric layers (not shown) having the plurality of conductive routes 148 formed from conductive traces (not shown) formed on the dielectric layers (not shown) that are connected with conductive vias (not shown) formed through the dielectric layers (not shown). The processes and materials use for forming the microelectronic substrate 160 are well known in the art, and, for the sake of brevity and conciseness, will not be described or illustrated herein.

As shown in FIG. 8, the structure of FIG. 6 may be attached to the microelectronic substrate 160, wherein the plurality of lower density interconnect structures 124 of the first microelectronic device 110₁ and the plurality of lower density interconnect structures 124 of the second microelectronic device 110₂ may be electrically attached to the plurality of substrate bond pads 164 formed in or on the microelectronic substrate first surface 162, wherein the microelectronic bridge 140 extends into the microelectronic substrate cavity 170. In one embodiment, the plurality of lower density interconnect structures 124 of the first microelectronic device 110₁ and the plurality of lower density interconnect structures 124 of the second microelectronic device 110₂ are in a mirror-image configuration to the plurality of microelectronic substrate bond pads 164, and are attached thereto with a solder material 176 by thermocompression bonding. In one embodiment, the solder material 176 may be applied to the plurality of substrate bond pads 164 with a microball process, as known in the art.

As shown in FIG. 9, an underfill material 178 may be disposed between the active surface 112 of the first microelectronic device 110₁ and the microelectronic substrate first surface 162, between the active surface 112 of the second microelectronic device 110₂ and the microelectronic substrate first surface 162, and within the microelectronic substrate cavity 170 to form a microelectronic structure 180. In one embodiment, as illustrated in FIG. 9, the underfill material 178 may be disposed between the second surface 144 of the microelectronic bridge 140

and the bottom surface 172 of the cavity 170. In another embodiment, as illustrated in FIG. 10, an adhesive material 182, such as a snap cure epoxy, can be disposed on the bottom surface 174 of the cavity 170 prior to the attachment of the first microelectronic device 110₁ and the second microelectronic device 110₂ to ensure that material is disposed between the second surface 144 of the microelectronic bridge 140 and the bottom surface 172 of the cavity 170. In an embodiment, a capillary underfill process may be used to dispose the underfill material 178. In another embodiment, a high pressure assisted curing process may be used to dispose the underfill material 178 due the complexity of the space to be filled, as will be understood to those skilled in the art. It is further noted that the underfill material 178 is a single material filling the space, as described.

FIGs. 11-16 illustrate a method of fabricating a microelectronic structure, according to another embodiment of the present description. As shown in FIG. 11, the first microelectronic device 110₁ and the second microelectronic device 110₂, as shown and discussed with regard to FIG. 1, may be aligned in a carrier 202, such as a thermocompression bonding pedestal. In one embodiment, the first microelectronic device 110₁ and the second microelectronic device 110₂ may be aligned with their back surfaces 114 abutting the carrier 202. In an embodiment, the first microelectronic device 110₁ and the second microelectronic device 110₂ may be aligned such that the plurality of high density interconnect structures 122 of the first microelectronic device 110₁ are directly adjacent the high density interconnect structures 122 of the second microelectronic device 110₂. As will be understood to those skilled in the art, precision pick and place equipment may be utilized with pre-defined spacing and orientation to assure proper alignment.

As shown in FIG. 12, a flux material 204, such as an epoxy flux material, may be dispensed onto the high density interconnect structures 122 of the first microelectronic device 110₁ and onto the high density interconnect structures 122 of the first microelectronic device 110₂. As shown in FIG. 13, the microelectronic bridge 140, as discussed with regard to FIG. 5, may be attached to the high density interconnect structures 122 of the first microelectronic devices 110₁ and to the high density interconnect structures 122 of the second microelectronic device 110₂ to form an electrical connection therebetween, wherein the flux material 204 extends between the first microelectronic device 110₁ and the microelectronic bridge 140, and between on the second microelectronic device 110₂ and the microelectronic bridge 140. In one embodiment, the plurality of interconnect structures 152 of the microelectronic bridge 140 are in a mirror-image configuration to the plurality of high density interconnect structures 122 of the first microelectronic device 110₁ and the second microelectronic device 110₂, and are attached thereto with a solder material 154 by

thermocompression bonding.

As shown in FIG. 14, the structure of FIG. 13 may be removed from the carrier 202 (see FIG. 13) and may be attached to the microelectronic substrate 160, as discussed with regard to FIG. 7, wherein the plurality of lower density interconnect structures 124 of the first

5 microelectronic device 110₁ and the plurality of lower density interconnect structures 124 of the second microelectronic device 110₂ may be electrically attached to the plurality of substrate bond pads 164 formed in or on the microelectronic substrate first surface 162, wherein the microelectronic bridge 140 extends into the microelectronic substrate cavity 170. In one embodiment, the plurality of lower density interconnect structures 124 of the first

10 microelectronic device 110₁ and the plurality of lower density interconnect structures 124 of the second microelectronic device 110₂ are in a mirror-image configuration to the plurality of microelectronic substrate bond pads 164, and are attached thereto with the solder material 176 by thermocompression bonding.

As shown in FIG. 15, the underfill material 178 may be disposed between the active

15 surface 112 of the first microelectronic device 110₁ and the microelectronic substrate first surface 162, between the active surface 112 of the second microelectronic device 110₂ and the microelectronic substrate first surface 162, and within the microelectronic substrate cavity 170 to form the microelectronic structure 180.

In some embodiments as illustrated in FIGs. 6-10 and 13-15, the microelectronic

20 bridge 140 can be a passive structure, in that it has no functionality other than to provide the conductive routes 148 between the first microelectronic device 110₁ and the second microelectronic device 110₂. In other embodiments, as shown in FIG. 16, the microelectronic bridge 140 may comprise at least one active component 214, having its own functionality apart from a bridging function, and, thus, may be a microelectronic device, a resistor, a capacitor, and

25 the like, embedded in the microelectronic bridge 140. In one embodiment, as illustrated in FIG. 16, the microelectronic bridge 140 may have a signal routing layer 212 with at least one active component 214 electrically attached to the signal routing layer 212 with solder balls 222 and/or wire bonds 224, wherein the active components 214 may be encapsulated within a dielectric material 216.

30 It is noted that the process embodiments of the present description attach the microelectronic bridge 140 to the first microelectronic device 110₁ and the second microelectronic device 110₂ prior to the incorporation thereof with the microelectronic substrate 160. Such processes may have advantages compared to processes wherein the microelectronic bridge 140 is embedded in the microelectronic substrate 160 prior to attaching

35 the first microelectronic device 110₁ and the second microelectronic device 110₂. For example,

if the microelectronic bridge 140 were embedded in the microelectronic substrate 160, it would require the first microelectronic device 110₁ and the second microelectronic device 110₂ to be simultaneously attached to a mixed pitch interconnects, which would make a one-step process no longer a viable option to produce uniform bump height required by the chip attach process. As
 5 will be understood to those skilled in the art, a solder-on-die process or a multi-step lithographic and plating process may be needed. However, the mixed pitch configuration and stringent bump height uniformity requirements make the solder-on-die process very difficult to develop due to process marginality, particularly for larger microelectronic structures.

It is understood that although the detailed description with regard to the embodiments of
 10 FIGs. 1-16 are directed to two microelectronic devices 110₁ and 110₂, one microelectronic bridge 140, and one cavity 170 in the microelectronic substrate 160, the subject matter of the present description is not so limited, as any number of microelectronic devices, microelectronics bridges, and microelectronic substrate cavities may be used. In one embodiment, three microelectronic devices may be attached to a triangular bridge. In another embodiment, six microelectronic
 15 devices may be attached to a hexagonal bridge. In a further embodiment, more than one microelectronic bridge may be disposed in a single microelectronic substrate cavity. In yet a further embodiment, multiple cavities may be formed in a single microelectronic substrate.

FIG. 17 is a flow chart of a process 300 of fabricating a microelectronic structure according to an embodiment of the present description. As set forth in block 302, a first and a
 20 second microelectronic device may be formed, wherein each of the first and the second microelectronic device includes a plurality of high density interconnect structures and a plurality of lower density interconnect structures on an active surface thereof. A microelectronic bridge may be attached to the plurality of high density interconnect structures of the first microelectronic device and to the plurality of high density interconnect structures of the second
 25 microelectronic device, as set forth in block 304. As set forth in block 306, a microelectronic substrate may be formed having a cavity defined therein extending from a first surface of the microelectronic substrate, wherein the cavity includes at least one sidewall and a bottom surface. The plurality of lower density interconnect structures of the first microelectronic device and the plurality of lower density interconnect structures of the second microelectronic device may be
 30 electrically attached to the first surface of the microelectronic substrate, wherein the microelectronic bridge extends into the microelectronic substrate cavity, as set forth in block 308.

FIG. 18 illustrates a computing device 400 in accordance with one implementation of the present description. The computing device 400 houses a board 402. The board may include a
 35 number of microelectronic components, including but not limited to a processor 404, at least one

communication chip 406A, 406B, volatile memory 408, (e.g., DRAM), non-volatile memory 410 (e.g., ROM), flash memory 412, a graphics processor or CPU 414, a digital signal processor (not shown), a crypto processor (not shown), a chipset 416, an antenna, a display (touchscreen display), a touchscreen controller, a battery, an audio codec (not shown), a video codec (not shown), a power amplifier (AMP), a global positioning system (GPS) device, a compass, an accelerometer (not shown), a gyroscope (not shown), a speaker (not shown), a camera, and a mass storage device (not shown) (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the microelectronic components may be physically and electrically coupled to the board 402. In some implementations, at least one of the microelectronic components may be a part of the processor 404.

The communication chips 406A, 406B enable wireless communications for the transfer of data to and from the computing device 400. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 306 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 400 may include a plurality of communication chips 406A, 406B. For instance, a first communication chip 406A may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 406B may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

Any of the microelectronic components within the computing device 400 may include microelectronic devices connected to one another with a microelectronic bridge embedded in a microelectronic substrate formed in accordance with implementations described above.

In various implementations, the computing device 400 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital

video recorder. In further implementations, the computing device 400 may be any other electronic device that processes data.

It is understood that the subject matter of the present description is not necessarily limited to specific applications illustrated in FIGs. 1-18. The subject matter may be applied to other microelectronic devices and assembly applications, as well as any appropriate electronic application, as will be understood to those skilled in the art.

The following examples pertain to further embodiments. Specifics in the examples may be used anywhere in one or more embodiments.

In Example 1, a method of forming a microelectronic structure may comprise forming a first and a second microelectronic device, wherein each of the first and the second microelectronic device include a plurality of high density interconnect structures and a plurality of lower density interconnect structures on an active surface thereof; attaching a microelectronic bridge to the plurality of high density interconnect structures of the first microelectronic device and to the plurality of high density interconnect structures of the second microelectronic device; forming a microelectronic substrate having a cavity defined therein extending from a first surface of the microelectronic substrate, wherein the cavity includes at least one sidewall and a bottom surface; and electrically attaching the plurality of lower density interconnect structures of the first microelectronic device and the plurality of lower density interconnect structures of the second microelectronic device to the first surface of the microelectronic substrate, wherein the microelectronic bridge extends into the microelectronic substrate cavity.

In Example 2, the subject matter of Example 1 can optionally include the microelectronic bridge electrically connects the first microelectronic device and the second microelectronic device.

In Example 3, the subject matter of Example 1 can optionally include the microelectronic bridge includes a plurality of conductive routes therein.

In Example 4, the subject matter of Example 1 can optionally include the microelectronic bridge includes at least one microelectronic device embedded therein.

In Example 5, the subject matter of Example 1 can optionally include disposing an underfill material between the first microelectronic device active surface and the microelectronic substrate first surface, between the second microelectronic device active surface and the microelectronic substrate first surface, and within the microelectronic substrate cavity.

In Example 6, the subject matter of any of Examples 1 to 5 can optionally include forming a reconstituted wafer from the first microelectronic device and the second microelectronic device prior to attaching the microelectronic bridge.

In Example 7, the subject matter of Example 6 can optionally include forming the

reconstituted wafer comprising disposing an encapsulant material between at least one side of the first microelectronic device and at least one side of the second microelectronic device.

In Example 8, the subject matter of Example 7 can optionally include aligning the first microelectronic device and the second microelectronic device on a carrier with the active surface of each of the first microelectronic device and the second device facing the carrier; and wherein disposing the encapsulant material comprises disposing the encapsulant material over a back surface of the first microelectronic device and a back surface of the second microelectronic device.

In Example 9, the subject matter of Example 8 can optionally include aligning the first microelectronic device and the second microelectronic device on the carrier further comprises adhering the first microelectronic device and the second microelectronic device to the carrier with an adhesive layer.

In Example 10, the subject matter of Example 8 can optionally include removing a portion of the encapsulant material to expose the back surface of the first microelectronic device and the back surface of the second microelectronic device.

In Example 11, the subject matter of Example 10 can optionally include removing a portion of the first microelectronic device and the second microelectronic device.

In Example 12, the subject matter of any of Examples 1 to 5 can optionally include attaching the microelectronic bridge to the plurality of high density interconnect structures of the first microelectronic device and to the plurality of high density interconnect structures of the second microelectronic device comprises aligning a back surface of each of the first microelectronic device and the second microelectronic device on a carrier and attaching the microelectronic bridge.

In Example 13, the subject matter of Example 12 can optionally include disposing a flux material on the plurality of high density interconnect surface of the first microelectronic device and on the plurality of high density interconnect surface of the second microelectronic device; and attaching the microelectronic bridge through the flux material.

In Example 14, a microelectronic structure may comprise forming a first and a second microelectronic device, wherein each of the first and the second microelectronic device include a plurality of high density interconnect structures and a plurality of lower density interconnect structures on an active surface thereof; a microelectronic bridge attached to the plurality of high density interconnect structures of the first microelectronic device and to the plurality of high density interconnect structures of the second microelectronic device; a microelectronic substrate having a cavity defined therein extending from a first surface of the microelectronic substrate, wherein the cavity includes at least one sidewall and a bottom surface, wherein the plurality of

lower density interconnect structures of the first microelectronic device and the plurality of lower density interconnect structures of the second microelectronic device are electrically attached to the first surface of the microelectronic substrate, and wherein the microelectronic bridge extends into the microelectronic substrate cavity; and an underfill material between the first

5 microelectronic device active surface and the microelectronic substrate first surface, between the second microelectronic device active surface and the microelectronic substrate first surface, and within the microelectronic substrate cavity.

In Example 15, the subject matter of Example 14 can optionally include the microelectronic bridge electrically connecting the first microelectronic device and the second
10 microelectronic device.

In Example 16, the subject matter of Example 14 can optionally include the microelectronic bridge including a plurality of conductive routes therein.

In Example 17, the subject matter of Example 14 can optionally include the microelectronic bridge including at least one microelectronic device embedded therein.

15 In Example 18, the subject matter of any of Examples 14 to 17 can optionally include a reconstituted wafer formed from the first microelectronic device and the second microelectronic device.

In Example 19, the subject matter of Example 18 can optionally include the reconstituted wafer including an encapsulant material between at least one side of the first microelectronic
20 device and at least one side of the second microelectronic device.

In Example 20, the subject matter of Example 14 can optionally include a flux material disposed between the first microelectronic device and the microelectronic bridge, and between on the second microelectronic device and the microelectronic bridge.

In Example 21, a computing device may comprise a board and a microelectronic structure
25 attached to the board, wherein the microelectronic structure comprises a first and a second microelectronic device, wherein each of the first and the second microelectronic device include a plurality of high density interconnect structures and a plurality of lower density interconnect structures on an active surface thereof; a microelectronic bridge attached to the plurality of high density interconnect structures of the first microelectronic device and to the plurality of high
30 density interconnect structures of the second microelectronic device; a microelectronic substrate having a cavity defined therein extending from a first surface of the microelectronic substrate, wherein the cavity includes at least one sidewall and a bottom surface, wherein the plurality of lower density interconnect structures of the first microelectronic device and the plurality of lower density interconnect structures of the second microelectronic device are electrically attached to
35 the first surface of the microelectronic substrate, and wherein the microelectronic bridge extends

into the microelectronic substrate cavity; and an underfill material between the first microelectronic device active surface and the microelectronic substrate first surface, between the second microelectronic device active surface and the microelectronic substrate first surface, and within the microelectronic substrate cavity.

5 In Example 22, the subject matter of Example 21 can optionally include the microelectronic bridge electrically connecting the first microelectronic device and the second microelectronic device.

 In Example 23, the subject matter of Example 21 can optionally include the microelectronic bridge including a plurality of conductive routes therein.

10 In Example 24, the subject matter of Example 21 can optionally include the microelectronic bridge including at least one microelectronic device embedded therein.

 In Example 25, the subject matter of any of Examples 21 to 24 can optionally include a reconstituted wafer formed from the first microelectronic device and the second microelectronic device.

15 In Example 26, the subject matter of Example 25 can optionally include the reconstituted wafer including an encapsulant material between at least one side of the first microelectronic device and at least one side of the second microelectronic device.

 In Example 27, the subject matter of Example 21 can optionally include a flux material disposed between the first microelectronic device and the microelectronic bridge, and between
20 on the second microelectronic device and the microelectronic bridge.

 Having thus described in detail embodiments of the present description, it is understood that the present description defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A method of forming a microelectronic structure, comprising:

forming a first and a second microelectronic device, wherein each of the first and the
5 second microelectronic device include a plurality of high density interconnect structures and a plurality of lower density interconnect structures on an active surface thereof;

attaching a microelectronic bridge to the plurality of high density interconnect structures of the first microelectronic device and to the plurality of high density interconnect structures of the second microelectronic device;

10 forming a microelectronic substrate having a cavity defined therein extending from a first surface of the microelectronic substrate, wherein the cavity includes at least one sidewall and a bottom surface; and

electrically attaching the plurality of lower density interconnect structures of the first microelectronic device and the plurality of lower density interconnect structures of the second
15 microelectronic device to the first surface of the microelectronic substrate, wherein the microelectronic bridge extends into the microelectronic substrate cavity.

2. The method of claim 1, wherein the microelectronic bridge electrically connects the first microelectronic device and the second microelectronic device.

3. The method of claim 1, wherein the microelectronic bridge includes a plurality of conductive routes therein.

4. The method of claim 1, wherein the microelectronic bridge includes at least one
25 microelectronic device embedded therein.

5. The method of claim 1, further including disposing an underfill material between the first microelectronic device active surface and the microelectronic substrate first surface, between the second microelectronic device active surface and the microelectronic substrate first
30 surface, and within the microelectronic substrate cavity.

6. The method of any of claims 1 to 5, further comprising forming a reconstituted wafer from the first microelectronic device and the second microelectronic device prior to attaching the microelectronic bridge.

7. The method of claim 6, wherein forming the reconstituted wafer comprises disposing an encapsulant material between at least one side of the first microelectronic device and at least one side of the second microelectronic device.

5 8. The method of claim 7, further including aligning the first microelectronic device and the second microelectronic device on a carrier with the active surface of each of the first microelectronic device and the second device facing the carrier; and wherein disposing the encapsulant material comprises disposing the encapsulant material over a back surface of the first microelectronic device and a back surface of the second microelectronic device.

10 9. The method of claim 8, wherein aligning the first microelectronic device and the second microelectronic device on the carrier further comprises adhering the first microelectronic device and the second microelectronic device to the carrier with an adhesive layer.

15 10. The method of claim 8, further comprising removing a portion of the encapsulant material to expose the back surface of the first microelectronic device and the back surface of the second microelectronic device.

20 11. The method of claim 10, further comprising removing a portion of the in the first microelectronic device and the second microelectronic device.

25 12. The method of any of claims 1-5, wherein attaching the microelectronic bridge to the plurality of high density interconnect structures of the first microelectronic device and to the plurality of high density interconnect structures of the second microelectronic device comprises aligning a back surface of each of the first microelectronic device and the second microelectronic device on a carrier and attaching the microelectronic bridge.

30 13. The method of claim 12, further comprising disposing a flux material on the plurality of high density interconnect surface of the first microelectronic device and on the plurality of high density interconnect surface of the second microelectronic device; and attaching the microelectronic bridge through the flux material.

35 14. A microelectronic structure comprising:
a first and a second microelectronic device, wherein each of the first and the second microelectronic device include a plurality of high density interconnect structures and a plurality

of lower density interconnect structures on an active surface thereof;

a microelectronic bridge attached to the plurality of high density interconnect structures of the first microelectronic device and to the plurality of high density interconnect structures of the second microelectronic device;

5 a microelectronic substrate having a cavity defined therein extending from a first surface of the microelectronic substrate, wherein the cavity includes at least one sidewall and a bottom surface, wherein the plurality of lower density interconnect structures of the first microelectronic device and the plurality of lower density interconnect structures of the second microelectronic device are electrically attached to the first surface of the microelectronic substrate, and wherein
10 the microelectronic bridge extends into the microelectronic substrate cavity; and

an underfill material between the first microelectronic device active surface and the microelectronic substrate first surface, between the second microelectronic device active surface and the microelectronic substrate first surface, and within the microelectronic substrate cavity.

15 15. The microelectronic structure of claim 14, wherein the microelectronic bridge electrically connects the first microelectronic device and the second microelectronic device.

16. The microelectronic structure of claim 14, wherein the microelectronic bridge includes a plurality of conductive routes therein.

20 17. The microelectronic structure of claim 14, wherein the microelectronic bridge includes at least one microelectronic device embedded therein.

18. The microelectronic structure of any of claims 14 to 17, further comprising a
25 reconstituted wafer formed from the first microelectronic device and the second microelectronic device.

19. The microelectronic structure of claim 18, wherein the reconstituted wafer includes an encapsulant material between at least one side of the first microelectronic device and
30 at least one side of the second microelectronic device.

20. The microelectronic structure of claim 14, further comprising a flux material disposed between the first microelectronic device and the microelectronic bridge, and between
on the second microelectronic device and the microelectronic bridge.

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21. A computing device, comprising:

a board;

a microelectronic structure attached to the board, wherein the microelectronic structure comprises:

5 a first and a second microelectronic device, wherein each of the first and the second microelectronic device include a plurality of high density interconnect structures and a plurality of lower density interconnect structures on an active surface thereof;

a microelectronic bridge attached to the plurality of high density interconnect structures of the first microelectronic device and to the plurality of high density interconnect structures of
10 the second microelectronic device;

a microelectronic substrate having a cavity defined therein extending from a first surface of the microelectronic substrate, wherein the cavity includes at least one sidewall and a bottom surface, wherein the plurality of lower density interconnect structures of the first microelectronic device and the plurality of lower density interconnect structures of the second microelectronic
15 device are electrically attached to the first surface of the microelectronic substrate, and wherein the microelectronic bridge extends into the microelectronic substrate cavity; and

an underfill material between the first microelectronic device active surface and the microelectronic substrate first surface, between the second microelectronic device active surface and the microelectronic substrate first surface, and within the microelectronic substrate cavity.

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22. The computing device of claim 21, wherein the microelectronic bridge electrically connects the first microelectronic device and the second microelectronic device.

23. The computing device of any of claims 21 to 22, further comprising a
25 reconstituted wafer formed from the first microelectronic device and the second microelectronic device.

24. The computing device of claim 23, wherein the reconstituted wafer includes an encapsulant material between at least one side of the first microelectronic device and at least one
30 side of the second microelectronic device.

25. The computing device of claim 21, further comprising a flux material disposed between the first microelectronic device and the microelectronic bridge, and between on the second microelectronic device and the microelectronic bridge.

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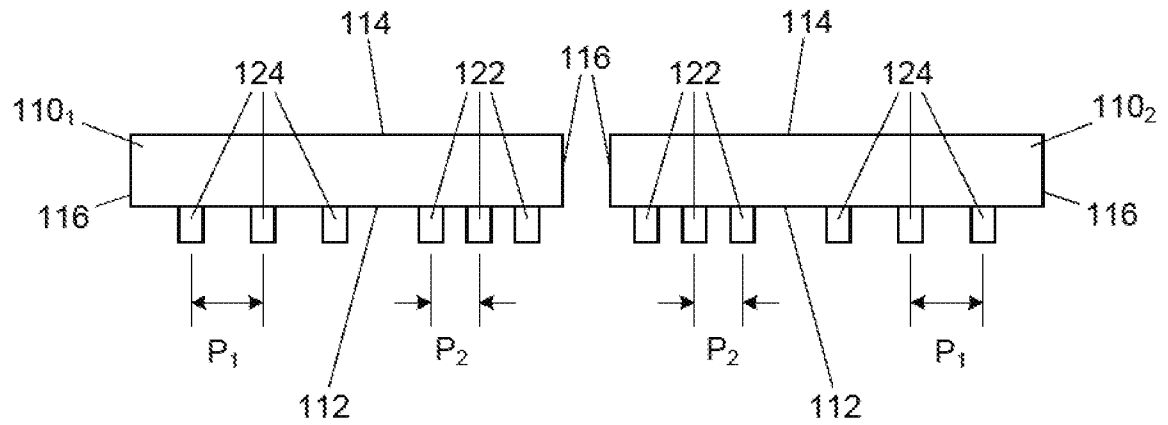


FIG. 1

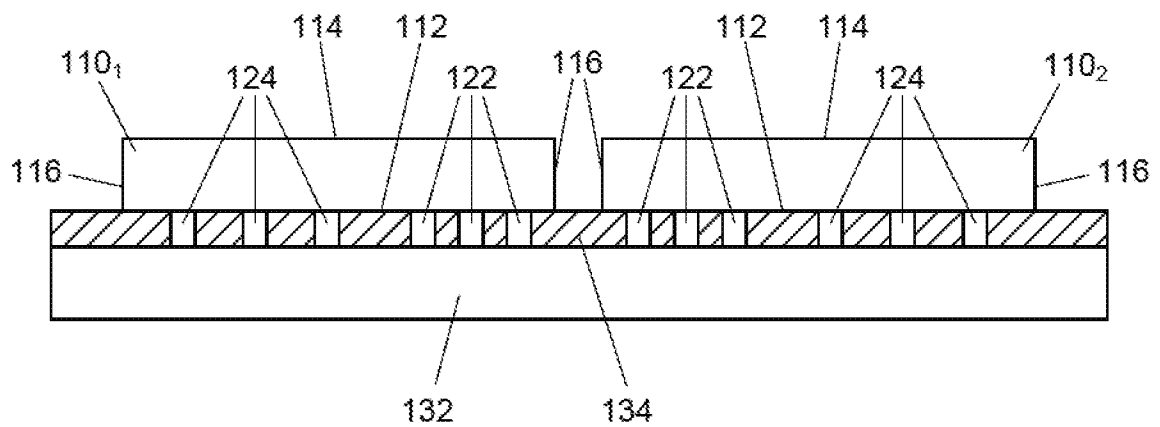


FIG. 2

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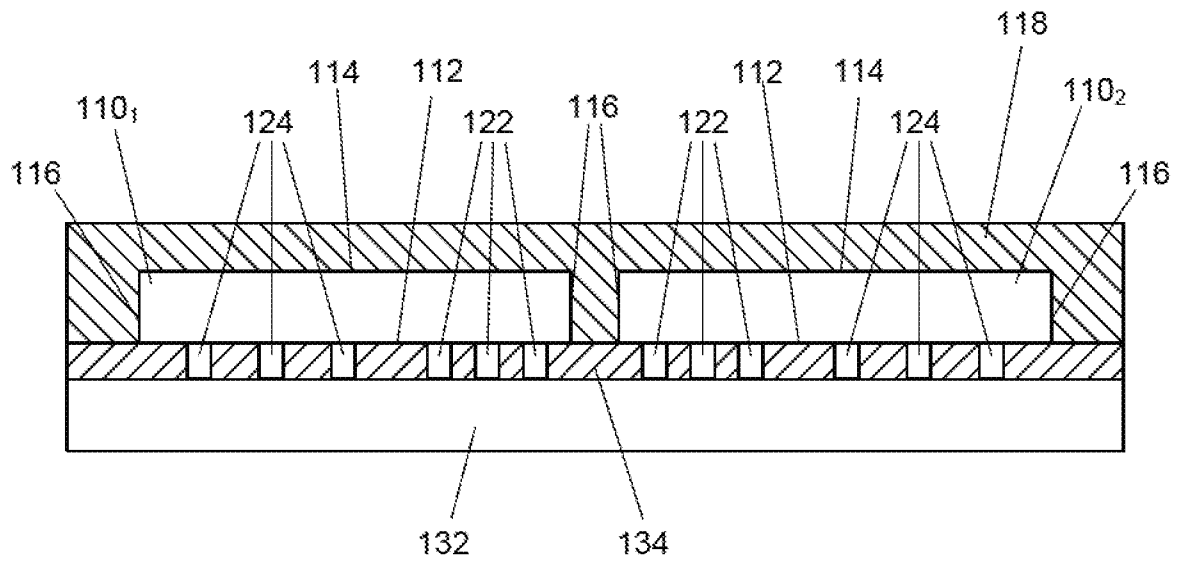


FIG. 3

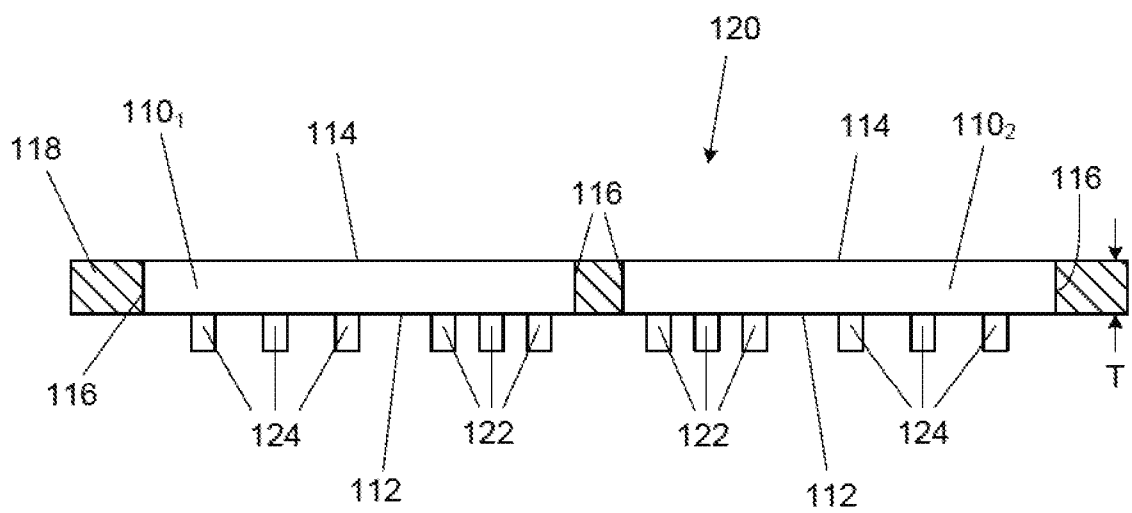


FIG. 4

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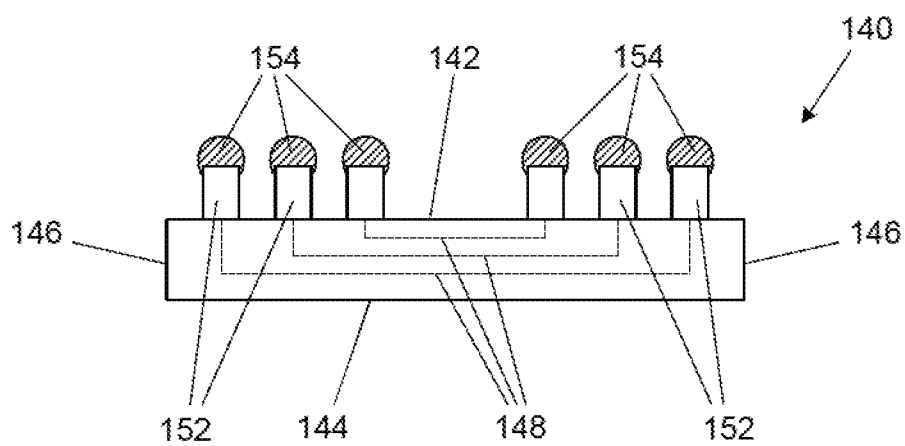


FIG. 5

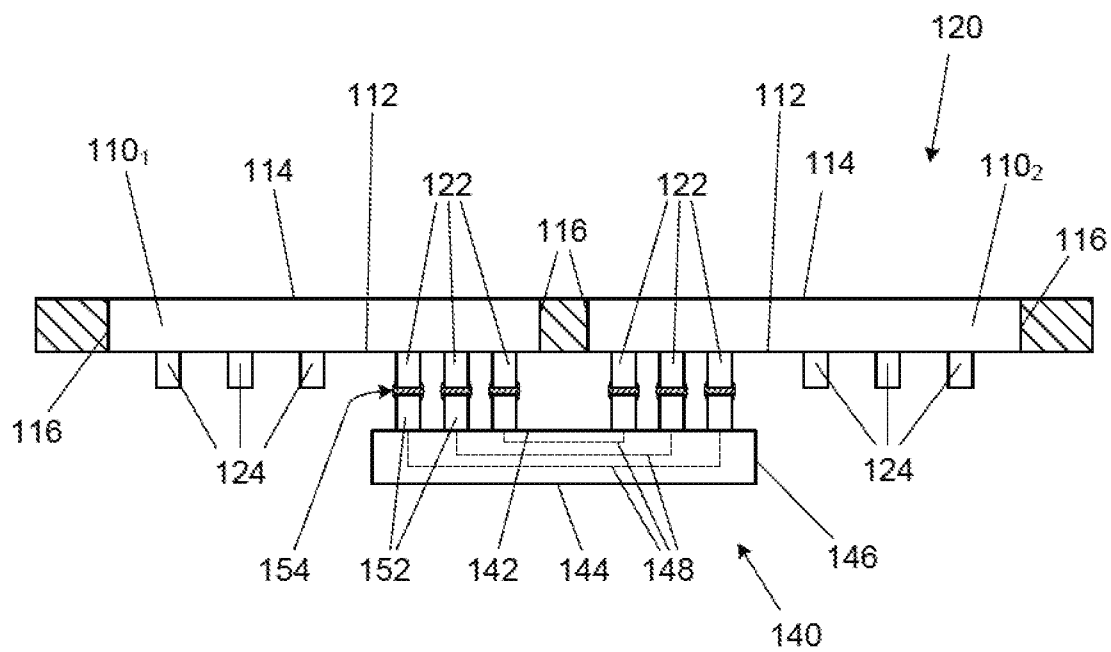


FIG. 6

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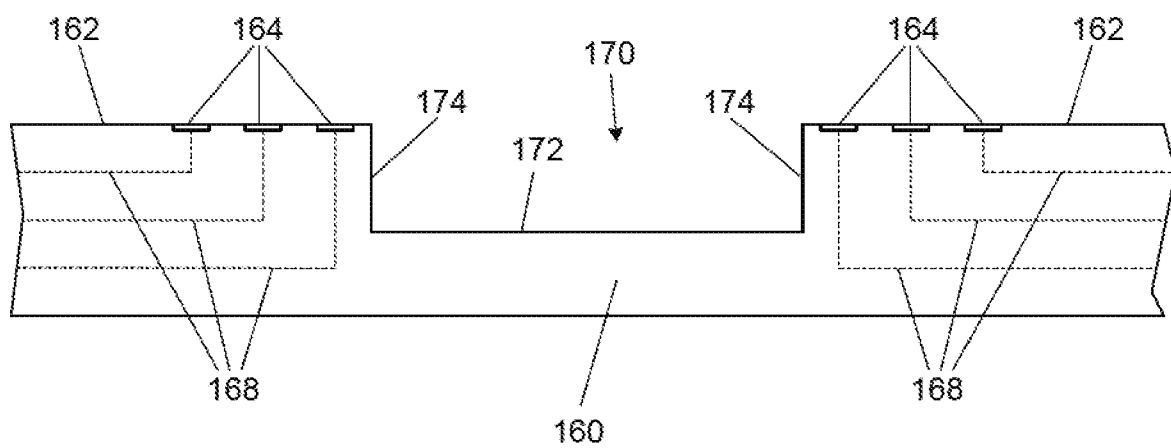


FIG. 7

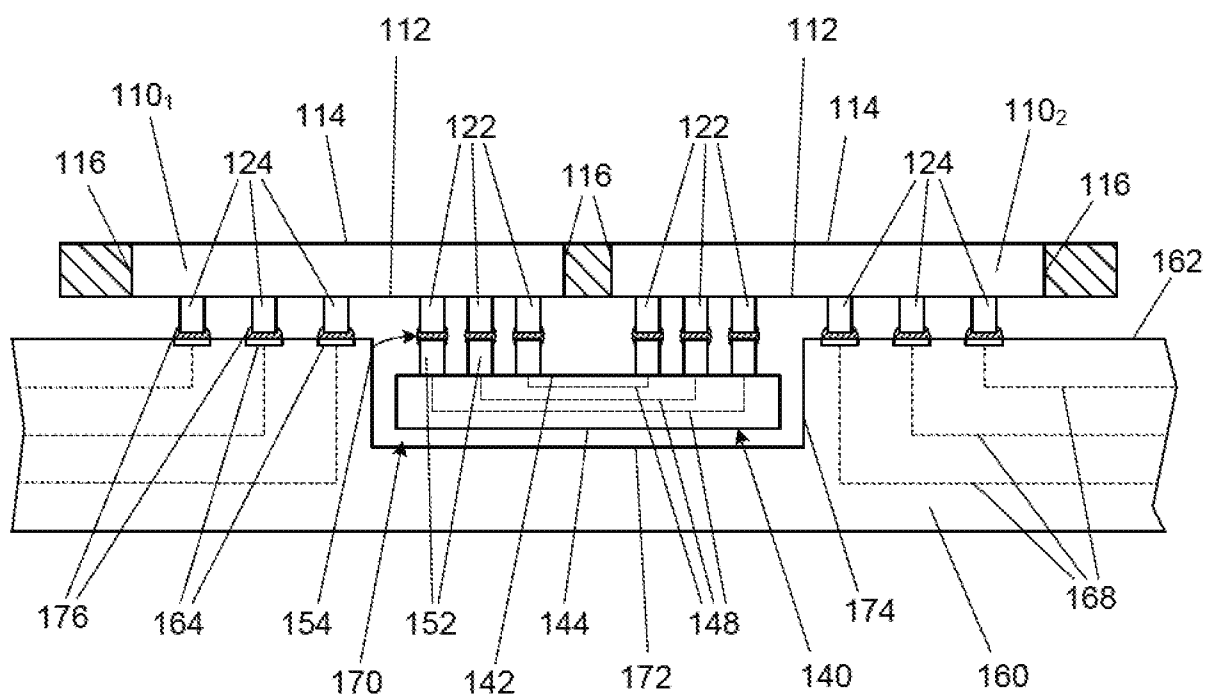


FIG. 8

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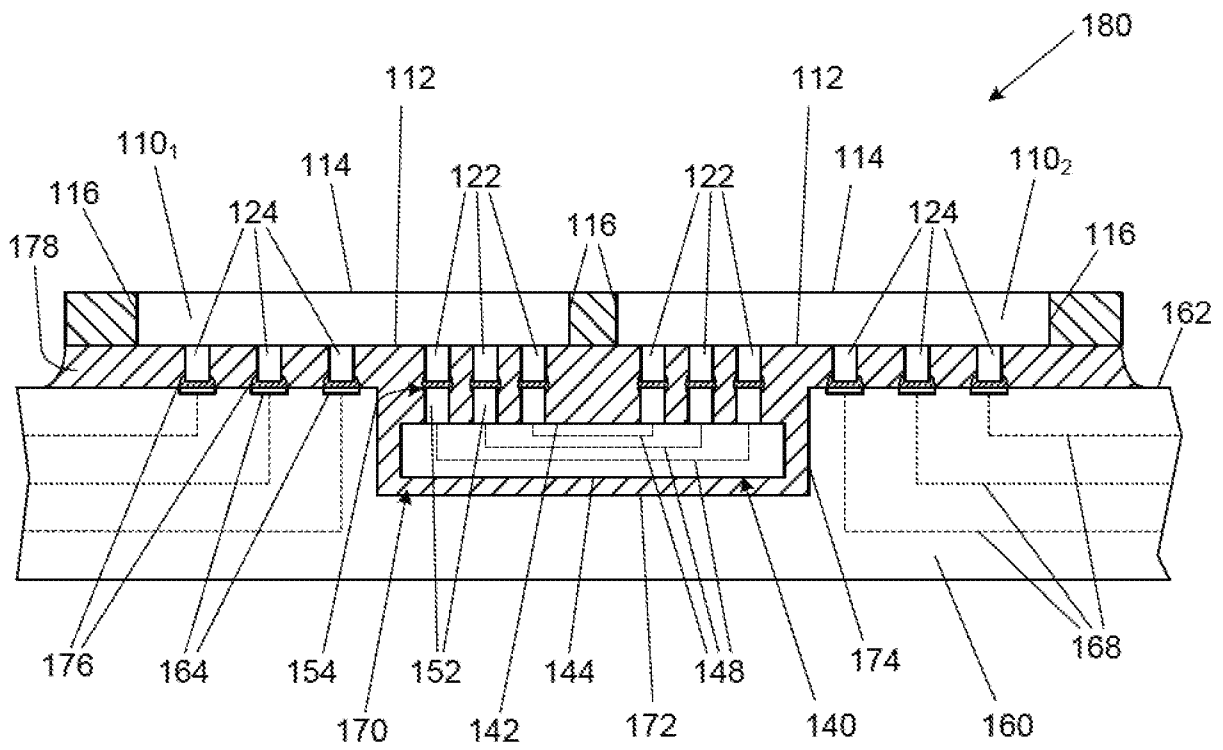


FIG. 9

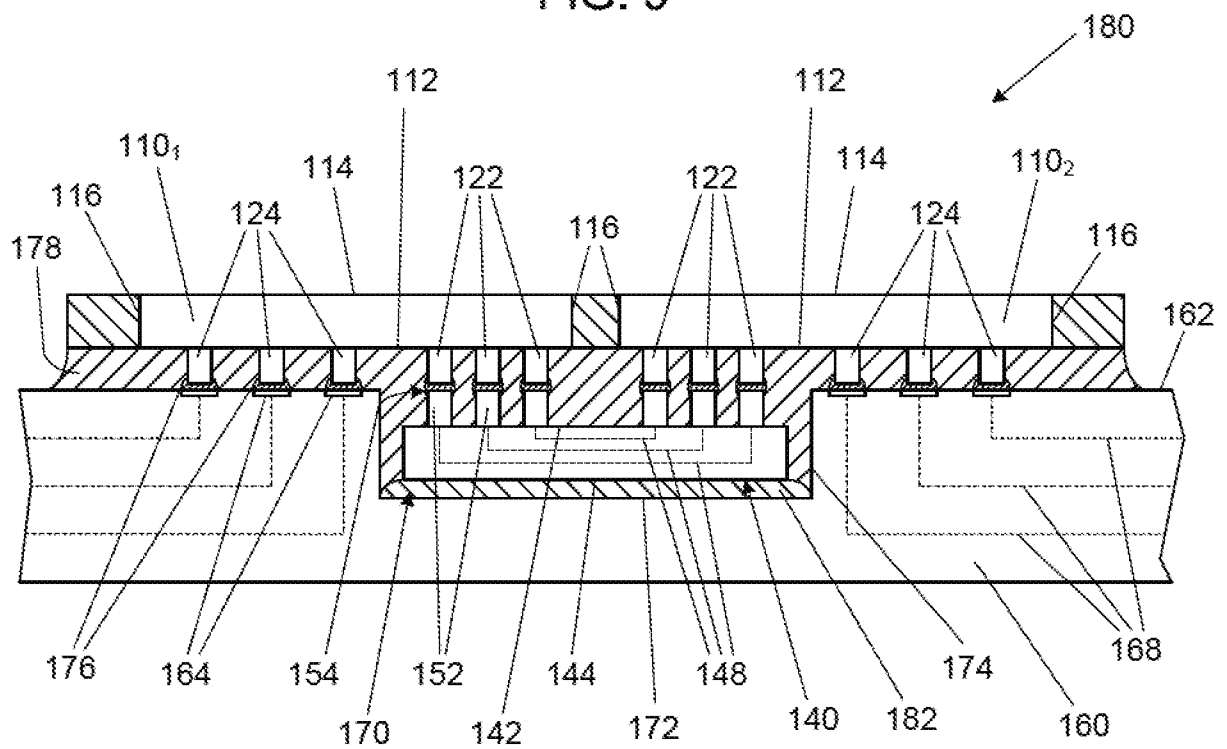


FIG. 10



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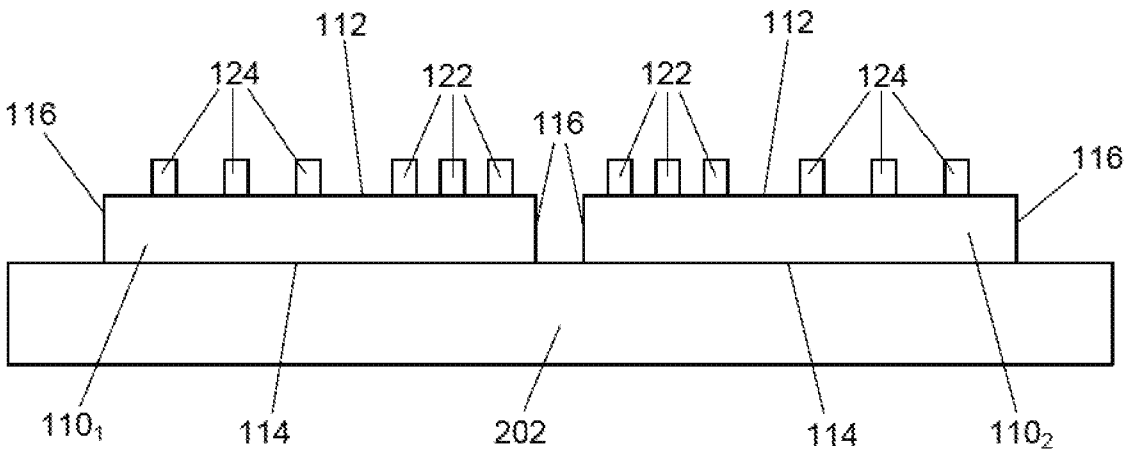


FIG. 11

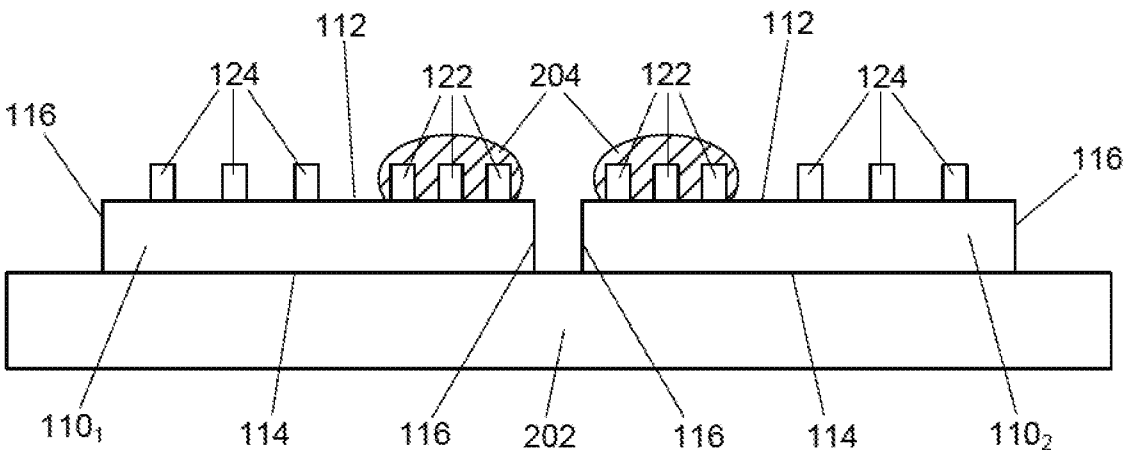


FIG. 12

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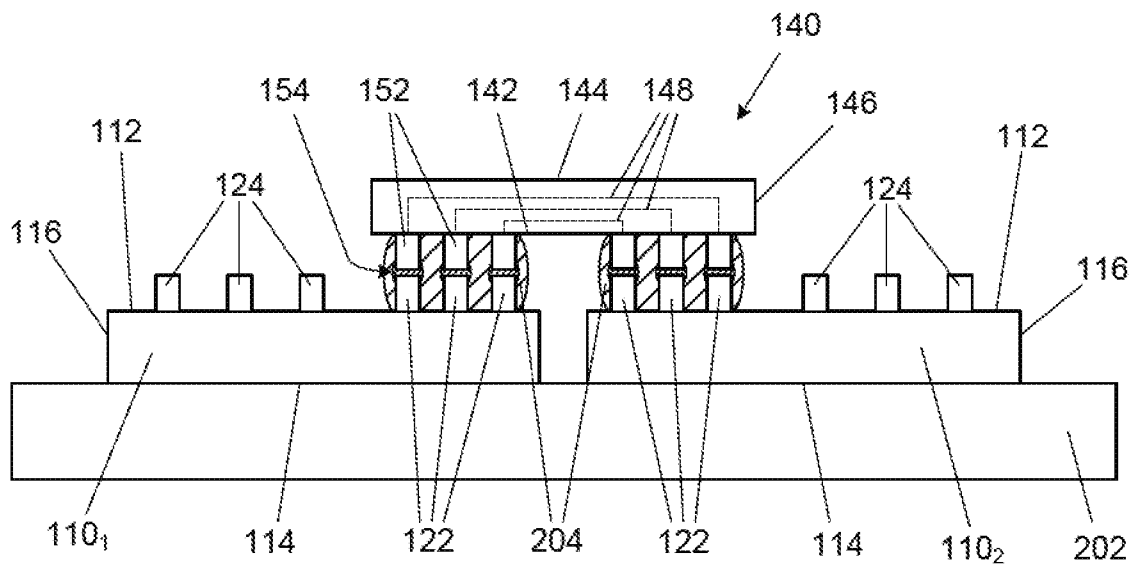


FIG. 13

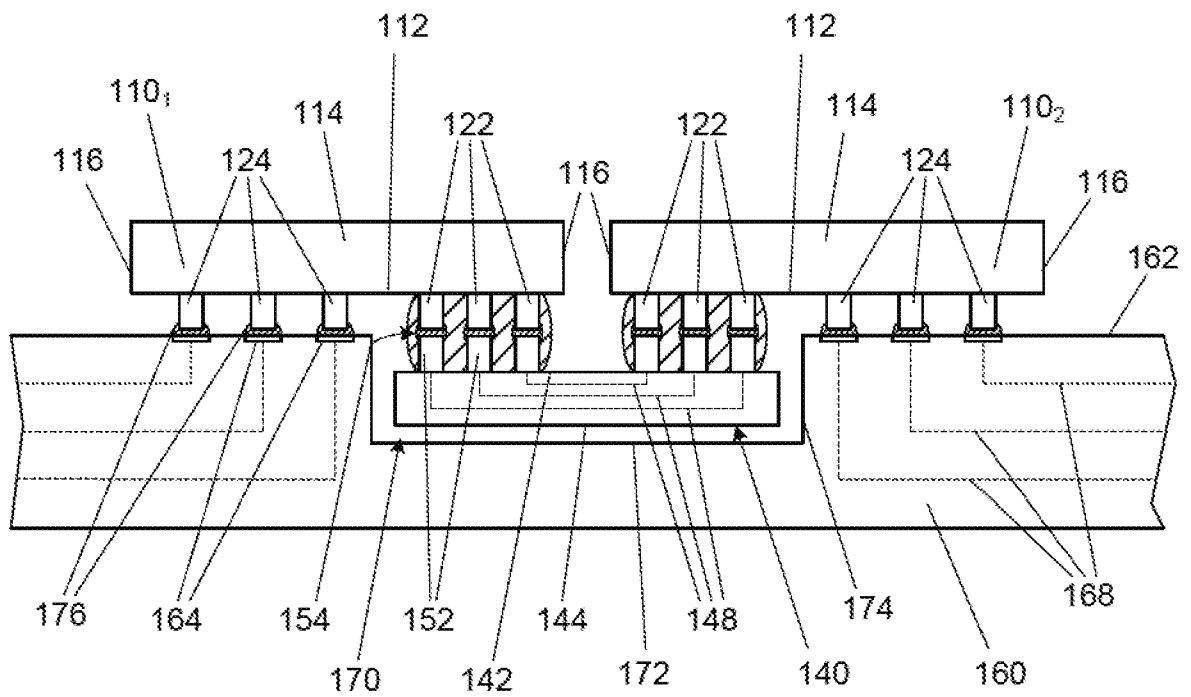


FIG. 14

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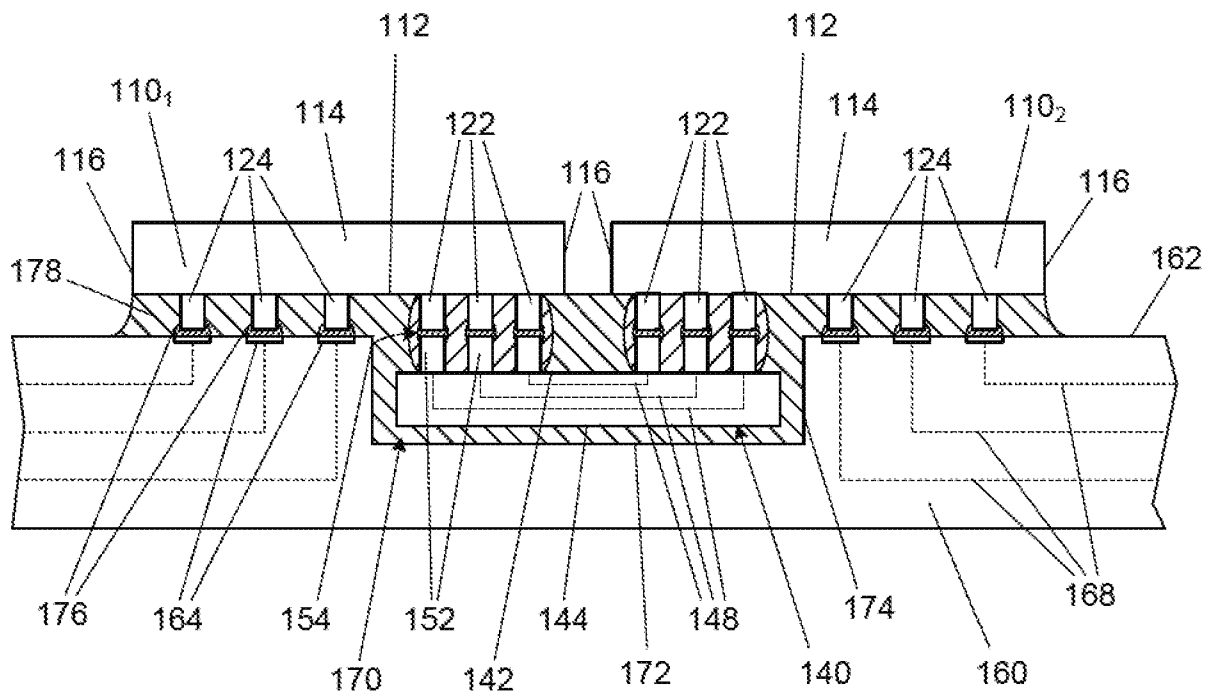


FIG. 15

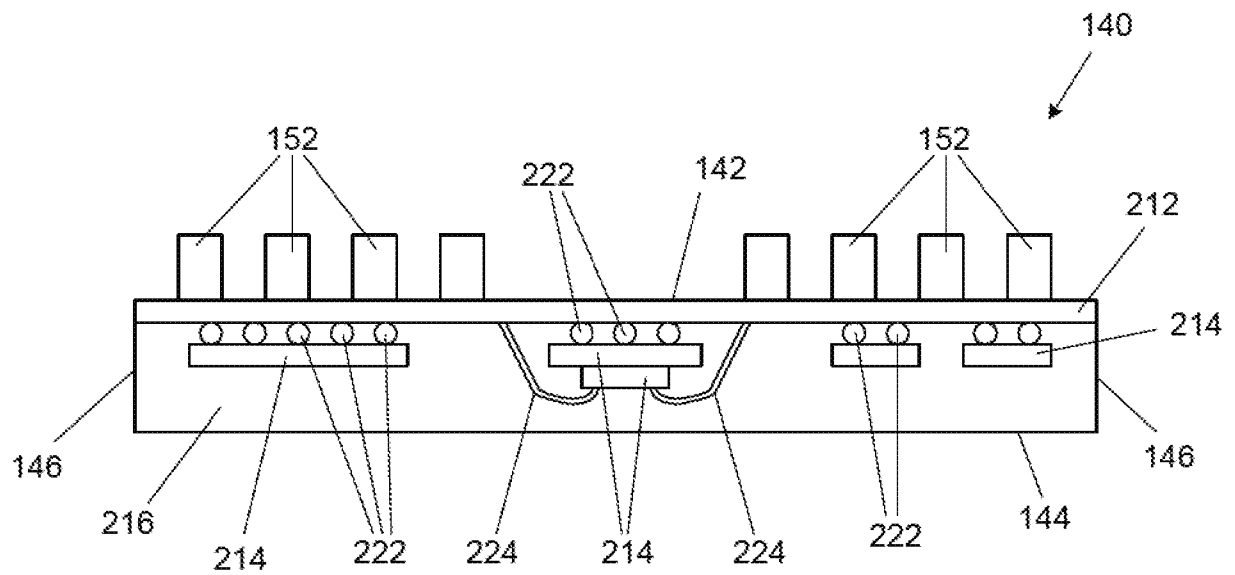


FIG. 16

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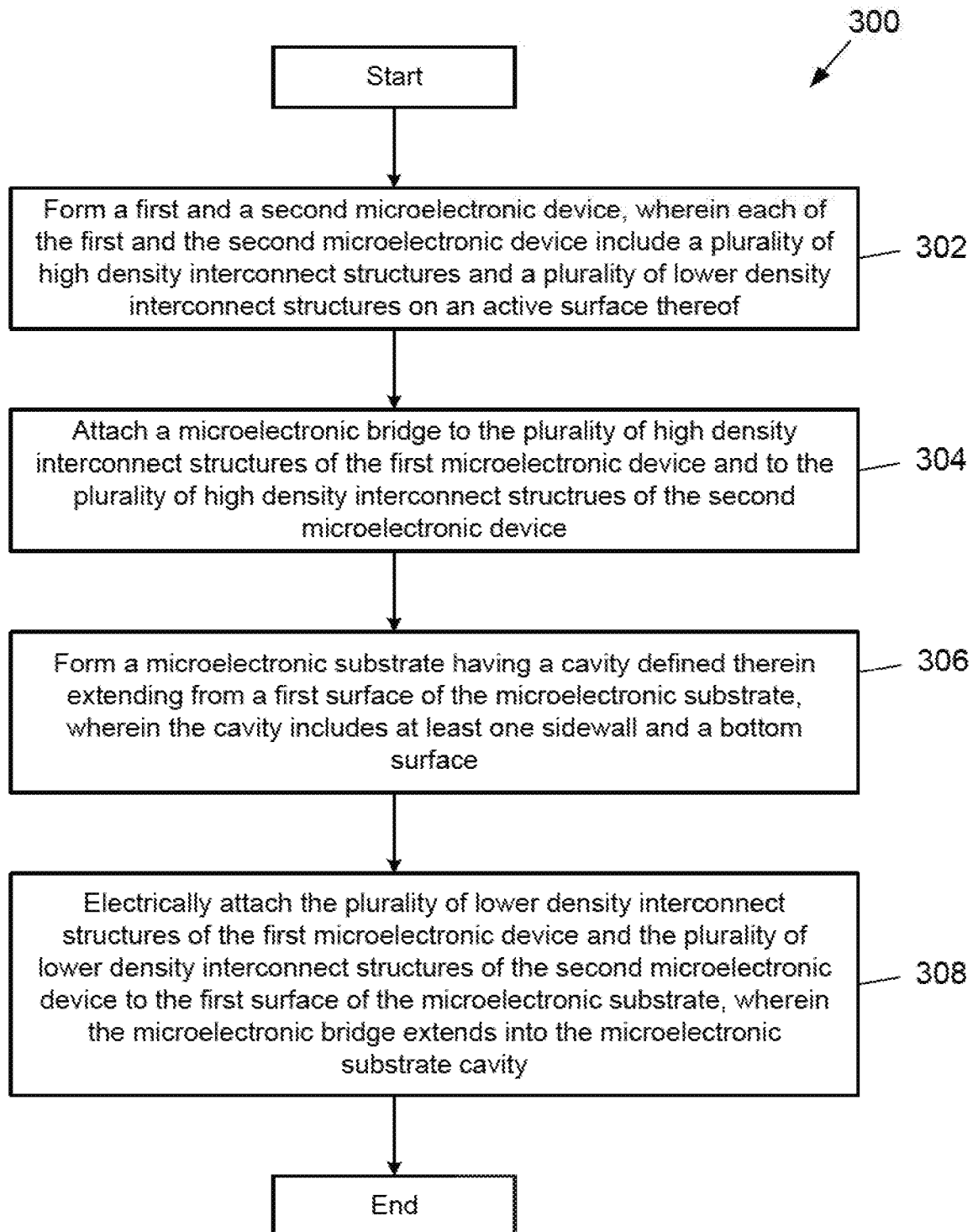


FIG. 17

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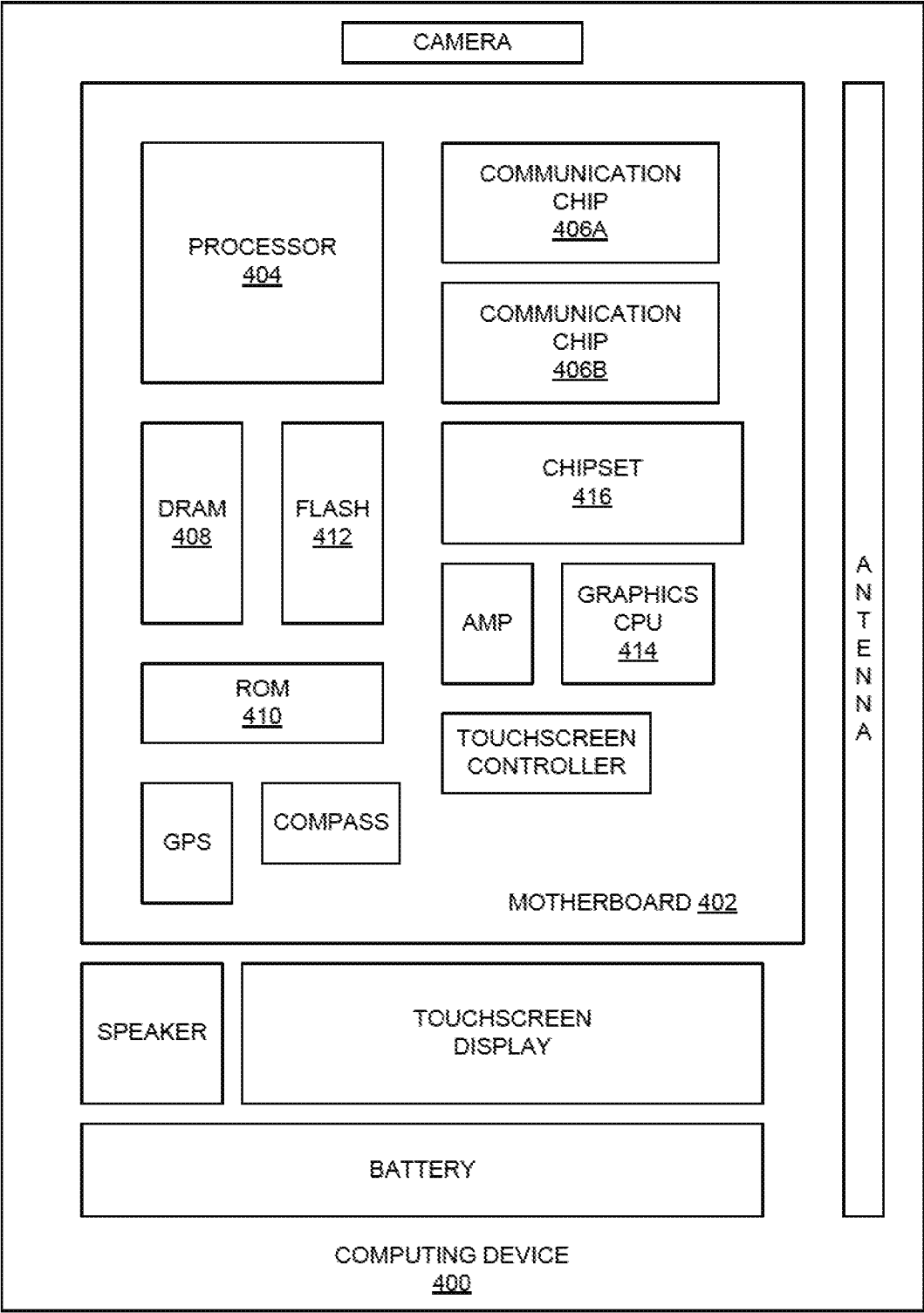


FIG. 18



A. CLASSIFICATION OF SUBJECT MATTER**H01L 25/065(2006.01)i, H01L 23/48(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 25/065; H01L 21/60; H01L 21/768; H01L 23/00; H01L 23/48; H01L 23/498; H01L 23/522; H05K 1/03; H01L 25/07

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: bridge, interconnect, cavity, density, package

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012-0261838 A1 (BRAUNISCH HENNING et al.) 18 October 2012 See abstract, paragraphs [0036]-[0057] and figures 4-9.	1-6, 12-18, 20-23, 25
A		7-11, 19, 24
A	US 2014-0174807 A1 (MIHIR K. ROY et al.) 26 June 2014 See abstract, claim 1 and figure 3.	1-25
A	US 2014-0264791 A1 (MATHEW J. MANUSHAROW et al.) 18 September 2014 See abstract, claim 1 and figure 1.	1-25
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A	KR 10-2014-0060435 A (AMKOR TECHNOLOGY, INC.) 20 May 2014 See abstract, claim 1 and figure 2.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

17 August 2016 (17.08.2016)

Date of mailing of the international search report

18 August 2016 (18.08.2016)

Name and mailing address of the ISA/KR

International Application Division

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/065165

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