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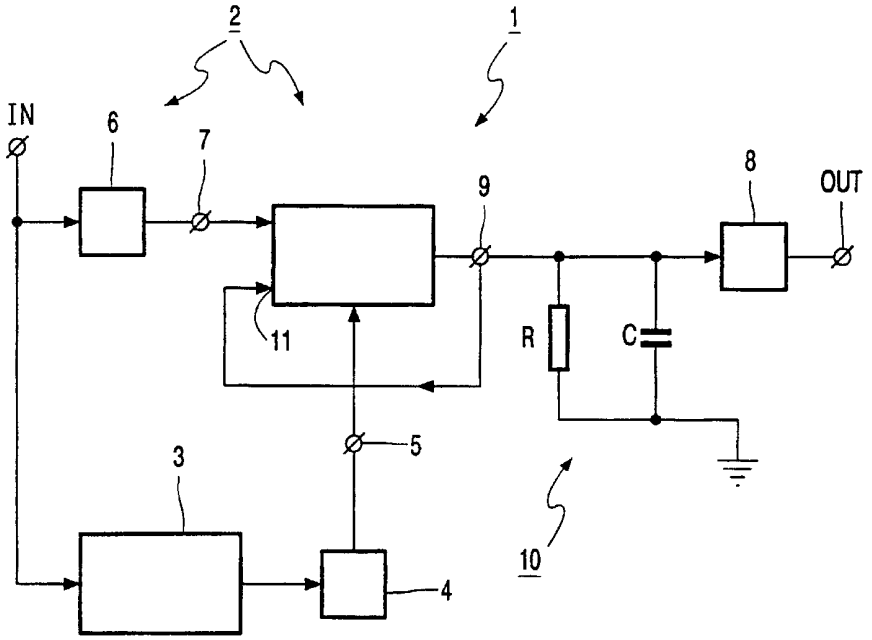
(54) Title: A MUTING CIRCUIT HAVING CONTROLLABLE IMPEDANCE MEANS FOR SOFT MUTING



(57) Abstract: A muting circuit for application in aN anti-distortion circuit or a receiver, such as a radio receiver comprises controllable impedance means for enabling passage of a signal by controlling the impedance between an input and an output in dependence on a muting control signal on a muting control terminal of the circuit. This solution provides for soft and improved muting without a distortion, which is self inflicted by the mute interruption.

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A muting circuit having controllable impedance means for soft muting.

The present invention relates to a muting circuit comprising a controllable passage means having an input, an output and a muting control terminal for enabling passage of a signal from the audio input to the output in dependence on a muting control signal on the muting control terminal.

The present invention also relates to an anti-distortion circuit, and/or a receiver, such as a radio receiver provided with such a muting circuit. These circuits are generally applied in radio reception devices, such as in cars e.g. for AM, SW, LW reception.

Such a muting circuit is known from WO 97/20387 and is provided with an audio input, an audio output and a muting control terminal. The known muting circuit comprises controllable passage means arranged as a pair of switchable antiparallel transistors, included in a differential amplifier, which transistors are switchable by means of a muting control signal on the muting control terminal. The muting circuit enables or disables passage by switching the pair of transistors. In particular the muting circuit controllably interrupts passage of the audio signal from the audio input to the audio output during a time interval, indicated by the muting control signal. The edges of the audio output signal interrupted by muting are rounded by the cosines-like behaviour of the conductance due to the switching of the pair of transistors.

It is a disadvantage of the known muting circuit that the switching itself gives rise to considerable spurious high harmonics and a rapidly changing amplitude of the interrupted audio signal, in particular where the interrupted audio output signal edge is around zero.

Therefore it is an object of the present invention to provide a muting circuit which does not in itself introduce distortion upon interruption of the signal during detection of interference.

Thereto the muting circuit according to the present invention is characterized in that the controllable passage means include controllable impedance means for enabling

passage by controlling the impedance between the input and the output in dependence on the muting control signal.

It is an advantage of the muting circuit according to the invention that the impedance control during a muting or blanking interval in the output signal provides for a soft mute without inflicting self introduced distortion or harmonics, in particular at the edges of mute periods of interruption in the signal. The after muting controlling to zero or to a constant value of the interrupted signal at the start of the muting interval may take a substantial part or even the full part of said interval, so that any abrupt changes during the whole of the interval are effectively avoided by the impedance control. This leads to a reduced self distortion during full mute periods of detected interference.

Furthermore it is an advantage that the muting circuit according to the invention is simple and provides a high performance/price ratio, improving the signal-to-distortion ratio with several Decibel for a large variety of signals.

One embodiment of the muting circuit according to the invention is characterized in that the muting circuit comprises a time constant network coupled to the audio output of the controllable impedance means.

Advantageously the time constant network provides for possibilities to influence the behaviour of the course of the interrupted signal within the whole muting of blanking interval.

Advantageously in a further embodiment of the invention the time constant network is an RC, an LC or a like simulated network. The time constant thereof may be adjustable at wish, but it is preferred in a further embodiment that the time constant of the time constant network amounts about half the duration of an interruption of the signal indicated by the muting control signal. This provides for an optimum, wherein the signal-to-distortion (SINAD) has improved approximately 1.8-2.2 dB compared to a conventional muting circuit. In a practical embodiment the time constant network has a time constant, which ranges between 0 and 500 μS, preferably 100-200 μS. The thereby further optimized SINAD is independent of the magnitude of the signal and independent of the repetition frequency of the blanking pulses.

In a still further embodiment the muting circuit according to the invention is provided with an anti-splatter filter, which is coupled to the output of the controllable impedance means. Such a anti-splatter filter, which is preferred to be embodied as a low pass filter filters out any possible remaining high frequency components or noise.

At present the muting/anti-distortion circuit according to the invention will be elucidated further together with its additional advantages while reference is being made to the appended drawing, wherein similar components are being referred to by means of the same reference numerals. In the drawing:

Fig. 1 shows an example of a possible embodiment of a muting circuit according to the invention; and

Fig. 2 shows possible effects of the application of the muting circuit of Fig. 1.

Fig. 1 shows a muting circuit 1, which is included in a anti-distortion circuit 2, which may be part of a receiver, such as a radio receiver. Such a receiver derives from a received signal a radio or data signal on a terminal IN of the circuit 2. Apart from the wanted audio signal the signal on terminal IN shows interference. In for example a car radio this interference or distortion is due to electrical disturbances emanating from e.g. on-board electronics, wind shield wipers, ignition spikes etc. The muting circuit 1 is used to mute or blank the audio input signal during periods of distortion or interference.

The anti-distortion circuit 2 as shown comprises an interference detection circuit 3 connected to the terminal IN, a pulse circuit 4 connected to the interference detection circuit 3 for generating a muting control signal in this case a pulse on a control terminal 5 of the muting circuit 1 during periods of detected interference. Interference in the audio signal on terminal IN may be detected with any suitable means. The muting circuit 1 is further provided with a delay circuit 6 connected between the terminal IN and an audio input 7 of the circuit 1 and in the embodiment as shown also with an anti-splatter filter 8 connected between an audio output 9 of the circuit 1 and a terminal OUT. The delay circuit 6 provides for a time delay between its input and output, which delay equals the time necessary for the interference detection circuit 3 and the pulse circuit 4 to intervene at a proper moment in time in the audio input signal after detection of an interference.

An example of possible effects realized with the muting circuit is given in fig. 2, which shows the audio signal amplitude on audio input 7 as a function of time. During a period referred to as I, interference is being detected by the circuit 3 and the start of the period I marks the start of the pulse on control terminal 5. The muting circuit 1 is arranged such that the passage of the distorted audio signal on audio input 7 to audio output 9 is

controlled by controlling the impedance and in particular the change of the impedance as a function of time. By doing so the course of the audio signal during the interference period I can be influenced. Possible courses are referred to by a, b, and c. Generally the audio signal amplitude at the end of the period I has to be allowed to gently return to some end amplitude, which may be zero or have some other value. For achieving specific courses the muting circuit 1 comprises a time constant network 10 coupled to the audio output 9 of the controllable impedance muting circuit 1. In particular fig. 2 shows a simple RC-circuit 10 having a capacitor C and a resistor R in parallel thereto. Appropriate choices of the capacity and resistance values will provide a possibly wanted first order course during interval I of the audio signal on output 9. Off course other types or higher order networks will provide alternative courses. These networks can also contain an LC network, or could be simulated or value adjusted by e.g. computer, gyrator or the like. The time constant network 10 may have a time constant, which ranges between 0 and 500 μS, preferably 100-200 μS.

For example the impedance control of the muting circuit 1 may be achieved by a controllable impedance (or conductance) amplifier having differential inputs 7, and in addition 11, the latter being connected to the output 9. Such an amplifier may be a current controlled amplifier, whereby the control current through muting control terminal 5 can then be supplied by the pulse circuit 4.

If the time constant of the time constant network 10 amounts about half the duration of an interruption period I of the audio signal, optimum signal-to-distortion values can be realized in practice. In an environment with many potential interference sources the anti-splatter filter 8 may be applied. This filter can be embodied as a simple low pass filter.

It is to be noticed that besides from the described audio application, the invention can be used much more generally. So also for all kinds of signals. The audio application has been described as an example.

CLAIMS:

1. A muting circuit comprising a controllable passage means having an input, an output and a muting control terminal for enabling passage of an signal from the input to the audio output in dependence on a muting control signal on the muting control terminal, characterized in that the controllable passage means include controllable impedance means for enabling passage by controlling the impedance between the input and the output in dependence on the muting control signal.

2. The muting circuit according to claim 1, characterized in that the muting circuit comprises a time constant network coupled to the output of the controllable impedance means.

3. The muting circuit according to claim 2, characterized in that the time constant network is an RC, an LC or a like simulated network.

4. The muting circuit according to claim 2 or 3, characterized in that the time constant network has a time constant, which is adjustable.

5. The muting circuit according to one of the claims 2-4, characterized in that the time constant of the time constant network amounts about half the duration of an interruption of the signal indicated by the muting control signal.

6. The muting circuit according to one of the claims 2-5, characterized in that the time constant network has a time constant, which ranges between 0 and 500 μS, preferably 100-200 μS.

7. The muting circuit according to one of the claims 1-6, characterized in that the muting circuit is provided with an anti-splatter filter, which is coupled to the output of the controllable impedance means.

8. The muting circuit according to claims 7, characterized in that the anti-splatter filter is embodied as a low pass filter.

9. Anti-distortion circuit provided with a muting circuit according to one of the claims 1-8.

10. Receiver, such as a radio receiver, provided with an anti-distortion circuit according to claim 9, or a muting circuit according to one of the claims 1-8.

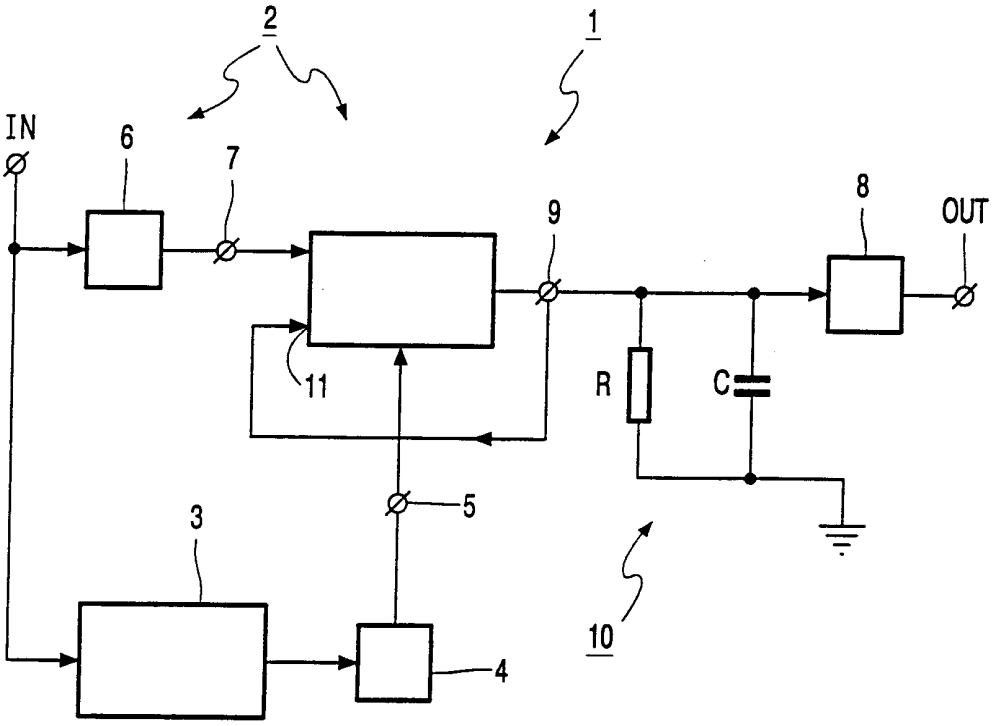

FIG. 1

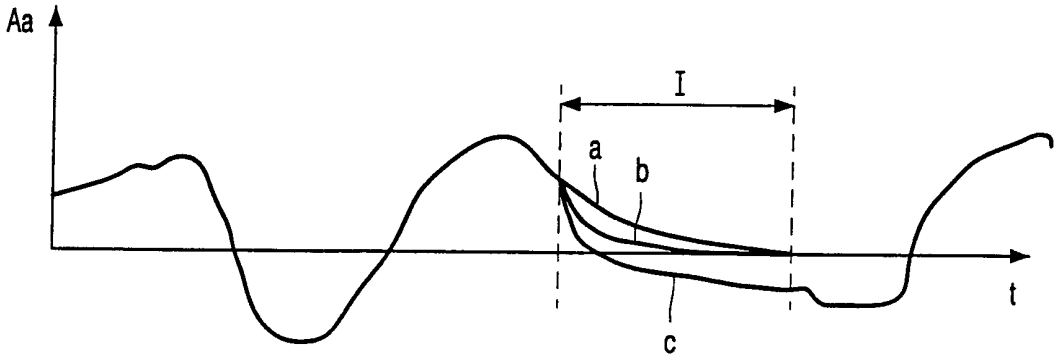

FIG. 2

INTERNATIONAL SEARCH REPORT

Inter ›nal Application No
PCT/EP 00/05914

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03G3/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 915 030 A (VIEBACH MICHAEL) 22 June 1999 (1999-06-22) column 2, line 223 -column 38	1-4,6,10
A	US 4 060 764 A (ANDREWS JAMES EDWARD ET AL) 29 November 1977 (1977-11-29) column 5, line 49 -column 6, line 22	1,7,8
A	US 4 466 129 A (SKUTTA FRANK R) 14 August 1984 (1984-08-14) column 4, line 12 -column 5, line 10	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 October 2000	02/11/2000

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter nal Application No
PCT/EP 00/05914

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5915030 A	22-06-1999	DE 19630395 C	02-10-1997
		EP 0821478 A	28-01-1998
US 4060764 A	29-11-1977	BR 7701665 A	24-01-1978
		CA 1072638 A	26-02-1980
		DE 2709575 A	29-09-1977
		GB 1521651 A	16-08-1978
		IT 1082689 B	21-05-1985
		JP 1093142 C	16-04-1982
		JP 52117014 A	01-10-1977
		JP 56032811 B	30-07-1981
		MX 142977 A	28-01-1981
US 4466129 A	14-08-1984	NONE	