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E. A. MEYER
TRANSISTOR DESIGN
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2,651,009

Fig. 1.

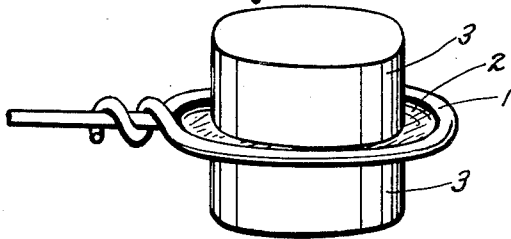


Fig. 2.

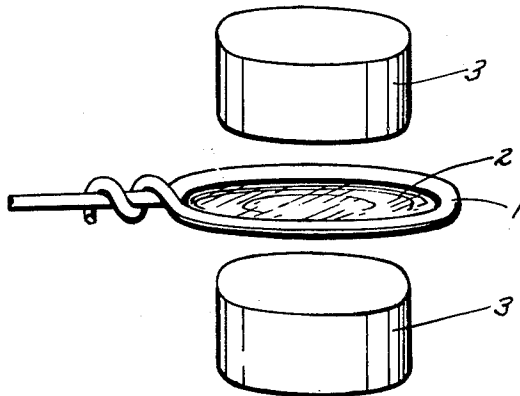
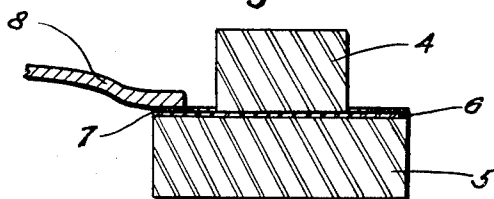


Fig. 3.



INVENTOR.
EARL A. MEYER
BY *[Signature]*
AGENT

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TRANSISTOR DESIGN

Earl A. Meyer, Madison, Wis., assignor to Bjorksten Research Laboratories, Inc., a corporation of Illinois

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8 Claims. (Cl. 317-235)

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This invention relates to transistors, and more particularly to methods for attaching leads to a thin p-layer section sandwiched between two n-layer sections in a triode system.

Transistors constructed so as to have a thin p-layer sandwiched between two n-layers are known, but have been extremely difficult to prepare, because of the precision required and, among other factors, because of the difficulty of attaching a lead to the dividing zone between n- and p-layer without causing shorts, and still having a good contact with the lead.

In accordance with my invention, this is accomplished in the following manner: A loop of metal wire is immersed in a p-layer melt, heated to a temperature moderately above its melting point. This is not extremely critical; however, the temperature must be above the melting point of the said p-layer composition. Generally the higher the viscosity of this layer, the easier is the practice of the invention. However, it may in some cases be carried out at temperatures even a couple of hundred degrees over the melting point of the p-layer.

The loop is rapidly dipped into the p-layer, and because of the surface tension conditions, a film of p-layer will form in the loop. This film will solidify and is then carefully placed between two layers of the n-layer. The ring which was originally used for forming this p-layer membrane now forms a lead. Dimensions are selected in such a manner that the ring does not touch either of the n-layers, thereby avoiding a short.

In this fashion, an exceedingly thin p-layer is accomplished, with a lead to all sides of it.

The invention is further shown in Figure 1, which is a perspective drawing of the finished assembly, 1 being the ring, 2 being the p-layer, 3 being the n-layers (or 2 being the n-layer, 3 being the p-layers), and in Figure 2, which shows these same elements before assembly, and in Figure 3, which shows in cross-section an embodiment having n-layers of different diameters.

This invention is applicable to germanium as well as to silicon type of transistors. In the p-layer I may use as transistor impurity a small amount of an element of group III, such as boron, aluminum, gallium or indium, or mixtures thereof, and in the n-layers a small amount of transistor impurities of group V, such as nitrogen, phosphorus, antimony or arsenic, or mixtures thereof.

This technique is generally applicable to the preparation of intermediate layers in transistors and is not necessarily confined to the specific ma-

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terials and conditions mentioned above by way of illustration and not of limitation.

In another embodiment of the invention, the blocks of n-type material are of different cross section at the point of contact with the p-layer. In Figure 3 reference numeral 4 indicates the n-layer of smaller diameter, 5 the n-layer of larger diameter, and 6 the p-layer.

The p-layer is in this case applied to the larger block of n-layer by evaporation, dipping, solution casting or any other applicable technique for depositing a thin film. The n-layer of smaller diameter is then superimposed by deposit, or by mechanical application. The part of the p-layer 6 which protrudes beyond the smaller layer 4 and is supported by the larger layer 5 on which it rests, is then attached to a lead for connection to the other elements in the circuit in which the transistor is employed. One way of achieving the attachment of such a lead is to apply a metal coating 7 to the said protruding p-layer, for example, by evaporation with rhodium vapor, until a lead 8 can be soldered, or make surface contact, to this rhodium coated area. Phosphor bronze contacts are found to be particularly suitable as leads to this rhodium layer. Application of a stop off coating or wax will prevent short circuits to the n-layers.

One method for preparing the layers in question is to withdraw the crystals slowly from the melt at such a rate as to have a stationary interface between the solid and liquid only slightly above the liquid surface. This procedure eliminates stresses in the silicon or germanium due to solidification within inflexible walls while the simple planar thermal gradient produced in this manner minimizes thermal stresses.

Bombardment of silicon and germanium by helium ions up to 30 kv. or by alpha particles from polonium are known to greatly enhance the rectifying action of diodes based on the properties of these substances.

Such irradiation of the contact surfaces with helium ions was found to exert a beneficial influence on the performance of the silicon and germanium transistors.

While reference has been made above to transistors having p-layer between two n-layers, I may also employ a construction having an n-layer between two p-layers.

It is thus seen that the invention is broad in scope and is not to be limited, excepting by the claims in which it is my intention to cover all novelty inherent in this invention as broadly as possible in view of prior art.

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Having thus disclosed my invention, I claim:

1. A transistor comprising two n-layers and between these a p-layer comprising a membrane adhered by surface tension powers to an annular conductor, having an inner diameter greater than the outer diameter of at least one of the n-layers.

2. The transistor described in claim 1, the base material of both p- and n-layers being germanium.

3. The transistor described in claim 1, the base material of both p- and n-layers being silicon.

4. The method of preparing a transistor of sandwich type construction which comprises the step of dipping an annular member into a fused bath of a substance selected from the group consisting of silicon and germanium, allowing said substance to form a membrane within said ring, and mounting said membrane between two layers of the same substance, differing from the said center layer only in the type of impurities present.

5. As an article of manufacture, a triode transistor having a center layer mounted within a metal ring and adhered thereto in the melted state; and adjoining on each side a side layer, said side layers and center layer differing from each other in the type of transistor impurities.

6. As an article of manufacture, a transistor having two side layers and a center layer, the center layer containing transistor impurities of

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a type differing from that present in the side layers, one of said side layers having a larger surface than the other at the areas of maximal proximity, the protruding rim of the said larger side layer being coated with a metallic conductor.

7. The method of making transistors, which comprises the step of preparing a relatively large surface of a p-layer, coating this surface with an n-layer, superposing a p-layer having a surface smaller than the first p-layer, metal coating the margin of the n-layer which protrudes around the smaller p-layer, and attaching a connection to the said metal coated n-layer.

8. The method of making transistors, which comprises the step of preparing a relatively large surface of n-layer, coating this surface with a p-layer, superposing an n-layer having a surface smaller than the first n-layer, metal coating the margin of the p-layer which protrudes around the smaller n-layer, and attaching a connection to the said metal coated p-layer.

EARL A. MEYER.

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