A reliable, inexpensive "back side" thinning process, capable of globally as well as locally thinning an integrated circuit die to a target thickness of 10 microns, and maintaining a yield of at least 80%, for chip repair and/or failure analysis of the packaged die. The flip-chip or wire-bond packaged die is mounted on a thinning/polishing tool with the backside accessible. The thinning/polishing tool can be a lapping machine used for global thinning, or a mini milling machine, laser, FIB, or E-beam machine for local thinning. The thickness of the die is measured at least five locations on the die before thinning. The thinning tool removes silicon on the exposed surface of the die to a thickness somewhat greater than the target thickness. The exposed surface of the die is polished. The thickness of the die is again measured optically with high accuracy. Based on the thickness data collected, appropriate machine operating parameters for further grinding and polishing of the exposed surface are determined. Further grinding and polishing are performed. These steps are repeated until the target thickness is reached.
Figure 1 (Prior Art)

Figure 2a (Prior Art)
Fig. 8
METHOD FOR BACKSIDE DIE THINNING AND POLISHING OF PACKAGED INTEGRATED CIRCUITS

CROSS REFERENCE TO RELATED APPLICATION


FIELD OF THE INVENTION

[0002] This invention relates to integrated circuits (ICs) having flip-chip or other packaging, and more particularly, to thinning the semiconductor die on which such an integrated circuit is disposed.

BACKGROUND

[0003] Demand for flip-chip interconnect technology is increasing, because it offers several advantages relative to traditional wire-bond packaging, including better speed performance, higher pin count, smaller form factor, and better heat management. In wire-bond packaging, the electrical interconnection between the crystalline semiconductor die (synonymously, chip) and the carrier (synonymously, package substrate) is made using conductive wires. As illustrated cross section in FIG. 1, the die 4 is attached to the carrier 6 with the die 4 front-side face up. An exemplary wire 2 is bonded first to the die 4, then looped and bonded to the carrier 6. Wires 2 are typically 1-5 mm in length, and 25-35 microns in diameter. Dies packaged in this manner may be accessed through the front side 7 of die 4 for performing testing and yield analyses. Solder bumps 5 on the underside of the carrier 6 are for external electrical contacts. Mold cap 12 is the top lid of the package.

[0004] In contrast, the interconnection between the die 4 and carrier 6 in flip-chip packaging is made through conductive “bumps” (e.g., of solder) 8 that are placed directly on the die surface, as illustrated cross section in FIG. 2a. The bumped die is then “flipped over” and placed face down, with the bumps 8 electrically connecting to the carrier 6 directly. The bumps are typically 100-125 microns in diameter.

[0005] If the electrical operation of the integrated circuit is to be preserved in its original package, then the only accessible part of the flip-chip packaging for chip repair and/or failure analysis is the “back side” 10 of the die 4, which typically is a relatively thick silicon substrate. The thickness of the silicon substrate of die 4 is typically about 400 to 800 microns.


[0007] Wire-bond packaging is some cases suited to back-side access. As examples FIG. 2b illustrates cavity-up and cavity-down Ball-Grid Array (BGA) packages, forms of wire-bond packages by way of example. Cavity-up packaging 200 has the silicon substrate 202 on the same side as solder bumps 204, which makes the silicon thinning/polishing difficult without damaging the solder bumps. Also shown are wire bond 206, encapsulation 208, stiffener 210, laminate 212, and circuit layer 214. In contrast, cavity-down packaging 216 allows full access to the silicon substrate 202 with low probability of damaging the device or compromising package functionality.

[0008] In order to access the internal nodes of an integrated circuit device to perform failure diagnostics and/or yield analyses using optical techniques or a charged-particle beam, the thickness of die 4 must be reduced to a workable penetrable range, usually 100 microns or less. More sophisticated techniques require an even thinner silicon substrate.

[0009] To perform such back side failure analysis or circuit editing using focused ion beam (FIB), a three-step process is currently used. In the first step, a flip-chip packaged or other packaged die as shown in FIG. 3A in a perspective view is typically mechanically globally thinned (i.e., thinned over its entire die surface area) such that the remaining silicon thickness, t, is around 100 microns, as illustrated in FIG. 3A. The pre-thinning thickness is shown by the broken lines. Using existing thinning techniques for this stock removal step, yield drops when the die is thinned to less than 100 microns. (That is, there is excessive thinning of the die 4 due to lack of thickness control, which may result in die breakage). As will be understood by those of ordinary skill in the art, FIG. 3A actually depicts a packaged die as in FIG. 2a with solder bumps 5 on its underside serving as the contacts; the back (top) side of the die 4 has been exposed by removing the top lid of the package. The other detail of FIG. 2a is omitted for simplicity.

[0010] After this silicon removal, alignment points 9 (typically three or more) are exposed and identified on the corners of die 4 to assist in navigation of a tool about the die 4, as illustrated in FIG. 3B. This process is referred as “Global alignment”. For example, a FIB system commercially available as the “IDS P3X” (Precision Probe Point extension) system, from NPTest, LLC., San Jose, Calif., provides software-based navigation tools in which the CAD layout and live FIB images of the die can be registered to one another. Once registered, these images are linked so that when the user selects a point or feature on one of the images, the corresponding location is identified on the other image. Note that fiducial marks are built into the circuit layer and are not on the surface. Therefore there is a need to expose the marks by removing the silicon above the marks before the alignment processes. The fiducial excavation is usually done by FIB milling.

[0011] In the second step (FIG. 3C), one or more local cavities or “trenches” 13 are defined in the silicon substrate of die 4, with a trench area size between about 100 and 400 microns. Currently, either laser micro-chemical etching (LMC) or the focused ion beam (FIB) is used to define the trench. While the laser micro-chemical etching method for trenching is fast and reliable, it is also very expensive. Typical systems, which include the laser and sophisticated, but necessary, navigation software, cost around $1.5M. An FIB system, while less expensive ($500K-$1M), is also much slower. Etching a 100 microns trench in a die with a FIB device typically takes about 30 minutes.
The distance d from the bottom of the trench 13 to the underlying active circuit layers is only 5 microns at most, as illustrated in FIG. 3D in partial cross section. FIGS. 3D, 3E show only a small part of the die; other illustrated structures are the passivation 19 and metal layers 15a, 15b. Also provided is silicon dioxide deposition layer 21. Moreover, trenching using either LMC or FIB techniques requires an additional thickness measuring tool to monitor the trenching optical beam induced current (OBIC) and imaging techniques are being used for this purpose. However, either an additional laser system or a high end imaging system is needed to measure silicon thickness inside the trench, further complicating overall requirements for the system.

In the third step (FIG. 3E), an FIB system is used to mill to the circuit layer 17 with small openings 23a, 23b to perform a circuit edit through the bottom of the trench 13 formed in the second step. A circuit edit can include shorting circuit elements, cutting a trace (metal layer interconnect), and changing an interconnect 15a, 15b. The FIB system is typically used in conjunction with chemical assistance for cutting or depositing metal trace 25 or an insulating layer, or for milling and quick, uniform removal of the silicon substrate. However, to mill a hole with FIB there is an aspect ratio (hole depth vs. hole opening) limitation in the use of an FIB device. Practically, the FIB hole 23a, 23b aspect ratio is less than 10:1. Therefore, the trench is preferably made as deep as possible within the silicon substrate.

Thus, existing processes for preparing a die having flip chip or wire-bond packaging for an FIB circuit edit are time-consuming (especially when trenching is required at several locations in the same die), and expensive (because a sophisticated tool is required to make the trenches).

The recently developed picosecond imaging circuit analysis (PICA) technique, which measures dynamic photon emission at the transistor level, has also demonstrated utility in device failure analysis. See, e.g., McManus et al., “Picosecond Imaging Circuit Analysis of the IBM G6 Microprocessor Cache,” Proceedings from the 25th International Symposium for Testing and Failure Analysis, pp. 35-38, 1999. However, effective use of PICA requires the silicon substrate to be thinned to 50 microns or less in order to acquire waveforms having a reasonable signal-to-noise ratio within a reasonable acquisition time. This requirement is due mainly to the fact that silicon absorbs emitted photons efficiently in the visible part of spectrum, leaving near-IR light partially transmitted, and that current photodetectors give a low response in the infrared part of the spectrum. Emission signal intensity increases exponentially as the bulk silicon thickness decreases. While an anti-reflection (A/R) coating on the silicon surface may be used to help improve signal transmission through silicon during PICA analyses, signal acquisition time is still on the order of a few hours at a silicon thickness of 50 microns. To further improve acquisition speed more silicon needs to be removed from the backside.

Ultra thinning of silicon is also applicable to silicon CCD and CMOS imaging sensors. Conventional CCD and CMOS sensors, detect light at the front side of the sensor, while the photons are absorbed and the photocurrent is generated in the P/N junction located at the back of the sensor. The presence of circuitry in the front reduces the light transmission to the back, and therefore lowers the detector quantum efficiency. The state-of-the-art CCD and CMOS sensors use a back illumination configuration in order to obtain higher quantum efficiency, especially in the UV and NIR spectra. Due to the absorptive nature of silicon, the back-illumination sensors need to be back-thinned as thin as possible. An accurate and non-destructive technique is required in order to monitor the CCD/CMOS thinning process.

Thus, a reliable, inexpensive “back side” global die thinning process is needed that is capable of globally thinning a die to a thickness of about 10 microns, without significantly reducing the yield. At a die thickness of 10 microns, the efficiency of PICA for failure analysis can be enhanced, the ease with which FIB circuit edit/repair is performed can be greatly increased, and the sensitivity of CCD and CMOS sensors can be greatly improved.

Additional to the aforementioned backside global die thinning process, a method for local backside substrate thinning which can reliably and inexpensively thin regions as large as an entire die or small fractions of a die to a thickness of about 10 microns or less would be of great benefit in several circumstances. As a first example, die warpage can be as high as 20-30 microns, which would preclude global thinning to 10 microns if the warpage cannot be corrected. As a second example, a wire-bond package as illustrated in FIG. 26 requires local thinning (which may include the entire die, but not the package periphery) to avoid unduly weakening the package and to allow encountering the ball grid. Use of such local thinning is important in backside FIB edit operations, where it is desirable to avoid too deep a milled tiny FIB hole. The use of a locally thinned cavity or trench with dimensions between 100 and 400 microns squared is preferred.

SUMMARY

The present invention is directed to a reliable, inexpensive “back side” thinning process that is capable of globally (over the entirety of one surface) or locally thinning a die to a predetermined thickness of, e.g., 10 microns, and maintaining a yield of, e.g., 80% or more. A first embodiment is directed to global thinning.

In a first sub-embodiment of the global thinning method, the packaged die is mounted on a lapping apparatus having a cutting media. The package cap has been removed or cut open. The thickness of the exposed die is measured at at least five locations on the die before lapping. The lapping apparatus grinds the exposed backside surface of the die to a thickness somewhat greater than the predetermined (target) thickness. The ground surface of the die is then polished to a mirror finish. The thickness of the die is measured at at least five locations using an optical tool. Based on the measured thickness, appropriate operating parameters for further grinding and polishing of the die exposed backside surface are determined. Further die grinding and polishing are performed by the apparatus according to the determined appropriate operating parameters. These steps are repeated until the target die thickness is reached.

In a second sub-embodiment of the global thinning method, useful in a die having warpage, additional steps are used. After the die is thinned to a thickness less than 40 microns, the die is heated to a temperature about 60 degrees
Celsius. The die is then allowed to cool. This heating/cooling process relieves the stress on the die, reducing warpage. Further grinding and polishing are performed according to the determined appropriate operating parameters. The thickness of the die is again measured at least five locations using an optical tool. If the warpage is still significant (i.e. greater than 10 um), and if the target thickness has not been reached, the die is again heated, allowed to cool, and further grinding and polishing are performed.

[0022] In a second embodiment of the invention, an improved process for local thinning of a die or a fraction thereof utilizes mechanical milling, or laser, electron-beam (E-beam), or FIB etching, as well as precise thickness measurement.

[0023] These and other aspects of the present invention may be better understood through the accompanying drawings and the following detailed description of the exemplary embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] FIG. 1 is a cross-sectional view of an integrated circuit having a die with conventional wire-bond packaging.

[0025] FIG. 2A is a cross-sectional view of an integrated circuit having a die with flip-chip packaging.

[0026] FIG. 2B shows cross-sectional view of integrated circuits having die with cavity-up and cavity-down BGA packaging, one form of wire-bond packaging.

[0027] FIG. 3A is a side view of an integrated circuit having a die that has been globally thinned in accordance with the prior art.

[0028] FIG. 3B is a side view of the integrated circuit of FIG. 3A, depicting alignment points on the exposed surface of the die that assist in navigation of a tool about the die.

[0029] FIG. 3C illustrates a local trench formed in the die of FIG. 3B.

[0030] FIG. 3D is an enlarged cross-sectional view of the trench illustrated in FIG. 3C.

[0031] FIG. 3E illustrates FIB editing in the trench shown in FIG. 3D.

[0032] FIG. 4 is a side view of a lapping machine suitable for practicing the present method.

[0033] FIG. 5 is a bottom view of an angle adjustment plate of the lapping machine of FIG. 4.

[0034] FIG. 6 is a schematic illustration of a system including an optical tool for measuring silicon thickness in accordance with the present method.

[0035] FIG. 7A is an enlarged side view of a large die mounted on a substrate, as it appears after solder relieve and the addition of underfill between the die and the substrate.

[0036] FIG. 7B is a side view of the die of FIG. 7A, following a first phase of die thinning and polishing.

[0037] FIG. 7C is a side view of the die of FIG. 7B, after the die has been heated and then allowed to cool, in accordance with an embodiment of the present method.

[0038] FIG. 7D is a side view of the die of FIG. 7C, after the die has been treated by a second phase of die thinning and polishing.

[0039] FIG. 8 illustrates local thinning as compared to global thinning.

[0040] FIG. 9 is a diagram of a FIB system with incorporated reflectometer.

DETAILED DESCRIPTION

[0041] In accordance with a first embodiment of the present method, a die of an integrated circuit with flip-chip packaging is thinned to a target thickness of, e.g., 10 microns over its entire backside surface area ("globally"). In other embodiments the thinning need not be global. To reach the target thickness, the thickness of the die is non-destructively measured by a very accurate optical tool at least once during the thinning process. Dies thinned by the present method typically have a yield rate of at least 80%.

[0042] Because of the large variations in die thickness (on the order of ±10 microns) in silicon wafers as supplied by wafer manufacturers or otherwise available, the main challenges in thinning a die from such a wafer down to 10 microns or less are controlling the levelness of the surface of the die, and controlling the silicon thickness removed across the surface of the die by the thinning tool. In meeting these challenges, the present method uses a multi-stage process. These stages include: preparation for mounting on the thinning machine and initial height map measurements; bulk silicon removal; collection of die thickness measurements using an optical tool; adjusting the thinning machine operating parameters; second die thinning/polishing stage; and iteration stage. The iteration stage is repeated until the target thickness is reached.

[0043] To practice the method successfully, the operator may need to compensate for warping of the die, packaging, and/or the uneven seating of the die in its packaging during the die thinning process. Techniques for compensating for these factors are also described herein.

[0044] In addition, the tool used for thinning the die is calibrated per the operating instructions from its manufacturer. For example, a typical lapping machine of the type commercially available from Allied High Tech. Products, Inc. (Rancho Dominguez, Calif.) requires daily calibration to ensure flatness of thinned and polished surface.

[0045] The discussion below first describes a first sub-embodiment of the present global thinning method, which is particularly useful for die where die warpage is insignificant. In this embodiment, the thinning tool used is a lapping machine. Then, a second sub-embodiment of the method is described, suitable for larger die, or for a die with warpage greater than about 10 microns between center and corner.

1. Global Thinning of Die

[0046] Preparation of Die for Mounting on Lapping Machine/Initial Height Map Measurements

[0047] Often, a die having flip-chip packaging will have a mold cap 12 (synonymously, back lid or heat spreader) above the die 4, as illustrated in cross section FIG. 2A. Mold cap 12 is typically used to conduct heat away from the silicon substrate at the back side 10 of the die 4 and is made, for example, of copper.
If mold cap 12 is present, then it is removed so as to speed up the thinning process. Mold cap 12 may be removed manually by using, for example, a razor blade or Exacto® knife together with mild heating on the cap 12 (40°). The back side 10 of die 4 (which is typically comprised of a silicon substrate) is thereby exposed.

After the mold cap (if present) is removed from the chip, the die is mounted to a lapping puck. A lapping puck is a disc with an extremely flat front side and back side, which is ultimately mounted to a lapping machine. Typical dimensions for a lapping puck are a diameter of 50 millimeters and a thickness of 10 millimeters. The lapping puck is preferably made from a substance that is substantially hard and strong (e.g., stainless steel). The chip is mounted to the lapping puck by using, for example, a low temperature wax applied to the heated lapping puck (e.g., melting point 50°C-80°C). When the lapping puck is heated by a hotplate to above a melting point of the wax, gently touching a wax stick to the puck will apply a thin layer of melted wax to the puck surface.

After a very thin layer of wax is thereby applied to the front side of the lapping puck, the puck is removed from the hotplate using an insulated tool and is placed on a flat surface to allow it to air cool. Immediately thereafter, the chip (packaged die) is placed on the melted wax layer applied to the front side of the puck. Using a hollow cylindrical tool having approximately the same cross section area as the package substrate, pressure is manually applied through the tool to the package substrate to evenly position the chip on the puck.

As the lapping puck cools, the wax solidifies, thereby anchoring the chip in position on the front side of the lapping puck.

To obtain approximate initial height map measurements, the starting height of the assembly (lapping puck plus chip package plus die) is measured at least 5 locations using a dial indicator or other tool to an accuracy of ±1 microns. The die height at its center is then referenced as zero. For example, a tabletop dial indicator (commercially available from Mitutoyo Corporation, Japan) may be used to measure the height of the assembly at the four corners referenced to center of the die (as determined by visual approximation). This step is to create a baseline on how evenly the chip is seated on the puck, and how much the die is warped.

Following the method described above should result in the four corners of the die being seated evenly relative to the lapping puck. The height measurements collected should not vary by more than 10 microns from one side of the die to the opposite side. If a height gradient between edges greater than 10 microns is present (in which case the die is said to be “wedged”), the chip should be re-blocked immediately.

After collecting the required height measurements, the lapping puck/chip assembly is mounted on a lapping machine. For example, in one embodiment, the lapping machine includes a MultiPrep™ Positioning Device, (commercially available from Allied High Tech Products, Inc., Rancho Dominguez, Calif.). The back side of the lapping puck (the side without the wax) is slid onto an angle adjustment plate at the base of the spindle of the Multi-Prep™ Positioning Device (as described in greater detail below).

For the purposes of this disclosure, “thickness” is defined as the thickness of the die as determined using an optical tool. “Height” refers to the combined heights of the lapping puck, the flip-chip package, and the die thickness, typically measured using a tabletop dial indicator or a dial indicator mounted on the lapping machine. Height map measurements do not directly indicate die thickness.

First Die Thinning/Polishing Stage

Most of the discussion which follows describes the use of a lapping machine as shown in FIGS. 4 and 5 to perform both a first phase of thinning and polishing of the die, and a second phase of thinning and polishing. The lapping machine should be calibrated prior to use each day. A lapping machine that is not properly calibrated will quickly generate a grinding thickness wedge, which makes a target thickness of, e.g., ten microns difficult to achieve.

After a lapping puck having a chip mounted thereto is attached to the spindle 16 by cam-lock lever 28, the puck is indexed downward by counterclockwise rotation of the vertical adjustment knob 38 until the sample makes contact with a rotating platen 48. Lapping machine 14 is calibrated so that puck when mounted on plate 18 is parallel to the plane of platen 48. Platen 48 may have an abrasive material disposed on its surface (e.g., diamond particles resin bonded to a polyester film backing). In the illustrated embodiment, platen 48 is housed in a polishing machine 19. One such polishing machine is the TechPrep™ polishing machine (also commercially available from Allied High Tech Products, Rancho Dominguez, Calif.). By continuing to lower the arm 36, the spindle pulley 42 is displaced farther from the arm 36. The displacement is measured in real time and is displayed on the digital dial indicator 46. This “measured distance” indicates the amount of material that will be removed from the die plus any compression the die makes into the abrasive on platen 48 before the spindle pulley 42 is displaced from the arm 36. As material is being removed, the spindle 16 will travel downward until the spindle pulley 42 makes contact with the arm 36.

In the first die thinning/polishing stage, the die is thinned down to a value somewhat greater than the target thickness and dependent on the expected variation in die thickness. For example, if the die has originally a thickness of approximately 600 microns, with a possible variation of ±12 microns, and the target thickness is 10 microns, then the first thinning/polishing stage must stop when the die has a thickness at or above 22 microns (10 microns+12 microns). To be conservative, it is recommended that the die be thinned to no less than 40 microns in the first die thinning/polishing phase.

Rough grades of cutting media may be used to minimize the time required to thin the die to 40 microns. For example, a 30 micron diamond lapping film, followed by a 15 micron diamond lapping film may be used (Allied High Tech Products Item Nos. 50-30040 and 50-30045, respectively). These diamond lapping films are precision graded diamond particles, resin bonded to a flat uniform polyester backing. The diamond lapping films are placed on and adhere to the rotating platen. The lapping puck 22, having the die 4 (not shown in FIG. 5) mounted thereto, and itself mounted on the angle adjustment plate 18 of the spindle 16, engages rotating platen 48, thereby “thinning” die 4 (removing silicon from its surface).
The speed with which the silicon is removed from the die depends on several operating parameters, including lapping head pressure, platen rotation speed, and cutting media disposed on the platen. Actual operating parameters and results obtained for thinning die using a MultiPrep™ Positioning Device, in conjunction with a TechPrep™ polishing machine (which houses rotating platen 48), are listed in Table A below. These results include die removal for both the first die thinning/polishing stage and a second die thinning/polishing stage (synonymously, fine lapping stage), which is discussed below.

### TABLE A

<table>
<thead>
<tr>
<th>Step</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abrasive size and material</td>
<td>3 μ diamond film</td>
<td>15 μ diamond film</td>
<td>6 μ diamond suspension</td>
<td>1 μ diamond suspension</td>
</tr>
<tr>
<td>Allied Item No.</td>
<td>50-30040</td>
<td>50-30045</td>
<td>90-30025-S</td>
<td>90-30015-S</td>
</tr>
<tr>
<td>Abrasive Surface</td>
<td>N/A</td>
<td>N/A</td>
<td>Kemppa B</td>
<td>Val-Cloth</td>
</tr>
<tr>
<td>Allied Item No.</td>
<td>N/A</td>
<td>N/A</td>
<td>85-150-100</td>
<td>90-150-400</td>
</tr>
<tr>
<td>Extender</td>
<td>Water</td>
<td>Water</td>
<td>Greenlube™</td>
<td>Greenlube™</td>
</tr>
<tr>
<td>Allied Item No.</td>
<td>N/A</td>
<td>N/A</td>
<td>90-208005</td>
<td>90-208005</td>
</tr>
<tr>
<td>Platen speed (rpm)</td>
<td>100</td>
<td>100</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>Time (min.)</td>
<td>10–15</td>
<td>10–15</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Die thickness removed (microns)</td>
<td>Bulk removal</td>
<td>50</td>
<td>5</td>
<td>none</td>
</tr>
</tbody>
</table>

In some situations, the IC package also includes a stiffener surrounding the die. Usually, the stiffener can be removed with the same procedure as removing the cap. In case that stiffener cannot be removed (since package substrate is too thin to stand alone) an aluminum oxide abrasive pad may be positioned on the platen to substitute for diamond films and used for the first part of the first die thinning/polishing stage. Actual operating parameters and results obtained for thinning a die having a copper stiffener using a MultiPrep™ Positioning Device, in conjunction with a TechPrep™ polishing machine, are listed below in Table B.

“Extenders,” which are listed in both Table A and Table B, are materials used to enhance the polishing performance of diamond suspensions, compounds, and sprays. They also reduce friction, and increase the life of the polishing cloths.

### TABLE B

<table>
<thead>
<tr>
<th>Step</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abrasive size and material</td>
<td>100 μ Al₂O₃ pad</td>
<td>40 μ Al₂O₃ pad</td>
<td>15 μ Al₂O₃ pad</td>
<td>6 μ diamond suspension</td>
<td>1 μ diamond suspension</td>
</tr>
<tr>
<td>Allied Item No.</td>
<td>50-40070</td>
<td>50-40085</td>
<td>50-40095</td>
<td>90-30025-S</td>
<td>90-30015-S</td>
</tr>
<tr>
<td>Abrasive Surface</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>Kemppa B</td>
<td>Val-Cloth</td>
</tr>
<tr>
<td>Allied Item No.</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>85-150-100</td>
<td>90-150-400</td>
</tr>
<tr>
<td>Extender</td>
<td>Greenlube™</td>
<td>Greenlube™</td>
<td>Greenlube™</td>
<td>Greenlube™</td>
<td>Greenlube™</td>
</tr>
<tr>
<td>Allied Item No.</td>
<td>90-208005</td>
<td>90-208005</td>
<td>90-208005</td>
<td>90-208005</td>
<td>90-208005</td>
</tr>
<tr>
<td>Platen speed (rpm)</td>
<td>75-100</td>
<td>100-125</td>
<td>100-150</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>Time (rpm)</td>
<td>30–40</td>
<td>5–10</td>
<td>5–10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Die thickness removed (microns)</td>
<td>Bulk removal</td>
<td>80</td>
<td>30</td>
<td>5</td>
<td>none</td>
</tr>
</tbody>
</table>
Obtain Die Thickness Measurements Using Optical Tool

After the die has been thinned to the upper limit of the target thickness (or, conservatively, 40 microns), and a mirror polish is present on the surface of the die thickness measurements is preferably obtained at a minimum of five points on the die (e.g., four corners and the center of the die) using an optical tool. The optical tool is, for example, a reflectance spectrometer, a confocal microscope, or an ellipsometer. Advantageously, these optical techniques for measuring thin films are very accurate, non-destructive, and require little or no additional sample preparation. The die thickness measurements should be collected from approximately the same points where they were collected when the table top dial indicator was used for the initial height map measurements, discussed above. Preferably, a fixture is fabricated that permits mounting of the lapping puck and die on or just above the viewing stage of the selected optical tool, so that the die need not be removed from the lapping puck to perform die thickness measurements.

In one embodiment, the optical tool used to obtain die thickness measurements is a reflectance spectrometer. Spectral reflectance is an expression of the amount of light reflected from a thin film and the substrate underneath over a range of wavelengths, with the incident light perpendicular to the sample surface. As illustrated in FIG. 6, a system 60 for measuring the thickness of a die 4 includes a light source 62 and a spectrometer 64, in communication with a computer 70.

As better appreciated by reference to FIG. 6, incident light of various wavelengths is propagated through a fiber optic cable 66 to a lens assembly 68, and from lens assembly 68 to the die 4. Some of the light provided by the light source 62 is transmitted into die 4, and some is reflected, depending on among other factors, the thickness of die 4. Reflected light travels back through the fiber optic cable 66 and into the spectrometer 64. Spectrometer 64 measures the intensity of the reflected light as a function of the wavelength of the incident light. This information is transmitted from spectrometer 64 to computer 70, which calculates the thickness of die 4 at a given point on die 4.

Advantageously, the reflectance spectrometer is relatively inexpensive, fast, and very accurate. For example, the Model F20 reflectance spectrometer (commercially available from Filmtronic, Inc., San Diego, Calif.) currently costs about $12,000, and is capable of making about one thickness measurement per 30 seconds including stage navigation. The spectrometer for the Model F20 is a fixed Czerny-Turner spectrometer with a 512-element silicon CCD array. The light source is a regulated tungsten halogen light source.

The spectrometer is modified such that it is tuned and calibrated in the near IR wavelength range, 700 nm to 1,000 nm, rather than the standard 400 nm to 700 nm range. This range of wavelengths is particularly useful because transmission of light through silicon is much higher in this near-infrared range. In addition, the lens system of the spectrometer was also modified by Applicants, because the beam spot size provided by the F20 is greater than 500 microns, which is too large for this application. As illustrated in FIG. 6, lens assembly 68 was modified to include a lens 72 having a focal length of 40 mm, which acts as a condenser to collimate the light beams exiting from fiber head 65 of fiber optic cable 66, and a 20x near-IR microscope objective lens assembly 74 (Mitutoyo model M plan) to focus the beam on die 4. Objective lens assembly 74 includes a lens with a custom coating, needed for working in the near-IR range. To properly position die 4 with respect to objective lens 74, a z stage focus adjustment 71 is provided, which is mounted to a post 73. Post 73, x stage 76 and y stage 77 are positioned on, for example, a bench breadboard 69, to minimize vibration while measuring die thickness. An x stage 76 and y stage 77 are also provided for positioning die 4. Advantageously, as a result of these modifications, a beam spot size on the order of 100 microns is provided, and dies having a thickness of up to 50 microns may be measured with an accuracy of ±0.1 microns. The cost of these modifications is relatively low.

In another embodiment, the optical tool used to obtain die thickness measurements is a confocal laser scanning microscope (CLSM). In a traditional microscope, the depth of focus is on the order of ten microns. Consequently, when a sample is viewed through a traditional microscope, the image viewed is a composite of 10 microns thick of the sample. In contrast, the depth of focus on a CLSM is very shallow, on the order of one micron, providing well-defined focused layer of the sample.

One such CLSM, the InfraScan 200 commercially available from Checkpoint Technology, San Jose, Calif.) may be used in conjunction with a high precision z stage on which the sample is mounted. The elevation of the z stage may be adjusted at 0.1 micron increments. To determine the thickness of the die, the z stage is first moved to focus the CLSM on the top surface of the die (the appearance of scratches or coating residue on the top surface of the die can be used to help determine the best image). When the best image is obtained of the top surface of the die, the associated z stage encoder value is recorded. Keeping the same x and y coordinates, the z stage is then moved up, to focus on the die diffusion layer. The z stage encoder value associated with this position is then recorded. The difference between the two z stage encoder value is the distance that the z stage has traveled. The thickness of the silicon is then calculated by multiplying the actual z stage travel distance by the refractive index of silicon, which range 3.5 and 3.7 depending on the substrate type and doping level.

While the CLSM can measure silicon thicknesses up to a few hundreds of microns, the CLSM is significantly more expensive than the reflectance spectrometer costing approximately $100,000 per unit. CLSM accuracy (about 1 micron, limited by depth-of-focus) is not as good as that of the reflectance spectrometer (0.1 micron) because of the finite depth-of-focus, CLSM gives poorer accuracy when measuring very thin sample, say less than 10 microns. Moreover, a skilled operator requires a few minutes to complete a single thickness measurement using a CLSM.

In another embodiment, the optical tool used to obtain die thickness measurements is an ellipsometer, another known tool for thin film measurement. An ellipsometer operates according to the principle that light polarization can be altered when the light travels from one medium to a different medium having a different index of refraction, and that the polarization change can be correlated to the media thicknesses (and other optical parameters). Although
an ellipsometer is the most accurate measurement tool for film thickness, the extra accuracy is not needed here, and it commands a higher price. Moreover, a higher degree of operator knowledge is needed to operate the ellipsometer than is required with either the reflectance spectrometer or CLSM.

[0077] Adjust Lapping Machine Operating Parameters

[0078] Based on the die thickness measurements obtained using an optical tool (as described above), the lapping machine operating parameters may need to be adjusted conventionally prior to beginning the second phase of thinning and polishing of the die. Parts of the lapping machine may require calibration and/or adjustment if the measurements obtained indicate wedging, as defined above. A die is said to be wedged when the die shows an uneven thickness map as determined the optical measurement mentioned above.

[0079] A wedged die may be caused by a lapping head that is out of calibration, or by an unevenly “blocked” die. Lapping head calibration should be checked before an attempt is made to re-block the die onto the lapping puck. If the lapping head is found to be properly calibrated, then to achieve an even layer of silicon at the target thickness, the chip must be re-blocked in a manner that physically raises only the low corners. The high and low corners of the die should be referenced first, and then the chip may be removed from the lapping puck.

[0080] Methods for Re-blocking Die Onto Lapping Puck

[0081] A properly positioned shim of known thickness or multiple shims can raise the low corner(s) of a die by an amount 10 microns and higher. The shim is positioned between the bottom of a low corner of the chip and the top surface of the puck (which has the wax applied to it). The lapping puck, having the chip and shim(s) mounted thereon, is again positioned on the lapping machine, which engages the rotating platen. High corners are then removed. However, this method is only effective in correcting for corners that are between 10 microns or more too high.

[0082] Another method that is more universal may be used for correcting for high corners (i.e., will level a die having corners that are less than 10 microns too high). In this method, one of two micrometers on the spindle hub of the lapping tool is adjusted so that the lapping puck (attached to the spindle hub) and the rotating platen are not parallel. Thus, when the spindle hub is rotating, it engages the rotating platen unevenly, such that a high corner of the die is machined, while the low corners are not. The amount that the micrometers are adjusted is determined by trial and error.

[0083] Second Die Thinning/Polishing Stage

[0084] In the second die thinning/polishing stage, the lapping machine is used to continue to thin the die from its thickness as determined by the optical tool to the target thickness (e.g., 10 microns) using adjusted operating parameters, if appropriate. From this point, the die thinning should proceed cautiously.

[0085] During the second die thinning/polishing stage, the chip should be visually inspected and/or optically measured more frequently to ensure that die thinning progress is in control. Moreover, great care needs to be taken to ensure that foreign debris does not fall into the lapping medium (e.g., diamond film) from the package or the chip copper stiffener. Such foreign debris may cause damage ranging from minor surface scratches (which may be polished away using a Vel-Cloth pad and a 1 micron diamond suspension) to complete destruction of the die when the die is extremely thin, e.g., less than 20 microns. Sometimes, scratching may be caused by the lapping medium itself, indicating the lapping medium may need to be changed.

[0086] For the second die thinning/polishing stage, a 9 micron diamond film can be used to bring the thickness from 40 microns to 20 microns and then a three micron particle diamond lapping film may be used to remove material (silicon) from the die at a rate of approximately one micron per minute, assuming a virgin diamond film, and a platen rotational velocity of 150 rpm. Prior to each subsequent thickness measurement with the optical tool, the die is polished to a mirror finish.

[0087] Iteration State

[0088] During this stage, the steps of die thickness measurement using an optical tool, adjusting lapping machine operating parameters, and second stage die thinning and polishing are repeated until the target thickness (e.g., 10 microns) is reached.

2. Global Thinning of Highly Warped Die

[0089] Referring again to FIG. 2, in flip-chip packaging, the interconnection between die 4 and package substrate 6 (synonymously, “carrier”) is made through a conductive “bump”8 that is placed directly on the front side of die 4. Conductive bumps 8 are attached to package substrate 6 using a solder reflow process. After die 4 is soldered to the package substrate 6 through bumps 8, underfill 11 (an epoxy) is added between die 4 and substrate 6, surrounding the space between bumps 8. Underfill 11 is added to absorb stress exerted on conductive bumps 8 resulting from the different rates of thermal expansion at which die 4 and substrate 6 contract while cooling after solder reflow. Underfill redistributes stress over the entire surface area of die 4, and reduces the stress on solder bumps 8.

[0090] Nevertheless, in die with larger surface areas (e.g., greater than 2 cm²), we have observed that die 4 itself tends to “bow” upward after underfill has cured, taking on a convex shape, as illustrated (highly exaggerated) in FIG. 7A. (For clarity, solder bumps 8 are omitted from FIGS. 7A-7D). As a result, after bulk silicon removal is achieved by the first die thinning/polishing stage, which also planarizes the top surface 90 of die 4, the thickness of die 4 at corners 86a, 86b (t₄) is significantly greater than at center 84 of die 4 (t₄), as illustrated in FIG. 7B.

[0091] The warpage is generally relatively small (5 microns or less) in ceramic-substrate packages, but is often significant for plastic packages. Often, in plastic flip-chip packages, there is a thickness difference of 30 microns or more between the center 84 and corners of die 4, two corners of which are shown as 86a and 86b in FIG. 7B (the remaining two corners are hidden in this view). The thickness difference is much greater than that associated with smaller die (e.g., 10 micron thickness difference in die having a surface area of 1 cm² or less). Obviously, when a target thickness of 10 microns ±2 microns is required for the entire surface of die 4, a thickness difference of 30 microns
or more between that at center 84 of die 4 and corners 86a, 86b, is unacceptable. Applicants have found that this thickness difference can be partially corrected by taking additional steps in treating the die.

[0092] Specifically, Applicants have found that when die is 40 microns or less thick, by heating die 4 to a temperature between 40° C. and 60° C. (by, for example, placing the lapping puck and die on a heating plate, as described earlier), and then allowing die 4 to cool to room temperature, the height profile of die 4 changes, such that the heights at the corners 86a, 86b (h) of die 4 are increased slightly, so that the overall die height profile has changed from convex to concave, as illustrated in FIG. 7C. Repeated experimentation with multiple similar-size die has shown that the corners of die 4 grow 10 microns to 15 microns in height as a result of the heating and subsequent cooling of the die as just described.

[0093] A second die thinning/polishing step is then performed, wherein die 4 is further planarized, so that the height at the corners of the die is reduced (relative to the center of the die), as shown in FIG. 7D. That is, the corners of the die “grown” in the previous step are removed, and die 4 is closer to its target thickness across its entire surface.

[0094] A second heating/cooling process may “grow” an additional zero to 15 microns on the corners depending on the packaging material or process. By performing a final fine lapping step, the additional height at the corners is again removed, and die 4 is globally thinned to a target thickness of 10 microns ±2 microns (as determined by again measuring with the optical tool).

[0095] In the case that die warpage cannot be overcome completely, particularly at the corner section of the die, a manual, local thinning may be used as a final resort. Diamond pastes of various roughness levels are applied locally to the silicon area that needs to be thinned. Suitable diamond pastes are 6 micron or 15 micron mono crystalline diamond compounds, e.g. Item nos. 9-21092 and 90-21085 supplied by Allied High Tech. Products. A Q-tip or other thin stick wrapped with soft cloth is used by operator with diamond paste to remove the silicon locally. Since this is only used to correct the thickness variation of a few microns on a small area, the process is fairly quick. Thickness is measured from time to time using an optical tool to monitor the local thinning progress.

3. Cleaning and Functional Testing of Die After Thinning

[0096] After the target thickness for the die has been reached, the chip is removed from the puck by melting the wax using the heat plate. All wax should be removed from the chip, because the wax will act as an electrical insulator, which could lead to false indications of device failure during later functional testing. The wax can be cleaned out by immersing the chip into a vessel containing acetone or citric-acid base solvent. The chip is then finally rinsed with acetone.

[0097] After the chip has been cleaned, an electrical functional test is recommended before the chip is further tested. The functional test will ensure that the global die thinning process has not affected performance and/or functional characteristics of the chip. Functional testing performed on die globally thinned according to the present method, and having a thickness of 10±2 microns, has proven a yield rate of 80% or more.

[0098] A heat sink may be required on top of the thinned die if the chip generates more power than the thinned silicon can dissipate during a functional test. The heat sink may take many forms, ranging from a solid heat spreader to a viscous thermal grease, so long as it is electrically insulating. However, if optical probing is performed (e.g., PICA), then the heat sink material must be optically transparent and its surface highly polished so that it does not absorb or scatter light. With sufficient heat dissipation capability, the thinned die will then be able to be tested at its normal operating speed for full characterization.

[0099] Local Thinning Methods

[0100] The above disclosed thickness measurement methods can be applied in varying combination to local thinning as well as to global thinning. Local thinning is of particular importance when die warpage cannot be entirely corrected, and also for wire-bond packaging, which would be unacceptable weakened if the whole package were globally thinned optimally for backside operations. Small area, local thinning of the die by laser, E-beam, or FIB is also important to the success of backside circuit edit using FIB.

[0101] FIG. 8 illustrates local thinning as compared to global thinning. According to an embodiment of this invention, an area which may include the entire die 800 excluding the package 802, or which may include a portion of the die as small as 100 square microns or smaller, is locally thinned to create cavity 804 instead of flat surface 810. Local thinning cannot be accomplished by lapping, and therefore is of necessity more time-consuming than global thinning. Several thinning methods have been successfully applied to local backside thinning, including mechanical milling, laser etching, E-beam etching, and FIB etching.

[0102] Mechanical milling may be accomplished with a diamond coated mini-milling bit. An example of a mechanical milling system which may be used is the ASAP-1 Selected Area Preparation System by Ultratec, which utilizes a Z-movable rotating milling tool and an X- and Y-movable table on which the sample is mounted. Laser etching may be accomplished using intense laser beam interaction with silicon in the presence of chemical assistance. An example of a laser system which could be used, is the 9850 SiliconEtcher system by Revise, Inc. FIB etching may be accomplished using high-energy ion beam with chemical assistance, or plain physical sputtering. Local thinning by FIB etching is described by Chun-Cheng Tsao et al in Proceedings of LSI Test Symposium 2001 (Editing of IC Interconnects Through Back Side Silicon with a Novel Coastal Photon-Ion Beam Column, pp 175-180). Electron beam etching works according to the same principles as FIB etching and also requires chemical assistance to enhance etching rate. E-beam etching has the advantage of causing less device damage and charging as compared to FIB etching. The main drawback is its very slow etching rate. E-beam etching was discussed by Jurgen Gstottner et al at the 2001 European FIB user group meeting in Arachon of France (http://www.imec.be/fug/EFUG2001_Gstottner.pdf).

[0103] Of these various methods, mechanical milling is the fastest, followed by laser etching, and then by FIB, with
E-beam etching being the slowest. Mechanical milling is useful in larger area operation, and the cavity dimensions are limited by the bit size and translation resolution of the mounting table. The mechanical milling method is generally best suited for the thinning of an entire die within a package or wafer, since the milling bit is relatively large and the removal rate is fast. For laser etching the size of the cavity is limited by the laser beam size, with a lower limit on the order of microns. E-beam and FIB have the smallest beam size and can etch the smallest cavities, with approximate lower limit of a fraction of a micron.

[0104] Use of the aforementioned optical thickness measurement techniques is critical to the achievement of 10 microns or less thickness for the local thinning as well as for the global thinning. The mechanical thickness measurement tools used in the ASAP-1 system yield specifications of about 50 micron thickness due to their large uncertainty in thickness determination. However, with use of a reflectance spectrometer as disclosed herein to provide iterative thickness measurement/thinning, 10 microns local thinning has been demonstrated using mechanical milling.

[0105] A first sub-embodiment of the local thinning embodiment employs iterative thickness measurement/local thinning to achieve 10 microns remaining cavity thickness. The thickness measurement may be accomplished using any of the aforementioned optical techniques, i.e., IR microscope, reflectometer, and ellipsometer. For the case of large area local thinning, multiple point measurement is recommended to avoid over-thinning of a portion of the die (due to such factors as die warpage or tilt). For small area cavities on the order of size of hundreds of microns, thickness measurement at one point may be sufficient, since the small cavities, particularly those etched by laser or FIB, are typically quite flat.

[0106] A second sub-embodiment of the local thinning embodiment utilizes in-situ thickness measurement when local thinning is done using FIB or laser etching. By way of example, by incorporating a reflectometer into a FIB instrument such as the IDS OptiFIB, made by NPTest, LLC, the thinning process can be monitored in real time, thus avoiding the risk of overshooting. A schematic diagram of an OptiFIB system with incorporated reflectometer system is shown in FIG. 9. Shown are column 900, lens system 902, light illumination unit 904, photon beam 906, ion beam 908, spectrometer 910, CCD camera 912, and sample 914.

[0107] CLSM can be incorporated into the OptiFIB system and used to do in-situ measurement of local trench floor thickness, however, there is no real-time measurement capability with CLSM measurement, because it involves Z stage motion which cannot occur during the FIB trenching process. Ellipsometry cannot be built into a FIB system, because it requires off-axis probing and detection of a laser beam.

[0108] Thus, the present method provides, in a first embodiment, an ultra-thin, highly flat, functioning integrated circuit die having an optical finish on its entire exposed surface. The method itself is controllable, predictable, and uses simple, relatively inexpensive laboratory tools. Moreover, the ultra-thin die can be produced within a reasonably short time, as compared with methods currently used for local die thinning, the trench approach. Expensive, time-consuming trenching within the die is avoided altogether. Furthermore, an optical finish may be provided on the exposed die surface. When an anti-reflective coating is applied to the exposed die surface, much better image quality and light transmission is achieved when using emission techniques such as pica.

[0109] In a second embodiment, the optical measurement tools used in the global thinning method are applied to local thinning for use with uncorrectable wafer warpage, wire-bond packaging, and structurally weak packages. The non-destructive optical measurement tools can also be used in a local trench created by laser, FIB, or E-beam. Ultra-thin cavities can be produced using a variety of milling or etching techniques chosen according to the application. Thickness measurement is done iteratively in a first sub-embodiment, and in-situ in a second sub-embodiment.

[0110] The presently disclosed embodiments of the inventions are illustrative and not limiting. Moreover, the method of the present invention is not limited to specific IC package materials or components. Modifications and substitutions for the steps of the method disclosed will be apparent to one skilled in the art in light of this disclosure and are intended to fall within the scope of the appended claims.

We claim:
1. A method of backside thinning of at least a portion of a packaged integrated circuit die to a predetermined thickness, comprising the steps of:
   mounting the packaged die on a support;
   measuring the thickness of the mounted packaged die at least one location on the die;
   contacting a region of the surface of the packaged die to a thickness medium to thin at least a portion of the die to a thickness lesser than the predetermined thickness;
   measuring the thickness of the thinned portion of the packaged die at at least one location;
   based on the measurement of the thinned portion of the packaged die, determining parameters for further thinning;
   performing further thinning according to the determined parameters; and
   repeating the acts of determining the parameters and performing further thinning until the predetermined thickness is reached.
2. The method of claim 1, wherein said step of contacting a region of the surface of the packaged die to a thickness medium to thin at least a portion of the die to a thickness greater than the predetermined thickness comprises grinding said surface of said packaged die.
3. The method of claim 2, wherein said packaged die is flip-chip mounted.
4. The method of claim 3, wherein:
   said steps of measuring the thickness of the packaged die and of measuring the thickness of the thinned portion of the packaged die are performed at a plurality of locations on the die; and
   said steps of grinding the surface of said packaged die are directly followed by polishing the ground surface of the packaged die.
5. The method of claim 4, further comprising the act of mounting the packaged die to a lapping puck prior to the act of mounting the packaged die on the support.

6. The method of claim 5, wherein the packaged die is mounted to the lapping puck using wax.

7. The method of claim 6, wherein the wax has a melting point of less than 45°C.

8. The method of claim 4, wherein media used in the act of grinding comprises two grades of particles.

9. The method of claim 4, wherein the act of measuring includes using an optical tool selected from a group consisting of a reflectance spectrometer, a confocal microscope, and an ellipsometer.

10. The method of claim 9, wherein the optical tool is a reflectance spectrometer, operating at NIR spectral range.

11. The method of claim 4, further comprising the act of: removing at least a portion of a lid from the die package prior to the act of mounting on the support.

12. The method of claim 4 further comprising the acts of: heating the die; and allowing the die to cool, prior to performing the further grinding and polishing.

13. The method of claim 12, wherein the die is heated to a temperature ranging from about 40 to about 60 degrees Celsius.

14. The method of claim 12, wherein the heating of the die is performed by placing the packaged die in heated wax.

15. The method of claim 4, wherein the predetermined thickness is less than about 10 microns.

16. The method of claim 4, further comprising de-warping the die.

17. An integrated circuit having a die thinned according to the method of claim 4.

18. An integrated circuit having a die thinned according to the method of claim 12.

19. The method of claim 1, wherein said step of contacting a region of the surface of the packaged die to a thinning medium to thin at least a portion of the die to a thickness greater than the predetermined thickness is accomplished using a method selected from the group consisting of: mechanical milling, laser etching, FIB etching, electron beam etching.

20. The method of claim 19, wherein said at least a portion of the die is less than the entire die.

21. The method of claim 20, wherein said steps of measuring the thickness of the packaged die and of measuring the thickness of the thinned portion of the packaged die include using an optical tool selected from a group consisting of a reflectance spectrometer, a confocal microscope, and an ellipsometer.

22. The method of claim 21, wherein said steps of measuring the thickness of the packaged die and of measuring the thickness of the thinned portion of the packaged die are performed in situ.

23. An integrated circuit having a die thinned according to the method of claim 21.

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