



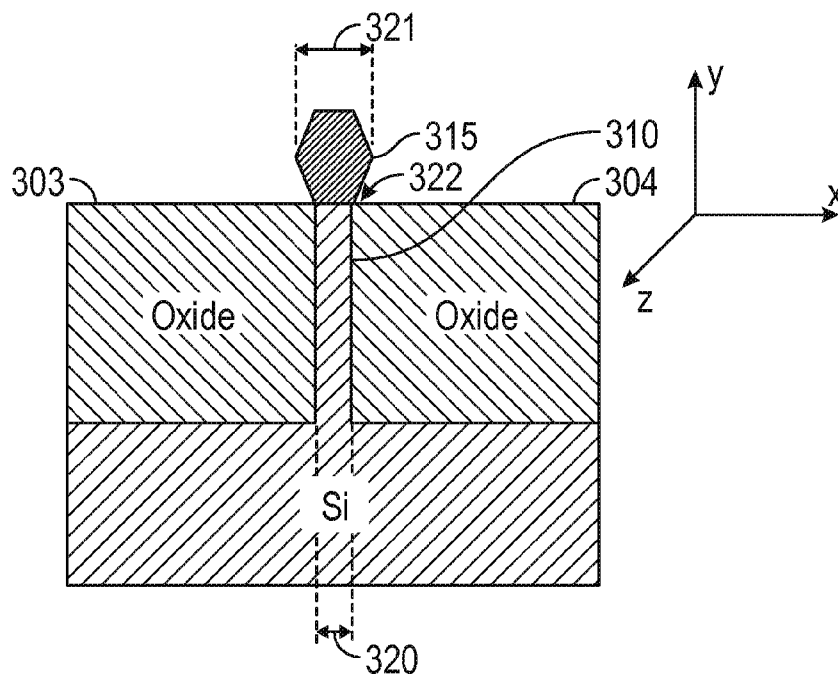
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[Continued on next page]

- (54) Title: EXPITAXIAL FILM ON NANOSCALE STRUCTURE



**FIG. 3B**

(57) Abstract: An embodiment of the invention includes an epitaxial layer that directly contacts, for example, a nanowire, fin, or pillar in a manner that allows the layer to relax with two or three degrees of freedom. The epitaxial layer may be included in a channel region of a transistor. The nanowire, fin, or pillar may be removed to provide greater access to the epitaxial layer. Doing so may allow for a "all-around gate" structure where the gate surrounds the top, bottom, and sidewalls of the epitaxial layer. Other embodiments are described herein.



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## EPITAXIAL FILM ON NANOSCALE STRUCTURE

### Background

[0001] A variety of electronic and optoelectronic devices can be enabled by developing, for example, high quality III-V semiconductors on elemental silicon (Si) substrates or IV semiconductors on Si substrates. Surface layers capable of achieving the performance advantages of III-V or IV materials may host a variety of high performance electronic devices such as CMOS and quantum well (QW) transistors fabricated from extremely high mobility materials such as, but not limited to, indium antimonide (InSb), indium arsenide (InAs), germanium (Ge), and silicon germanium (SiGe). Optical devices such as lasers, detectors and photovoltaics may also be fabricated from various other direct band gap materials, such as, but not limited to, gallium arsenide (GaAs) and indium gallium arsenide (InGaAs). These devices can be further enhanced by monolithically integrating them with conventional devices of Si since use of a Si substrate has the additional advantage of cost reduction.

[0002] The growth of III-V and IV materials upon Si substrates, however, presents many challenges. Crystal defects are generated by lattice mismatch, polar-on-nonpolar mismatch, and thermal mismatch between the III-V semiconductor epitaxial (EPI) layer and the Si semiconductor substrate or the IV semiconductor EPI layer and the Si semiconductor substrate. When the lattice mismatch between the EPI layer and substrate exceeds a few percent, the strain induced by the mismatch becomes too large and defects are generated in the EPI layer by relaxing the EPI film. Once the film thickness is greater than the critical thickness (i.e., film is fully strained below this thickness and partially relaxed above this thickness), the strain is relaxed by creating misfit dislocations at the film and substrate interface as well as in the EPI film. The EPI crystal defects may be in the form of threading dislocations, stacking faults and twins. Many defects, particularly threading dislocations and twins, tend to propagate into the "device layer" where the semiconductor device is fabricated. Generally, the severity of defect generation correlates to the amount of lattice mismatch between the III-V semiconductor and the Si substrate or the IV semiconductor and the Si substrate.

### Brief Description Of The Drawings

[0003] Features and advantages of embodiments of the present invention will become apparent from the appended claims, the following detailed description of one or more example embodiments, and the corresponding figures, in which:

Figures 1(a)-(c) depict a nanowire based embodiment of the invention.

Figures 2(a)-(d) depict a nanowire based embodiment of the invention.

Figures 3(a)-(d) depict a fin based embodiment of the invention.

Figure 4 depicts a fin based embodiment of the invention.

Figure 5 includes a process in an embodiment of the invention.

Figure 6 includes a process in an embodiment of the invention.

Figures 7(a)-(f) include a CMOS process in an embodiment of the invention.

### Detailed Description

[0004] In the following description, numerous specific details are set forth but embodiments of the invention may be practiced without these specific details. Well known circuits, structures and techniques have not been shown in detail to avoid obscuring an understanding of this description. "An embodiment", "various embodiments" and the like indicate embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Some embodiments may have some, all, or none of the features described for other embodiments. "First", "second", "third" and the like describe a common object and indicate different instances of like objects are being referred to. Such adjectives do not imply objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner. "Connected" may indicate elements are in direct physical or electrical contact with each other and "coupled" may indicate elements co-operate or interact with each other, but they may or may not be in direct physical or electrical contact. Also, while similar or same numbers may be used to

designate same or similar parts in different figures, doing so does not mean all figures including similar or same numbers constitute a single or same embodiment.

[0005] An embodiment includes depositing a material onto a substrate where the material includes a different lattice constant than the substrate (e.g., III-V EPI material on a Si substrate or IV EPI material on a Si substrate). An embodiment of the invention includes an EPI layer that directly contacts, for example, a nanowire, fin, or pillar substrate in a manner that allows the EPI layer to relax with two degrees of freedom (e.g., X and Y) or three degrees of freedom (e.g., X, Y, and Z). The relaxed EPI layer may be included in a channel region of a transistor. The nanowire, fin, or pillar substrate may be removed (fully or partially) to provide greater access to the EPI layer. Doing so may allow for an "all-around gate" where the gate surrounds the top, bottom, and sidewalls of the more exposed EPI layer. Other embodiments are described herein.

[0006] An embodiment differs from a conventional technique that involves deposition of thick buffers (that are 0.5 or more microns thick) that bridge the lattice constant difference between the substrate and the layers of interest (device layers including III-V materials and the like). In such conventional techniques complicated anneals and compositional grading processes are used to "bend" the defects into each other within the thick buffer so the defects annihilate. Many thick buffer techniques are time consuming, expensive, include undesirable surface roughness of the buffer, and the minimum defect density still remains high.

[0007] Embodiments also differ from a conventional technique that includes Aspect Ratio Trapping (ART). ART is based on threading dislocations that propagate upwards at a specific angle. In ART a trench is made with a high enough aspect ratio such that the defects terminate on the sidewall of the trench and any layer above the terminations is defect free.

[0008] In contrast to the above mentioned thick buffer and ART based approaches, an embodiment uses a nanostructure to allow an extra dimension (X and Y directions) or extra dimensions (X, Y, and Z directions) for the EPI film to relax (as opposed to planar EPI films that primarily relax in the Y direction). This nanostructure

may be, for example, grown around a nanowire (on the top and/or bottom and/or side wall or walls of the nanowire) and/or grown on top of (or on the bottom of or on a sidewall of or walls of) a fin or pillar (a shorter fin). These nanowire, fin, and pillar based embodiments, among other embodiments, are described below.

[0009] Figures 1(a)-(c) depict a nanowire based embodiment of the invention. Figure 5 depicts a method in an embodiment of the invention. Figures 1 and 5 are discussed below.

[0010] Block 505 includes forming a superlattice with etch selectivity between the layers. For example, device 100 includes alternating Si/SiGe layers but other combinations (e.g., InGaAs/InP) are included in alternative embodiments. Next, the process continues with fin formation (e.g., block 510 and fin 101), wells implant, and the like until a previously formed dummy gate is removed leaving void 102. This exposes area 106, which is adjacent portions 105, 107 (block 515) that are protected by oxide regions 103, 104. In block 520 a sacrificial layer is etched out (e.g., SiGe in Figure 1(a)), leaving voids 112, 113 and free standing nanowires or nanoribbons 110, 111 that are made of a core material (e.g., Si or SiGe).

[0011] In block 525 EPI layers are deposited on the nanowires. The EPI layer(s) can be differing thicknesses such as, for example, 4, 6, 8, 10, 12, or 14 nm. In some embodiments the Si nanowires are left in place and EPI is formed on the top, bottom, and opposing sides of the nanowires (not shown). However, in other embodiments (such as Figure 1(c)) the EPI on the opposing side walls (or possibly just one wall) of the nanowire(s) is removed (e.g., via wet etch) to provide access to the Si nanowires (block 530). The Si core nanowires may then be removed (e.g., via etch) in block 535 leaving relatively free standing EPI ribbons or wires 115, 116, 117, 118. In one embodiment the voids may remain or may be filled with oxide, insulators, metals and the like. Blocks 530, 535 (shown using dashed lines to indicate the blocks as options for process 500) may be beneficial if the Si core nanowires will degrade electrostatics for the apparatus. In one embodiment, the voids left from removing nanowire portions may be filled or occupied by a high-k/metal gate.

[0012] Thus, Figures 1(a)-(c) include an apparatus comprising a fin structure from which Si ribbons or wires 110, 111 are formed. EPI layers 115, 116, 117, 118 (having a lattice constant mismatched with the fin lattice constant) are formed directly on the top and sidewall portions of the fin structure. There is no buffer layer between the fin structure and the EPI layer and there is no annealing of the EPI or any ART trenches used to control EPI defects. However, in other embodiments there may be annealing of the EPI and still other embodiments ART trenches may be used to control EPI defects. Furthermore, there may be a buffer in other embodiments. Still, that buffer layer may be very thin (e.g., less than 250, 100, 50, 30, or 15 nm as compared to conventional buffer layers that are more than 0.5 micron in thickness). This may be a critical value to prevent defects that might be included with thicker values. EPI layers 115, 116, 117, 118 may comprise IV and/or III-V materials. For example, EPI layers 115, 116, 117, 118 may include one of Ge, SiGe, GaAs, AlGaAs, InGaAs, InAs, and InSb and the fin structure may include Si (e.g., Si, SiGe), alternating layers of Si and SiGe, InGaAs, InP, and alternating layers of InGaAs and InP. Any of EPI layers 115, 116, 117, 118 may be included in a channel of a transistor and couple to a source and a drain of the transistor (where the source and/or drain may be partially or fully included in fin 101). In an embodiment the critical thickness for the EPI layers is greater than 1, 3, 5, 7, 9, or 11 nm. In an embodiment fin 101 is monolithic with substrate 108 and the EPI layer includes three portions formed directly on the top and sidewall portions of the ribbon and the three portions are monolithic with one another.

[0013] Figures 2(a)-(d) depict a nanowire based embodiment of the invention. This concerns an embodiment with a raised source and/or drain. In Figure 2(a) a superlattice is formed as described above, however apparatus 200 includes dummy gate 202 adjacent oxide spacers 203, 204. Figure 2(b) shows how the spacers are used to protect portions of sacrificial layers (e.g., SiGe) when other portions of those layers (located between the spacers and under location previously occupied by dummy gate 202) are removed. The spacers also provide for EPI layer depositions 215, 216, 217, 218 in place of the removed sacrificial layer (SiGe) portions located between the spacers. Protective layer 219 (e.g., a second dummy gate that is applied after dummy gate 202 was removed) is located between the spacers after

EPI layers 215, 216, 217, 218 are formed. Layer 219 will keep EPI layers used to construct source/drain (see Figure 2(c) described below) away from the gate region.

[0014] Figure 2(c) shows how spacers 203, 204 are used to etch out old source/drain regions and deposit new raised EPI source/drains portions ( $R_{SD}$ ). As an option, the spacers may be used to remove nanowire portions (Figure 2(d)) located between the spacers after layer 219 is removed. As a result portions of former nanowire and/or sacrificial layers (located in regions 220, 224) remain coupled to EPI layers 215, 216, 217, 218. In one embodiment, the voids left from removing nanowire portions may be filled or occupied by a high-k/metal gate, oxide, insulator, and the like.

[0015] While Figures 2(a)-(d) discuss an embodiment where  $R_{SD}$  are formed after EPI ribbons/wires are included in the apparatus, other embodiments may include forming the  $R_{SD}$  before EPI ribbons are included in the apparatus. Doing so may still utilize spacers to control lateral  $R_{SD}$  growth to preserve Si ribbons that are later accessed via removal of a dummy gate residing above those Si portions. Those Si ribbons or portions may then be used to form EPI ribbons (and the Si ribbons (or any other core ribbon including a material other than Si) may or may not be removed).

[0016] Figures 3(a)-(d) depict a fin based embodiment of the invention. Figure 6 depicts a method in an embodiment of the invention. Figures 3 and 6 are discussed below.

[0017] In block 605 a support structure is formed. The support structure may be a fin or a pillar (a shortened fin in an embodiment of the invention). Figure 3(a) shows fin 310 formed between oxide portions 303, 304. Fin 310 may be monolithic with substrate 308 in an embodiment. The top surface of fin 310 may be modified through the use of, for example, dry or wet chemical pretreatments to foster film growth on facets other than the  $\langle 100 \rangle$  surface. In block 610 EPI layer 315 is grown on fin 310 (Figure 3(b)). In an embodiment oxide portions 303, 304 control EPI growth to focus on fin 310. However, in another embodiment a spacer may be used on either side of the fin to control EPI growth.

[0018] Figure 4 is based on a scanning electron microscope (SEM) micrograph of 7 EPI “balls” atop 7 fins. The balls may be located in a transistor channel with a source located elsewhere in the fin (e.g., located in the unseen foreground of Figure 4 along the fin) and a drain located elsewhere in the fin (e.g., located in the unseen background of Figure 4 along the fin). In an embodiment, spacers may be used to prevent EPI from growing on the sidewall of the fin but in other embodiments such sidewall growth may be encouraged.

[0019] Returning to Figure 3(b), EPI layer 315 is at the fin height seen in conventional multigate fin based transistors in an embodiment of the invention. The shortest distance between the sidewall portions 320 is less than 1, 3, 5, 7, 9, or 11 nm and the EPI layer has a maximum thickness 321 respectively greater than 1, 3, 5, 7, 9, or 11 nm (although the EPI layer has no minimum thickness). The fin and the EPI layer meet at junction point 322 and maximum width 321 of the EPI layer is greater than a width of the fin at the junction point (although in other embodiments the EPI layer is not necessarily wider than the fin at the junction point considering, for example, when the EPI layer is located on top of the fin but not along the fin side walls or, for example, when the fin is extremely narrow). Generally, the higher the fin/EPI lattice mismatch, the smaller the fin width needs to be (to allow for more relaxation of the EPI layer). EPI layer 315 has a general absence of defects along its outer perimeter that borders the fin structure at point 322 in part due to increased degrees of freedom (X, Y, and/or Z).

[0020] In an embodiment, if the substrate/subfin leakage is unacceptable/undesirable then the pillar/fin can be removed leaving EPI 315 “floating” (Figure 3(c)) in block 615 (i.e., not immediately surrounded on all sides by supporting material). Analogous material removal was described above regarding the removal of Si portions in Figure 2(d). The material may be removed after, for example, dummy gate removal. This is optional and other embodiments do not remove this material. Thus, block 615 is shown dashed to show its optional nature.

[0021] Block 620 addresses how a gate is formed (directly or indirectly) on some or all exposed portions of EPI 315. If the fin/pillar was removed this allows the gate to be formed as an “all-around gate”. In other words, a “tri gate” may provide for a gate

that is on top of the EPI as well as along the EPI side walls (e.g., when Fin 310 is not removed). However, the removal of the support structure allows the gate to form under the EPI as well. Doing so may eliminate or at least reduce subfin leakage current.

[0022] With support structure removal, void 316 may be located within EPI 315 (Figure 3(d)). This void may be left a void, filled with dielectric, filled with gate material, and the like. Void 316 may retain the shape of the former fin (used to construct EPI 315) or may otherwise include irregular boundaries or smooth boundaries left after support structure removal. In other words, deformation 316 may not be a square with 90 degree angles but instead leave an EPI layer that is asymmetrical.

[0023] Figures 7(a)-(f) include a process for forming CMOS devices with EPI that includes multiple degrees of freedom (e.g., along the X, Y, and Z planes). Figures 7(a)-(f) concern a pillar or fin but for nanowire embodiments (e.g., in Figures 1(a)-(c)) the same concept is applicable: where there is an EPI deposition step an oxide hardmask is deposited and used to determine which polarity EPI is deposited. Figure 7(a) includes fin formation; Figure 7(b) shows a mask in place; Figure 7(c) shows EPI 715 grown atop one fin (with multiple degrees of freedom along the X, Y, and Z planes); Figure 7(d) shows the mask changing locations to protect EPI 715 so that in Figure 7(e) EPI 716 is formed atop another fin. Figure 7(f) shows the different polarities for EPI 715, 716.

[0024] Thus, as shown above embodiments allow an extra degree or degrees of freedom for the EPI layer to relax. For example, with a conventional planar EPI configuration the relaxation is largely limited to the vertical direction (and restrained in the X and Z directions). However, the nanowire embodiments as well as the EPI on pillar/fin embodiments allow for relaxation not only in the Y or vertical but also in the X or horizontal dimension (which runs parallel to the long axis of the fin or wire). Also, depending on the length of the wire or fin (e.g., a very short fin or wire amounts to a pillar) relaxation in the Z is also allowed. Further, the nanowire, pillar, and fin based embodiments have increased critical layer thickness as opposed to planar configurations. In addition, the smaller the wire, fin, or pillar, the larger the benefit to

the critical layer thickness (i.e., critical layer thickness increases as the ability to relax in the X and/or Z direction increases). Also, wire, fin, and pillar embodiments allow for a thin EPI layer such as, for example, the same thickness as the channel region in a transistor. Doing so increases throughput and decreases cost of the precursors to growing the material. Further, various wire, fin, and pillar embodiments need no additional process steps beyond the EPI growth. For example, no annealing is necessary (although annealing is used in other embodiments). Also, with the ART approach the creation of the ART trench needs to be done prior to any EPI growth. But with various wire, fin, and pillar embodiments after replacement metal gate (i.e., dummy gate is removed) or after fin/pillar formation, the EPI layers are deposited (without need for ART trenches although other embodiments use ART trenches). Further still, various wire, fin, and pillar embodiments allow for CMOS integration. More specifically, conventional technologies require the distinction between NMOS and PMOS be accomplished through implantation. However, various wire, fin, and pillar embodiments allow for the same masks to be used to mask off the areas for NMOS and PMOS growth, resulting in increased manufacturing efficiency.

[0025] In an embodiment an apparatus comprises: a fin structure having a first lattice constant and a top and opposing sidewall portions extending from the top towards a substrate; and an EPI layer, having a second lattice constant different from the first lattice constant, formed on one of the top and sidewall portions. In the case where the fin is very short the fin may be considered a pillar. In an embodiment the EPI layer is formed on the top and sidewall portions. In an embodiment the EPI layer comprises one of a IV and a III-V material and the fin structure includes Si (e.g., SiGe or Si). An embodiment includes an apparatus comprising: a fin structure having a first lattice constant and a top and opposing sidewall portions extending from the top towards a substrate; and an EPI layer, having a second lattice constant different than the first lattice constant, formed on one of the top and sidewall portions; wherein the EPI layer comprises one of a group IV material and a group III-V material and the fin structure includes Si. In an embodiment the EPI layer comprises the group III-V material. In an embodiment the EPI layer is included in a channel of a transistor and couples to a source and a drain of the transistor. The EPI layer, source and drain may all be included in/on the same fin but in other

embodiments that is not the case. In an embodiment there is no buffer layer between the fin structure and the EPI layer and the EPI layer directly contacts one of the top and the sidewall portions. In an embodiment the fin structure includes one of silicon and a superlattice structure. In an embodiment there is a buffer layer between the fin structure and the EPI layer, the buffer layer is less than 30 nm thick, and the EPI layer directly contacts the buffer layer. In an embodiment the critical thickness for the EPI layer is greater than 3 nm. In other embodiments the critical thickness is greater than 5, 7, 9, or 11 nm. In an embodiment the fin is monolithic with the substrate and the EPI layer includes three portions directly contacting the top and sidewall portions and the three portions are monolithic with one another. In another embodiment the top may be removed as well as portions of the side walls. In an embodiment the EPI layer has a general absence of defects along its outer perimeter that borders the fin structure (in contrast to other conventional technologies such as ART, which has defects along the EPI/substrate border).

[0026] In an embodiment an apparatus comprises first and second columns each including a column portion comprising a lattice constant and one of silicon, a IV material, and a III-V material; and a nanowire including an EPI layer, the EPI layer (a) having an additional lattice constant different from the lattice constant, (b) coupling to each column portion of the first and second columns by one of a direct connection and a buffer layer that is less than 30 nm thick, and (c) comprising one of a IV material and a III-V material. In an embodiment the EPI layer forms an EPI wire of sorts. The support portions of the EPI wire gain support by contacting the support columns. The support columns, in one embodiment, may be portions of a fin that were not etched away (as opposed to a fin portion where a sacrificial layer of SiGe or the like was etched away and later replaced with an EPI layer). These support areas then provide support for the EPI layer and even a core wire such as a Si wire stretching between the columns. In an embodiment the EPI layer includes a first EPI support portion, a second EPI support portion, and an EPI middle portion coupling the first and second EPI support portions to one another; the first and second EPI support portions, but not the EPI middle portion, each directly contact the column portions of the first and second columns; and the EPI layer is included in a transistor channel. In an embodiment the first and second columns couple to each other with a

coupling portion that includes silicon and the EPI middle portion directly contacts the silicon of the coupling portion. Thus, the coupling portion may constitute part of a Si wire or core wire upon which an EPI wire is located. In an embodiment the nanowire includes an additional EPI layer that includes an additional first EPI support portion, an additional second EPI support portion, and an additional EPI middle portion coupling the additional first and second EPI support portions; wherein the additional first and second EPI support portions couple to the first and second columns and the additional EPI layer does not directly contact the EPI layer. In an embodiment the first and second columns couple to each other with a coupling portion, having opposing faces that each include silicon, and the EPI middle portion and the additional EPI middle portion directly contact the opposing faces. In an embodiment no silicon is located directly between the EPI middle portion and the additional EPI middle portion and the column portions of the first and second columns include one of silicon and silicon germanium. In some embodiments a core material, such as a Si ribbon wire that served as a location for EPI layer growth, may later be removed so no or little Si is between middle portions of adjacent EPI layers. In an embodiment a nanowire may be composed of several EPI layers or EPI wires that do not directly contact one another. In one embodiment a core wire (e.g., Si wire) may include EPI layers on its top and bottom. In an embodiment, such a wire may include an EPI layer on its side wall or EPI layers on its side walls but other embodiments do not include such side wall EPI layers. In an embodiment the EPI middle portion includes a top, bottom, and opposing sidewalls and the apparatus includes a gate surrounding the top, bottom and opposing sidewalls. Thus, an embodiment may include an "all-around gate" formed around an EPI layer that is exposed on its top, bottom, and sides.

[0027] In an embodiment an apparatus comprises: a substrate having a first lattice constant; an EPI layer, having a second lattice constant different from the first lattice constant, including a bottom portion and opposing sidewall portions; and a transistor channel including the EPI layer; wherein the bottom portion includes a recess. In an embodiment the recess is collinear with a long axis of a fin included in the apparatus. In an embodiment the bottom portion includes a recess formed by a fin. In an embodiment the recess may exist where a portion of a fin once existed. However,

other portions of the fin may remain (e.g., in a source/drain region and/or in a support column) and those portions may align with void or recess.

[0028] In an embodiment the EPI layer is unannealed. In an embodiment the EPI layer may, in another embodiment, also be located nonadjacent to any ART trench. In an embodiment the EPI layer is wider than the fin (as judged by the fin's short horizontal axis and not the fin's long horizontal axis). In an embodiment the fin and the EPI layer meet at a junction point and a maximum width of the EPI layer is greater than a width of the fin at the junction point. The EPI layer is wider than the fin's short horizontal axis. In other embodiments the EPI layer is not wider than the fin.

[0029] While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

- 1 1. An apparatus comprising:  
2 a fin structure having a first lattice constant and a top and opposing sidewall  
3 portions extending from the top towards a substrate; and  
4 an epitaxial (EPI) layer, having a second lattice constant different than the first  
5 lattice constant, formed on one of the top and sidewall portions;  
6 wherein the EPI layer comprises one of a group IV material and a group III-V  
7 material and the fin structure includes Si.
- 1 2. The apparatus of claim 1 wherein the EPI layer is formed on the top and  
2 sidewall portions.
- 1 3. The apparatus of claim 1 wherein the EPI layer comprises the group III-V  
2 material.
- 1 4. The apparatus of claim 3 wherein the EPI layer is included in a channel of a  
2 transistor and couples to a source and a drain of the transistor.
- 1 5. The apparatus of claim 4 wherein there is no buffer layer between the fin  
2 structure and the EPI layer and the EPI layer directly contacts one of the top and the  
3 sidewall portions.
- 1 6. The apparatus of claim 1 wherein the fin structure includes one of silicon and  
2 a superlattice structure.
- 1 7. The apparatus of claim 1 wherein there is a buffer layer between the fin  
2 structure and the EPI layer, the buffer layer is less than 30 nm thick, and the EPI  
3 layer directly contacts the buffer layer.
- 1 8. The apparatus of claim 7 wherein the critical thickness for the EPI layer is  
2 greater than 3 nm.

1 9. The apparatus of claim 1 wherein the fin is monolithic with the substrate and  
2 the EPI layer includes three portions directly contacting the top and sidewall portions  
3 and the three portions are monolithic with one another.

1 10. The apparatus of claim 1 wherein the EPI layer has a general absence of  
2 defects along its outer perimeter that borders the fin structure.

1 11. An apparatus comprising:  
2 first and second columns each including a column portion comprising a lattice  
3 constant and one of silicon, a IV material, and a III-V material; and  
4 a nanowire including an epitaxial (EPI) layer, the EPI layer (a) having an  
5 additional lattice constant different from the lattice constant, (b) coupling to each  
6 column portion of the first and second columns by one of a direct connection and a  
7 buffer layer that is less than 30 nm thick, and (c) comprising one of a IV material and  
8 a III-V material.

1  
2 12. The apparatus of claim 11 wherein:  
3 the EPI layer includes a first EPI support portion, a second EPI support  
4 portion, and an EPI middle portion coupling the first and second EPI support portions  
5 to one another;  
6 the first and second EPI support portions, but not the EPI middle portion, each  
7 directly contact one of the buffer layer and the column portions of the first and  
8 second columns; and  
9 the EPI layer is included in a transistor channel.

1 13. The apparatus of claim 12 wherein the first and second columns couple to  
2 each other with a coupling portion that includes silicon and the EPI middle portion  
3 directly contacts the silicon of the coupling portion.

1 14. The apparatus of claim 12 the nanowire including an additional EPI layer that  
2 includes an additional first EPI support portion, an additional second EPI support

3 portion, and an additional EPI middle portion coupling the additional first and second  
4 EPI support portions;  
5 wherein the additional first and second EPI support portions couple to the first and  
6 second columns and the additional EPI layer does not directly contact the EPI layer.

1 15. The apparatus of claim 14 wherein the first and second columns couple to  
2 each other with a coupling portion, having opposing faces that each include silicon,  
3 and the EPI middle portion and the additional EPI middle portion directly contact the  
4 opposing faces.

1 16. The apparatus of claim 14 wherein no silicon is located directly between the  
2 EPI middle portion and the additional EPI middle portion and the column portions of  
3 the first and second columns include one of silicon and silicon germanium.

1 17. The apparatus of claim 14, wherein the EPI middle portion includes a top,  
2 bottom, and opposing sidewalls and the apparatus includes a gate surrounding the  
3 top, bottom and opposing sidewalls.

1 18. An apparatus comprising:  
2 a substrate having a first lattice constant;  
3 an epitaxial (EPI) layer, having a second lattice constant different from the first lattice  
4 constant, including a bottom portion and opposing sidewall portions; and  
5 a transistor channel including the EPI layer;  
6 wherein the bottom portion includes a recess.

1 19. The apparatus of claim 18, wherein the recess is collinear with a long axis of a  
2 fin included in the apparatus.

- 1 20. The apparatus of claim 18, wherein the bottom portion includes a recess
- 2 formed by a fin.

1/11

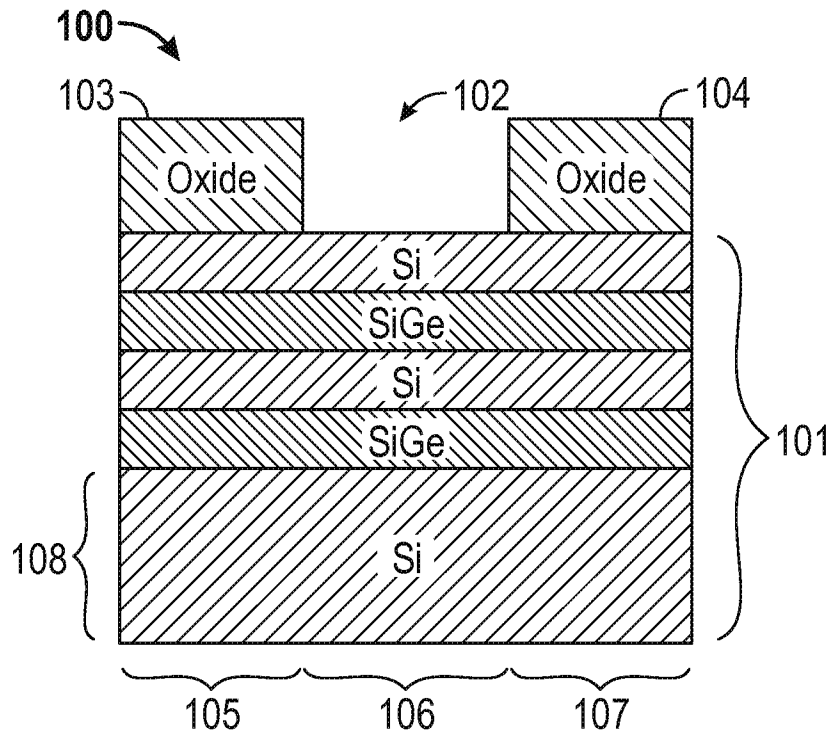


FIG. 1A

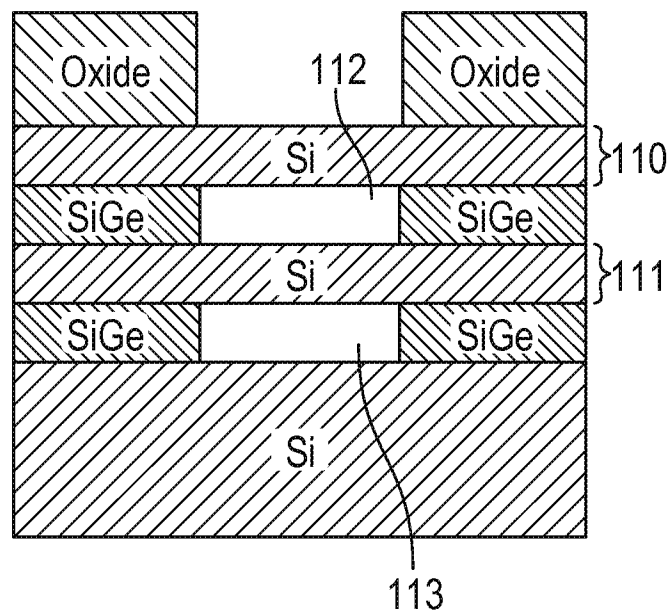


FIG. 1B

2/11

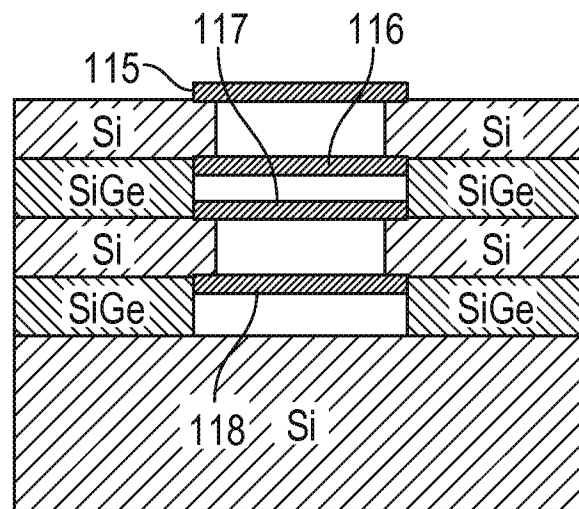


FIG. 1C

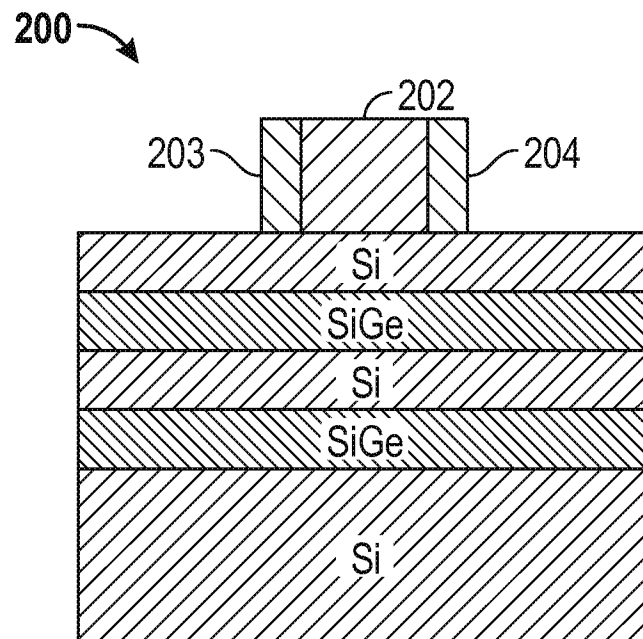


FIG. 2A

3/11

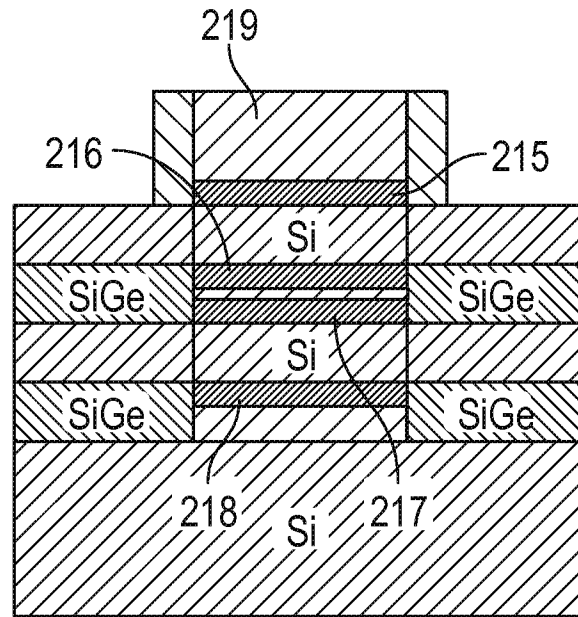


FIG. 2B

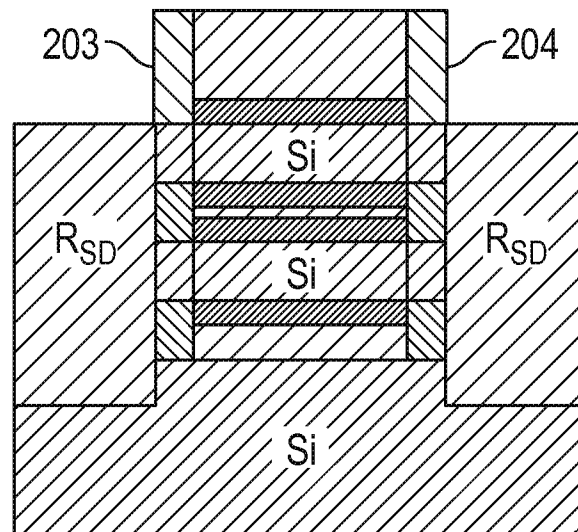


FIG. 2C

4/11

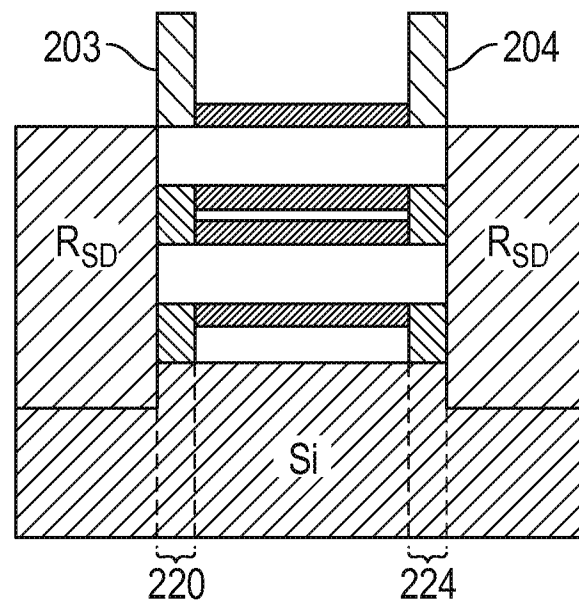


FIG. 2D

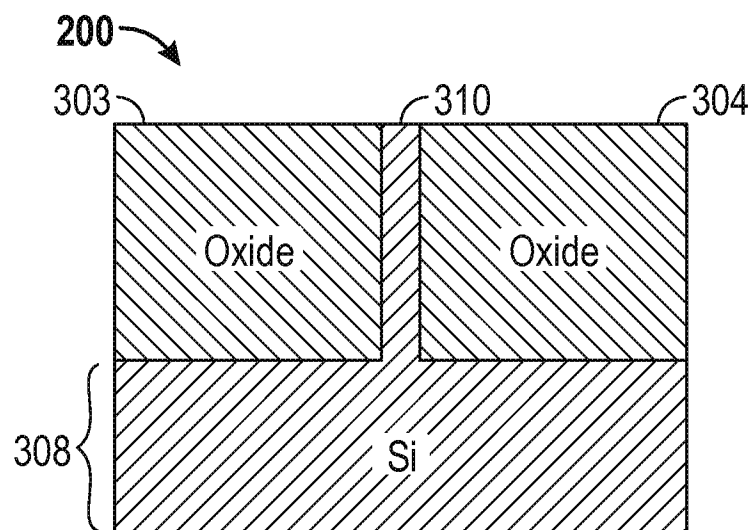


FIG. 3A

5/11

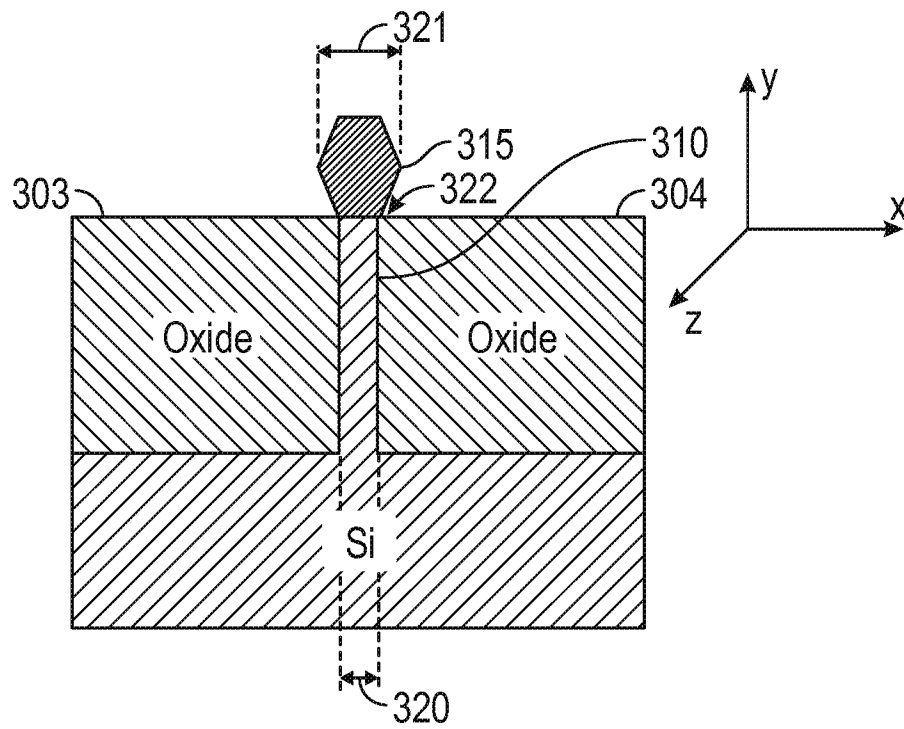


FIG. 3B

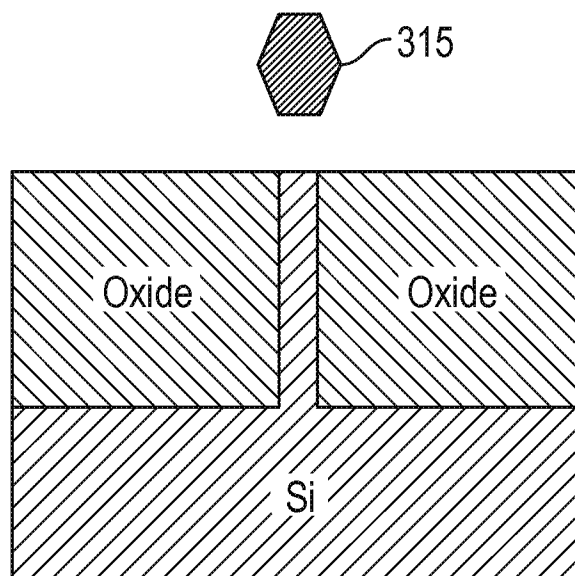


FIG. 3C

6/11

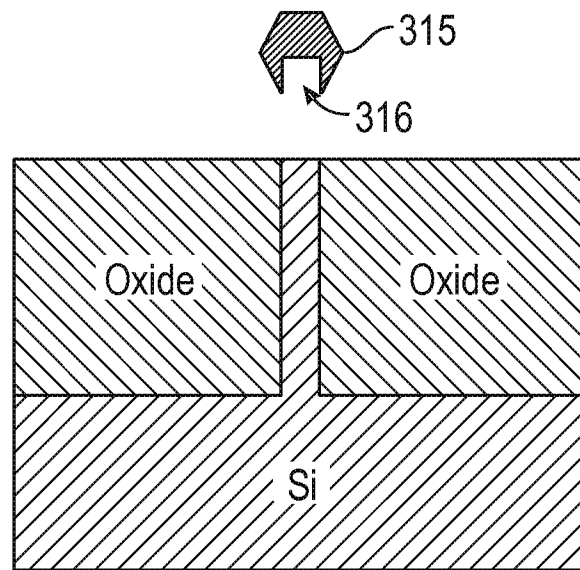


FIG. 3D

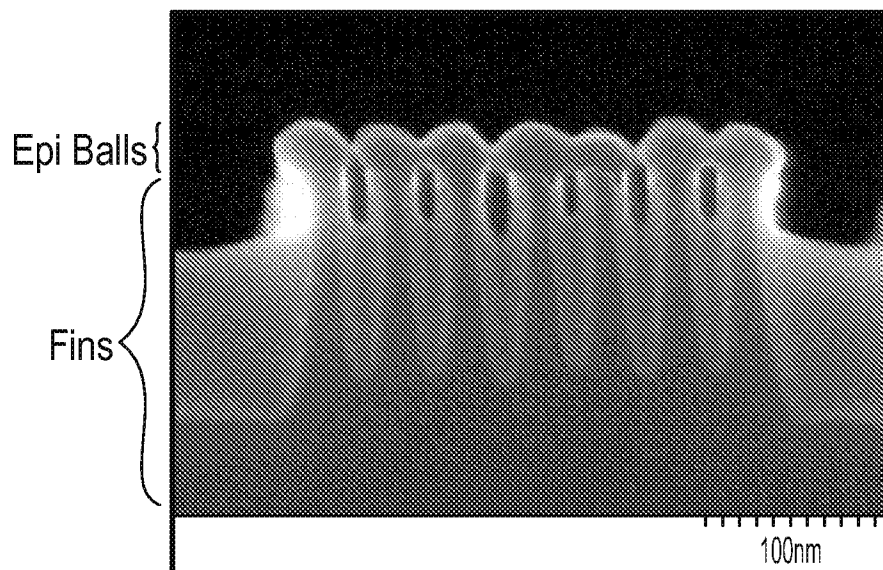


FIG. 4

7/11

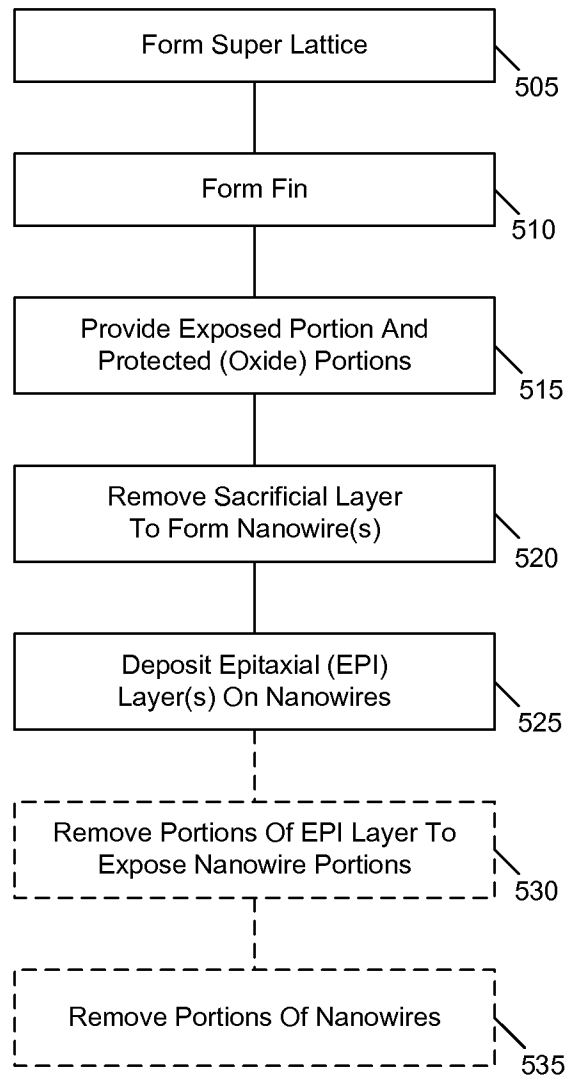
500

FIG. 5

8/11

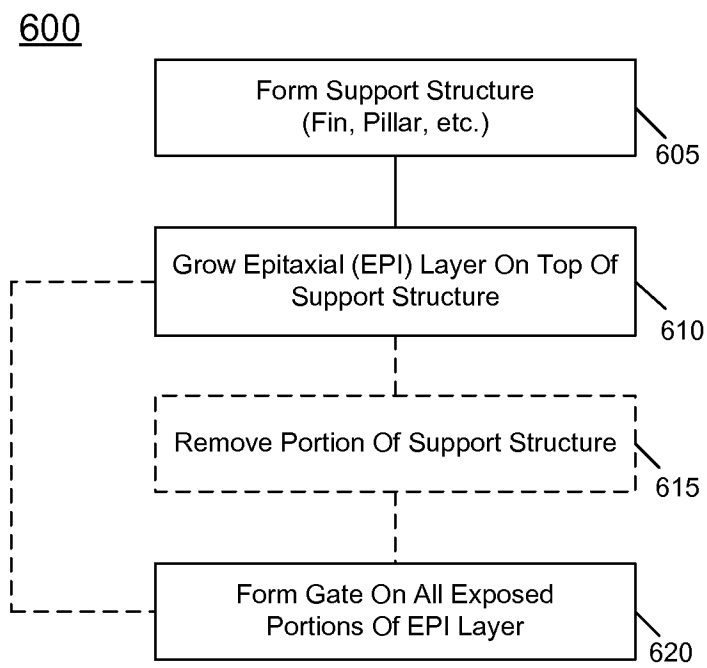


FIG. 6

9/11

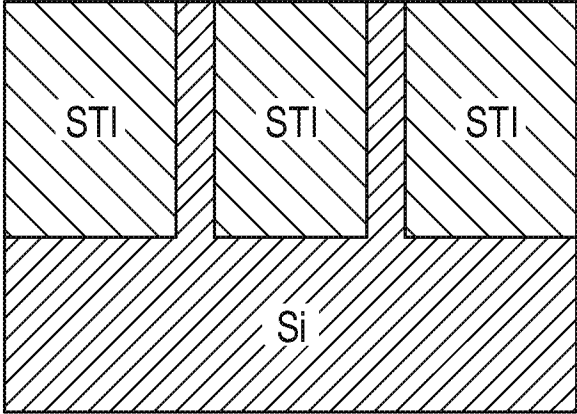


FIG. 7A

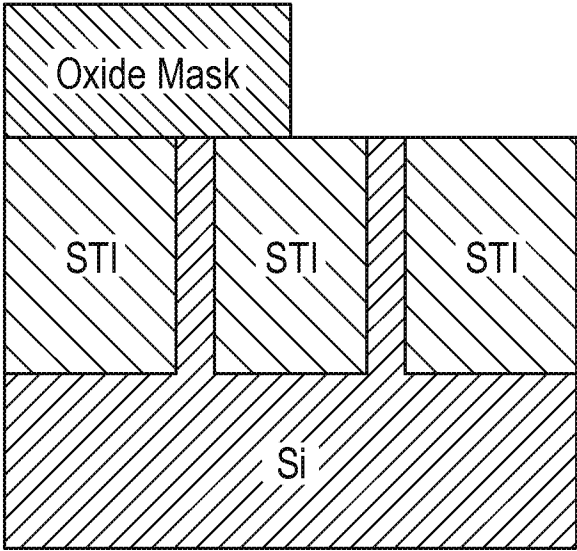


FIG. 7B

10/11

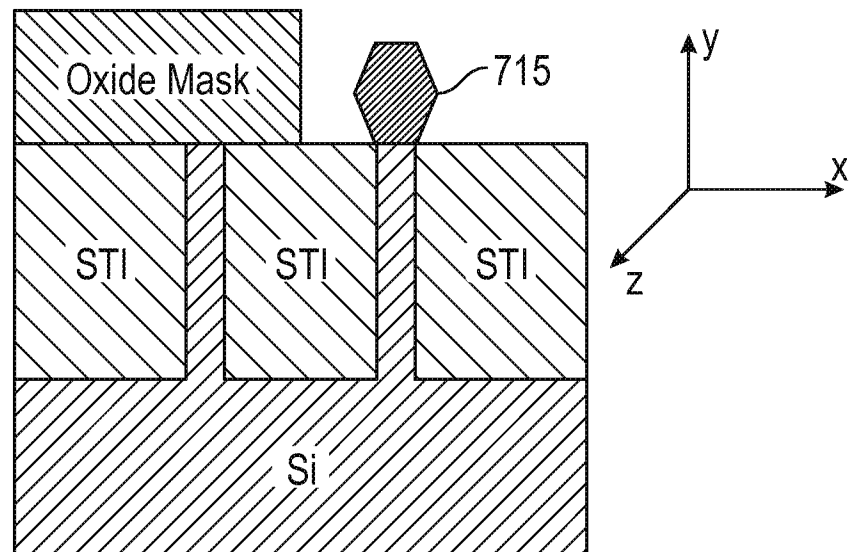


FIG. 7C

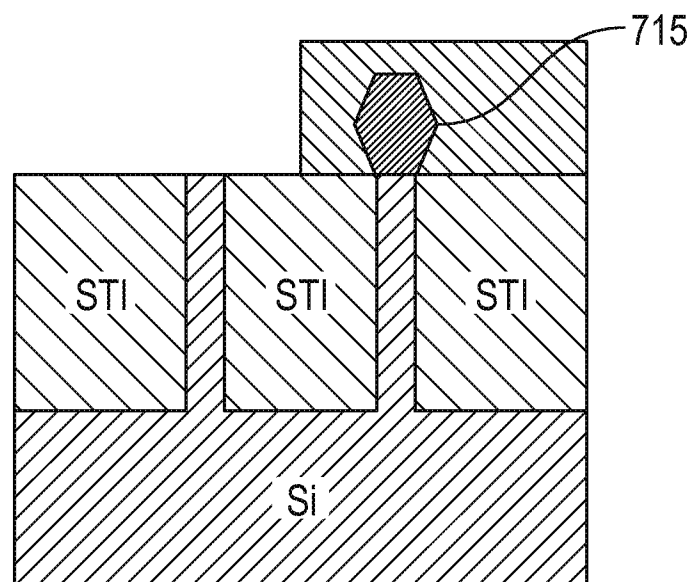


FIG. 7D

11/11

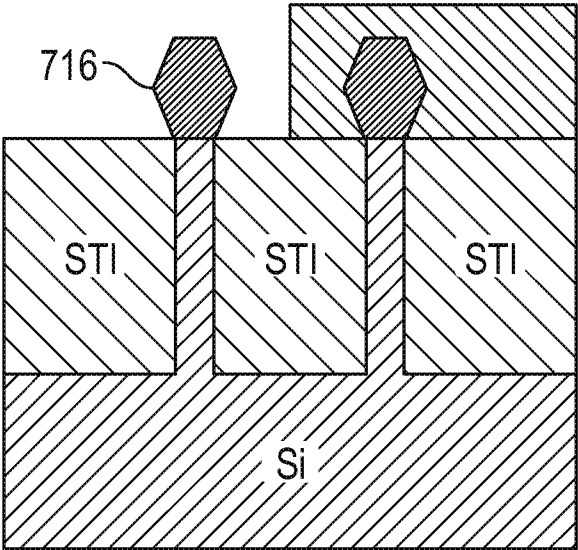


FIG. 7E

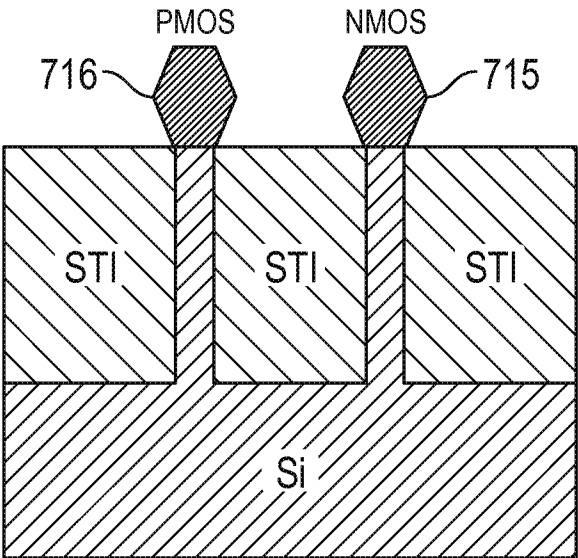


FIG. 7F

**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/20(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/20; H01L 21/205; H01L 21/336; H01L 29/12; H01L 29/78; H01L 27/01; H01L 21/8238; H01L 21/00; H01L 31/109

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) &amp; Keywords: sidewall, lattice constant, EPI, group III-V and fin

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                                  | Relevant to claim No. |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| Y         | US 6803631 B2 (SRIKANTESWARA DAKSHINA-MURTHY et al.) 12 October 2004<br>See column 1, lines 31-40, column 3, line 8 - column 4, line 30, claims 1, 9 and figure 4A. | 1-10                  |
| A         |                                                                                                                                                                     | 11-20                 |
| Y         | US 2009-0085027 A1 (BEEN-YIH JIN et al.) 02 April 2009<br>See paragraphs [0016], [0031], [0048], claim 1 and figures 1A-1B.                                         | 1-10                  |
| A         | US 2012-0187482 A1 (LAHIR S. ADAM et al.) 26 July 2012<br>See paragraphs [0014]-[0028], claims 1-4 and figures 1-7.                                                 | 1-20                  |
| A         | US 7348284 B2 (BRIAN S DOYLE et al.) 25 March 2008<br>See column 5, line 26 - column 6, line 36 and figures 1D-1G.                                                  | 1-20                  |
| A         | US 2005-0130358 A1 (DURESETI CHIDAMBARRAO et al.) 16 June 2005<br>See paragraphs [0034]-[0044], claims 1-10 and figures 7-13.                                       | 1-20                  |



Further documents are listed in the continuation of Box C.



See patent family annex.

\* Special categories of cited documents:

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"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

28 October 2013 (28.10.2013)

Date of mailing of the international search report

**29 October 2013 (29.10.2013)**

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**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/US2013/048797**

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s)                                                                                                                                                                    | Publication<br>date                                                                                                                      |
|-------------------------------------------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|
| US 6803631 B2                             | 12/10/2004          | CN 100521230 C<br>CN 1742375 A<br>EP 1593161 A1<br>JP 2006-516821 A<br>KR 10-2005-0096155 A<br>TW I326489 A<br>US 2004-0145019 A1<br>US 2004-0195627 A1<br>US 6897527 B2<br>WO 2004-068585 A1 | 29/07/2009<br>01/03/2006<br>09/11/2005<br>06/07/2006<br>05/10/2005<br>21/06/2010<br>29/07/2004<br>07/10/2004<br>24/05/2005<br>12/08/2004 |
| US 2009-0085027 A1                        | 02/04/2009          | US 7767560 B2                                                                                                                                                                                 | 03/08/2010                                                                                                                               |
| US 2012-0187482 A1                        | 26/07/2012          | US 2013-134523 A1<br>US 8372705 B2                                                                                                                                                            | 30/05/2013<br>12/02/2013                                                                                                                 |
| US 7348284 B2                             | 25/03/2008          | US 2006-0033095 A1<br>US 2008-0169512 A1<br>US 7960794 B2                                                                                                                                     | 16/02/2006<br>17/07/2008<br>14/06/2011                                                                                                   |
| US 2005-0130358 A1                        | 16/06/2005          | CN 100356525 C<br>CN 1667794 A<br>JP 2005-175495 A<br>JP 4130652 B2<br>US 7198995 B2                                                                                                          | 19/12/2007<br>14/09/2005<br>30/06/2005<br>06/08/2008<br>03/04/2007                                                                       |