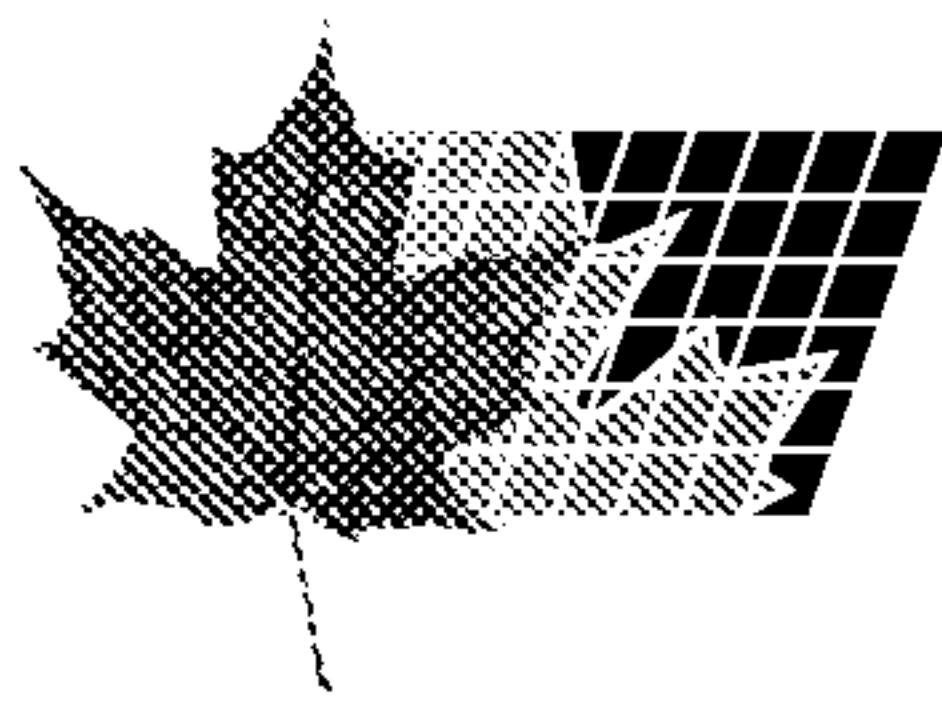




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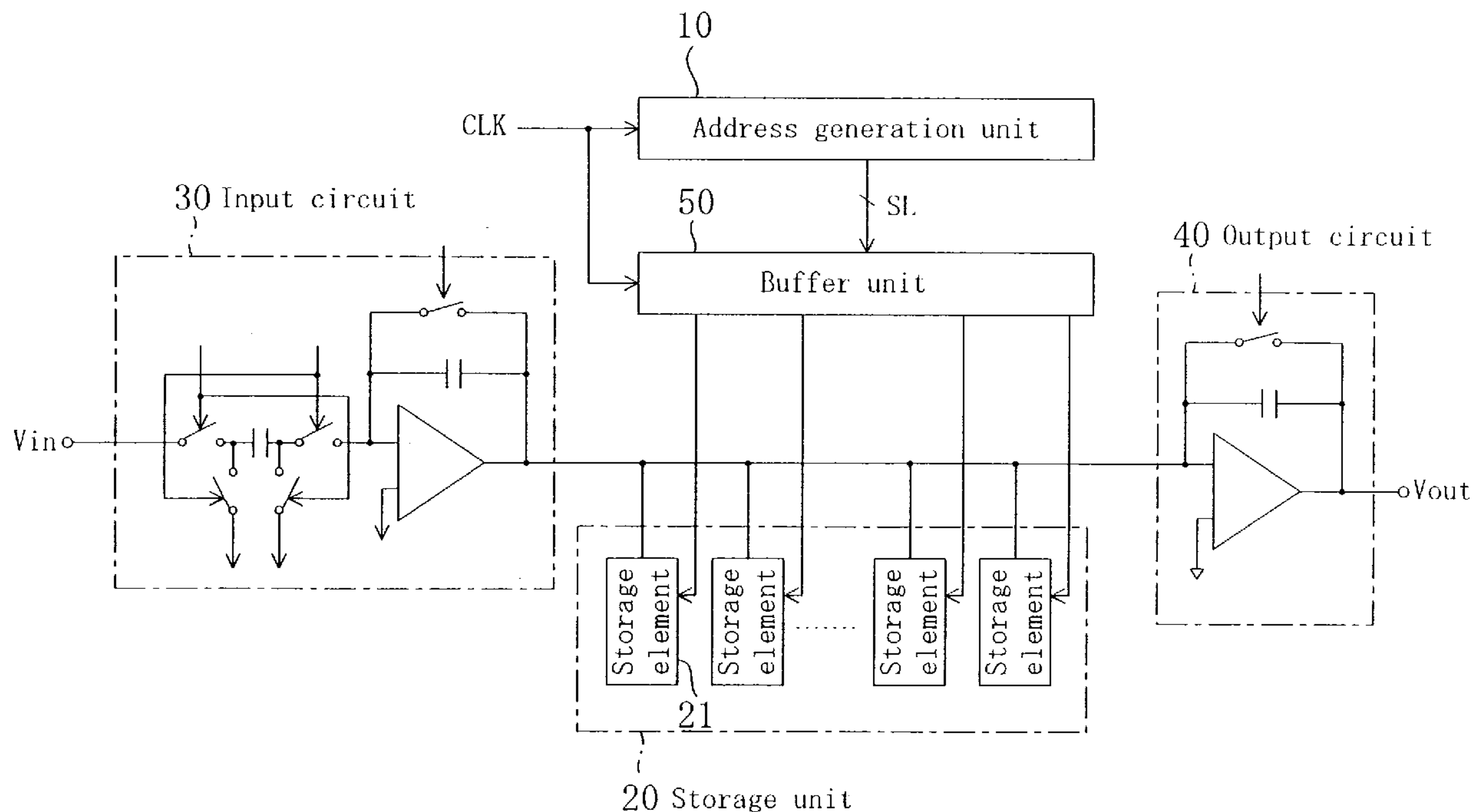
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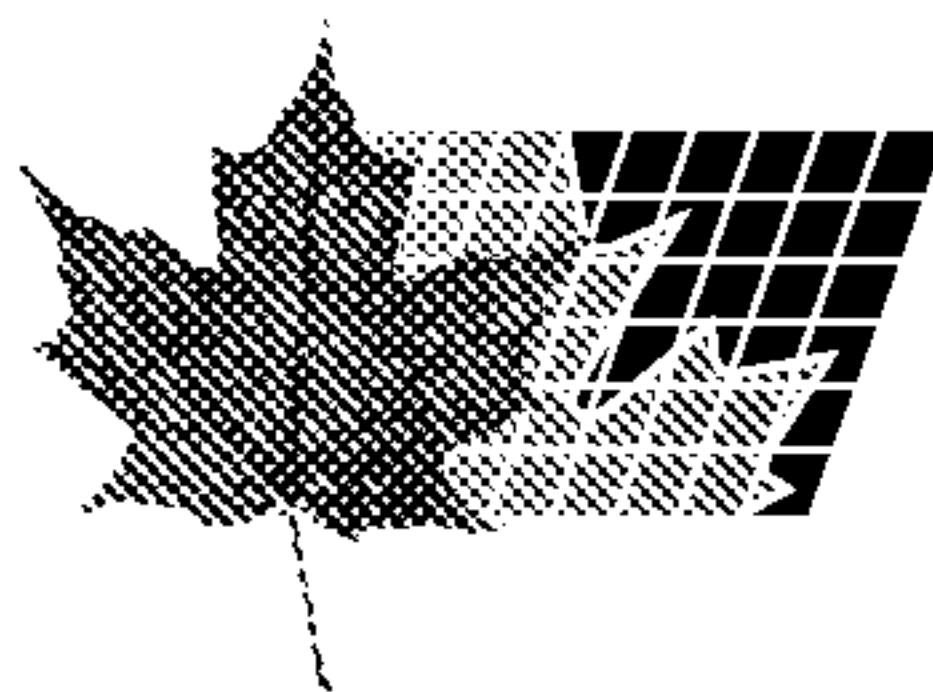
(54) **MEMOIRE ANALOGIQUE ET SYSTEME DE TRAITEMENT
D'IMAGE**

(54) **ANALOG MEMORY AND IMAGE PROCESSING SYSTEM**



(57) Selon cette invention, on réduit le bruit de structure fixe d'une mémoire analogique. Les voies de transmission d'un signal (SL) de sélection d'adresse entre un générateur (10) d'adresses et des mémoires (21) sont conçues de sorte que les caractéristiques électriques, lorsque le signal (SL) de sélection d'adresse commande

(57) The fixed pattern noise of an analog memory is reduced. The transmission paths of an address selection signal (SL) between an address generating unit (10) and memory devices (21) are so constructed so that the electrical characteristics when the address selection signal (SL) drives the memory devices (21) are nearly



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les mémoires (21), soient quasiment uniformes au point que le bruit de structure fixe ne soit pas inclus dans le signal de sortie de la mémoire analogique. Une unité tampon (50), enregistrant provisoirement et émettant le signal de sélection d'adresse, est ménagée entre le générateur (10) d'adresses et les mémoires (21), les caractéristiques de sortie de l'unité tampon (50) étant uniformes pour les mémoires (21). De plus, le câblage entre l'unité tampon (50) et les mémoires (21) est conçu de sorte que ses caractéristiques électriques soient à peu près uniformes. Avec cette structure, le bruit de la traversée de la charge des mémoires (21) peut être à peu près uniforme, et le bruit de structure fixe supprimé.

uniform to an extent that fixed pattern noise is not included in the output signal of the analog memory. A buffer unit (50) which stores the address selection signal temporarily and outputs it is provided between the address generating unit (10) and the memory devices (21) and the output characteristics of the buffer unit (50) are uniform for the memory devices (21). Further, the wiring between the buffer unit (50) and the memory devices (21) are so constructed that the electrical characteristics of the wiring are nearly uniform. With this construction, the charge feed-through noise of the memory devices (21) can be nearly uniform, and the fixed pattern noise can be suppressed.

Abstract

Fixed pattern noise of an analog memory is reduced. Transfer paths of an address selection signal (SL) between an address generation unit (10) and respective storage elements (21) for storing an analog signal are constructed to have a substantially uniform electric characteristic in driving the storage elements (21) by the address selection signal (SL) to such an extent that the output signal of the analog memory is free from fixed pattern noise. A buffer unit (50) for temporarily storing and outputting the address selection signal is provided between the address generation unit (10) and the respective storage elements (21), and the buffer unit (50) is constructed to have an output characteristic substantially uniform between the storage elements (21). Also, lines between the buffer unit (50) and the storage elements (21) are constructed to have substantially the same electric characteristic. In this manner, charge feed through noise of the respective storage elements (21) are made substantially uniform, resulting in suppressing the fixed pattern noise.

· Problems to be solved ·

In the analog memory, a capacity element is generally used as a storage element. However, since a capacity element is easily affected by noise, an offset voltage **Vnoise** resulting from accumulation of noise in the capacity element is added to the input voltage **Vin** of the analog memory. It is known that the offset voltage **Vnoise** is varied depending upon the physical position of a storage element. Specifically, assuming that the storage element has an address **n**, the output voltage **Vout** can be represented by the following formula (1):

$$V_{out} = V_{in} + V_{noise}(n) \quad \dots \quad (1)$$

In other words, the offset voltage **Vnoise** is represented as a function of the address **n** of the storage element. Such an offset voltage **Vnoise(n)** is generally designated as fixed pattern noise.

The fixed pattern noise becomes a serious obstacle when the analog memory is used in image signal processing. In a system dealing with an image signal, the specification of the SN ratio is as strict as -60 dB or less because the eyes of a human being are very sensitive to brightness. Noise appears on a screen unless the fixed pattern noise of the analog memory is reduced so as to satisfy the specification. However, the specification of -60 dB or less is very difficult to attain in an analog circuit.

Various developments have been made so far (for example, Document 1: Matsui, K., T. Matsuura, et al., "CMOS video Filters Using Switched Capacitor 14 MHz Circuits", IEEE J. Solid-State Circuits, pp. 1096 - 1101, 1985; and Document 2: Ken A. Nishimura, Paul R. Gray, "A Monolithic Analog Video Comb Filter in 1.2-um CMOS", IEEE Journal of Solid-State Circuits, VOL. 28, NO. 12,

pp. 1331-1339, December 1993). However, such developments have not been put to practical use due to the fixed pattern noise described above. The problem of the fixed pattern noise has remained unsolved for more than 10 years since the first report.

5

Disclosure of the Invention

The present invention was devised in view of the aforementioned problem, and an object is reducing the fixed pattern noise occurring within an analog memory so as to suppress the harmful influence on picture quality in using the analog memory in the image processing, whereby the analog memory is usable in an image processing system.

Specifically, the analog memory of this invention including plural storage elements for storing an analog signal, comprises an address generation unit for outputting an address selection signal for directing any of the plural storage elements to conduct a write or read operation, and transfer paths of the address selection signal between the address generation unit and the plural storage elements are constructed with a substantially uniform electric characteristic in driving the storage elements by the address selection signal to such an extent that an output signal of the analog memory is free from fixed pattern noise.

In the present analog memory, the electric characteristic in driving the respective storage elements by the address selection signal can be made uniform to the extent that the output signal of the analog memory is free from the fixed pattern noise. Accordingly, the charge feed through noise can be made substantially uniform between the storage elements, resulting

in suppressing the fixed pattern noise occurring in the output signal of the analog memory.

Preferably, the analog memory further comprises temporary storage means for temporarily storing and outputting the address
5 selection signal disposed between the address generation means and the storage elements, and the temporary storage means is constructed to have an output characteristic substantially uniform with respect to the storage elements.

Furthermore, it is preferred that the temporary storage
10 means is provided with respect to each of the storage means and includes plural flip-flops having substantially the same characteristic. In this manner, the temporary storage means having an output characteristic substantially uniform with respect to the respective storage elements can be realized by a very
15 simple circuit configuration.

Moreover, lines between the temporary storage means and the storage elements are preferably constructed to have substantially the same characteristic.

Further preferably, in the analog memory, plural storage
20 elements are arranged in a two-dimensional array forming a storage unit, the address generation unit outputs, as the address selection signal, a row address selection signal for specifying a row of the storage elements in the array and a column address selection signal for specifying a column of the storage elements in the
25 array, first temporary storage means for temporarily storing and outputting the row address selection signal is disposed between the address generation unit and each row of the storage unit, second temporary storage means for temporarily storing and

outputting the column address selection signal is disposed between the address generation unit and each column of the storage unit, and the first temporary storage means is constructed to have an output characteristic substantially uniform with respect to
5 the respective rows of the storage unit and the second temporary storage means is constructed to have an output characteristic substantially uniform with respect to the respective columns of the storage unit.

In this manner, the first and second temporary storage means
10 for suppressing the fixed pattern noise occurring in the output signal of the analog memory are provided with respect to each row and each column of the storage unit. Therefore, as compared with the case where the temporary storage means is provided with respect to each storage element, the circuit scale and the power
15 consumption can be reduced.

Moreover, it is preferred that lines between the first temporary storage means and the storage elements are constructed to have substantially the same electric characteristic, and that lines between the second temporary storage means and the storage
20 elements are constructed to have substantially the same electric characteristic.

In addition, each of the storage elements preferably includes a capacity element; a logic circuit for receiving the row address selection signal and the column address selection signal; and
25 an analog switch disposed between the capacity element and a signal line for transferring an input/output signal to be switched in accordance with an output signal of the logic circuit, and a line between the logic circuit and the analog switch is preferably

constructed to have an electric characteristic substantially uniform between the storage elements.

Alternatively, the analog memory of this invention including plural storage elements for storing an analog signal, comprises
5 an address generation unit for outputting an address selection signal for directing any of the plural storage elements to conduct a write or read operation; and temporary storage means for temporarily storing and outputting the address selection signal disposed between the address generation unit and the storage
10 elements, and the temporary storage means is constructed to have an output characteristic substantially uniform with respect to the plural storage elements.

Moreover, it is possible to realize an image processing system comprising a comb filter including the analog memory of
15 this invention for YC separating a composite signal. This image processing system is applicable to various TV systems including the NTSC system and the PAL system.

Brief Description of Drawings

20 Figure 1 is a diagram for showing the configuration of an analog memory according to Embodiment 1 of the invention.

Figure 2 is a diagram for showing an exemplified configuration of a main part of Figure 1.

Figure 3 is a diagram for showing the configuration of an
25 analog memory according to Embodiment 2 of the invention.

Figure 4 is a diagram for showing the configuration of a storage element of Figure 3.

Figure 5(a) is a schematic diagram for showing the

configuration of a conventional TV signal processing LSI and Figure 5(b) is a schematic diagram for showing the configuration of a TV signal processing LSI using an analog memory of the invention.

Figure 6 is a schematic diagram for showing influence of charge feed through noise on a storage element of an analog memory.

Figure 7 is a diagram for showing an exemplified configuration of a conventional analog memory.

Figures 8(a) and 8(b) are diagrams for explaining cause of occurrence of fixed pattern noise in the conventional analog memory, wherein Figure 8(a) is a diagram for showing an exemplified configuration of an address generation unit of Figure 7 and Figure 8(b) is a diagram for showing a difference in the signal waveform of an address selection signal.

Figure 9 is a diagram for showing whisker noise appearing on a TV screen due to the fixed pattern noise of an analog signal.

Best Mode for Carrying Out the Invention

Before describing embodiments of the present invention, examination made by the present inventors on the cause of occurrence of fixed pattern noise in an analog memory will be described.

Figure 6 is a diagram for showing the basic configuration of a storage element of an analog memory. As is shown in Figure 6, the storage element of the analog memory generally includes a capacity element 71 for storing signal charge, and an analog switch 72 formed from a CMOS circuit and disposed between a signal line DL for transferring an analog signal and the capacity element 71. The analog switch 72 is turned on/off in accordance with a pulse signal applied to the gate thereof. At this point, in

switching the analog switch 72, charge feed through noise is accumulated as charge in the capacity element 71 through a parasitic capacity 73 of the analog switch 72. It seems that the fixed pattern noise is caused due to variation in the amounts of charge
 5 accumulated in respective storage elements.

At this point, the charge feed through noise occurring in a conventional analog memory will be examined.

Figure 7 is a diagram for showing an exemplified circuit configuration of the conventional analog memory. In Figure 7,
 10 an input signal V_{in} is input to a switched capacitor sample and hold circuit 31 of the input circuit 30 so as to be stored in a capacity 31a (with a capacity value $C1$) as charge. The signal stored in the capacity 31a is subsequently transferred to a capacity 32a between input and output (with a capacity value $C2$) of an
 15 operational amplifier 32. Accordingly, the operational amplifier 32 outputs a voltage signal represented by the following formula (2):

$$V_{in} \times C1 / C2 \quad \dots \quad (2)$$

Simultaneously with the output of the voltage signal from the
 20 operational amplifier 32, an analog switch 33 is turned on, so as to connect the output of the operational amplifier 32 to the storage unit 20.

The voltage signal output from the operational amplifier 32 is stored in a capacity element 23 (with a capacity value
 25 $C3$) of a storage element 21 selected by the address generation unit 10. Specifically, an analog switch 22 of the selected storage element 21 is turned on, so as to equalize a voltage applied to the ends of the capacity element 23 to the voltage output

from the operational amplifier 32, and the settling is then completed. In reading a signal from the capacity element 23, an analog switch 41 is turned on, so as to transfer the charge stored in the capacity element 23 to a capacity 40a (with a capacity value C4) of the output circuit 40. Accordingly, the output circuit 40 outputs a voltage signal V_{out} represented by the following formula (3):

$$V_{out} = V_{in} \times (C1 / C2) \times (C3 / C4) \dots \quad (3)$$

It is herein assumed that a cyclic shift register as shown in Figure 8(a) is used as the address generation unit 10. The cyclic shift register is constructed so that a latch 11a at the first stage alone outputs "H" to the storage element 21 in reset.

Thereafter, "H" is successively shifted up to a latch 11h at the eighth stage and cycled to the first latch 11a at the first stage again in synchronization with a clock CLK. In other words, the address generation unit 10 works as a counter so as to successively and repeatedly select each of the storage elements 21.

In the configuration of Figure 8(a), the first latch 11a outputs an inverted output $\overline{NQ}$ while each of the second through eighth latches 11b through 11h outputs a non-inverted output Q. Therefore, the first latch 11a is different in the output characteristic from the second through eighth latches 11b through 11h. Accordingly, an address selection signal SL1 output from the first latch 11a and an output address signal SL2 output from, for example, the second latch 11b have different signal waveforms as is shown in Figure 8(b) in driving the analog switch 22 of the storage element 21. As a result, the amount of charge

accumulated in the capacity element 23 due to the charge feed through noise is different between the storage element driven by the output of the first latch 11a and the storage element driven by the output of any of the other latches 11b through
5 11h.

Accordingly, the offset voltage V_{noise} of the storage element driven by the output of the first latch 11a is naturally different from the offset voltage V_{noise} of the other storage element. This causes the fixed pattern noise. This phenomenon is a fatal
10 fault particularly when the analog memory is used in a TV system.

For example, in reading the same DC signal values stored in the analog memory, a portion corresponding to the signal dealt with by the first latch 11a alone appears as whisker noise on a TV screen as shown in Figure 9.

15 Since an analog memory is occasionally used as a FIFO memory, the aforementioned configuration as a counter is generally adopted for the address generation unit. Actually, the configuration of the address generation unit 10 is more complicated, and hence, when storage elements are directly driven by the address generation
20 unit, the signal waveform in driving the respective storage elements is more largely varied. Also, the operation timing of a storage element to be driven and the electric characteristics, such as a parasitic capacity on a signal path from the address generation unit to each storage element, are varied. These
25 variation also cause the fixed pattern noise, which seems the cause of the occurrence of the whisker noise.

The present invention was devised on the basis of the aforementioned examination. Now, preferred embodiments of the

invention will be described with reference to the accompanying drawings.

EMBODIMENT 1

Figure 1 is a diagram for showing the configuration of an analog memory according to Embodiment 1 of the invention. Like reference numerals are used to refer to like elements used in the conventional analog memory of Figure 7 and the detailed description is omitted.

As is shown in Figure 1, the analog memory of this embodiment is provided with a buffer unit 50 between an address generation unit 10 and a storage unit 20. The buffer unit 50 serving as temporary storage means temporarily stores an address selection signal SL output from the address generation unit 10 and outputs the address selection signal SL to each storage element 21. In outputting the address selection signal SL, the output characteristic is substantially uniform between the respective storage elements 21. The analog switch of each storage element 21 is driven by the address selection signal SL output from the buffer unit 50. Thus, the electric characteristic in driving the respective storage elements 21 by the address selection signal SL is prevented from varying between the storage elements 21.

Figure 2 is a diagram for showing specific configurations of the address generation unit 10, the storage unit 20 and the buffer unit 50 of Figure 1. In Figure 2, the address generation unit 10 is constructed from a cyclic shift register, and the buffer unit 50 includes D flip-flops 51a through 51h respectively corresponding to registers 11a through 11h included in the cyclic

shift register of the address generation unit 10. The analog switches 22 of the respective storage elements 21 are driven by outputs of the D flip-flops 51a through 51h of the buffer unit 50, respectively.

5 In the circuit configuration of Figure 2, the electric characteristic in driving the analog switches 22 of the storage elements 21 by the outputs of the D flip-flops 51a through 51h can be substantially made uniform, and hence, the charge feed through noise can be made substantially uniform between the analog
10 switches 22. Accordingly, no fixed pattern noise occurs in the output signal of the analog memory.

By providing each of the D flip-flops 51a through 51h with the same configuration, the output characteristic of the buffer unit 50 can be made substantially uniform with respect to the
15 respective storage elements 21. Also, the transfer paths of the outputs of the D flip-flops 51a through 51h can be made to have substantially the same electric characteristic by setting lines 52a through 52h connected thereto to have the same length and the same shape. When the analog memory of this embodiment
20 is realized by using an LSI, the mask layout patterns for the lines 52a through 52h for transferring the outputs of the D flip-flops 51a through 51h are preferably designed to be completely the same.

In this manner, the address selection signal SL generated
25 by the address generation unit 10 is temporarily stored in the buffer unit 50 including the D flip-flops 51a through 51h, so as to drive the respective storage elements 21 by the output of the buffer unit 50. Thus, the variation in the electric

characteristic in driving the storage elements 21 can be avoided from the viewpoint of both the circuit configuration and the layout.

As a result, by using the analog memory of this embodiment, the whisker noise as is shown in Figure 9 can be prevented from appearing on the TV screen.

EMBODIMENT 2

In an analog memory according to Embodiment 2 of the invention, storage elements are arranged in a two-dimensional array.

Figure 3 is a diagram for showing the configuration of the analog memory of this embodiment, wherein like reference numerals are used to refer to like elements used in Figure 1 and the detailed description is omitted.

In Figure 3, a storage unit 60 includes storage elements 61 (indicated as "M" in Figure 3) arranged in the two-dimensional array and analog switches 62 disposed on input and output of each row of the array. An address generation unit 10A outputs a row address selection signal SLA and a column address selection signal SLB to the storage unit 60. The row address selection signal SLA is temporarily stored in each D flip-flop (indicated as "DFF" in Figure 3) included in a row buffer unit 50a working as first temporary storage means, and then transferred to each storage element 61 on the corresponding row of the storage unit 60 through a signal line 54. On the other hand, the column address selection signal SLB is temporarily stored in each D flip-flop 53 included in a column buffer unit 50b working as second temporary storage means, and then transferred to each storage element 61 on the corresponding column of the storage unit 60 through a

signal line 55.

Figure 4 is a diagram for showing the configuration of the storage element 61. The storage element 61 has two control input terminals 63a and 63b, at which the row address selection signal SLA and the column address selection signal SLB are respectively received. The row address selection signal SLA and the column address selection signal SLB are input to an AND circuit 64 serving as a logic circuit, and merely when both the row address selection signal SLA and the column address selection signal SLB are "H", the logical level of a signal line SS becomes "H", thereby turning an analog switch 65 on.

The output characteristic of the row buffer unit 50a can be made substantially uniform with respect to the respective rows of the storage unit 60 by providing each of the respective D flip-flops 52 with the same configuration. Also, the output characteristic of the column buffer unit 50b can be made substantially uniform with respect to the respective columns of the storage unit 60 by providing each of the D flip-flops 53 with the same configuration.

Furthermore, the signal lines 54 for transferring the row address selection signal SLA are constructed so as to have an electric characteristic substantially uniform with respect to the respective storage elements 61, and the signal lines 55 for transferring the column address selection signal SLB are constructed to have an electric characteristic substantially uniform with respect to the respective storage elements 61.

Moreover, in each of the storage elements 61, the signal line SS from the logic circuit 64 to the analog switch 65 is

constructed so as to have an electric characteristic uniform between the storage elements 61.

The circuit configuration of the analog memory of this embodiment is particularly effective when the number of the storage
5 elements 61 is large. As described above, in this embodiment, the D flip-flops are disposed on each of the rows and the columns of the storage unit 60 for forming the temporary storage means.

Therefore, the number of the D flip-flops is much smaller than that in Embodiment 1 where the D flip-flops are disposed in the
10 same number as that of the storage elements. Accordingly, this embodiment is remarkably advantageous in the circuit area and power consumption. Furthermore, when the number of the storage elements is large, the circuit shape can be approximated to a square without irregularities by arranging the storage elements
15 in a two-dimensional array. Therefore, the circuit configuration of this embodiment attains another advantage in using the analog memory together with another circuit in LSI design that the length of a wire between circuits can be shortened.

In this manner, in Embodiment 1 of the invention, the electric
20 characteristic in driving the respective storage elements by the address selection signal can be made substantially uniform, which can make substantially uniform the charge feed through noise occurring in the respective storage elements. As a result, the occurrence of the fixed pattern noise in the output signal
25 of the analog memory can be suppressed.

In Embodiment 2 of the invention, the electric characteristic in driving the respective storage elements by the address selection signal can be made substantially uniform even when the storage

elements are arranged in a two-dimensional array, and hence, the occurrence of the fixed pattern noise can be suppressed similarly to Embodiment 1. Also, the number of the D flip-flops for forming the temporary storage means can be reduced, resulting
5 in reducing the circuit area and the power consumption.

Industrial Applicability

The analog memory of this invention is applicable to, for example, an image processing system for processing a TV signal
10 and a video signal.

For example, in a Japanese TV system, storage means for an analog signal is necessary as one component of a comb filter for separating an input composite NTSC signal into a luminance signal (mono-chrome signal) and a color difference signal (color
15 signal). In a currently used TV system, a CCD delay line externally provided to a TV system LSI is used as the storage means for an analog signal as is shown in Figure 5(a). The CCD delay line is thus externally provided because there is conventionally no device usable as the storage means for an analog signal that
20 can be fabricated by the CMOS process or BiCMOS process, that is, the general fabricating procedures for an LSI, and can satisfy the specification required for processing an image signal.

The analog memory of this invention can be used instead of the CCD delay line as the storage means for an analog signal
25 as is shown in Figure 5(b). In this case, the TV system LSI can be fabricated as a whole by the general CMOS process or BiCMOS process including the analog memory of this invention. Accordingly, the TV system LSI can be realized as a completely

one-chip LSI, resulting in largely decreasing the fabrication cost. It is needless to say that the analog memory is applicable to a system other than the NTSC system, for example, the PAL system.

5 Also, another effect can be attained by using the analog memory of this invention instead of the CCD delay line. The CCD delay line tends to emit digital radiated noise (EMI noise) structurally. Therefore, in the conventional TV system, it is necessary to additionally provide means for preventing the
10 influence of the emission noise, such as a noise removing filter.

In contrast, when the TV system LSI is fabricated as a completely one-chip LSI by using the analog memory of this invention, there is no need to provide the means for preventing the noise.

15

CLAIMS

1. An analog memory including plural storage elements each for storing an analog signal, comprising:

an address generation unit for outputting an address selection
5 signal for directing any of said plural storage elements to conduct a write or read operation,

wherein transfer paths of said address selection signal between said address generation unit and said plural storage elements are constructed with a substantially uniform electric
10 characteristic in driving said storage elements by said address selection signal to such an extent that an output signal of said analog memory is free from fixed pattern noise.

2. The analog memory of Claim 1, further comprising temporary storage means for temporarily storing and outputting said address
15 selection signal disposed between said address generation means and said storage elements,

wherein said temporary storage means is constructed to have an output characteristic substantially uniform with respect to said plural storage elements.

20 3. The analog memory of Claim 2,

wherein said temporary storage means includes plural flip-flops provided with respect to each of said storage elements and having substantially the same characteristic.

4. The analog memory of Claim 2,

25 wherein lines between said temporary storage means and said storage elements are constructed to have substantially the same electric characteristic.

5. The analog memory of Claim 1,

wherein said plural storage elements are arranged in a two-dimensional array forming a storage unit,

said address generation unit outputs, as said address selection signal, a row address selection signal for specifying
5 a row of said storage elements in said array and a column address selection signal for specifying a column of said storage elements in said array,

first temporary storage means for temporarily storing and outputting said row address selection signal is disposed between
10 said address generation unit and each row of said storage unit,

second temporary storage means for temporarily storing and outputting said column address selection signal is disposed between said address generation unit and each column of said storage unit, and

15 said first temporary storage means is constructed to have an output characteristic substantially uniform with respect to the rows of said storage unit and said second temporary storage means is constructed to have an output characteristic substantially uniform with respect to the columns of said storage unit.

20 6. The analog memory of Claim 5,

wherein lines between said first temporary storage means and said storage elements are constructed to have substantially the same electric characteristic, and lines between said second temporary storage means and said storage elements are constructed
25 to have substantially the same electric characteristic.

7. The analog memory of Claim 5,

wherein each of said storage elements includes:

a capacity element;

a logic circuit for receiving said row address selection signal and said column address selection signal; and

an analog switch disposed between said capacity element and a signal line for transferring an input/output signal to
5 be switched between a conductive state and a nonconductive state in accordance with an output signal of said logic circuit, and

a line between said logic circuit and said analog switch is constructed to have an electric characteristic substantially uniform between said storage elements.

10 8. An analog memory including plural storage elements each for storing an analog signal, comprising:

an address generation unit for outputting an address selection signal for directing any of said plural storage elements to conduct a write or read operation; and

15 temporary storage means for temporarily storing and outputting said address selection signal disposed between said address generation unit and said storage elements,

wherein said temporary storage means is constructed to have an output characteristic substantially uniform with respect to
20 said plural storage elements.

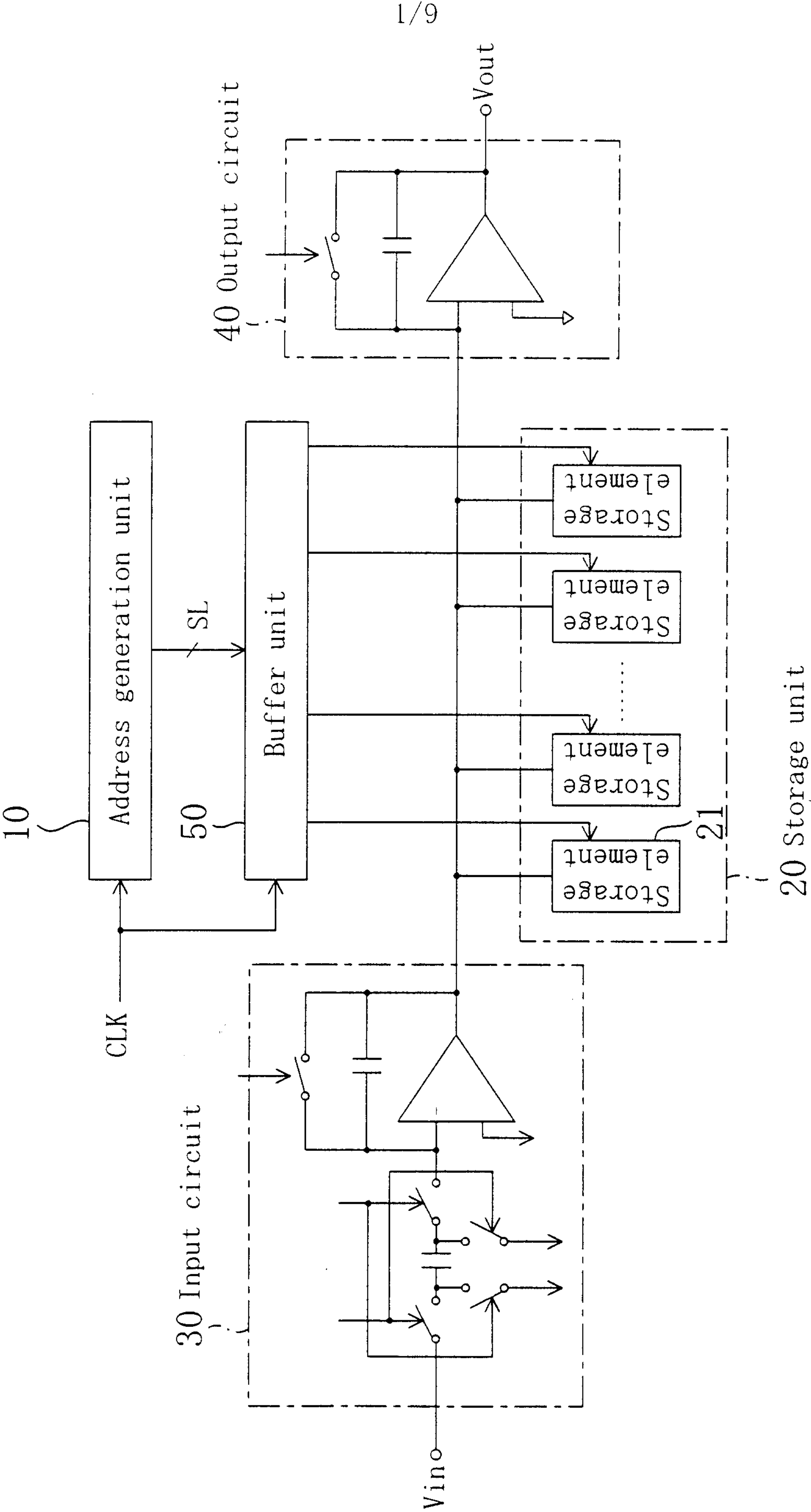
9. An image processing system comprising a comb filter for YC separating a composite signal,

wherein said comb filter includes the analog memory of Claim 1.

25 10. The image processing system of Claim 9,

wherein said image processing system is applicable to an NTSC or PAL system.

Fig. 1



Fi. 2

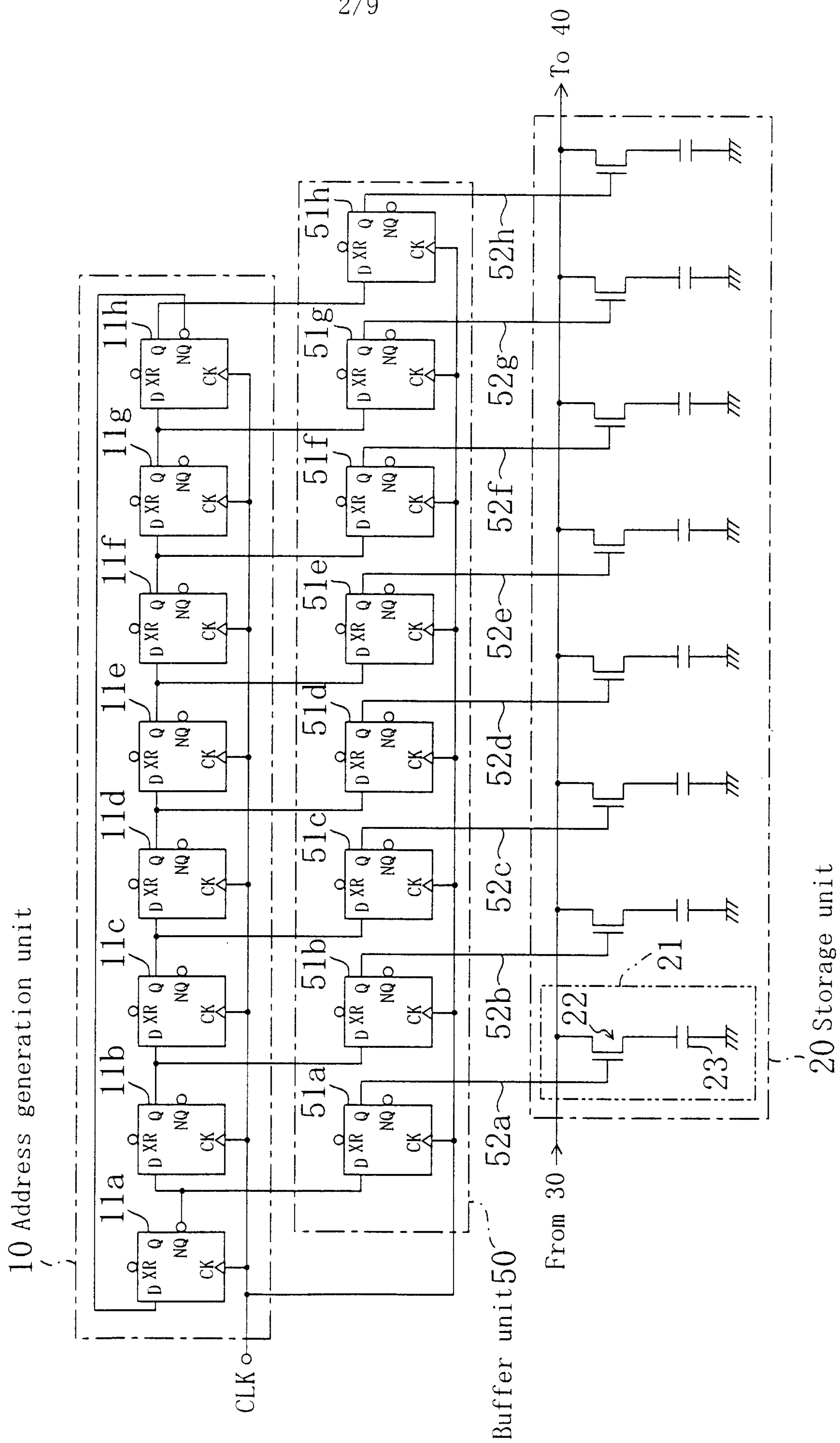
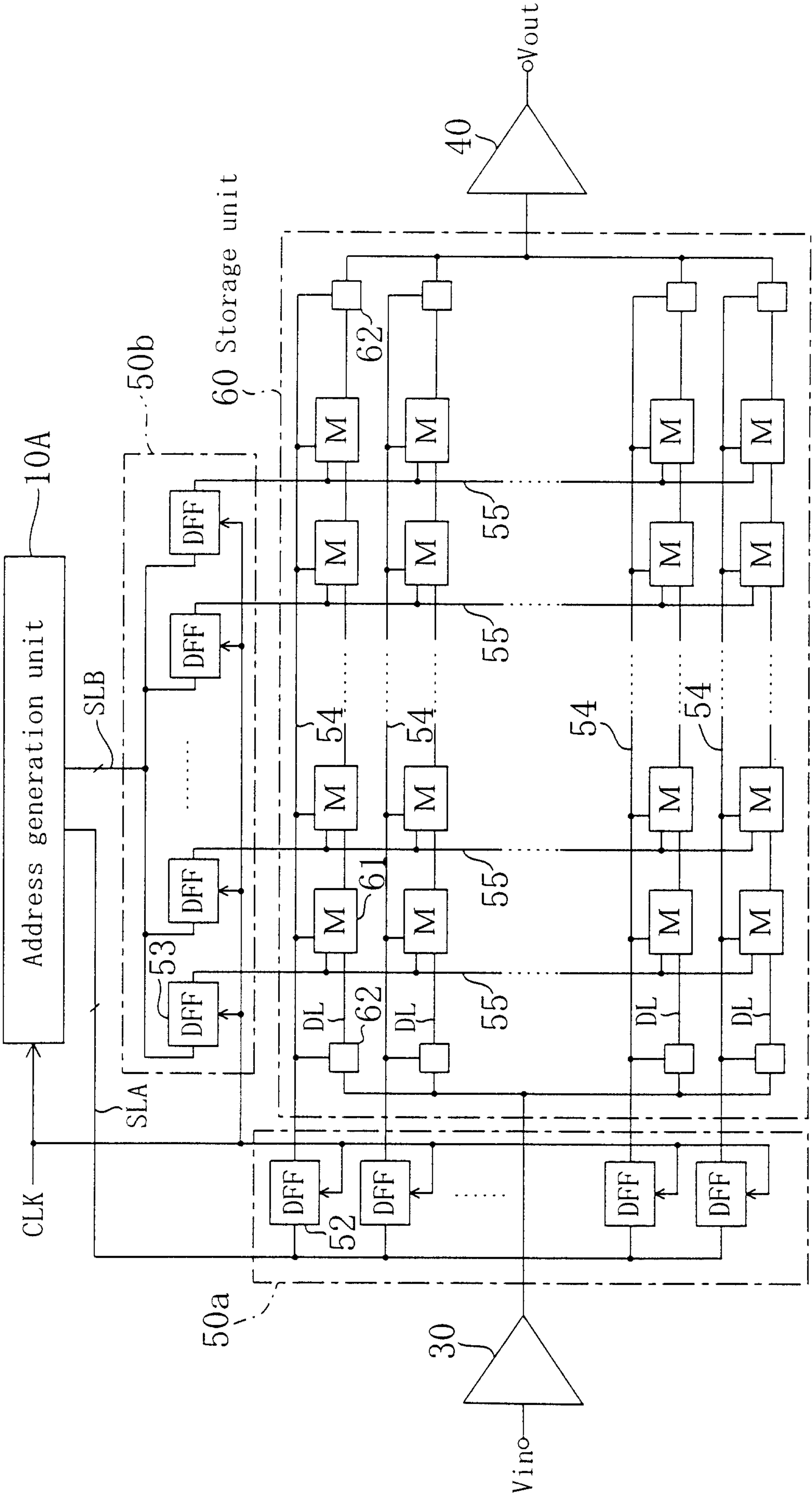


Fig. 3



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Fig. 4

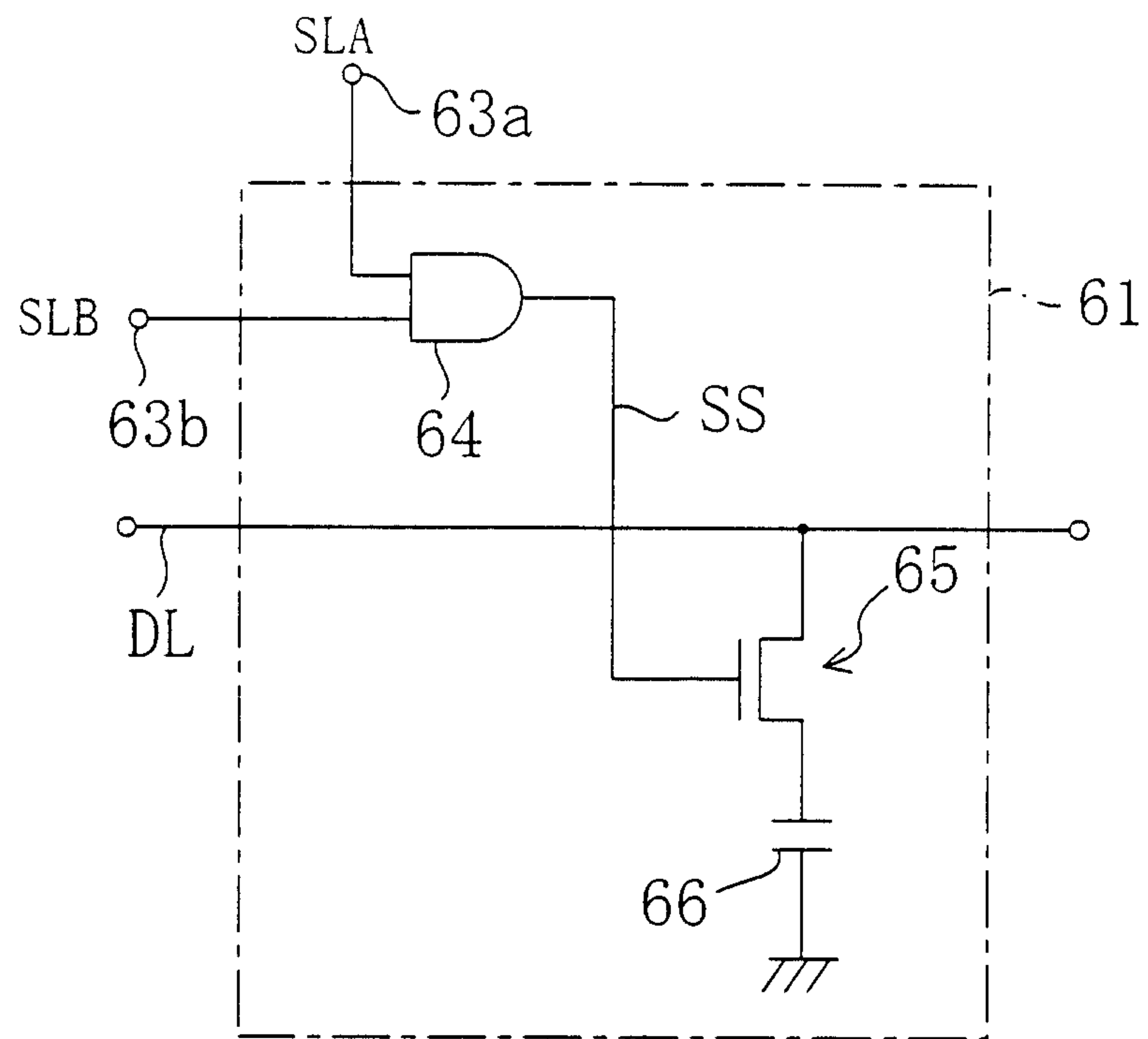


Fig. 5a

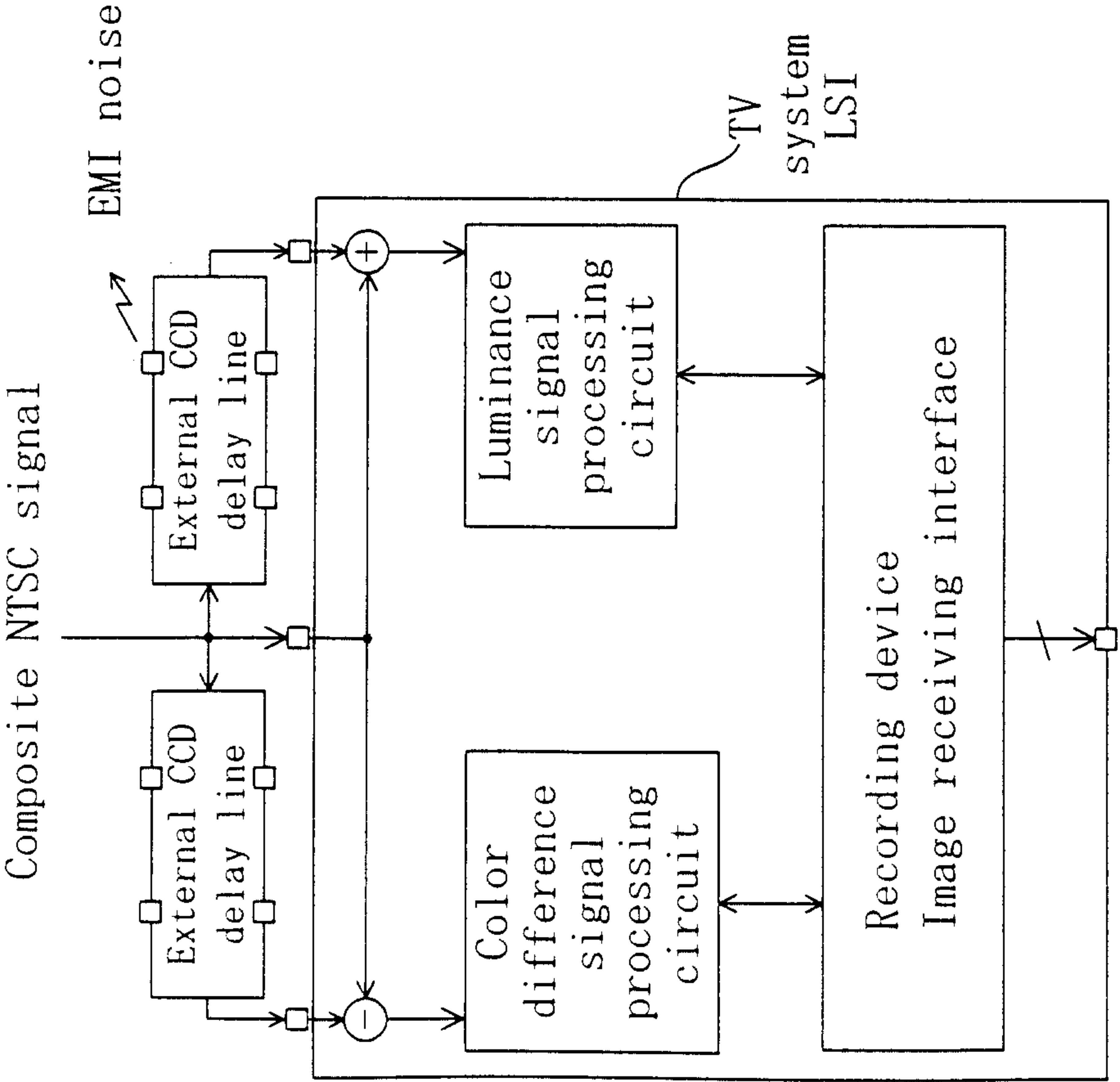
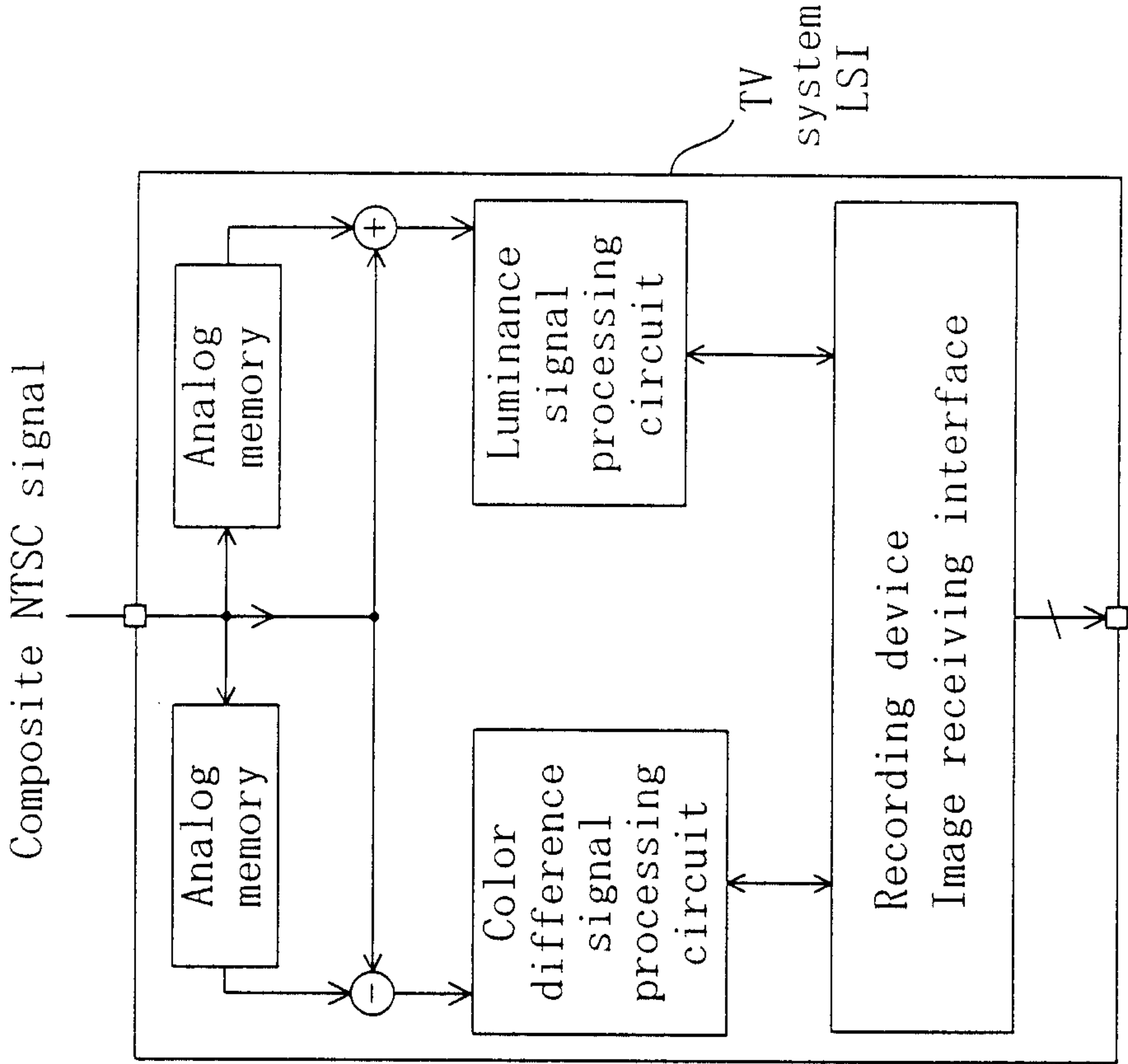


Fig. 5b



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Fig. 6

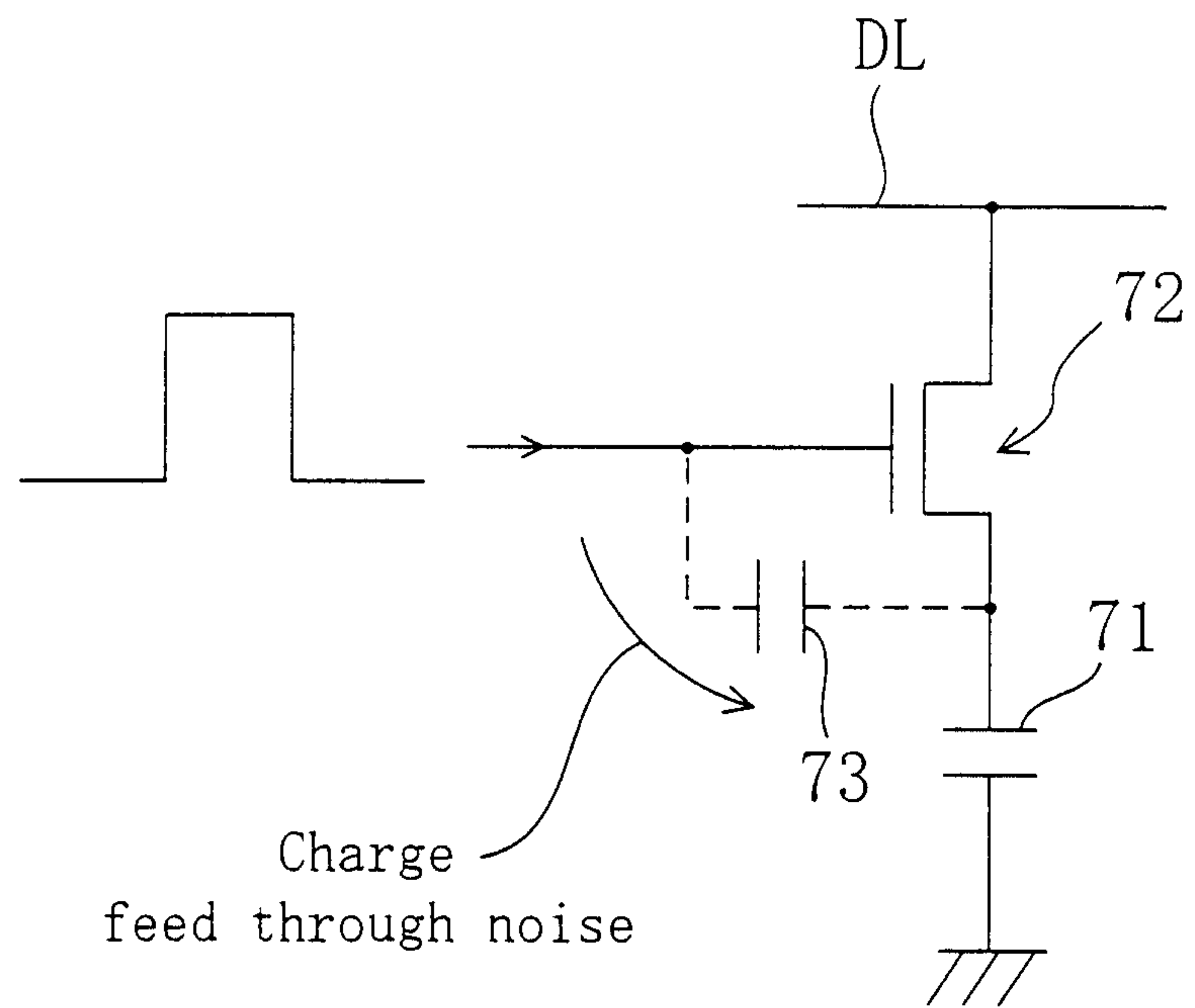


Fig. 7

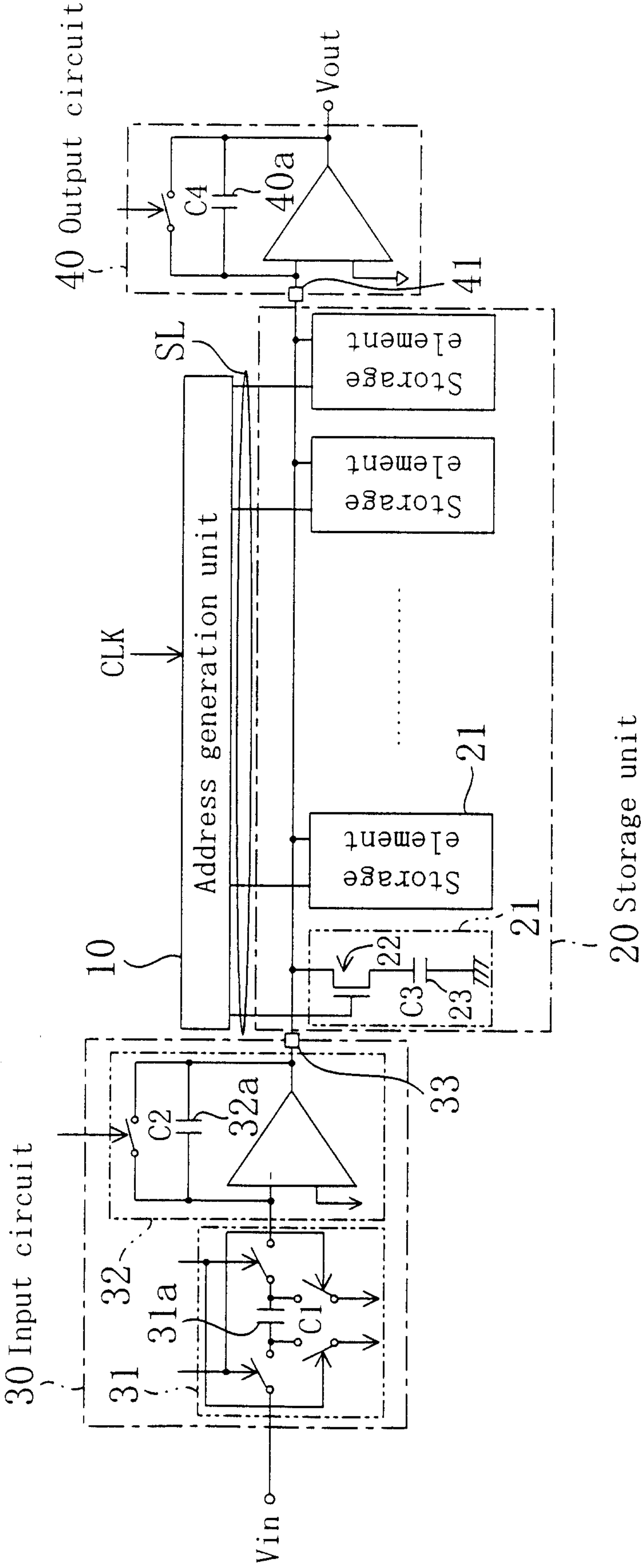


Fig. 8a

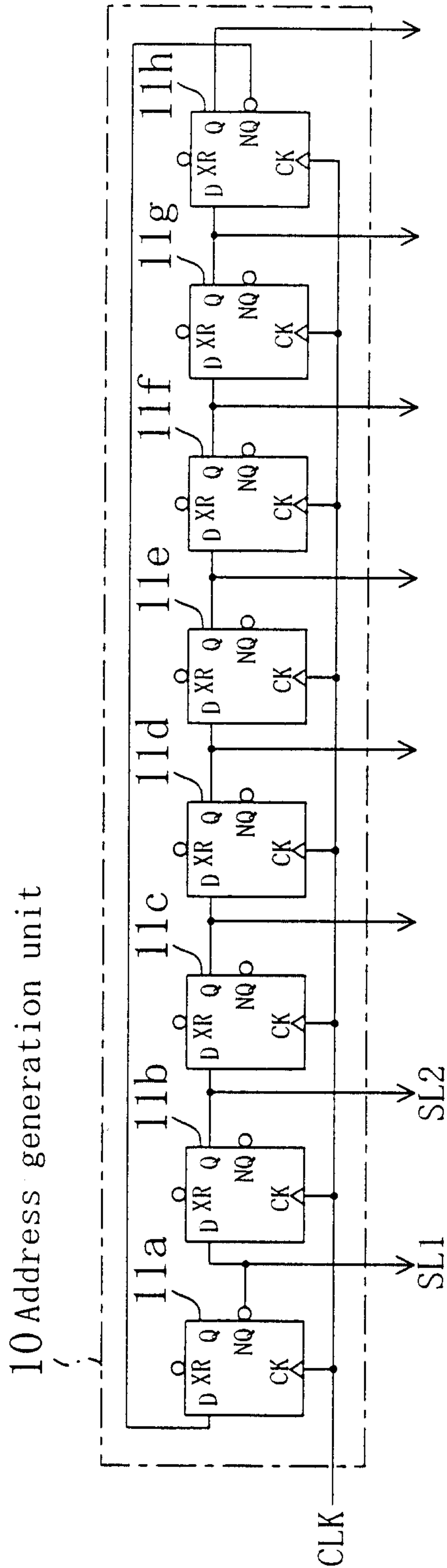
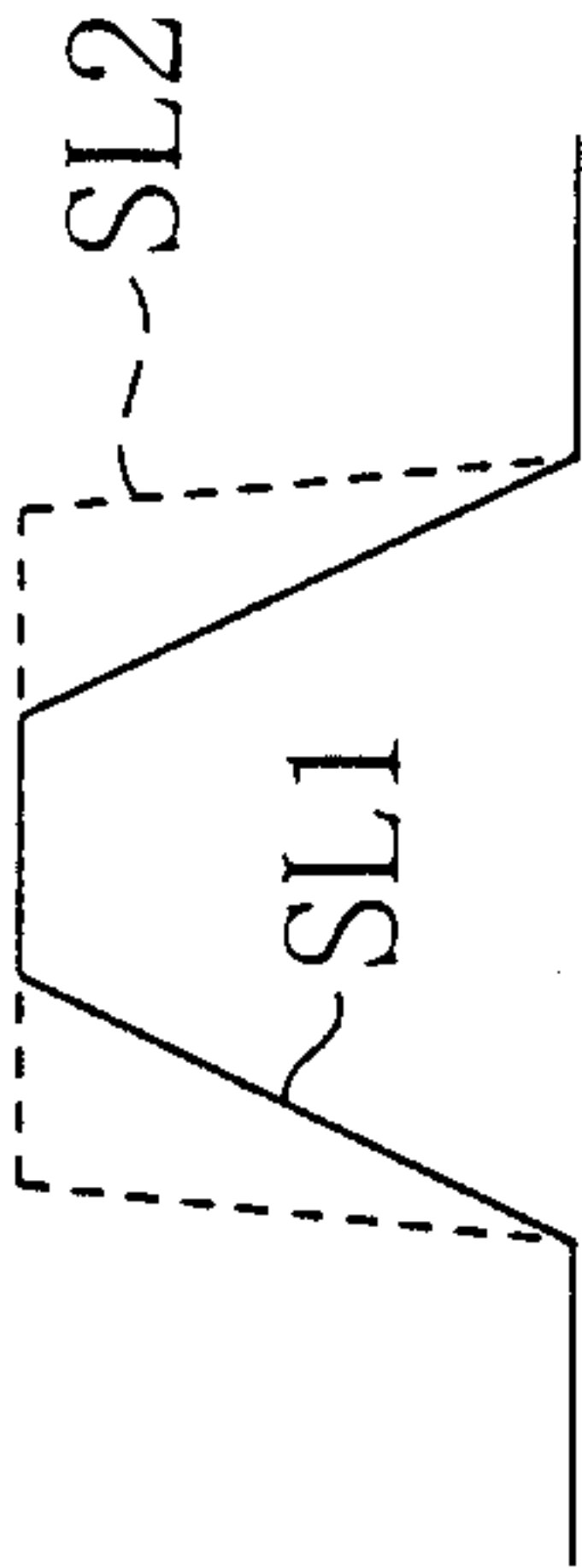


Fig. 8b



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Fig. 9

