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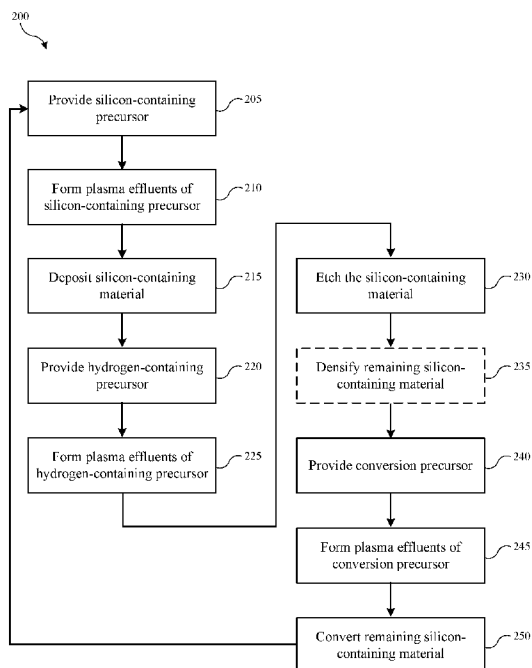


FIG. 2

(57) Abstract: Exemplary processing methods may include providing a silicon-containing precursor to a processing region of a semiconductor processing chamber. A substrate may be housed in the processing region. The substrate may define a feature. The methods may include forming plasma effluents of the silicon-containing precursor and depositing a silicon-containing material on the substrate. The methods may include providing a hydrogen-containing precursor to the processing region, forming plasma effluents of the hydrogen-containing precursor, and etching the silicon-containing material from a sidewall of the feature.

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DENSIFIED SEAM-FREE SILICON-CONTAINING MATERIAL GAP FILL PROCESSES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit and priority of U.S. Patent Application No.
5 18/209,732, filed June 14, 2023, entitled “DENSIFIED SEAM-FREE SILICON-
CONTAINING MATERIAL GAP FILL PROCESSES”, which is hereby incorporated by
reference in its entirety.

TECHNICAL FIELD

10 **[0002]** The present technology relates to semiconductor processing. More specifically, the
present technology relates depositing, etching, and converting materials to form densified
seam-free silicon-containing materials.

BACKGROUND

15 **[0003]** Integrated circuits are made possible by processes which produce intricately
patterned material layers on substrate surfaces. Producing patterned material on a substrate
requires controlled methods of formation and removal of exposed material. As device sizes
continue to shrink, material formation may affect subsequent operations. For example, in gap
filling operations a material may be formed or deposited to fill a trench or other feature
20 formed on a semiconductor substrate. As features may be characterized by higher aspect
ratios and reduced critical dimensions, these filling operations may be challenged. For
example, as the deposition may occur at the top and along sidewalls of the feature, continued
deposition may pinch off the feature including between sidewalls within the feature, and may
produce voids within the feature. This can impact device performance and subsequent
25 processing operations.

[0004] Thus, there is a need for improved systems and methods that can be used to produce
high quality devices and structures. These and other needs are addressed by the present
technology.

SUMMARY

[0005] Exemplary processing methods may include providing a silicon-containing precursor to a processing region of a semiconductor processing chamber. A substrate may be housed in the processing region. The substrate may define a feature. The processing region may be at least partially defined between a faceplate and a substrate support on which the substrate is seated. The methods may include forming plasma effluents of the silicon-containing precursor. The methods may include depositing a silicon-containing material on the substrate. The methods may include providing a hydrogen-containing precursor to the processing region of the semiconductor processing chamber. The methods may include forming plasma effluents of the hydrogen-containing precursor. The methods may include etching the silicon-containing material from a sidewall of the feature with the plasma effluents of the hydrogen-containing precursor.

[0006] In some embodiments, the feature may be characterized by an aspect ratio of greater than or about 1:1. The feature may be characterized by a width across the feature of less than or about 100 nm. The methods may include providing a conversion precursor to the processing region of the semiconductor processing chamber, forming plasma effluents of the conversion precursor, and converting the remaining silicon-containing material to a silicon-and-nitrogen-containing material or a silicon-and-oxygen-containing material. A wet etch rate of the converted silicon-containing material may be less than or about 5 Å/minute. A plasma power source may be operated at greater than or about 20 MHz while converting remaining silicon-containing material to a silicon-and-nitrogen-containing material or a silicon-and-oxygen-containing material. The plasma effluents of the silicon-containing precursor may be formed at a first power level from a plasma power source. The plasma effluents of the hydrogen-containing precursor may be formed at a second power level from the plasma power source greater than the first power level. The plasma effluents of the conversion precursor may be formed at a third power level from a plasma power source greater than the second power level. The methods may include densifying the remaining silicon-containing material within the feature. The densifying may include reducing a hydrogen content of the silicon-containing material to less than or about 30 at.%. The etching may be performed halogen-free. The method may be repeated for a second cycle. A temperature of the substrate may be maintained at a temperature of less than or about 450 °C.

A pressure within the semiconductor processing chamber is maintained at a pressure of greater than or about 1 Torr.

[0007] Some embodiments of the present technology may include semiconductor processing methods. The methods may include i) forming plasma effluents of a silicon-containing precursor. The methods may include ii) depositing a silicon-containing material on a substrate. The substrate may define a feature. The substrate may be seated on a substrate support. The methods may include iii) forming plasma effluents of a hydrogen-containing precursor. The methods may include iv) etching the silicon-containing material from a sidewall of the feature with the plasma effluents of the hydrogen-containing precursor. The methods may include v) forming plasma effluents of a conversion precursor. The methods may include vi) converting remaining silicon-containing material to a silicon-and-nitrogen-containing material or a silicon-and-oxygen-containing material. The methods may include repeating operations i) through vi) to iteratively fill the feature.

[0008] In some embodiments, a thickness of the silicon-containing material at a bottom of the feature may be less than or about 5 nm per cycle. The methods may include applying a bias power to the substrate support while converting remaining silicon-containing material to a silicon-and-nitrogen-containing material or a silicon-and-oxygen-containing material. The etching may fully remove the silicon-containing material from sidewalls of the feature above a base fill of the feature. The conversion precursor may include a nitrogen-containing precursor or an oxygen-containing precursor. The methods may include densifying remaining silicon-containing material within the feature. A temperature of the substrate may be maintained at a temperature of less than or about 350 °C.

[0009] Some embodiments of the present technology may include semiconductor processing methods. The methods may include providing a silicon-containing precursor to a processing region of a semiconductor processing chamber. A substrate may be housed in the processing region. The substrate may define a feature. The processing region may be at least partially defined between a faceplate and a substrate support on which the substrate is seated. The methods may include forming plasma effluents of the silicon-containing precursor. The plasma effluents of the silicon-containing precursor may be formed at a first power level from a plasma power source. The methods may include depositing a silicon-containing material on the substrate. The methods may include providing a hydrogen-containing precursor to the processing region of the semiconductor processing chamber. The methods may include

forming plasma effluents of the hydrogen-containing precursor. The plasma effluents of the hydrogen-containing precursor may be formed at a second power level from the plasma power source greater than the first power level. The methods may include etching the silicon-containing material from a sidewall of the feature with the plasma effluents of the hydrogen-containing precursor. The etching may fully remove the silicon-containing material from sidewalls of the feature above a base fill of the feature. The methods may include densifying remaining silicon-containing material within the feature. The methods may include providing a conversion precursor to the processing region of the semiconductor processing chamber. The methods may include forming plasma effluents of the conversion precursor. The methods may include converting remaining silicon-containing material to a silicon-and-nitrogen-containing material or a silicon-and-oxygen-containing material.

[0010] In some embodiments, the silicon-containing material may be or include amorphous silicon.

[0011] Such technology may provide numerous benefits over conventional systems and techniques. For example, by performing a sequential deposition, etch, and conversion operation according to embodiments of the present technology, sidewall coverage can be limited or controlled, which may limit seam or void formation in small features. Additionally, by performing conversion operations subsequent to etch operations according to embodiments of the present technology, sidewall coverage may be reduced before converting the material which increases resistance of the material to subsequent etching. These and other embodiments, along with many of their advantages and features, are described in more detail in conjunction with the below description and attached figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] A further understanding of the nature and advantages of the disclosed technology may be realized by reference to the remaining portions of the specification and the drawings.

[0013] FIG. 1 shows a schematic cross-sectional view of an exemplary processing chamber according to some embodiments of the present technology.

[0014] FIG. 2 shows exemplary operations in a processing method according to some embodiments of the present technology.

[0015] FIGS. 3A-3C show schematic cross-sectional views of a substrate during a processing according to some embodiments of the present technology.

[0016] Several of the figures are included as schematics. It is to be understood that the figures are for illustrative purposes, and are not to be considered of scale unless specifically stated to be of scale. Additionally, as schematics, the figures are provided to aid comprehension and may not include all aspects or information compared to realistic representations, and may include exaggerated material for illustrative purposes.

[0017] In the appended figures, similar components and/or features may have the same reference label. Further, various components of the same type may be distinguished by following the reference label by a letter that distinguishes among the similar components. If only the first reference label is used in the specification, the description is applicable to any one of the similar components having the same first reference label irrespective of the letter.

DETAILED DESCRIPTION

[0018] Silicon-containing materials may be used in semiconductor device manufacturing for a number of structures and processes, including as a sacrificial material, for example as a dummy gate material, or as a trench fill material, including as a trench bottom isolation material. In gap filling operations, some processing may utilize plasma-enhanced deposition under process conditions to increase the directionality of the deposition, which may allow the deposited material to better fill features on the substrate. In some deposition processes, the deposited material may be characterized by relatively high amounts of hydrogen. The increased amounts of hydrogen may form a material that is less dense than other formed films.

[0019] As feature sizes continue to shrink, plasma-enhanced depositions may be challenged for narrow features, which may be further characterized by higher aspect ratios. For example, pinching of the feature may more readily occur due to deposition on sidewalls of the feature, which in small feature sizes may further restrict flow and deposition further into the feature, and may produce seams or voids in the deposited material. Conventional technologies have attempted to address the formation of seams or voids by performing intermittent etch operations to remove materials from the sidewalls of the features being filled. However, conventional etch operations have required many cycles and/or the use of halogen etchants to remove materials from the sidewalls of the features being filled to limit

seam or void formation. The incorporation of halogen etchants may leave halogen residue that may interfere with further processing operations. Additionally, conventional technologies may form silicon-containing material of poor quality with underperforming mechanical and/or electrical characteristics.

5 **[0020]** The present technology may overcome these limitations by performing an intermittent etch of the formed film that may be halogen-free. The etch may limit or prevent sidewall coverage during trench fill, allowing improved fill operations to be performed. Additionally, the etch may not leave any halogen residues that may interfere with further processing operations. Specifically, the halogen-free etch operations may prevent any non-
10 uniformity in the structure. Further, the present technology may deposit silicon-containing material that may be converted to, for example, silicon-and-nitrogen-containing material or silicon-and-oxygen-containing material with desirable mechanical and/or electrical characteristics. By depositing and converting material according to the present technology high quality materials may be formed.

15 **[0021]** After describing general aspects of a chamber according to some embodiments of the present technology in which plasma processing operations discussed below may be performed, specific methodology may be discussed. It is to be understood that the present technology is not intended to be limited to the specific films, chambers, or processing
20 discussed, as the techniques described may be used to improve a number of film formation processes, and may be applicable to a variety of processing chambers and operations.

[0022] **FIG. 1** shows a cross-sectional view of an exemplary processing chamber 100 according to some embodiments of the present technology. The figure may illustrate an overview of a system incorporating one or more aspects of the present technology, and/or which may perform one or more deposition or other processing operations according to
25 embodiments of the present technology. Additional details of chamber 100 or methods performed may be described further below. Chamber 100 may be utilized to form film layers according to some embodiments of the present technology, although it is to be understood that the methods may similarly be performed in any chamber within which film formation may occur. The processing chamber 100 may include a chamber body 102, a substrate
30 support 104 disposed inside the chamber body 102, and a lid assembly 106 coupled with the chamber body 102 and enclosing the substrate support 104 in a processing volume 120. A substrate 103 may be provided to the processing volume 120 through an opening 126, which

may be conventionally sealed for processing using a slit valve or door. The substrate 103 may be seated on a surface 105 of the substrate support during processing. The substrate support 104 may be rotatable, as indicated by the arrow 145, along an axis 147, where a shaft 144 of the substrate support 104 may be located. Alternatively, the substrate support 104
5 may be lifted up to rotate as necessary during a deposition process.

[0023] A plasma profile modulator 111 may be disposed in the processing chamber 100 to control plasma distribution across the substrate 103 disposed on the substrate support 104. The plasma profile modulator 111 may include a first electrode 108 that may be disposed adjacent to the chamber body 102, and may separate the chamber body 102 from other
10 components of the lid assembly 106. The first electrode 108 may be part of the lid assembly 106, or may be a separate sidewall electrode. The first electrode 108 may be an annular or ring-like member, and may be a ring electrode. The first electrode 108 may be a continuous loop around a circumference of the processing chamber 100 surrounding the processing volume 120, or may be discontinuous at selected locations if desired. The first electrode 108
15 may also be a perforated electrode, such as a perforated ring or a mesh electrode, or may be a plate electrode, such as, for example, a secondary gas distributor.

[0024] One or more isolators 110a, 110b, which may be a dielectric material such as a ceramic or metal oxide, for example aluminum oxide and/or aluminum nitride, may contact the first electrode 108 and separate the first electrode 108 electrically and thermally from a
20 gas distributor 112, also referred to as a faceplate, and from the chamber body 102. The gas distributor 112 may define apertures 118 for distributing process precursors into the processing volume 120. The gas distributor 112 may be coupled with a first source of electric power 142, such as an RF generator, RF power source, DC power source, pulsed DC power source, pulsed RF power source, or any other power source that may be coupled with
25 the processing chamber. In some embodiments, the first source of electric power 142 may be an RF power source.

[0025] The gas distributor 112 may be a conductive gas distributor or a non-conductive gas distributor. The gas distributor 112 may also be formed of conductive and non-conductive components. For example, a body of the gas distributor 112 may be conductive while a face
30 plate of the gas distributor 112 may be non-conductive. The gas distributor 112 may be powered, such as by the first source of electric power 142 as shown in FIG. 1, or the gas distributor 112 may be coupled with ground in some embodiments.

[0026] The first electrode 108 may be coupled with a first tuning circuit 128 that may control a ground pathway of the processing chamber 100. The first tuning circuit 128 may include a first electronic sensor 130 and a first electronic controller 134. The first electronic controller 134 may be or include a variable capacitor or other circuit elements. The first
5 tuning circuit 128 may be or include one or more inductors 132. The first tuning circuit 128 may be any circuit that enables variable or controllable impedance under the plasma conditions present in the processing volume 120 during processing. In some embodiments as illustrated, the first tuning circuit 128 may include a first circuit leg and a second circuit leg coupled in parallel between ground and the first electronic sensor 130. The first circuit leg
10 may include a first inductor 132A. The second circuit leg may include a second inductor 132B coupled in series with the first electronic controller 134. The second inductor 132B may be disposed between the first electronic controller 134 and a node connecting both the first and second circuit legs to the first electronic sensor 130. The first electronic sensor 130 may be a voltage or current sensor and may be coupled with the first electronic controller
15 134, which may afford a degree of closed-loop control of plasma conditions inside the processing volume 120.

[0027] A second electrode 122 may be coupled with the substrate support 104. The second electrode 122 may be embedded within the substrate support 104 or coupled with a surface of the substrate support 104. The second electrode 122 may be a plate, a perforated plate, a
20 mesh, a wire screen, or any other distributed arrangement of conductive elements. The second electrode 122 may be a tuning electrode, and may be coupled with a second tuning circuit 136 by a conduit 146, for example a cable having a selected resistance, such as 50 ohms, for example, disposed in the shaft 144 of the substrate support 104. The second tuning circuit 136 may have a second electronic sensor 138 and a second electronic controller 140,
25 which may be a second variable capacitor. The second electronic sensor 138 may be a voltage or current sensor, and may be coupled with the second electronic controller 140 to provide further control over plasma conditions in the processing volume 120.

[0028] A third electrode 124, which may be a bias electrode and/or an electrostatic chucking electrode, may be coupled with the substrate support 104. The third electrode may
30 be coupled with a second source of electric power 150 through a filter 148, which may be an impedance matching circuit. The second source of electric power 150 may be DC power, pulsed DC power, RF bias power, a pulsed RF source or bias power, or a combination of

these or other power sources. In some embodiments, the second source of electric power 150 may be an RF bias power.

[0029] The lid assembly 106 and substrate support 104 of FIG. 1 may be used with any processing chamber for plasma or thermal processing. In operation, the processing chamber
5 100 may afford real-time control of plasma conditions in the processing volume 120. The substrate 103 may be disposed on the substrate support 104, and process gases may be flowed through the lid assembly 106 using an inlet 114 according to any desired flow plan. Gases may exit the processing chamber 100 through an outlet 152. Electric power may be coupled with the gas distributor 112 to establish a plasma in the processing volume 120. The
10 substrate may be subjected to an electrical bias using the third electrode 124 in some embodiments.

[0030] Upon energizing a plasma in the processing volume 120, a potential difference may be established between the plasma and the first electrode 108. A potential difference may also be established between the plasma and the second electrode 122. The electronic
15 controllers 134, 140 may then be used to adjust the flow properties of the ground paths represented by the two tuning circuits 128 and 136. A set point may be delivered to the first tuning circuit 128 and the second tuning circuit 136 to provide independent control of deposition rate and of plasma density uniformity from center to edge. In embodiments where the electronic controllers may both be variable capacitors, the electronic sensors may adjust
20 the variable capacitors to maximize deposition rate and minimize thickness non-uniformity independently.

[0031] Each of the tuning circuits 128, 136 may have a variable impedance that may be adjusted using the respective electronic controllers 134, 140. Where the electronic controllers 134, 140 are variable capacitors, the capacitance range of each of the variable capacitors, and
25 the inductances of the first inductor 132A and the second inductor 132B, may be chosen to provide an impedance range. This range may depend on the frequency and voltage characteristics of the plasma, which may have a minimum in the capacitance range of each variable capacitor. Hence, when the capacitance of the first electronic controller 134 is at a minimum or maximum, impedance of the first tuning circuit 128 may be high, resulting in a
30 plasma shape that has a minimum aerial or lateral coverage over the substrate support. When the capacitance of the first electronic controller 134 approaches a value that minimizes the impedance of the first tuning circuit 128, the aerial coverage of the plasma may grow to a

maximum, effectively covering the entire working area of the substrate support 104. As the capacitance of the first electronic controller 134 deviates from the minimum impedance setting, the plasma shape may shrink from the chamber walls and aerial coverage of the substrate support may decline. The second electronic controller 140 may have a similar
5 effect, increasing and decreasing aerial coverage of the plasma over the substrate support as the capacitance of the second electronic controller 140 may be changed.

[0032] The electronic sensors 130, 138 may be used to tune the respective circuits 128, 136 in a closed loop. A set point for current or voltage, depending on the type of sensor used, may be installed in each sensor, and the sensor may be provided with control software that
10 determines an adjustment to each respective electronic controller 134, 140 to minimize deviation from the set point. Consequently, a plasma shape may be selected and dynamically controlled during processing. It is to be understood that, while the foregoing discussion is based on electronic controllers 134, 140, which may be variable capacitors, any electronic component with adjustable characteristic may be used to provide tuning circuits 128 and 136
15 with adjustable impedance.

[0033] Processing chamber 100 may be utilized in some embodiments of the present technology for processing methods that may include formation or etching of materials for semiconductor structures. It is to be understood that the chamber described is not to be considered limiting, and any chamber that may be configured to perform operations as
20 described may be similarly used. **FIG. 2** shows exemplary operations in a processing method 200 according to some embodiments of the present technology. The method may be performed in a variety of processing chambers and on one or more mainframes or tools, including processing chamber 100 described above. Method 200 may include a number of optional operations, which may or may not be specifically associated with some
25 embodiments of methods according to the present technology. For example, many of the operations are described in order to provide a broader scope of the structural formation, but are not critical to the technology, or may be performed by alternative methodology as would be readily appreciated. Method 200 may describe operations shown schematically in **FIGS. 3A-3C**, the illustrations of which will be described in conjunction with the operations of
30 method 200. It is to be understood that the figures illustrate only partial schematic views, and a substrate may contain any number of additional materials and features having a variety of characteristics and aspects as illustrated in the figures.

[0034] Method 200 may include additional operations prior to initiation of the listed operations. For example, additional processing operations may include forming structures on a substrate, which may include both forming and removing material. For example, transistor structures, memory structures, or any other structures may be formed. Prior processing
5 operations may be performed in the chamber in which method 200 may be performed, or processing may be performed in one or more other processing chambers prior to delivering the substrate into the semiconductor processing chamber or chambers in which method 200 may be performed. Regardless, method 200 may optionally include delivering a semiconductor substrate to a processing region of a semiconductor processing chamber, such
10 as processing chamber 100 described above, or other chambers that may include components as described above. The substrate may be deposited on a substrate support, which may be a pedestal such as substrate support 104, and which may reside in a processing region of the chamber, such as processing volume 120 described above.

[0035] A substrate on which several operations have been performed may be substrate 305
15 of a structure 300, which may show a partial view of a substrate on which semiconductor processing may be performed. It is to be understood that structure 300 may show only a few top layers during processing to illustrate aspects of the present technology. The substrate 305 may include a material in which one or more features 310 may be formed. Substrate 305 may be any number of materials used in semiconductor processing. The substrate material may be
20 or include silicon, germanium, dielectric materials including silicon oxide or silicon nitride, metal materials, or any number of combinations of these materials, which may be the substrate 305, or materials formed in structure 300. Features 310 may be characterized by any shape or configuration according to the present technology. In some embodiments, the features may be or include a trench structure or aperture formed within the substrate 305.

[0036] Although the features 310 may be characterized by any shapes or sizes, in some
25 embodiments the features 310 may be characterized by higher aspect ratios, or a ratio of a depth of the feature to a width across the feature. For example, in some embodiments features 310 may be characterized by aspect ratios greater than or about 1:1, and may be characterized by aspect ratios greater than or about 2:1, greater than or about 3:1, greater than
30 or about 5:1, greater than or about 10:1, or greater. Additionally, the features may be characterized by narrow widths or diameters across the feature including between two sidewalls, such as a dimension less than or about 100 nm, and may be characterized by a width across the feature of less than or about 90 nm, less than or about 80 nm, less than or

about 70 nm, less than or about 60 nm, less than or about 50 nm, less than or about 40 nm, less than or about 30 nm, less than or about 20 nm, less than or about 17 nm, less than or about 15 nm, less than or about 12 nm, less than or about 10 nm, less than or about 9 nm, less than or about 8 nm, less than or about 7 nm, less than or about 6 nm, less than or about 5 nm, or less.

[0037] In some embodiments, method 200 may include optional treatment operations, such as a pretreatment, that may be performed to prepare a surface of substrate 305 for deposition. Once prepared, method 200 may include providing one or more precursors to a processing region of the semiconductor processing chamber housing the structure 300 at operation 205.

10 The precursors may include one or more silicon-containing precursors, as well as one or more diluents or carrier gases such as an inert gas or other gas delivered with the silicon-containing precursor. Silicon-containing precursors that may be used during the silicon-containing material 315 may include, but are not limited to, silane (SiH_4), disilane (Si_2H_6), trisilane (Si_3H_8), tetrasilane (Si_4H_{10}), pentasilane (Si_5H_{12}), or other organosilanes including
15 cyclohexasilanes, silicon tetrafluoride (SiF_4), silicon tetrachloride (SiCl_4), dichlorosilane (SiH_2Cl_2), tetraethyl orthosilicate (TEOS), as well as any other silicon-containing precursors that may be used in silicon-containing film formation. The silicon-containing material may be nitrogen-free, oxygen-free, and/or carbon-free in some embodiments.

[0038] Deposition plasma effluents may be formed of the deposition precursors including
20 the silicon-containing precursor at operation 210. The deposition plasma effluents may be formed within the processing region, which may allow deposition materials to deposit on the substrate. For example, in some embodiments a capacitively-coupled plasma may be formed within the processing region by applying plasma power to the faceplate or substrate support as previously described.

25 **[0039]** The power applied during deposition may be a lower power plasma, which may limit dissociation, and which may maintain an amount of hydrogen incorporation in the deposited materials. Accordingly, in some embodiments a plasma power source may deliver a plasma power to the faceplate or substrate support of less than or about 300 W, and may deliver a power of less than or about 250 W, less than or about 200 W, less than or about 150
30 W, less than or about 100 W, less than or about 50 W, or less. At plasma powers to the faceplate or substrate support of greater than, for example, 350 W, the substrate 305, such as the sidewalls defining the features 310, may be damaged.

[0040] During the deposition operation, an additional power source, a bias power source, may be engaged and coupled with the substrate support as previously described to provide a bias to the plasma generated above the substrate 305. The bias may draw plasma effluents to the substrate 305, which may increase deposition at the bottom of the features 310. The bias
5 power applied may be relatively low to limit damage to the structure. Accordingly, in some embodiments a bias power source may deliver a plasma power to the faceplate or substrate support of less than or about 1,000 W, and may deliver a power of less than or about 750 W, less than or about 600 W, less than or about 500 W, less than or about 400 W, or less. Additionally, by adjusting the source power and the bias power applied, densification of the
10 deposited silicon-containing material 315 may occur during the deposition operation. In embodiments, both the source power and the bias power may be applied to the substrate support, such as via second source of electric power 150 as previously described.

[0041] A silicon-containing material may be deposited on the substrate at operation 215 from plasma effluents of the silicon-containing precursor. The silicon-containing material
15 may be or include amorphous silicon. The deposited materials may at least partially fill the features on the substrate to provide a bottom-up type of gap fill. As illustrated in FIG. 3A, silicon-containing material 315 may be deposited on the substrate 305, and deposit at the bottom of the features 310, as well as above the features 310 on the substrate 305 and on the sidewalls of the features 310. Although the amount of silicon-containing material 315
20 deposited on the sidewalls may be relatively small or thin, continued formation may cause the features 310 to be pinched off. If pinched off, the formation of a seam or void in the material may occur as the gap fill continues. Accordingly, a series of depositions and etches, as further described below, may be performed to deposit seam-free silicon-containing material 315 in the features 310.

[0042] Subsequent an amount of deposition, in some embodiments of the present
25 technology a treatment or modification process may be formed that is configured to etch back the formed material. This process may be performed in the same chamber as the deposition, and may be performed in a cyclic process to fill the feature. In some embodiments, the silicon-containing precursor flow may be halted and the processing region may be purged.
30 Subsequent a purge, a hydrogen-containing precursor may be provided to the processing region of the semiconductor processing chamber at operation 220. Treatment plasma effluents may be formed at operation 225, which may also be a capacitively-coupled plasma formed within the processing region, although in some embodiments an inductively-coupled

plasma may similarly be applied. The treatment plasma effluents may be formed by applying a plasma power to the faceplate or substrate support, and in some embodiments no other power source may be engaged.

[0043] Similar to the deposition operation, during the treatment operation, the bias power source may be engaged to provide a bias to the plasma generated above the substrate. This may draw plasma effluents to the substrate, which may bombard the film and cause densification of the deposited silicon-containing material 315. Although any hydrogen-containing material may be used, in some embodiments diatomic hydrogen or deuterium may be used as the hydrogen-containing precursor to produce the treatment plasma, along with one or more additional precursors. The hydrogen radicals and ions may readily penetrate the materials formed within the features 310, and may release incorporated hydrogen from the silicon-containing material 315 causing densification. The bias power applied may be relatively low to limit sputtering of the produced film as well as to limit any potential damage to the structure. Materials delivered to form the plasma may similarly have a reduced amount of heavier materials to limit sputtering of the deposited films. Additionally, by adjusting the source power and the bias power applied, an etching operation may be performed, which may reduce sidewall coverage of the deposited material.

[0044] The etch operation may be performed halogen-free. The presence of halogen-containing materials may result in halogen residues remaining in the features 310 subsequent filling of the features 310 with silicon-containing material 315. This halogen residue may contaminate the structure 300, and may cause non-uniformities to result during further processing. Accordingly, the etch operation may be performed without the presence of halogens or halogen-containing materials.

[0045] As previously discussed, hydrogen, or any other hydrogen-containing material may be utilized to generate a plasma within the processing region by delivering power to the faceplate from the plasma power source. The source plasma power in some embodiments may be greater than a plasma power used during the deposition. For example, the plasma power delivered may be greater than or about 100 W, and may be greater than or about 200 W, greater than or about 300 W, greater than or about 400 W, or more. By increasing the source plasma power during the treatment plasma formation, a greater amount of plasma effluents may be generated. However, the source plasma power may be maintained at less than or about 1000 W to not damage the underlying structure, and may be maintained at less

than or about 900 W, less than or about 800 W, less than or about 700 W, less than or about 600 W, or less. Additionally, aspects of the bias power may also be adjusted, which may also limit damage to the underlying structure. For example, the bias power may be maintained below or about 1,000 W, and may be below or about 750 W, below or about 600 W, below or about 500 W, below or about 400 W, or less. While in some operations, a bias power may be higher than a plasma source power, the bias power may alternatively be maintained below the plasma power in other operations.

[0046] Applying greater bias may increase a directionality of delivery perpendicular to a plane across the substrate. Accordingly, by reducing the bias power supplied, the amount of directionality may reduce, which may increase interaction of the plasma effluents within the feature. The plasma effluents may then etch the silicon-containing material 315 at operation 230, and may remove the silicon-containing material 315 from the sidewalls of the features 310. The plasma effluents may fully remove silicon-containing material 315 from the sidewalls of the features 310 above a base fill of the silicon-containing material 315. The base fill of the silicon-containing material may refer to the silicon-containing material 315 deposited at the bottom of the features 310, or on the previously deposited silicon-containing material 315 toward the bottom of the features 310. In embodiments, a ratio of silicon-containing material 315 at the bottom of the feature relative to the sidewall, subsequent etching, may be greater than or about 1:1, such as greater than or about 2:1, greater than or about 3:1, greater than or about 4:1, greater than or about 5:1, greater than or about 6:1 or more. Due to the depth of the feature, silicon-containing material 315 at the bottom of the feature may be etched less due to plasma effluents not reaching the material.

[0047] Simultaneously, or additionally, plasma effluents delivered more directionally may penetrate the remaining silicon-containing material 315 formed at the bottom of the features 310 and/or on the substrate 305. This penetration may reduce hydrogen incorporation to densify the film at optional operation 235. The densification at operation 235 may result from the plasma effluents of one or more precursors or, in embodiments, may be a separate operation using, for example, an inert precursor to densify the remaining silicon-containing material 315. As illustrated in FIG. 3B, silicon-containing material 315 may be removed from sidewalls of the features 310, from overhang regions of the substrate 305, and/or from an upper surface of the substrate 305. This removal may maintain the deposited silicon-containing material 315 at bottom regions of the features 310. The process may also provide a reduced hydrogen incorporation in the remaining material, such as a hydrogen

incorporation of less than or about 40 at.%, and may provide a reduced hydrogen incorporation of less than or about 35 at.%, less than or about 30 at.%, less than or about 25 at.%, less than or about 20 at.%, less than or about 15 at.%, less than or about 10 at.%, less than or about 5 at.%, or less.

5 [0048] Additional adjustments may be made to further increase etching of deposited material along sidewalls of the features by adjusting one or more characteristics of the plasma power or bias power being supplied. For example, in some embodiments both the plasma power source and bias power source may be operated in a continuous wave mode. Additionally, one or both of the power sources may be operated in a pulsed mode. In some
10 embodiments, the source power may be operated in a continuous wave mode or pulsed mode while the bias power is operated in a pulsed mode. A pulsing frequency for the source power may be greater than or about 1 MHz, and may be greater than or about 3 MHz, greater than or about 5 MHz, greater than or about 13.5 MHz, greater than or about 15 MHz, greater than or about 17.5 MHz, greater than or about 20 MHz, greater than or about 22.5 MHz, greater than
15 or about 25 MHz, greater than or about 27.5 MHz, or more. A pulsing frequency for the bias power may be less than or about 5 MHz, and may be less than or about 4 MHz, less than or about 3 MHz, less than or about 2 MHz, or less. The duty cycle of the bias power may be less than or about 75%, and the bias power may be operated at a duty cycle of less than or about 70%, less than or about 60%, less than or about 50%, less than or about 40%, less than
20 or about 30%, less than or about 20%, less than or about 10%, less than or about 5%, or less. By operating the bias power for a reduced duty cycle, such as an on-time duty of less than or about 50%, a greater amount of time per cycle may be performing a more isotropic etch within the feature, which may better remove material from the sidewalls.

[0049] Subsequent to etching the silicon-containing material 315 from a sidewall of the
25 feature with the plasma effluents of the hydrogen-containing precursor, a thickness of the silicon-containing material 315 at a bottom of the feature may be less than or about 5 nm. At greater thicknesses, the subsequent conversion of the silicon-containing material 315 may not treat the entire thickness of the material. Accordingly, a thickness of the silicon-containing material 315 at a bottom of the feature after etching may be less than or about 4.5 nm, less
30 than or about 4 nm, less than or about 3.5 nm, less than or about 3 nm, less than or about 2.5 nm, less than or about 2 nm, less than or about 1.5 nm, less than or about 1 nm, less than or about 0.5 nm, or less.

[0050] In embodiments, the silicon-containing material 315 may be converted to another silicon-containing material. Flow of the hydrogen-containing precursor used during the etching may be halted and the processing region may be purged. Subsequent a purge, a conversion precursor may be provided to the processing region of the semiconductor processing chamber at operation 240. Depending on what the silicon-containing material 315 is to be converted to, the conversion precursor may be or include a nitrogen-containing precursor, an oxygen-containing precursor, or any other precursor useful in semiconductor processing. Exemplary nitrogen-containing precursors may be or include molecular nitrogen (N_2), nitrous oxide (N_2O), ammonia (NH_3), or any other nitrogen-containing material useful in semiconductor processing. In one exemplary embodiment, the nitrogen-containing precursor may include molecular nitrogen (N_2) with molecular hydrogen (H_2). Exemplary oxygen-containing precursors may be or include molecular oxygen (O_2), ozone (O_3), or any other oxygen-containing material useful in semiconductor processing.

[0051] Conversion plasma effluents may be formed of the conversion precursor including the nitrogen-containing precursor or the oxygen-containing precursor at operation 245. The conversion plasma effluents may be formed within the processing region, which may allow the conversion of the remaining silicon-containing material 315 after the etching at operation 230. For example, in some embodiments a capacitively-coupled plasma may be formed within the processing region by applying plasma power to the faceplate or substrate support as previously described. In some embodiments an inductively-coupled plasma may similarly be applied.

[0052] The plasma effluents of the conversion precursor may be formed at a third power level from a plasma power source greater than the second power level. For example, the plasma power source may deliver a plasma power to the faceplate or substrate support of greater than or about 500 W, and may deliver a power of greater than or about 600 W, greater than or about 700 W, greater than or about 800 W, greater than or about 900 W, greater than or about 1,00 W, or more. At plasma powers greater than or about 500 W, full conversion of the material may be achieved. However, in order to prevent damage to the structure, plasma power source may deliver a plasma power to the faceplate or substrate support of less than or about 2,000 W, and may deliver a power of less than or about 1,750 W, less than or about 1,500 W, less than or about 1,250 W, less than or about 1,000 W, or less.

[0053] Similar to the deposition and/or etching operations, during the conversion operation, the bias power source may be engaged to provide a bias to the plasma generated above the substrate. This may draw plasma effluents to the substrate, which may bombard the film and cause sufficient interaction to of the silicon-containing material 315. The bias power applied
5 may be relatively low to limit damage to the structure. Accordingly, in some embodiments a bias power source may deliver a plasma power to the faceplate or substrate support of less than or about 1,000 W, and may deliver a power of less than or about 750 W, less than or about 600 W, less than or about 500 W, less than or about 400 W, or less.

[0054] In embodiments, the plasma power source may be operated at greater than or about
10 20 MHz while converting remaining silicon-containing material 315 to a silicon-and-nitrogen-containing material or a silicon-and-oxygen-containing material. By operating at higher plasma power frequencies, a bias power may not be necessary. A higher frequency plasma power source may generate high density plasma with an increased radical portion compared to a decreased ion portion. The increased radical portion may sufficiently convert
15 the silicon-containing material 315 without the need for bias power. Accordingly, in some embodiments, the conversion operation may be performed without bias power.

[0055] Method 200 may include converting remaining silicon-containing material 315 to, for example, a silicon-and-nitrogen-containing material or a silicon-and-oxygen-containing material. By contacting the remaining silicon-containing material 315 with the conversion
20 precursor, the conversion precursor may modify the structure of the silicon-containing material 315. For example, when the conversion precursor comprises a nitrogen-containing precursor, nitrogen may be incorporated in the remaining silicon-containing material 315 to form silicon-and-nitrogen-containing material. By operating the deposition, etch, and conversion operation to intermittently fill the feature, an entire thickness of the remaining
25 silicon-containing material 315 may be converted.

[0056] Due to the high quality of the material, a wet etch rate of the converted silicon-containing material may be less than or about 5 Å/minute. For example, the wet etch rate of the converted silicon-containing material may be less than or about 4.8 Å/minute, less than or about 4.6 Å/minute, less than or about 4.4 Å/minute, less than or about 4.2 Å/minute, less
30 than or about 4 Å/minute, less than or about 3.8 Å/minute, less than or about 3.6 Å/minute, less than or about 3.4 Å/minute, less than or about 3.2 Å/minute, less than or about 3 Å/minute, or less. Due to the operations of method 200, high quality silicon-containing

material may be deposited and converted that is similar to atomic layer deposition (ALD) quality material. Therefore, the silicon-containing material 315 of the present technology may be characterized by increased wet etch resistance compared to conventional technologies.

5 [0057] The present technology may also provide material with desirable electrical characteristics. For example, a leakage current of the converted silicon-containing material at 2 MV/cm may be maintained at less than or about $1.0\text{E-}7$ A/cm², and may be maintained at less than or about $9.0\text{E-}8$ A/cm², less than or about $8.0\text{E-}8$ A/cm², less than or about $7.0\text{E-}8$ A/cm², less than or about $6.0\text{E-}8$ A/cm², less than or about $5.0\text{E-}8$ A/cm², less than or about
10 $4.0\text{E-}8$ A/cm², less than or about $3.0\text{E-}8$ A/cm², less than or about $2.0\text{E-}8$ A/cm², less than or about $1.0\text{E-}8$ A/cm², or less. Additionally, a breakdown voltage of the converted silicon-containing material at 0.001 A/cm² may be maintained at greater than or about 5.0 MV/cm, and may be maintained at greater than or about 5.5 MV/cm, greater than or about 6.0 MV/cm, greater than or about 6.5 MV/cm, greater than or about 7.0 MV/cm, or higher. Finally, a
15 dielectric constant of the converted silicon-containing material may be less than or about 8, and may be maintained at less than or about 7.8, less than or about 7.6, less than or about 7.4, less than or about 7.2, less than or about 7, or less.

[0058] As shown in FIG. 2, the deposition, etch, and conversion processes may be repeated any number of times in cycles to fill features in embodiments of the present technology. As
20 shown in FIG. 3C, the deposition, etch, and conversion operations may fill features with silicon-containing material 315, such as silicon-and-nitrogen-containing material, silicon-and-oxygen-containing material, or any other silicon-containing material. For example, the processes may be repeated for a second cycle, a third cycle, a fourth cycle, a fifth cycle, a sixth cycle, a seventh cycle, or any number of cycles necessary to fill the features 310 with
25 silicon-containing material 315 to a desired level.

[0059] Temperature and pressure may also impact operations of the present technology. For example, the process may be performed at a temperature below or about 450 °C, and may be performed at a temperature less than or about less than or about 400 °C, less than or about 350 °C, less than or about 300 °C, less than or about 250 °C, less than or about 225 °C, less
30 than or about 200 °C, less than or about 180 °C, less than or about 160 °C, less than or about 140 °C, less than or about 120 °C, less than or about 100 °C, less than or about 80 °C, less than or about 60 °C, less than or about 40 °C, or lower. The temperature may be maintained

in any of these ranges throughout the method, including during the deposition, etching, and conversion. At higher temperatures, crystallized silicon-containing material may be formed instead of an amorphous silicon-containing material. However, the present technology is not limited to amorphous silicon-containing material, as crystallized silicon-containing material
5 may also be etched and converted in subsequent operations. However, higher temperatures may also form higher quality material characterized by increased wet etch resistance, as previously discussed. Accordingly, the process may be performed at a temperature greater than or about 200 °C, and may be performed at a temperature greater than or about less than or about 225 °C, greater than or about 250 °C, greater than or about 275 °C, greater than or
10 about 300 °C, greater than or about 325 °C, greater than or about 350 °C, greater than or about 375 °C, greater than or about 400 °C, or higher.

[0060] Pressure within the semiconductor processing chamber may be kept relatively low for any of the processes as well, such as at a chamber pressure of less than or about 20 Torr, and pressure may be maintained at less than or about 18 Torr, less than or about 16 Torr, less
15 than or about 14 Torr, less than or about 12 Torr, less than or about 10 Torr, less than or about 8 Torr, less than or about 6 Torr, less than or about 4 Torr, less than or about 2 Torr, or less. However, lower pressures may result in a slower fill rate of the features. Additionally, higher pressures may result in reduced pattern loading and/or line bending. Accordingly, pressure within the semiconductor processing chamber may be kept maintained at greater
20 than or about 1 Torr, greater than or about 2 Torr, and pressure may be maintained at greater than or about 3 Torr, greater than or about 4 Torr, greater than or about 5 Torr, greater than or about 6 Torr, greater than or about 7 Torr, or more. By performing processes according to some embodiments of the present technology, improved fill of narrow features utilizing silicon-containing materials may be produced.

25 **[0061]** In the preceding description, for the purposes of explanation, numerous details have been set forth in order to provide an understanding of various embodiments of the present technology. It will be apparent to one skilled in the art, however, that certain embodiments may be practiced without some of these details, or with additional details.

30 **[0062]** Having disclosed several embodiments, it will be recognized by those of skill in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the embodiments. Additionally, a number of well-known processes and elements have not been described in order to avoid unnecessarily obscuring the

present technology. Accordingly, the above description should not be taken as limiting the scope of the technology. Additionally, methods or processes may be described as sequential or in steps, but it is to be understood that the operations may be performed concurrently, or in different orders than listed.

- 5 **[0063]** Where a range of values is provided, it is understood that each intervening value, to the smallest fraction of the unit of the lower limit, unless the context clearly dictates otherwise, between the upper and lower limits of that range is also specifically disclosed. Any narrower range between any stated values or unstated intervening values in a stated range and any other stated or intervening value in that stated range is encompassed. The
- 10 upper and lower limits of those smaller ranges may independently be included or excluded in the range, and each range where either, neither, or both limits are included in the smaller ranges is also encompassed within the technology, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either or both of those included limits are also included.
- 15 **[0064]** As used herein and in the appended claims, the singular forms “a”, “an”, and “the” include plural references unless the context clearly dictates otherwise. Thus, for example, reference to “a silicon-containing precursor” includes a plurality of such precursors, and reference to “the silicon-containing material” includes reference to one or more materials and equivalents thereof known to those skilled in the art, and so forth.
- 20 **[0065]** Also, the words “comprise(s)”, “comprising”, “contain(s)”, “containing”, “include(s)”, and “including”, when used in this specification and in the following claims, are intended to specify the presence of stated features, integers, components, or operations, but they do not preclude the presence or addition of one or more other features, integers, components, operations, acts, or groups.

CLAIMS:

1. A semiconductor processing method comprising:
providing a silicon-containing precursor to a processing region of a
semiconductor processing chamber, wherein a substrate is housed in the processing region,
5 wherein the substrate defines a feature, and wherein the processing region is at least partially
defined between a faceplate and a substrate support on which the substrate is seated;
forming plasma effluents of the silicon-containing precursor;
depositing a silicon-containing material on the substrate;
providing a hydrogen-containing precursor to the processing region of the
10 semiconductor processing chamber;
forming plasma effluents of the hydrogen-containing precursor; and
etching the silicon-containing material from a sidewall of the feature with the
plasma effluents of the hydrogen-containing precursor to provide a remaining silicon-
containing material.
- 15 2. The semiconductor processing method of claim 1, wherein:
the feature is characterized by an aspect ratio of greater than or about 1:1; and
the feature is characterized by a width across the feature of less than or about
100 nm.
- 20 3. The semiconductor processing method of claim 1, further comprising:
providing a conversion precursor to the processing region of the
semiconductor processing chamber;
forming plasma effluents of the conversion precursor; and
converting the remaining silicon-containing material to a silicon-and-nitrogen-
containing material or a silicon-and-oxygen-containing material.
- 25 4. The semiconductor processing method of claim 3, wherein a wet etch
rate of the converted silicon-containing material is less than or about 5 Å/minute.
5. The semiconductor processing method of claim 3, wherein a plasma
power source is operated at greater than or about 20 MHz while converting remaining silicon-
containing material to a silicon-and-nitrogen-containing material or a silicon-and-oxygen-
30 containing material.
6. The semiconductor processing method of claim 1, wherein:

the plasma effluents of the silicon-containing precursor are formed at a first power level from a plasma power source; and

the plasma effluents of the hydrogen-containing precursor are formed at a second power level from the plasma power source greater than the first power level.

5 7. The semiconductor processing method of claim 3, wherein:
the plasma effluents of the silicon-containing precursor are formed at a first power level from a plasma power source;

the plasma effluents of the hydrogen-containing precursor are formed at a second power level from the plasma power source greater than the first power level; and

10 the plasma effluents of the conversion precursor are formed at a third power level from a plasma power source greater than the second power level.

8. The semiconductor processing method of claim 1, further comprising:
densifying the remaining silicon-containing material within the feature,
wherein the densifying comprises reducing a hydrogen content of the silicon-containing
15 material to less than or about 30 at. %.

9. The semiconductor processing method of claim 1, wherein the etching is performed halogen-free.

10. The semiconductor processing method of claim 1, wherein the method is repeated for a second cycle.

20 11. The semiconductor processing method of claim 1, wherein:
a temperature of the substrate is maintained at a temperature of less than or about 450 °C; and

a pressure within the semiconductor processing chamber is maintained at a pressure of greater than or about 1 Torr.

25 12. A semiconductor processing method comprising:
i) forming plasma effluents of a silicon-containing precursor;
ii) depositing a silicon-containing material on a substrate, wherein the substrate defines a feature, wherein the substrate is seated on a substrate support;
iii) forming plasma effluents of a hydrogen-containing precursor;

iv) etching the silicon-containing material from a sidewall of the feature with the plasma effluents of the hydrogen-containing precursor;
v) forming plasma effluents of a conversion precursor;
vi) converting remaining silicon-containing material to a silicon-and-nitrogen-
5 containing material or a silicon-and-oxygen-containing material; and
repeating operations i) through vi) to iteratively fill the feature.

13. The semiconductor processing method of claim 12, wherein a thickness of the silicon-containing material at a bottom of the feature is less than or about 5 nm per cycle.

10 14. The semiconductor processing method of claim 12, further comprising:
applying a bias power to the substrate support while converting remaining silicon-containing material to a silicon-and-nitrogen-containing material or a silicon-and-oxygen-containing material.

15 15. The semiconductor processing method of claim 12, wherein the etching fully removes the silicon-containing material from sidewalls of the feature above a base fill of the feature.

16. The semiconductor processing method of claim 12, wherein the conversion precursor comprises a nitrogen-containing precursor or an oxygen-containing precursor.

20 17. The semiconductor processing method of claim 12, further comprising:
densifying remaining silicon-containing material within the feature.

18. The semiconductor processing method of claim 12, wherein a temperature of the substrate is maintained at a temperature of less than or about 350 °C.

25 19. A semiconductor processing method comprising:
providing a silicon-containing precursor to a processing region of a semiconductor processing chamber, wherein a substrate is housed in the processing region, wherein the substrate defines a feature, and wherein the processing region is at least partially defined between a faceplate and a substrate support on which the substrate is seated;

forming plasma effluents of the silicon-containing precursor, wherein the plasma effluents of the silicon-containing precursor are formed at a first power level from a plasma power source;

depositing a silicon-containing material on the substrate;

5 providing a hydrogen-containing precursor to the processing region of the semiconductor processing chamber;

forming plasma effluents of the hydrogen-containing precursor, wherein the plasma effluents of the hydrogen-containing precursor are formed at a second power level from the plasma power source greater than the first power level;

10 etching the silicon-containing material from a sidewall of the feature with the plasma effluents of the hydrogen-containing precursor, wherein the etching fully removes the silicon-containing material from sidewalls of the feature above a base fill of the feature;

densifying remaining silicon-containing material within the feature;

15 providing a conversion precursor to the processing region of the semiconductor processing chamber;

forming plasma effluents of the conversion precursor; and

converting remaining silicon-containing material to a silicon-and-nitrogen-containing material or a silicon-and-oxygen-containing material.

20 20. The semiconductor processing method of claim 19, wherein the silicon-containing material comprises amorphous silicon.

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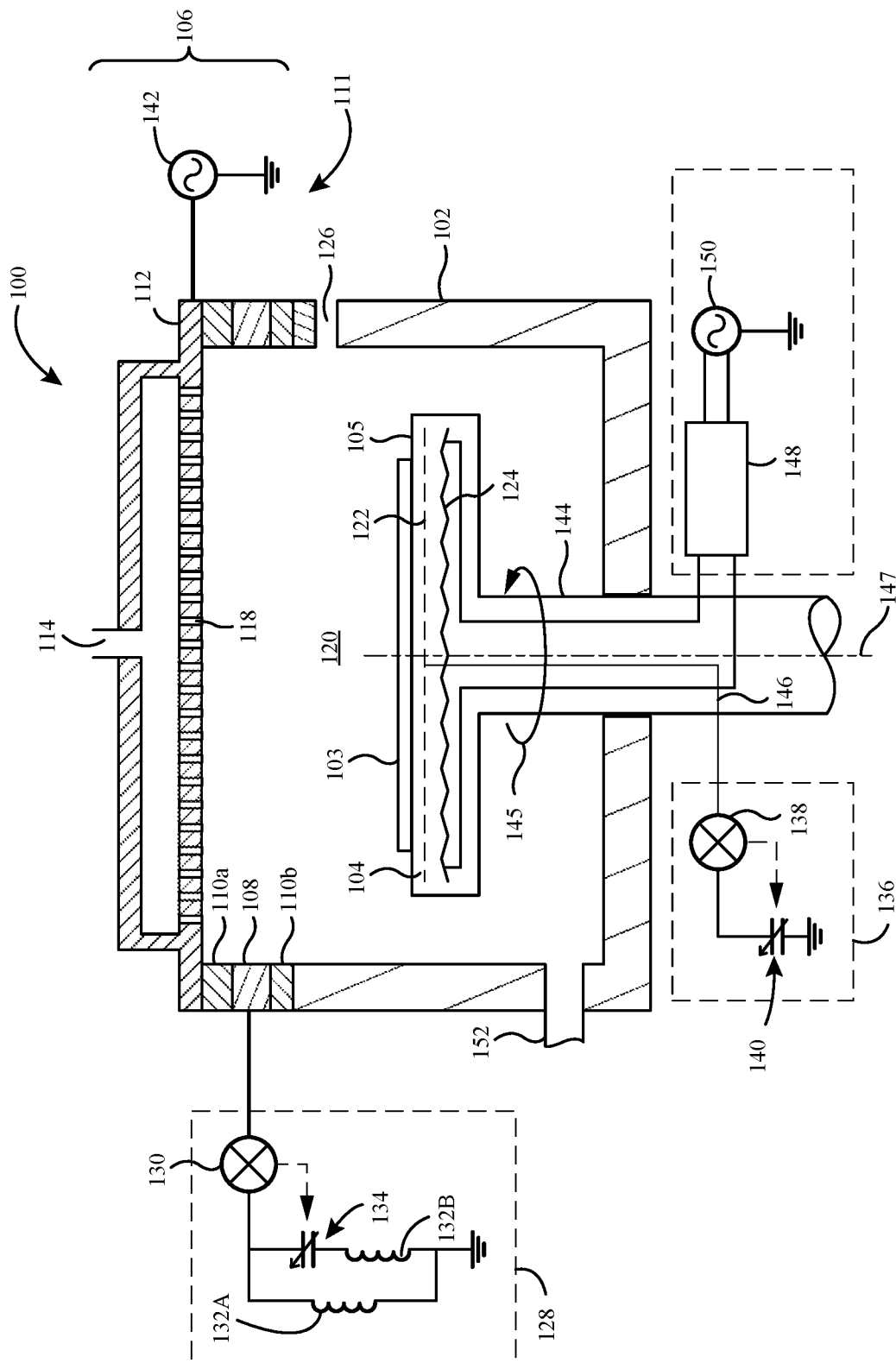


FIG. 1

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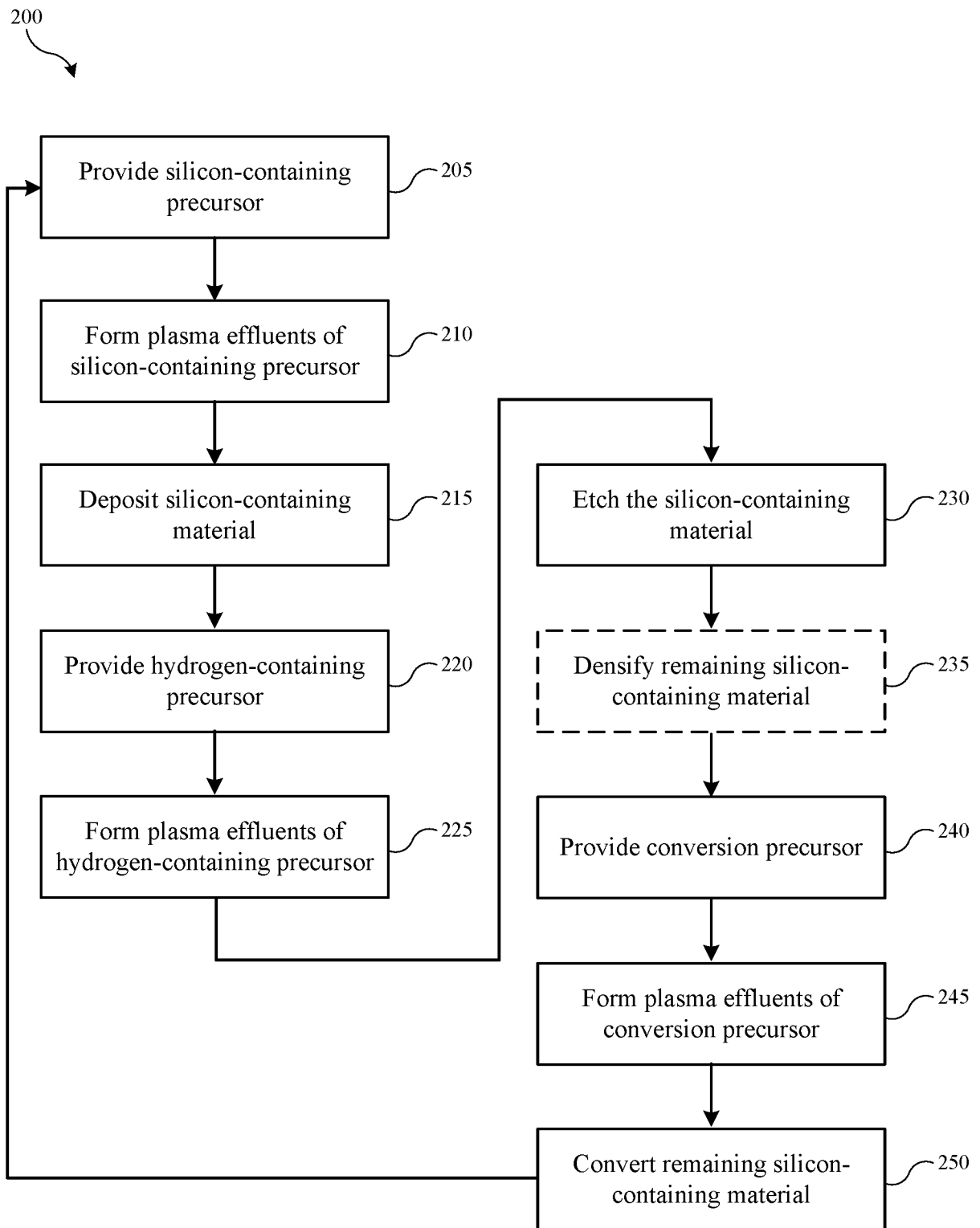


FIG. 2

FIG. 3A

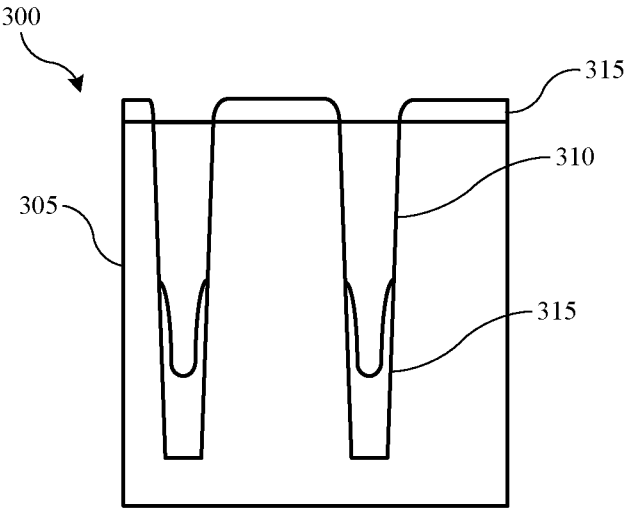


FIG. 3B

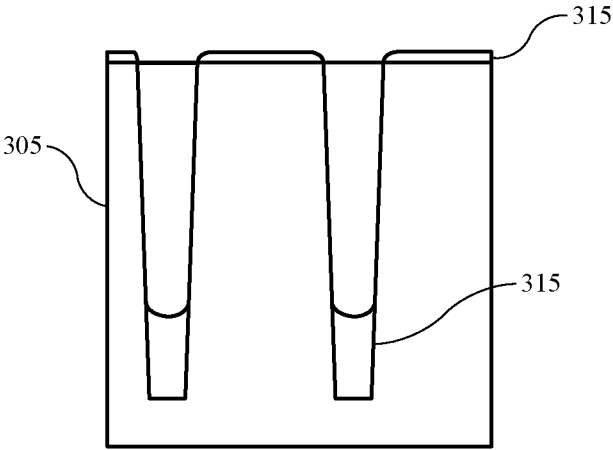
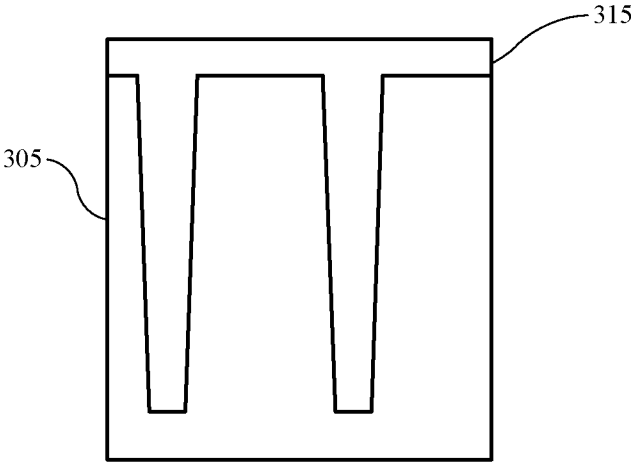


FIG. 3C



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2024/025649

A. CLASSIFICATION OF SUBJECT MATTER H01L 21/02(2006.01)i; H01L 21/3065(2006.01)i; H01L 21/687(2006.01)i; H01J 37/32(2006.01)i According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L 21/02(2006.01); H01J 37/32(2006.01); H01L 21/3065(2006.01); H01L 21/311(2006.01); H01L 21/768(2006.01) Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models Japanese utility models and applications for utility models Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & Keywords: silicon oxide, gap-fill, hydrogen, plasma, etch, densify		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2023-0071366 A1 (APPLIED MATERIALS, INC.) 09 March 2023 (2023-03-09) See paragraphs [0004]-[0051] and claims 1-10, 16-18.	1-8,10-20
Y		9
Y	US 7476621 B1 (MINH ANH NGUYEN et al.) 13 January 2009 (2009-01-13) See claim 1 and figures 1A-1D.	9
A	US 2022-0301823 A1 (ASM IP HOLDING B.V.) 22 September 2022 (2022-09-22) See paragraphs [0084]-[0086], claim 1 and figures 12-13.	1-20
A	KR 10-2020-0120750 A (APPLIED MATERIALS, INC.) 21 October 2020 (2020-10-21) See claims 1, 9-10.	1-20
A	KR 10-2016-0140884 A (APPLIED MATERIALS, INC.) 07 December 2016 (2016-12-07) See the entire document.	1-20
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents: “A” document defining the general state of the art which is not considered to be of particular relevance “D” document cited by the applicant in the international application “E” earlier application or patent but published on or after the international filing date “L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) “O” document referring to an oral disclosure, use, exhibition or other means “P” document published prior to the international filing date but later than the priority date claimed “T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention “X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone “Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art “&” document member of the same patent family		
Date of the actual completion of the international search 19 August 2024		Date of mailing of the international search report 19 August 2024
Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon 35208, Republic of Korea Facsimile No. +82-42-481-8578		Authorized officer LEE, Kang Ha Telephone No. +82-42-481-5687

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/US2024/025649

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