

[54] **LOGIC SENSING CIRCUIT HAVING SWITCH CONTACT ANTI-BOUNCE FEATURE**

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[51] Int. Cl.**H03k 17/00**

[58] Field of Search.....**307/215, 208, 218, 246, 247, 307/247 A, 260, 265, 268, 269; 328/59-61, 92**

[56]

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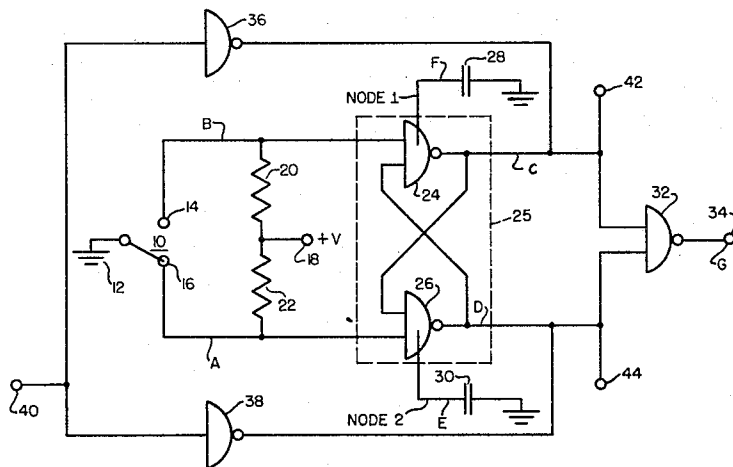
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[57]

ABSTRACT

A strobe pulse is produced in response to the change in state of a switch without responding to switch contact bounce. Capacitors connected to node inputs of gates in a bistable multivibrator provide a delayed response of the multivibrator so that both outputs thereof are simultaneously at the same signal level sufficient to enable a gate producing strobe pulse.

13 Claims, 3 Drawing Figures



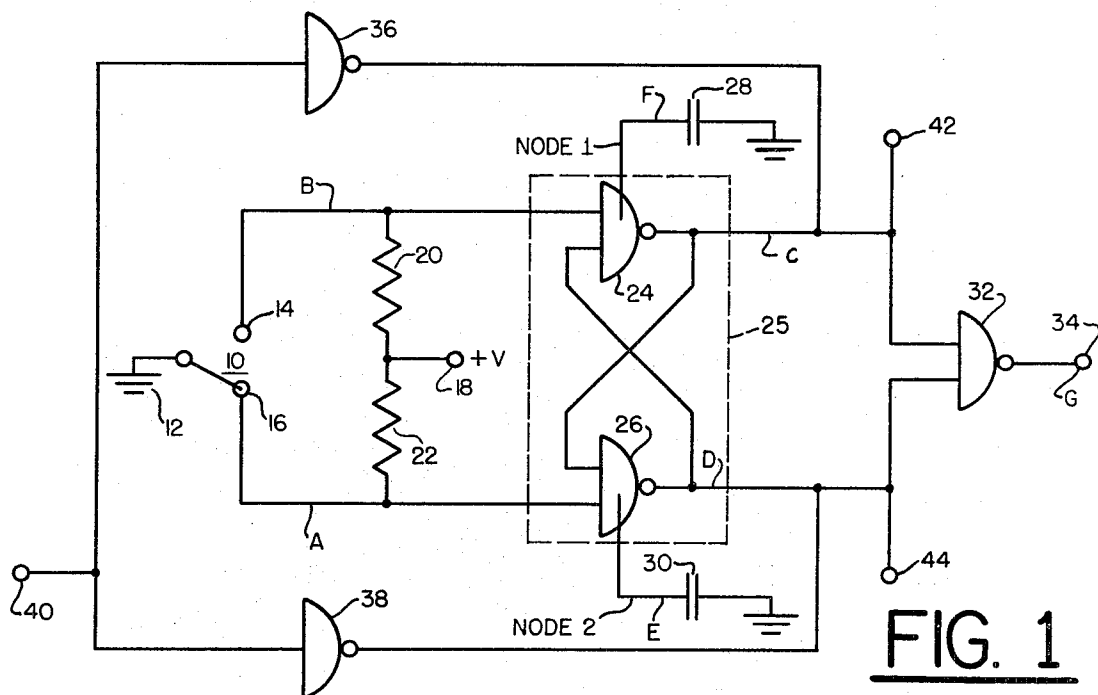


FIG. 1

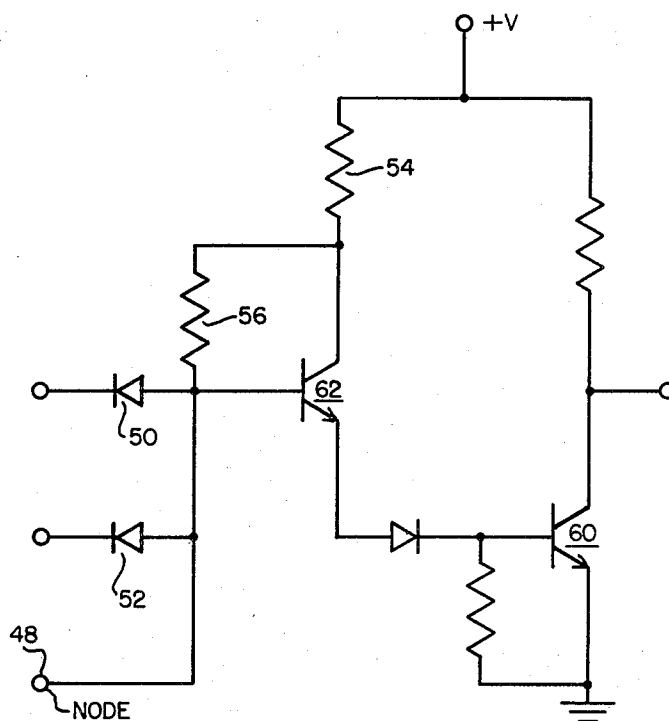


FIG. 3

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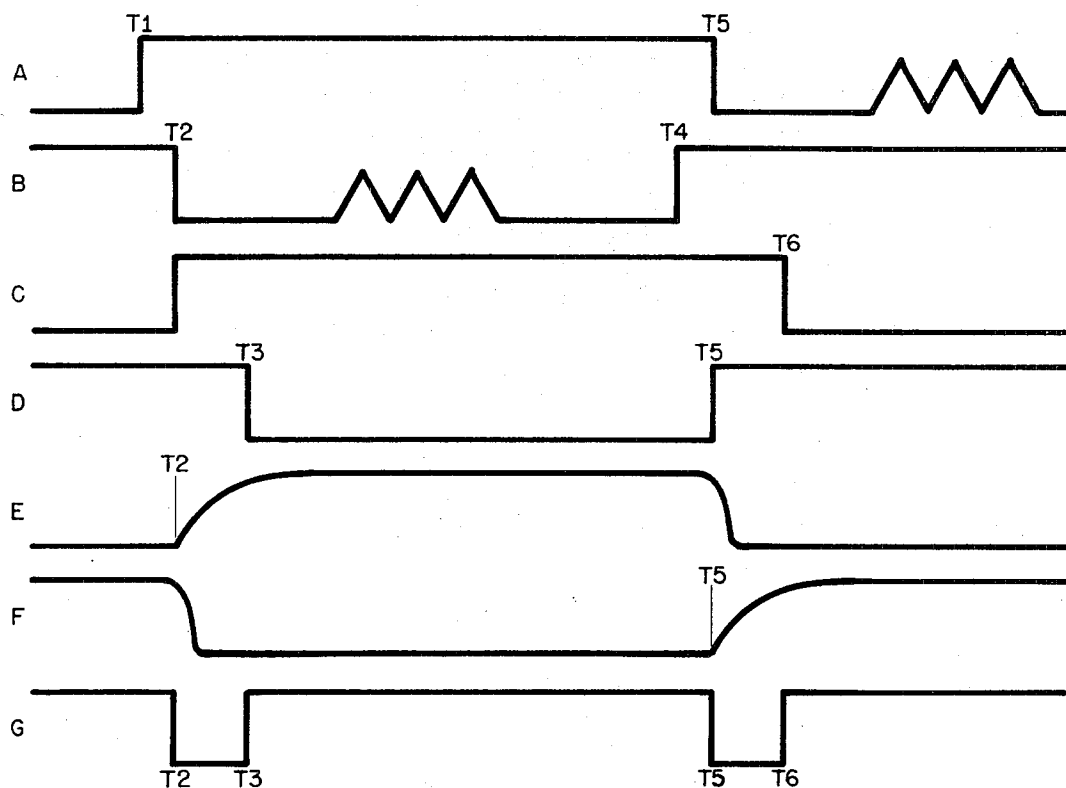


FIG. 2

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LOGIC SENSING CIRCUIT HAVING SWITCH CONTACT ANTI-BOUNCE FEATURE

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to logic sensing circuits which may be used in a data processing system and more particularly to circuits producing pulses in response to the change in state of a switch without responding to switch contact bounce.

2. Prior Art

A widespread use is made of switches in the data processing field for activating or deactivating computer circuits. Although such switches are generally reliable, they have a drawback in that, for a mechanical switch, the switch contacts are subject to what is known as "bounce." Bounce occurs when during operation, the contacts strike each other forcibly and rebound to some degree breaking contact. Although the contacts ultimately make good contact (i.e. the bounce has ceased), this bouncing often results in incorrect signals passing to subsequent circuitry. In data processors, erroneous signals are very undesirable and often intolerable.

In the prior art, U.S. Pat. Nos. 3,381,143 and 3,508,079 disclose anti-bounce circuits. The invention of the former patent provides a bistable multivibrator responsive to the change in state of a switch. The outputs of the multivibrator provides a signal having a level rather than a signal of pulse form. It is much more desirable in fast computing systems to provide short duration pulses as is provided by the circuit of this invention. The invention of the latter patent also provides an anti-bounce feature but at the expense, in combination with a single sensing feature, of more complex circuitry.

It is therefore an object of the invention to provide an improved logic sensing circuit having an anti-bounce feature.

It is a further object of the invention to provide a logic sensing circuit which produces a pulse in response to the change in state of a switch.

It is another object of the invention to provide a simplified logic sensing circuit which may be bypassed and which automatically produces a pulse upon termination of the bypassed condition.

SUMMARY OF THE INVENTION

The purposes and objects of the invention are satisfied by providing a logic sensing circuit responsive to the change in state of a switch. In accordance with a preferred embodiment of the invention, a bistable means having two inputs and outputs is provided. The inputs are adapted to respond to alternate state changes of the switch, whereas the outputs are coupled to two inputs of a first gate whose output is the strobe pulse terminal. Capacitors coupled to the nodes of each of the two gates included in the bistable means, delay the change in state of the bistable means output levels thereby providing similar signal levels to the first gate sufficient to enable a strobe pulse.

BRIEF DESCRIPTION OF THE DRAWINGS

The advantages of the foregoing configuration of the present invention become more apparent upon reading the accompanying detailed description in conjunction with the figures in which:

FIG. 1 is a schematic diagram of the logic sensing circuit of the invention;

FIG. 2 is a timing diagram including waveforms A through G illustrating the operation of the circuit of FIG. 1; and

FIG. 3 is a schematic diagram of a gate element used in the circuit of FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 illustrates a logic sensing circuit comprising a bistable multivibrator 25 and a gate 32. A switch 10 provides a

ground potential level shown by the symbol for circuit ground 12 to either of its output terminals 14 or 16. Terminals 14 and 16 connect respectively to inputs of gates 24 and 26 in the bistable multivibrator 25. The outputs of multivibrator 25 connect to dual inputs of the gate 32. The output of gate 32 connects to terminal 34 where the strobe pulse is generated. Capacitors 28 and 30 connect respectively to the nodes of gates 24 and 26. A node which is an input bypassing the gating elements of a gate, is sometimes referred to as the expandable input of the gate. The capacitors cause a delay of change in state of the multivibrator output when switch 10 is changed in state. During this delay it will be seen that a strobe pulse is generated at terminal 34. The signal levels on terminals 42 and 44 coupled to the multivibrator outputs are used to determine the functional operation, i.e., a strobe pulse combined with a low level signal on terminal 42 may indicate and command a data processor to perform a first function, whereas a low level signal at terminal 44 in combination with a strobe pulse may command a second function to be performed by the data processor. Another means for indicating the function is to utilize different values for capacitors 28 and 30 thereby changing the time duration of the strobe pulse. A wide pulse could be utilized to indicate a first function while a narrow pulse could be utilized to indicate a second function. Further, a signal produced at terminal 40 in combination with gates 36 and 38 are utilized to determine either local or remote operation of the logic sensing circuit of the invention. During remote operation, a change in state of switch 10 is not responded to; whereas during local operation, normal operation of the logic sensing circuit is allowed so that a change in state of switch 10 is responded to.

Generally, the operation of the logic sensing circuit of FIG. 1 is as follows. A change in state of switch 10 from the state or position shown causes the gate 24 to change state. At this time capacitor 28 discharges to ground and further, capacitor 30 starts to charge. From the time that the gate 24 changes state until the time that the charge on capacitor 30 reaches a threshold level, gate 32 is enabled and a strobe pulse is produced at terminal 34. When the charge on capacitor 30 reaches the threshold level, the Node 2 input which is effectively a third input to gate 26 in combination with the signals appearing at the other inputs of gate 26 cause the output of gate 26 to change state thereby disabling any further appearance of the strobe pulse until the switch 10 is again changed in state.

Before discussing more detailed operation of the logic sensing circuit of the invention, it should be pointed out that the gates 24 and 26 are well known in the art and may be those gates manufactured by Motorola, Inc., having model number MC930G. FIG. 3 illustrates such a gate. The node input 48 is a third input shunting or bypassing the gating elements, i.e., the input diodes 50 and 52. The delay capacitor, 28 or 30, connected between the node input and circuit ground is charged by means of supply voltage, +V, through resistors 54 and 56, through the delay capacitor to ground 12, but only when the diodes 50 and 52 receive a binary one signal which is represented by a positive potential. The delay capacitor discharges rapidly through whichever of diodes 50 and/or 52 receive a binary zero which is represented by circuit ground potential. The charging time constant is determined by the values of resistors 54 and 56 and the delay capacitor. The discharge time is very rapid through the short circuit provided by one or both of diodes 50 and 52. The threshold level referred to herein is a voltage level approaching the high logical level of a binary one and is that level at which the input transistor 62 of the gate circuit conducts. The operation of the gate shown in FIG. 3 is well known and will not be further explained here.

Although the gates 24 and 26 are shown to be of the diode transistor logic (DTL) type, any type gate such as transistor transistor logic (TTL) types, may have been used so long as a node input is provided. In addition, the other gates 32 as well as gates 36 and 38 may be similar to gates 24 and 26 except

that a node input is not required. Each of the gates is of the NAND configuration and in general produces a binary zero output when all of its inputs are a binary one and produces a binary one output when any of its inputs are a binary zero.

In more detailed operation and now referring to the circuit of FIG. 1 and the waveforms of FIG. 2, the initial conditions before time T1 with the switch 10 connected to ground terminal 16 are as follows. The input to gate 26 shown by waveform A is at zero volts or circuit ground. The input to gate 24 shown by waveform B is at a positive potential supplied by the voltage, +V, at terminal 18 through resistor 20. Capacitor 28 is charged whereas capacitor 30 is discharged. The outputs of gates 24 and 26 are low and high respectively, thereby disabling gate 32 and producing a high level at terminal 34. The operation of gates 36 and 38 will be discussed hereinafter.

When switch 10 is changed in state at time T1, waveform A goes to a high level potential determined by voltage, +V, through resistor 22. At time T2 after connection has been made from circuit ground 12 to terminal 14, waveform B goes low. This causes capacitor 28 to immediately discharge as shown by waveform F and at the same time the output of gate 24 as represented by waveform C goes high. Note that for ease of explanation, circuit propagation delays are not shown in the timing diagram. As soon as waveform C goes high (essentially at time T2) capacitor 30 connected to the node of gate 26 starts to charge. Also at time T2, since waveform C is now high and since waveform D was and is now high, gate 32 becomes enabled to produce the negative transition of the strobe pulse shown by waveform G. Note that waveform D was high because gate 26 had a low level input shown by waveform C and that waveform D is still now high because of the low level input of waveform E indicating that capacitor 30 remains discharged. However, as soon as the charge on capacitor 30 reaches a threshold level, and since the other inputs to gate 26 are at such threshold level, gate 26 is enabled producing a low level at time T3. This causes gate 32 to become disabled thereby producing the trailing positive going edge of the strobe pulse (waveform G). Thus, the strobe pulse terminates and will not be produced again until switch 10 is again toggled. The strobe pulse occurring between times T2 and T3 may be utilized in conjunction with the low level state of waveform D beginning at time T3 to command a utilizing device such as a data processor to perform a specified function.

It can be seen that the switch 10 contact bounce occurring after time T3 and before time T4 as shown by waveform B does not affect the operation of the logic sensing circuit of the invention and such contact bounce is effectively eliminated. The only way that such bounce can affect the operation of the circuit is if the bounce occurs before capacitor 28 discharges (waveform F). However, this is not the case since in actual operation capacitor 28 discharges in microseconds whereas the bouncing does not start until milliseconds have elapsed after the switch is changed in state. After discharge of capacitor 28, the logic sensing circuit of the invention is not affected since although waveform B may be high, waveform D is low, maintaining the output of gate 24 at a high level (waveform C).

The operation of the logic sensing circuit is similar to that explained above when switch 10 is again changed in state grounding terminal 16. At time T4, switch 10 is toggled causing waveform B to go high. When the terminal 16 is connected to circuit ground 12 at time T5, waveform A goes low. This causes waveform D to go high and at the same time causes the charge on capacitor 30 shown by waveform E to discharge. Also at time T5, since both inputs to gate 32 are high, gate 32 is enabled to produce the negative going transition of a strobe pulse as shown by waveform G. Further, at essentially time T5, capacitor 28 starts to charge (waveform F) and upon reaching a threshold level at time T6 causes the output of gate 24 (waveform C) to go low thereby disabling gate 32 and producing the trailing positive going edge of the strobe pulse at terminal 34.

A preferred embodiment of the invention has thus been shown wherein a strobe pulse is generated in response to the change in state of a switch, wherein the effects of switch contact bounce have been avoided, and wherein the strobe pulse in combination with levels appearing at terminals 42 and 44 may determine the function to be performed by a utilizing circuit. In such utilizing circuits such as a data processor, bypassing any response to the toggling of a switch 10 is sometimes desirable, for example when a function is being performed by the data processor which function is not to be interrupted. For this purpose, terminal 40 and gates 36 and 38 are provided.

Terminal 40 connects to the inputs of gates 36 and 38 which provide an inverting function. The outputs of gates 36 and 38 connect in a "wired or" configuration respectively to the outputs of gates 24 and 26. During normal or noninhibit operation of the logic sensing circuit of the invention, the potential at terminal 40 is low, which potential may be supplied by a data processor under program control. Normally, the outputs of gates 36 and 38 would be high with a low input at terminal 40. However, because of the connection of the gate output transistors 60 (FIG. 3), the waveforms C or D will remain low if either of the "wired or" gates 24 and 36 or either of the "wired or" gates 26 and 38 have low outputs. Thus, there will be no effect on the normal operation of the logic sensing circuit.

When in the remote or inhibit operation, the terminal 40 potential is high and any response to the change in state of switch 10 will be bypassed. Because of the high level, the outputs of gates 36 and 38 are low, causing waveforms C and D to be low and thereby inhibiting gate 32 from producing a negative going strobe pulse. Because waveforms C and D are low, at least one input to gates 24 and 26 is also low, thereby discharging the capacitors 28 and 30. Because capacitors 28 and 30 are discharged, removal of the inhibit mode or high level from terminal 40 will automatically cause a strobe pulse to be produced regardless of the position of switch 10. That is, when the potential of terminal 40 goes low, the outputs of gates 36 and 38 or respectively waveforms C and D go high since at least one of the inputs including the node inputs to gates 24 and 26 are at a low level thereby producing a high output. At this time the leading negative going transition of the strobe pulse is enabled. With switch 10 in the position shown, i.e. terminal 16 grounded, capacitor 28 will then charge since both inputs to gate 24 are high. As soon as the charge on capacitor 28 reaches a threshold level, the output of gate 24 will go low thereby producing the trailing positive going transition of the strobe pulse. A change in state of the switch 10 will then cause operation of the circuit as stated hereinbefore. It can be seen that this feature of providing a strobe pulse automatically upon change from the remote (inhibit) to the local (normal or noninhibit) mode is very desirable since this allows local operation to continue with the same function command automatically after remote operation and without operator intervention.

It should also be appreciated that although the circuit of FIG. 1 is designed to eliminate the effects of switch contact bounce as produced by a mechanical or electromechanical switch, the circuit of FIG. 1 may also be used with a transistorized switch without departing from the scope of the invention. It should also be understood that although NAND gates are utilized in the circuit of the invention, AND gates as well as other logic elements may have been utilized without departing from the scope of the invention.

Having now described the invention what is claimed as new and novel and for which it is desired to secure Letters Patent is:

1. A logic sensing circuit responsive to the change in state of a switch, said circuit comprising:

- A. bistable means including two inputs adapted to respond to alternate state changes of said switch, said bistable means including two outputs;
- B. first gate means coupled to receive said two bistable means outputs; and

C. means for delaying the response of said bistable means to a change in state of said switch so that said two outputs provide simultaneous similar signal levels enabling said first gate means to produce a pulse.

2. A circuit as defined in claim 1 further comprising circuit means coupled to said bistable means outputs for inhibiting the producing of said pulse when said circuit means receives a first signal.

3. A circuit as defined in claim 2 wherein said circuit means includes means for automatically producing a pulse without a change in state of said switch when said first signal received by said circuit means is disabled.

4. A circuit as defined in claim 1 further comprising first means, coupled to receive one of said bistable means outputs and said produced pulse, for indicating a first function in accordance with the state of said switch and second means, coupled to receive the other of said bistable means outputs and said produced pulse, for indicating a second function in accordance with the state of said switch.

5. A circuit as defined in claim 1 wherein said bistable means include two further gate means in circuit arrangement, at least one of said two further gate means including a node input bypassing the input gating elements of said gate means, and wherein said means for delaying includes capacitive means in circuit with said node input.

6. A circuit as defined in claim 5 wherein any contact bounce produced by the change in state of said switch does not affect operation of said circuit when said capacitive means is in a discharged condition.

7. A circuit as defined in claim 5 wherein each of said two further gate means includes a node input and wherein each of said node inputs includes a capacitive means in circuit with said node input, wherein in response to a change in state of said switch one of said capacitive means discharges and the other of said capacitive means charges, and wherein said first gate means produces a pulse while said other of said capacitive means charges to a predetermined threshold value.

8. A logic sensing circuit comprising:

A. bistable means having two inputs and two outputs;
B. means responsive to a change in state of said inputs for delaying a change in state of one of said outputs; and

C. means responsive to said delayed change in state of one of said outputs for producing a pulse during said delay in response to said change in state of said inputs.

9. A circuit as defined in claim 8 wherein said bistable means includes first and second gate means in circuit arrangement, each of said gate means including a node input bypassing semiconductor gate elements in said gate means, and wherein said means for delaying includes first and second

capacitors coupled to said node inputs of said first and second gate means respectively.

10. A logic sensing circuit comprising:

A. a switch comprising an input coupled to a first potential and first and second outputs, said first potential coupled to one of said outputs depending on the state of said switch;

B. bistable means comprising first and second gate means, each of said gate means including a node input bypassing gating elements included in said first and second gate means, said first and second gate means each having outputs and first and second inputs, said second input of each gate means coupled to said output of the other gate means, said first input of said first gate means coupled to said first output of said switch and said first input of said second gate means coupled to said second output of said switch;

C. a first capacitor coupled between said node input of said first gate means and said first potential;

D. a second capacitor coupled between said node input of said second gate means and said first potential;

E. a second potential coupled to whichever one of said first inputs of said first and second gate means is not coupled to said first potential by said switch; and

F. third gate means having first and second inputs coupled respectively to said outputs of said first and second gate means and having an output terminal at which a pulse is produced in response to a change in state of said switch.

11. A logic sensing circuit responsive to the change in state of a switch, said circuit comprising:

A. bistable means comprising two inputs adapted to respond to alternate state changes of said switch, said bistable means further comprising two outputs and two gate means in circuit arrangement between said two inputs and said two outputs, at least one of said two gate means including a node input bypassing the input gate elements of said gate means; and

B. means for delaying the response of said bistable means to a change in state of said switch, said means for delaying including capacitive means in circuit with said node input.

12. A circuit as defined in claim 11 further comprising means responsive to said delayed change in state of one of said outputs for producing a signal during said delay in response to a change in state of said switch.

13. A circuit as defined in claim 12 further comprising circuit means coupled to said bistable means outputs for inhibiting the producing of said signal when said circuit means receives a first signal.

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