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(71) Applicant: **NATIONAL UNIVERSITY OF SINGAPORE** [SG/SG]; 21 Lower Kent Ridge Road, Singapore 119077 (SG).

(72) Inventors: **CHEN, Wei**; c/o National University of Singapore, Faculty of Science / Department of Chemistry, 21 Lower Kent Ridge Road, Singapore 119077 (SG). **XIANG, Du**; c/o National University of Singapore, Faculty of Science / Department of Chemistry, 21 Lower Kent Ridge Road, Singapore 119077 (SG). **LIU, Tao**; c/o National University of Singapore, Faculty of Science / Department of Chemistry, 21 Lower Kent Ridge Road, Singapore 119077 (SG).

(74) Agent: **DAVIES COLLISON CAVE ASIA PTE. LTD.**;
10 Collyer Quay #07-01, Ocean Financial Centre, Singapore 049315 (SG).

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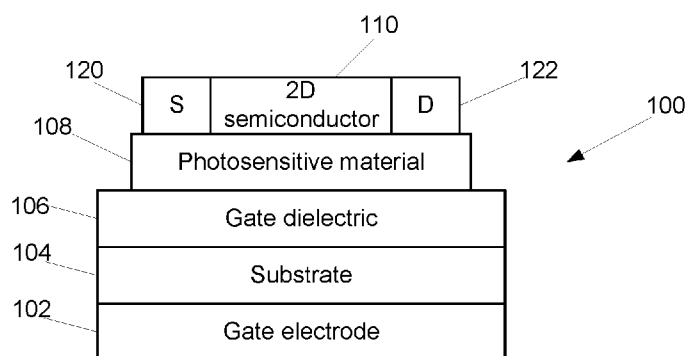


FIGURE 1

(57) Abstract: A semiconductor device comprises a gate electrode and a gate dielectric that is a photosensitive material and/or is disposed adjacent to a photosensitive material; a channel layer at least partly contacting the photosensitive material to form a heterojunction region, the channel layer being formed from a two-dimensional semiconductor material; and at least one pair of electrodes between which at least part of the channel layer extends, at least partly in the heterojunction region, to thereby form a transport channel of the field effect transistor.

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A SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

Technical Field

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The present invention relates to a semiconductor device and to a method of manufacturing a semiconductor device.

Background

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Optoelectronic memories have attracted tremendous attention owing to their unique capability of accumulating and releasing photo-generated carriers under electrical stress and light irradiation. This advantage enables the great potential of optoelectronic memories in image capturing, confidential information recording, and logic data processing. The last few decades have witnessed the exponential advance of silicon-based nonvolatile optoelectronic memories. However, continued device miniaturization and the feasibility of integration into flexible, wearable, and transparent circuits greatly restrict the development of conventional silicon-based optoelectronic memories.

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Two-dimensional (2D) thin layered materials have been considered as promising building blocks for next-generation electronic and optoelectronic devices due to their extraordinary and unique properties. The 2D thin layered structure enables immunity against short channel effects, while the mechanical strength and structural flatness allow integration into flexible and wearable circuits.

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Various optoelectronic memory devices that make use of 2D materials have previously been proposed, such as devices based on mechanically exfoliated few-layer copper indium selenide ($\text{CuIn}_7\text{Se}_{11}$), monolayer molybdenum disulfide (MoS_2), and a graphene/ MoS_2 vertical heterostructure. However, these previous proposals suffer from one or more disadvantages, including

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short retention time, low current switching ratio, and/or limited data storage capacity.

In addition to data storage capability, it would be desirable to provide an
5 optoelectronic memory that can distinguish light wavelength for color sensing
in digital imaging. In currently available commercial color sensors, spectrum
distinction is achieved by combining broadband inorganic semiconductor-
based photodetectors with a set of optical filters, including organic dye filters
and plasmonic color filters. However, these filters not only increase the
10 architectural complexity and cost of the color sensors, but also limit the pixel
density in the imaging system. Furthermore, image sharpness and color
constancy are degraded by the interference effect of the optical filter.

The present invention seeks to address one or more of the above difficulties
15 with existing semiconductor devices such as optoelectronic memory devices,
or at least to provide a useful alternative.

Summary

20 In accordance with the present disclosure, there is provided a semiconductor
device, comprising:

a gate electrode and a gate dielectric that is a photosensitive material
and/or is disposed adjacent to a photosensitive material;

a channel layer at least partly contacting the photosensitive material to
25 form a heterojunction region, the channel layer being formed from a two-
dimensional semiconductor material; and

at least one pair of electrodes between which at least part of the channel
layer extends, at least partly in the heterojunction region, to thereby form a
transport channel of the field effect transistor.

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The channel layer may be formed from a two-dimensional direct
bandgap semiconductor material.

In certain embodiments, the photosensitive material has a bandgap containing one or more mid-gap states that are excitable by optical radiation.

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The photosensitive material may be boron nitride, such as hexagonal boron nitride (h-BN), or a metal oxide film.

10 In certain embodiments, the two-dimensional semiconductor material is a transition metal dichalcogenide. For example, the transition metal dichalcogenide may be MoTe_2 or WSe_2 .

In certain embodiments, the two-dimensional semiconductor material is phosphorene.

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In certain embodiments, the channel layer is a monolayer of the two-dimensional semiconductor material, or comprises multiple layers of the two-dimensional semiconductor material.

20 The back gate may comprise a graphene layer disposed between the insulator and the photosensitive layer.

The channel layer may partially contact the photosensitive material and partially contact the insulator.

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Further disclosed is a method of fabricating a semiconductor device, comprising:

forming a back gate on a substrate, the back gate comprising a back gate electrode and a gate dielectric, wherein the gate dielectric is a photosensitive material and/or is disposed adjacent to a photosensitive material;

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applying a channel layer to at least part of the photosensitive layer to form a heterojunction region, the channel layer being formed from a two-dimensional semiconductor material; and

forming electrodes on at least the photosensitive material, whereby at least part of the channel layer extends, at least partly in the heterojunction region, between two of the electrodes to thereby form a transport channel of the field effect transistor.

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Brief description of the drawings

Certain embodiments are described, by way of non-limiting example only, with reference to the accompanying drawings in which:

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Figure 1 is a schematic cross-sectional view of a semiconductor device according to an embodiment.

Figure 2 is a schematic cross-sectional view of a semiconductor device according to another embodiment.

Figure 3 is a schematic cross-sectional view of a semiconductor device according to a further embodiment.

Figure 4 is a schematic cross-sectional view of a semiconductor device according to a yet further embodiment.

Figure 5 shows the operational mechanism of an example WSe₂/BN heterostructure-based optoelectronic memory. **a** Schematic illustration of the optoelectronic memory fabricated by transferring WSe₂ flake on BN flake. The dark blue, red, yellow, and light blue balls represent the W, Se, B, and N atoms, respectively. Inset: optical image of the fabricated WSe₂/BN heterostructure. The scale bar is 10 μm. **b** The transfer curves of pristine, programmed, and erased WSe₂/BN device at $V_{sd} = 1$ V. The programming gate is -20 V. The transport characteristic of the WSe₂/BN FET was converted from hole-domination to electron-domination after programming, followed by a return to hole-domination after erasing. **c** A single program-readout-erase

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cycle of the WSe₂/BN memory at $V_{\text{pro}} = -20$ V. The shaded backgrounds in light yellow, blue, gray, and green represent the device states as pristine, programming, readout, and erasing, respectively. Inset: plot of the erased current. Schematic of the band diagrams of the WSe₂/BN optoelectronic memory under programming (**d**), readout (**e**), and erasing processes (**f**). The rectangle in grayish green represents the Si band diagram, while the parallelograms in white, blue and khaki represent the band diagrams of SiO₂, BN, and WSe₂, respectively. The red and blue circles represent the positive charges and electrons, respectively. E_F^{Si} is the Fermi level energy of Si substrate. E_C^{BN} and E_V^{BN} represent the minimum energy of conduction band and the maximum energy of valence band of BN, respectively.

Figure 6 shows programming gate controlled WSe₂/BN optoelectronic memory and reliability tests. **a** Transfer characteristics evolution of the memory device with respect to V_{pro} . **b** Dynamic behavior of the memory at different programming gate ranging from 0 to -80 V with step -10 V. The readout current increases stepwise, generating nine clear storage states. **c** The plot of switching ratio as a function of V_{pro} . Current retention (**d**) and cycling tests (**e**) for the WSe₂/BN memory at different V_{pro} ($V_{\text{pro}} = 0, -20, -40, -60$, and -80 V). The squares in black represent the device in the erased state, while the symbols in red, yellow, green, blue, and purple represent the programmed state under $V_{\text{pro}} = 0, -20, -40, -60$, and -80 V, respectively.

Figure 7 shows one hundred thirty storage states. **a** The dynamic behavior of the memory under the exposure of light pulse ($t_{\text{pro}} = 0.5$ s, $\lambda = 405$ nm, $P = 2$ nW) at $V_{\text{pro}} = -80$ V, and the enlargements in region I (**b**), II (**c**), III (**d**), and IV (**e**), respectively. The regions shaded in red, green, blue, and purple in **a** correspond to the enlarged regions plotted in the same colors in **b–e**, respectively.

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Figure 8 shows wavelength distinguishing ability of WSe₂/BN optoelectronic memory. **a** Dynamic behavior of the WSe₂/BN memory illuminated by a wide

spectrum of lights with wavelength ranging from 750 to 410 nm. Nine distinguishable storage states are clearly observed under different programming wavelengths. **b** The corresponding transfer characteristic with respect to wavelength after each programming. **c** Programming rate as a function of photon energy. Inset: plot of the enlargement from 1.55 to 2.48 eV.

Figure 9 shows an example of an integrated WSe₂/BN pixel matrix for a color image sensor. **a** False-colored SEM image of the fabricated WSe₂/BN pixel matrix in arrays (three rows and nine columns). The scale bar is 10 μm. The channel length is almost the same for each pixel after deep RIE etching, approximately 2 μm. **b** The corresponding schematic of the pixel matrix with selective exposure under three different wavelength lights (red 638 nm, green 515 nm, and blue 473 nm). The programming gate, time and laser power were fixed the same as -80 V, 2 s, and 10 nW, respectively for each exposure. The color bar was achieved by reading the storage current of pixel 11 under different lights with photon energy (E_{photon}) from 1.90 to 2.75 eV.

Figure 10 shows Raman and photoluminescence (PL) spectra of WSe₂ and BN crystals. **(a)** Optical microscope image of the WSe₂ setup. **(b)** Raman spectrum of the exfoliated WSe₂ flake. **(c)** PL spectrum of the exfoliated WSe₂ flake. **(d)** Raman intensity map of the mode of the WSe₂ flake. **(e)** Raman spectrum of the exfoliated BN flake.

Figure 11 shows AFM images of WSe₂ and BN flakes. **(a)** AFM image of the as-fabricated WSe₂/BN device. Line profiles at the edges of the WSe₂ **(b)** and BN **(c)** flakes. The thickness of WSe₂ flake is around 0.75 nm (monolayer), in good agreement with the Raman result. BN flake shows a thickness of 10 nm, corresponding to layer number of 20.

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Figure 12 shows backgate screening effect of an example WSe₂/BN device under light illumination. Backward transfer characteristics (V_g from 50 V to -

80 V) of the WSe₂/BN device under dark and light conditions. The light is switched on when V_g is sweeping from 0 V to -80 V. The on current of the pristine WSe₂/BN device at negative gate regime reaches up to 28 nA, exhibiting a typical p-type transport behavior. In contrast, when the light is on, the hole transport current drops dramatically. This phenomenon is mainly due to the generation of ionized positive defects in BN under light illumination. These positively charged defects are able to effectively screen the electric field induced by the negative backgate exerting on the WSe₂, which, in turn, resulting in the significant decrease of the hole transport current in the WSe₂ device.

Figure 13 illustrates the non-volatility property of an example WSe₂/BN memory. Readout current as a function of waiting time up to 4.34×10^4 s. P and R refer to program and readout respectively. The graph was spread separately with an interval of 6.2×10^3 s. In order to further investigate the non-volatility of the memory, its charge retention time was analysed. The memory was kept in the absence of external perturbation (no voltage and no light) after programming, and the storage currents were readout in a fixed interval (3.1×10^3 s). Figure 9 shows the storage currents as a function of waiting time up to 4.34×10^4 s at three different programming gates ($V_{pro} = 0$ V, -40 V, -80 V). To simplify the graph, we plotted the data with an interval of 6.2×10^3 s. The storage currents almost keep unchanged in the time range 4.34×10^4 s for all the programming gates, which verifies the memory is retained in the absence of external perturbation.

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Figure 14 shows 10 years linear extrapolation of the storage currents without electrical and optical pulses after programming at different programming gates ($V_{pro} = 0$ V, -20 V, -40 V, -60 V, and -80 V). Nearly half the storage currents can be retained after 10 years for all V_{pro} , which indicates the practical application of the WSe₂/BN optoelectronic memory.

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Figure 15 shows saturation of the storage current. **(a)** Dynamic behavior of

the memory under the exposure of light pulse ($t_{\text{pro}} = 0.5$ s, $\lambda = 405$ nm, $P = 2$ nW) at $V_{\text{pro}} = -80$. **(b)** Enlargement of the dynamic behavior from 130th storage level onwards.

- 5 Figure 16 shows noise calculations for reliable storage states. **(a)** Storage currents and the STDs of states 58 and 59. **(b)** Gap to STD ratio for all the storage states.

- Figure 17 shows repeatability of the memory. Dynamic behavior and the gap
10 to STD sum ratios of the memory in the 1st (a), 10th (b), and 20th (c) cycle.

- Figure 18 shows erased currents of the memory. Erased current for the 1st
15 **(a)**, 10th **(b)**, and 20th **(c)**. **(d)** Summary of the erased currents for the 20 independent cycles.

- Figure 19 shows Raman and PL characterizations of CVD grown large area
WSe₂. Optical image **(a)**, Raman **(b)**, and PL **(c)** of the CVD WSe₂. Figure
15(a) shows the optical image of CVD grown WSe₂ in triangle shape with scale
around 100 μm . Both the Raman and PL spectra confirm the monolayer
20 characteristic of the CVD WSe₂.

- Figure 20 shows thickness variation of the BN substrate in WSe₂/BN pixel
matrix. AFM image **(a)** and its corresponding line profile **(b)** of the BN
substrate at the interface of the bright and dark regions in WSe₂/BN pixel
25 matrix SEM image. The bright and dark zones are clearly observed in the
false-colored SEM image of the fabricated WSe₂/BN pixel matrix, which is due
to the thickness variation (approximating 3 nm) of the BN substrate.

- Figure 21 shows storage states of the selected pixels under different
30 wavelength lights. Transfer characteristics (a) and the corresponding dynamic
behaviors of the three selected pixels (11, 14, and 17) under red 638 nm (b),
green 515 nm (c), and blue 473 nm (d) lights respectively. P, R, and E refer to

program, readout, and erase respectively. As shown in Figure 17(a), the on current at the electron regime gradually rises with reducing light wavelength, which is consistent with the dynamic behavior in Figures 17(b)-(d). The storage currents for the selected pixels are around 5.2 nA, 12.8 nA, and 31.5 nA under the wavelengths of 638 nm, 515 nm, and 473 nm respectively.

Figure 22 shows Raman spectra of BP and BN crystals. (a) Optical image of the BP/BN heterostructure. Raman spectra of the exfoliated BP (b) and BN (c) flakes. The first order Raman spectrum of exfoliated few-layer BP exhibits the characteristic peaks nearly located at 363 cm^{-1} , 440 cm^{-1} , and 468 cm^{-1} , corresponding to the three different vibration modes A_g^1 , B_{2g} , and A_g^2 in BP crystal lattice, respectively. The position of the characteristic peak for BN flake is located at 1367 cm^{-1} , almost the same as the position of the BN flake measured in WSe₂/BN structure above.

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Figure 23 shows AFM images of BP and BN flakes. **(a)** AFM image of the as-fabricated BP/BN memory device. The height profiles of BP **(b)** and BN **(c)** flakes. The thickness of BP and BN flakes are 8.0 nm and 19.4 nm, corresponding to the layer numbers of 13 and 39, respectively.

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Figure 24 shows gate controlled BP/BN memory. **(a)** Transfer characteristics evolution of the BP/BN memory with respect to V_{pro} at $V_{\text{sd}} = 0.1\text{ V}$. The light pulse is the same for each programming process with intensity 10 mW cm^{-2} and dwell time 200 s. **(b)** Gate dependent dynamic behavior of the BP/BN memory. The storage current is readout and erased at $V_g = 15\text{ V}$ since the current minimum of the pristine BP/BN FET is around 15 V. **(c)** Plot of switching ratio as a function of programming gate.

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Figure 25 shows wavelength discrimination of BP/BN memory. (a) Transfer characteristics evolution of the BP/BN memory with respect to photon energy from 2.48 eV to 3.02 eV at $V_{\text{sd}} = 0.1\text{ V}$, $V_{\text{pro}} = -30\text{ V}$. The programming time is the same for each process. (b) Wavelength controlled dynamic behavior of

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the BP/BN memory. (c) Programming rate versus photon energy. The transfer curve progressively moves towards negative gate voltage with increasing the photon energy, suggesting the greater number of positive charges generated in BN, same as the effect observed in WSe₂/BN memory. This result is
 5 consistent with the dynamic behavior shown in Figure 21(b). When increasing the photon energy from 2.81 eV to 3.10 eV, 5 distinct storage states are clearly identified. The PR increases slowly at the photon energy smaller than 2.8 eV, before a sharp rise with the continual increase of the photon energy. This photon energy dependent property is similar to that of the WSe₂/BN
 10 memory, which is due to the distribution of donor-like states in BN material.

Figure 26 shows data reliability tests for BP/BN memory. Data retention **(a)** and cyclic endurance **(b)** of the BP/BN memory. The tests were taken at 5 different V_{pro} from -10 V to -60 V with -10 V step. The black squares
 15 represent the device in the erased state, while the symbols in red, yellow, green, blue, and purple represent the programming gate -10V, -20V, -30V, -40V, and -60V respectively. The storage currents after each programming nearly remain in the time range of 4×10^4 s, which indicates the excellent data retention property of the BP/BN memory. Moreover, the fluctuations in the
 20 cyclic tests are quite small, suggesting that the programmed data in the BP/BN memory is highly reproducible.

Figure 27 shows photoresponse of BP/BN photodetector. **(a)** Time dependence of photocurrent (I_{ph}) measured at different programming gates (V_{pro} = -10 V, -20 V, -40 V, -60 V, -80 V). V_{sd} = 1 V for all the photoresponse
 25 measurements. **(b)** Calculated photo responsivity as a function of the V_{pro} .

Figure 28 shows **(a)** optical microscopy image of a fabricated MoTe₂ FET on BN flake. The scale bar is 10 μ m. **(b)** Linear plot of the transfer curves at photodoping gate V_{pd} = -5 V and -20 V with respect to the pristine MoTe₂. The
 30 source-drain voltage V_{sd} = 1 V. **(c)** Schematic of the device structure and corresponding energy band diagram of the MoTe₂/BN heterostructure under

photodoping. MoTe₂ is the transport channel. BN and SiO₂ are the gate dielectric. BN also serves as the photosensitive medium. Si is the controlling gate. In the photodoping process, the device is under light illumination and negative backgate. The red and blue circles represent the positive charges and

5 electrons, respectively. E_C^{BN} and E_V^{BN} represent the minimum energy of conduction band and the maximum energy of valance band of BN respectively.

d) Schematic of the device structure and energy band diagram of the device after photodoping. The device is kept in absence of external perturbation (no light and no electric field) after photodoping.

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Figure 29 shows **a)** Transfer characteristics evolution of the MoTe₂ device as increasing V_{pd} from -10 V to -70 V with 10 V step. **b)** Electron concentration (n_e) at $V_g = 40$ V and electron mobility of MoTe₂ versus V_{pd} . The error bars are defined by the errors from the 20 independent photodoping cycles. **c)** Transfer characteristics evolution in both logarithmic and linear scale (inset) as prolonging retention time to 14 days after photodoping at $V_{pd} = -70$ V. The device is kept in dark condition without electric field, and the transfer measurement was taken every 2 days. **d)** Plot of electron concentration and mobility with respect to the retention time. Cycling test for electron

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20 concentration **(e)** and mobility **(f)** at four different photodoping gates ($V_{pd} = -10V, -30 V, -50 V, -70 V$).

Figure 30 shows **a)** Optical image of MoTe₂/BN heterostructure. The scale bar is 10 μm . **b)** AFM image of the MoTe₂ flake. Half MoTe₂ is on SiO₂, with another half on h-BN flake. Inset: AFM line profile of the MoTe₂ on SiO₂ and h-BN. SKPM image of MoTe₂ flake before **c)** and after **e)** photodoping at $V_{pd} = -50V$. The line scan, denoted by a white dotted line in the MoTe₂ SKPM image before **d)** and after **f)** photodoping.

30 Figure 31 shows **a)** Schematic illustration of the homogeneous MoTe₂ p-n junction achieved by controlling the MoTe₂/BN heterostructure configuration. The left MoTe₂ channel on BN is electron doped, while the right channel on

SiO₂ retains original hole-dominated transport behavior. **b)** Optical microscopy image of the fabricated MoTe₂ p-n junction. Half MoTe₂ flake is on BN with another half on SiO₂. The scale bar is 10 μm. **c)** The I_{sd} - V_{sd} characteristics (V_{sd} from -2 V to 2 V) of the MoTe₂ p-n junction in both linear and logarithmic scale (inset) at $V_{pd} = -50$ V. The rectifying behavior of the MoTe₂ diode is tunable by backgate V_g after photodoping. The V_g is tuned from -65 V to -51 V with 2 V step. **d)** The rectification characteristic of the MoTe₂ diode at $V_g = -53$ V in both linear and logarithmic scale.

Figure 32 shows **a)** Schematic illustration of the homogeneous MoTe₂ inverter achieved by controlling the light illumination region. Graphene (Gr) is the controlling gate, which also provides the input signal. BN serves as the gate dielectric and photosensitive medium. MoTe₂ is the transport channel with three planar electrodes which serve as V_{DD} , V_{OUT} , and ground (GND), respectively. The left MoTe₂ channel is illuminated by a fine-focused laser beam under negative backgate, while the right channel is left unilluminated. **b)** Optical microscopy image of the MoTe₂ inverter. Graphene was exfoliated on SiO₂/Si substrate, followed by the transfer of BN and MoTe₂ flakes. The scale bar is 10 μm. **c)** The output characteristic of the MoTe₂ inverter at $V_{DD} = 1$ V, 2 V, and 3V, respectively. The output curves are clearly divided in three regimes, that is, the "high state" for high V_{OUT} , "steep slope" for the sharp decrease of V_{OUT} , and "low state" for low V_{OUT} , a hall mark of inverter behavior. **d)** The extracted gains of the inverter as a function of input voltage. The highest gains at $V_{DD} = 1$ V, 2 V, and 3V are 18, 42, and 98, respectively.

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Figure 33 shows Raman spectrum of the exfoliated MoTe₂ (a) and BN (b) flakes. The Raman spectrum of MoTe₂ shows three characteristic peaks at 172 cm⁻¹ (A_g^1), 235 cm⁻¹ (E_{2g}^1), and 291 cm⁻¹ (B_g^2), respectively. BN exhibits one characteristic peak at 1365 cm⁻¹ (E_{2g}^1).

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Figure 34 shows a) AFM image of the as-fabricated MoTe₂/BN heterostructure. Line profiles at the edges of the MoTe₂ (b) and BN (c) flakes. The thickness of

MoTe₂ and BN flakes are ~2.1 nm and ~14.5 nm, corresponding to the layer number of 3 and 30, respectively.

Figure 35 shows photodoping rate as a function of photon energy.

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Figure 36 shows transfer characteristic evolution of a MoTe₂/BN device as a function of photodoping duration time at $V_{pd} = -30$ V.

Figure 37 shows a) Transfer characteristics of the pristine MoTe₂/BN device under both forward and backward sweeping directions. Transfer characteristics of the photodoped MoTe₂/BN device under both forward and backward sweeping directions at $V_{pd} = -30$ V (b), -50 V (c), and -70V (d).

Figure 38 shows an optical image of the MoTe₂ device on BN (a) and SiO₂ (d) substrate. The scale bar is 10 μ m. Time dependent photoresponse of the MoTe₂ device on BN (b) and SiO₂ (e) substrate. Transfer characteristic of the MoTe₂ device before and after light illumination on BN (c) and SiO₂ (f) substrate at $V_{sd} = 1$ V.

Figure 39 shows Raman characterization of the pristine and photodoped MoTe₂ flake on BN. The *in-situ* Raman characterization was also carried out to investigate whether other effects, such as gate-bias stress, lattice distortion, and oxidation occurred during photodoping, as shown in Figure 35. The pristine MoTe₂ flake exhibits three characteristic peaks at 172 cm^{-1} (A_g^1), 235 cm^{-1} (E_{2g}^1), and 291 cm^{-1} (B_g^2), respectively. After photodoping for 3 mins, we did not observe any obvious peak shift or broadening for all characteristic peaks of MoTe₂, and there was no additional Raman peak emerged, implying that photodoping does not introduce any additional non-negligible effects in the MoTe₂ flake.

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Figure 40 shows a) Optical image of the new-fabricated MoTe₂/BN heterostructure device. b) Transfer characteristics of the pristine and

photodoped MoTe₂ device at $V_{pd} = -50$ V. $I_{sd} - V_{sd}$ curves of the pristine (c) and photodoped (d) MoTe₂ device at different backgates, V_g from 0 V to 50 V with 10 V step.

- 5 Figure 41 shows transfer characteristic evolution of the MoTe₂ device at $V_{pd} = -10$ V (a), -30 V (c), -50 V (e) as prolonging the retention time to 8 hours. Electron concentration and mobility as a function of retention time at $V_{pd} = -10$ V (b), -30 V (d), -50 V (f).
- 10 Figure 42 shows a) Schematic of the MoTe₂/BN energy band diagram under erasing process. b) Transfer characteristics of the pristine, photodoped, and erased MoTe₂ device. During the erasing process, the MoTe₂/BN device is illuminated under positive backgate. The ionized positive defects in BN are filled by photon-excited electrons from BN valence band, generating large
- 15 quantity of holes. Attributing to the external electric field, the generated holes in BN move to MoTe₂. Consequently, the localized positive charges in BN are vanished and the device returns to its original transport behavior after erasing (Figure 38(b)).
- 20 Figure 43 shows a) Rectification ratio versus backgate (V_g from -65 V to -51 V). b) Transfer characteristics of MoTe₂ diode with four different junction regimes. c) Schematic energy band diagram of the diode for four different junction configurations through tuning the backgate. The rectangle in yellow color represents the MoTe₂ channel on BN with photodoping. E_F is the Fermi
- 25 level energy.

Figure 44 shows that a MoTe₂ inverter is nearly free of interfacial bubbles and residues after the dry transfer process, as observed in the dark-field microscopy image, indicating the clean interfaces between MoTe₂/BN and

30 BN/Gr, which promises the high quality of the inverter.

Figure 45 shows the electron transport in the doped MoTe₂ channel is

significantly enhanced, while the undoped MoTe₂ still preserves hole-dominated transport behavior. Moreover, the subthreshold swings of the undoped and doped MoTe₂ channel are as small as 178 mV dec⁻¹ and 126 mV dec⁻¹ respectively, ensuring the fast switching between the high state and low state for the MoTe₂ inverter, which thereby results in the high gain.

Figure 46 shows a) Optical image of a newly-fabricated MoTe₂ inverter. b) Output characteristic and static power consumption of MoTe₂ inverter as a function of V_{IN} at different V_{DD} from 0.1V to 3V. The dashed line marks the peak position of the power consumption at each V_{DD} . c) Static power consumption versus V_{DD} .

Detailed description

Embodiments generally relate to semiconductor devices that include 2D semiconductor materials that at least partly contact a photosensitive material to form a heterojunction. The heterojunction thus formed is, or is part of, a channel of the semiconductor device that extends between two electrodes (e.g., source and drain electrodes of a field effect transistor). Embodiments also relate to methods of manufacturing field effect transistors.

For example, in a first embodiment and referring to Figure 1, a semiconductor device in the form of a field effect transistor 100 comprises a gate electrode 102 disposed on one side of a substrate 104. A gate dielectric 106 is disposed on the other side of the substrate 104. A layer 108 of a photosensitive material is disposed on the gate dielectric layer 106. It will be appreciated that the photosensitive material may itself be a dielectric, in which case layers 106, 108 may collectively be considered to be a "gate dielectric" that is photosensitive. That is, the gate dielectric may be the photosensitive material, and/or may be disposed adjacent to (for example, disposed directly on) the photosensitive material.

The substrate 104 may be silicon, and the gate dielectric 106 may be SiO₂, for example.

Advantageously, the photosensitive material 108 has a bandgap containing
5 one or more mid-gap states that are excitable by optical radiation. For example, the photosensitive material may be hexagonal boron nitride (h-BN). In another example, the photosensitive material may be a metal oxide, for example in the form of a film.

10 A channel layer 110 directly contacts the photosensitive material 108. The channel layer 110 is formed from a two-dimensional semiconductor material, preferably a direct bandgap semiconductor material, such as a transition metal dichalcogenide (TMD). In particular, the TMD may be WSe₂ or MoTe₂. In other embodiments, the semiconductor material may be phosphorene (also
15 referred to herein as black phosphorus).

The channel layer 110 may comprise a monolayer of the 2D semiconductor material, or alternatively, may comprise multiple layers of the 2D semiconductor material. In particular, the channel layer 110 may be a
20 monolayer of WSe₂ or multilayer WSe₂, or may be multilayer MoTe₂ or phosphorene.

The FET 100 also comprises, disposed on photosensitive material 108, a pair of electrodes 120 and 122. Electrode 120 is a source electrode and electrode
25 122 is a drain electrode, though it will be appreciated that their roles may be reversed depending on the voltage that is applied to each.

Electrodes 120 and 122 are arranged such that the region of the channel layer 110 which forms a heterojunction with the photosensitive material 108
30 extends between them. This heterojunction region forms a transport channel of the field effect transistor 100 in a manner which will be described in more detail below.

In one embodiment, the FET 100 may be, or may form part of, a multibit nonvolatile optoelectronic memory-based on a hybrid structure of thin layered tungsten diselenide (WSe_2) as 2D semiconductor material 110 and boron nitride (BN) as the photosensitive material 108. Advantageously, the storage current of the WSe_2/BN optoelectronic memory can be effectively modulated by the backgate voltage, resulting in a memory switching ratio of approximately 1.1×10^6 . This large switching ratio coupled with the optically tunable characteristic ensures over 128 distinct storage levels (7 bit storage). As will be discussed in further detail below, the device is also highly reliable, as reflected by its long retention time and large number of program-erase testing cycles. Moreover, the WSe_2/BN optoelectronic memory has a wavelength distinguishing property, and may therefore advantageously be applied in a filter-free color image sensor.

With reference to Figure 2, in another embodiment, a semiconductor device in the form of a p-n junction device 200 comprises a gate electrode 202 disposed on one side of a substrate 204. A gate dielectric 206 is disposed on the other side of the substrate 204. A layer 208 of a photosensitive material is disposed on the gate dielectric layer 206. As for device 100, it will be appreciated that the photosensitive material may itself be a dielectric, in which case layers 206, 208 may collectively be considered to be a "gate dielectric" that is photosensitive. That is, the gate dielectric may be the photosensitive material, and/or may be disposed adjacent to (for example, disposed directly on) the photosensitive material.

Advantageously, the photosensitive material 208 has a bandgap containing one or more mid-gap states that are excitable by optical radiation. For example, the photosensitive material may be hexagonal boron nitride (h-BN). In another example, the photosensitive material may be a metal oxide, for example in the form of a film.

A channel layer 210 of a two-dimensional semiconductor material, preferably a direct bandgap semiconductor material, such as a transition metal dichalcogenide (TMD), directly contacts the photosensitive material 208. In particular, the TMD may be WSe_2 or MoTe_2 . In other embodiments, the
5 semiconductor material may be phosphorene (also referred to herein as black phosphorus).

The channel layer 210 also directly contacts the gate dielectric 206.
10 Accordingly, during a photodoping process in which channel layer 210 is illuminated, the part of channel layer 210 that contacts the photosensitive material 210 is electron-doped, while the part of channel layer 210 that contacts the gate dielectric 206 retains hole-dominated transport behaviour. A non-volatile homogeneous p-n junction is therefore formed at the
15 homointerface between the two parts of channel layer 210.

The channel layer 210 may comprise a monolayer of the 2D semiconductor material, or alternatively, may comprise multiple layers of the 2D semiconductor material. In particular, the channel layer 210 may be a
20 monolayer of WSe_2 or multilayer WSe_2 , or may be multilayer MoTe_2 or phosphorene.

The p-n junction device 200 also comprises, disposed on photosensitive material 208, a pair of electrodes 220 and 222. Electrode 220 is a source
25 electrode and electrode 222 is a drain electrode, though it will be appreciated that their roles may be reversed depending on the voltage that is applied to each.

Electrodes 220 and 222 are arranged such that the region of the channel layer
30 210 which forms a heterojunction with the photosensitive material 208 extends between them.

With reference to Figure 3, in a further embodiment, a semiconductor device in the form of an inverter 300 comprises a first dielectric layer 306 disposed on a substrate 304. A gate electrode 302 is disposed on the first dielectric layer 306.

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Also disposed on the first dielectric layer 306, in contact with gate electrode 302, is a graphene layer 303 (which may be few-layer graphene, for example). The graphene layer 303 is used as the back gate to provide the input signal in this configuration, which improves the performance of the inverter 300. It will be appreciated that the back gate may alternatively be configured in similar fashion to that of the embodiments of Figures 1 and 2.

A layer of photosensitive material 308 is disposed on the graphene layer 303. For example, the photosensitive material 308 may be one having a bandgap containing one or more mid-gap states that are excitable by optical radiation. For example, the photosensitive material may be hexagonal boron nitride (h-BN). In another example, the photosensitive material 308 may be a metal oxide, for example in the form of a film.

20 In the embodiment of Figure 3, the photosensitive material may be a dielectric, and as such, the photosensitive layer 308 acts as a gate dielectric in this arrangement.

Two channel layers 310, 312 of a two-dimensional semiconductor material, preferably a direct bandgap semiconductor material, such as a transition metal dichalcogenide (TMD), directly contact the photosensitive material 308. In particular, the TMD may be WSe_2 or MoTe_2 . In other embodiments, the semiconductor material may be phosphorene (also referred to herein as black phosphorus).

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Each channel layer 310, 312 may comprise a monolayer of the 2D semiconductor material, or alternatively, may comprise multiple layers of the

2D semiconductor material. In particular, the channel layers 310, 312 may each be a monolayer of WSe₂ or multilayer WSe₂, or may be multilayer MoTe₂ or phosphorene.

- 5 The inverter 300 also comprises, disposed on photosensitive material 308, three electrodes 320, 322 and 324. The electrodes are arranged such that heterojunction regions of the respective channel layers 310, 312 (i.e., the regions of contact between the channel layer 310 or 312 and the photosensitive material 308) extend between pairs thereof. For example, electrodes 320 and 324 may be source electrodes (serving as ground and power supply respectively) and electrode 322 a drain electrode (serving as output signal).

- Due to the separation of the two channel layers 310, 312, they may be selectively photodoped, such that for example, first channel layer 310 may be illuminated to configure it as an N-FET, while second channel layer 312 is not illuminated and thus configured as a P-FET.

- A yet further embodiment of a semiconductor device 400 is shown in Figure 4. Device 400 is similar in many respects to the device 100 of Figure 1 (and Figure 4 adopts like reference numerals to label like components accordingly), but is a top gate configuration which also includes a metal oxide layer 402 disposed on semiconductor layer 110, and a top electrode 404 disposed on metal oxide layer 402. It will be appreciated that similar top gate configurations may be adopted for the embodiments of Figures 2 and 3.

Examples

- Embodiments of the invention are further illustrated by reference to the following non-limiting examples.

Example 1 – FET comprising a WSe₂/BN heterojunction

Figure 5a shows a schematic of a hybrid WSe₂/BN optoelectronic memory that is a specific example of the device 100 of Figure 1. The optoelectronic memory is fabricated in a field-effect-transistor (FET) structure, in which a
5 monolayer WSe₂ flake is transferred on top of a BN flake. The crystallinity and thicknesses of both WSe₂ and BN are characterized by Raman and AFM, respectively. With reference to Figures 10 and 11, Figure 10(b) shows the Raman spectrum of the exfoliated WSe₂, with two characteristic peaks located at 250 cm⁻¹ and 261 cm⁻¹ respectively. There is no distinct peak at 316 cm⁻¹,
10 indicating the monolayer nature of the WSe₂ flake. This result is further confirmed by the PL spectrum (Figure 10(c)) which exhibits a strong PL peak at 1.65 eV, belonging to single-layer WSe₂. The Raman mapping of the E_{2g}^1 mode indicates the high uniformity of the monolayer WSe₂ flake (Figure 10(d)). Figure 10(e) illustrates the Raman spectrum of the BN flake, with one
15 characteristic peak at 1365 cm⁻¹. The hybrid WSe₂/BN FET demonstrates p-type transport behavior (Fig. 5b).

Figure 5c shows the dynamic behavior of the WSe₂/BN optoelectronic memory in a single cycle, which includes programming, readout, and erasing
20 processes. The mechanism of these three processes is illustrated in Fig. 5d–f, respectively. Since WSe₂ is intrinsically p-type, the current of the pristine WSe₂/BN FET in the positive gate regime is considerably low. In order to program the memory, the device is illuminated by a light pulse (duration 0.5 s, wavelength 405 nm, intensity 210 mW cm⁻²) under negative gate pulse, which
25 results in remarkable excitation of electrons from the mid-gap donor-like states (defects) of BN to its conduction band (Fig. 5d). The photon-excited electrons in BN conduction band can transfer into WSe₂ driven by the electric field, leaving the positive charges localized in the middle of the BN bandgap. It is worth noting that these localized positive charges in BN can effectively
30 screen the negative gate and hence weaken the electric field exerted on WSe₂ during the programming process (Figure 12). The elimination of the effective electric field in BN symbolizes the termination of the programming

process. The positive charges can be stored in BN even after removing the negative gate and switching off the light, thereby serving as an effective local gate and generating a stable electron-storage effect in WSe₂. The storage current I_{store} after programming is readout at a positive gate under dark
 5 condition, as shown in Fig. 5e. When the gate is switched to 50 V, a sharp rise of current can be observed, followed by stabilization at around 22 nA, which indicates the nonvolatile property of the WSe₂/BN memory (Fig. 5c).

The erasing operation is realized by applying positive gate on WSe₂/BN with
 10 light illumination (Fig. 5f). In this process, the ionized positive defects in BN are filled by photon-excited electrons from the BN valence band, generating a large quantity of holes. Because of the external electric field, the generated holes in BN move to WSe₂. As a consequence, the localized positive charges in BN disappear and the device returns to its original hole-domination transport
 15 behavior after erasing, as shown in Fig. 5b. It is noted that the charge erasing is completed in 2 s, indicating the fast switching of the WSe₂/BN memory. Moreover, the average erased current I_{erase} is read as 1.3×10^{-12} A (inset of Fig. 5c), contributing to a large switching ratio with $I_{\text{store}}/I_{\text{erase}}$ of approximately 1.7×10^4 .

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Programming gate controlled optoelectronic memory

Figure 6a shows the transfer characteristics evolution of the WSe₂/BN device under different programming gates (V_{pro} from 0 V to -80 V). The on current in
 25 the electron-domination regime gradually rises with increasing V_{pro} , which indicates a significant gate-tunable electron-doping effect on WSe₂. The dynamic behavior of the WSe₂/BN optoelectronic memory modulated by V_{pro} was also investigated (Fig. 6b). When the V_{pro} is switched from 0 V to -80 V with a -10 V step, the storage current increases stepwise, generating 9
 30 clear storage states. The switching ratio at different V_{pro} is obtained through extracting the storage current. As shown in Fig. 6c, the switching ratio is largely enhanced from 3.8×10^3 to 1.1×10^6 when V_{pro} increases from 0 to

–80 V. The larger negative backgate can better stabilize the generated positive charges in the middle of the BN bandgap and facilitate the formation of a higher concentration of positive charges in BN, which can result in more effective electron-doping and greater storage current in WSe₂.

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In order to evaluate the reliability of an optoelectronic memory for practical application, both the retention time and the cyclic program/erase endurance of the device were investigated. Figure 6d shows the nonvolatile and data retention property of the memory under different V_{pro} , in which highly stabilized storage states are observed within the time range of 4.5×10^4 s. It is worth noting that the memory is kept isolated from any external perturbation (no voltage and no light) after programming and the storage currents in Fig. 6d were extracted in a fixed interval of 3.1×10^3 s (Figure 13). The retention curves are then extrapolated to 10 years, which is a technical requirement for commercial nonvolatile memory (Figure 14). Nearly half the stored currents are expected to be maintained after 10 years with clearly distinguished storage states, indicating the excellent data retention property of the WSe₂/BN optoelectronic memory. Figure 6e displays the repeatability of the program/erase process at different V_{pro} (0, –20, –40, –60, and –80 V) for 200 cycles. The deviation from the average value of the readout currents for each V_{pro} is less than 10%, indicating that the programmed data is highly reproducible.

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One hundred thirty current-level optoelectronic memory

The WSe₂/BN optoelectronic memory of the presently disclosed embodiments demonstrates a high switching ratio, which indicates the possibility to achieve multibit memory with excellent storage capability. Figure 7a shows the dynamic behavior of the memory under periodic exposures of light pulses (130 pulses, $t_{pro} = 0.5$ s, $\lambda = 405$ nm, $P = 2$ nW) at $V_{pro} = -80$ V, and Fig. 7b–e are the enlarged regions I–IV, respectively. The storage current rises progressively with increasing the pulse number, a phenomenon that represents the

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continual accumulation of electrons in WSe₂ as prolonging the light exposure on the memory. One hundred and thirty light pulses may be used, resulting in 130 effective storage states before the current saturation.

- 5 With reference to Figure 15, it was observed that the storage current gradually saturates with increasing the pulse number, as shown in Figure 15(a). The storage current almost stays constant when the storage level is more than 130 (Figure 15(b)). In embodiments of the WSe₂/BN memory, the photon-excited electrons in the BN conduction band can transfer into WSe₂ driven by the
 10 electric field, leaving the positive charges localized in the middle of the BN bandgap.

The reliability of the storage states was evaluated by comparing the gaps between two neighboring states, and their noise.

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- Figure 16(a) shows an example of a calculation of the storage currents and standard deviations (STDs) for states 58 and 59. When the gate voltage is switched to 50 V after programming, the electron-domination current increases sharply followed by stabilization. Both the average storage currents
 20 and their STDs are calculated in the area where the current becomes stable (encircled by a rectangle in Figure 16(a)). The storage currents of states 58 and 59 are 47.7 nA and 52.0 nA, while their STDs are 0.8 nA and 1.2 nA respectively. The gap between states 58 and 59 should be larger than their STD sums, so that these two states are distinguishable. Therefore, the gap to
 25 STD sum ratio may be defined as:

$$Ratio = \frac{I_{store}(n+1) - I_{store}(n)}{STD(n+1) + STD(n)}$$

- Where n = 1, 2, 3..., 129. Through substituting the storage currents and STDs
 30 of states 58 and 59 in the formula, a ratio of 2.15 can be computed, larger

than 1, indicating that these two states are distinguished from each other. The reliability of the other states is evaluated by the same method, and the result is plotted in Figure 16(b). All the ratios are beyond the critical line $Y = 1$, which suggests the validity of all the storage states.

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The result demonstrates that all the storage states for our WSe₂/BN optoelectronic memory are valid. During 20 repetitions of the program-erase cycle, at least 130 valid storage levels were achieved for each of the 20 independent cycles, which suggests excellent repeatability of the WSe₂/BN memory. The dynamic behavior of the 1st, 10th, and 20th cycle is shown in Figure 17 for illustration. The storage current rises progressively with increasing pulses, followed by a gradual saturation when the pulse number goes beyond 130, which is consistent with the result shown in Fig. 7a. The Y ratios for all the selected cycles have also been plotted in Figure 17, indicating the validity of the 130 states for each cycle by ensuring $Y > 1$. It is proposed that the repeatability is mainly due to the similar erased currents (in the magnitude of 10^{-12} A) after each cycle (Figure 18). The same level of base current means the same starting point for each independent cycle, which ensures the high repeatability of the WSe₂/BN memory. Accordingly, the presently disclosed structure may be used to fabricate an optoelectronic memory with data storage capacity of more than 7 bits (128 levels).

The number of storage states may be limited by the noise level. More storage states could be achieved by further minimizing the noise. Moreover, the memory device can be operated under light energy of 1 nJ, indicating its high light sensitivity.

Spectrum distinction of WSe₂/BN optoelectronic memory

Optoelectronic memory with the capability of wavelength discrimination is particularly superior for the application of filter-free color image sensor. Figure 8a shows the dynamic behavior of the WSe₂/BN optoelectronic memory

illuminated by light with wavelengths from 750 (1.65 eV) to 410 nm (3.02 eV). The corresponding readout current increases stepwise from 3×10^{-2} to $1.5 \mu\text{A}$ when the wavelength decreases from 750 to 410 nm. The on current in the electron-domination regime after each programming process also rises gradually when shortening the programming wavelength (Fig. 8b), in good agreement with the dynamic results. Moreover, the storage states at different wavelengths are highly distinct, indicating excellent wavelength distinguishing capability of the WSe₂/BN optoelectronic memory. In order to quantify the modulating ability of different wavelengths, the programming rate (PR) may be defined as below,

$$\text{PR} = \frac{I_{\text{store}}}{P_{\text{density}} \cdot S \cdot t_{\text{pro}}} \quad (1)$$

Where P_{density} is the power density of light, S is the device area. The relationship between PR and photon energy is plotted in Fig. 8c. The monotonic increase of PR with photon energy suggests that light with higher photon energy (shorter wavelength) can induce greater amount of stable localized positive charges in BN in a unit time. It is notable that the PR starts increasing rapidly when the photon energy exceeds 2.6 eV.

Integrated memory matrix for color image sensor

A WSe₂/BN optoelectronic memory is capable of detecting and discriminating lights with different wavelengths, indicating its applicability for filter-free color image sensors. In certain practical applications, a large quantity of image sensors may be fabricated in an integrated circuit, for example.

The large area CVD grown WSe₂ may be used to fabricate the sensor matrix, with its monolayer characteristic confirmed by the Raman and PL spectra (Figure 19). Figure 9a displays a false-colored SEM image of the integrated pixel matrix with 27 WSe₂/BN image sensors arranged in a 3×9 array. The darker color in the upper right part of the image is due to the slight thickness variation of BN substrate (Figure 20). Each pixel with channel length

approximately 2 μm is able to function independently since the pixels can be isolated by e-beam lithography (EBL) and deep reactive ion etch (RIE). In order to investigate the color sensing property of an individual pixel and the image capture ability of the matrix, three laser beams (spot diameter 3 μm) with different wavelengths (red 638 nm, green 515 nm, and blue 473 nm) can be used to expose the selected pixels in sequence. Three pixel groups (group I: 11, 13, 21, 22, 23, 31, 33; group II: 14, 16, 24, 26, 34, 35, 36; and group III: 17, 19, 27, 29, 37, 39) record the three different lights, while the other pixels are left unexposed. Figure 9b demonstrates the corresponding schematic of the matrix after selective exposures. The image NUS is captured in the matrix, in which N, U, and S record the three different lights (red, green, and blue), respectively. More intriguingly, the three different pixel groups display three distinct storage states with slightly fluctuating I_{store} 5, 12, and 31 nA, respectively (Figure 21), which enables the realization of a color image.

Fabrication and characterization of optoelectronic memory

The hybrid structure of WSe₂ and BN was achieved by a dry transfer method. Firstly, few-layer BN flakes with thickness around 10 nm were mechanically exfoliated onto 300 nm SiO₂/Si substrate. In the following, the WSe₂ flake exfoliated on a transparent polydimethylsiloxane (PDMS) substrate was aligned on the BN flake using optical microscope. After the alignment, the PDMS film was pressed on the Si substrate for 2 min followed by a slow lift up, during which the WSe₂ flake was transferred onto the BN flake. The BP/BN heterostructure was obtained by the same dry transfer method. To avoid oxidation of the BP flakes, the experiment was carried out in a glovebox. Standard EBL was employed to define the memory channel and the electrodes (Ti/Au) was deposited by thermal evaporation. After lift-off, the memory device was loaded into a vacuum chamber (pressure below 10⁻⁷ mbar) for characterizations. The optoelectronic measurements were conducted by using an Agilent 2912A source measure unit. Four laser beams (638, 515, 473, and 405 nm) and an exon light source configured with a monochromator were used

to program or erase the memories. The light density was calibrated by THORLABS GmbH (PM 100A) power meter.

CVD WSe₂ growth

A one-zone tube furnace was used to grow WSe₂. Hundred milligram Se powder (Sigma-Aldrich, 99.5%) was loaded at upstream, and kept at 300 °C during growth. A mixture of WO_{2.9} (30 mg, Alfa Aesar, 99.99%) and NaCl (10 mg, Sigma-Aldrich, 99.5%) was loaded at the center of reaction zone. The temperature of reaction zone gradually increased to 830 °C in 22 min, and cooled down to room temperature after staying at 830 °C for 15 min. Pure Ar and H₂ (90/10 sccm) were used as carrying gas.

Fabrication of 2D pixel matrix

CVD WSe₂ was transferred onto BN flake by a wet transfer method. Firstly, the as-grown WSe₂ on Si substrate coated with 300 nm SiO₂ was spin coated by polymethyl methacrylate (PMMA). The Si substrate was then left in 2 M KOH solution for several hours, yielding PMMA coated WSe₂ film. The WSe₂/PMMA film was washed in deionized water for three times before transferring onto exfoliated BN flake. EBL was used to pattern pixel matrix on the large area heterostructure followed by RIE to isolate each pixel. The electrodes were then patterned using standard EBL, thermal deposition, and lift-off.

20 Example 2 - BP/BN optoelectronic memory

The configuration of the heterostructure-based optoelectronic memory in accordance with the device 100 of Figure 1 can be applied to other 2D crystals. Phosphorene or Black Phosphorus (BP), a 2D material, has been widely investigated recently due to its superior optical and electrical transport properties.

The BP/BN optoelectronic memory fabricated in the same configuration as in Figure 1 also demonstrates excellent data storage ability. Referring to Figures 22-24, the initial transfer curve presents a current minimum of 15 V. When increasing the V_{pro} to -60 V, the current minimum progressively moves to -48

V. This suggests a significant electron-doping effect in BP modulated by backgate, a characteristic similar to that of the WSe₂/BN memory of Example 1. The dynamic behavior shows that the storage current increases stepwise with the increase of V_{pro} , consistent with the transfer characteristics evolution.

5 7 distinguishable storage states are observed in Figure 24(b) through applying 7 different V_{pro} . The switching ratio rises in a nearly linear trend with respect to V_{pro} , from 49 to 415 (Figure 24(c)).

The erasing time of the BP/BN memory (150 s) is longer compared to that of the WSe₂/BN memory. It is proposed that the long erasing time in BP/BN

10 memory is mainly due to the electron trapping states in BP which was studied before. During programming, the photogenerated electrons in BN can transfer and be stored in BP driven by the external electric field. Some of these transferred electrons could be trapped by the trapping sites inside BP. In the erasing process, the ionized positive defects are filled by photon-excited

15 electrons from the BN valence band, generating a large quantity of holes. Because of the external electric field induced by the positive gate, the generated holes in BN and the stored electrons in BP accumulate at the BP/BN interface. Consequently, the electron-hole pairs intensely recombine, which leads to the erasure of stored electrons in BP. However, those trapped

20 electrons in BP are quite localized, which makes them difficult to be recombined, therefore, resulting in the long erasing time. In the case of WSe₂, the shorter erasing time is expected due to the absence of locally trapped electrons.

The storage states of the BP/BN memory can be effectively modulated by light

25 wavelength and the device possesses high reliability (Figures 25 and 26), similarly to the WSe₂/BN memory. However, the switching ratio of the BP/BN memory (around 415) is lower than that of the WSe₂/BN device, which is mainly due to the large off current of our BP FET. It is possible to further improve the switching ratio by selecting thinner BP flakes. Unexpectedly, the

30 BP/BN heterostructure is particularly sensitive to weak light. An ultrahigh photo responsivity approximately $1.2 \times 10^7 \text{ A W}^{-1}$ is observed for the device,

making BP/BN heterostructure a promising candidate for photodetector application.

Referring to Figure 27, I_{ph} is defined as the current difference of the BP/BN device under dark and light illumination conditions: $I_{ph} = I_{light} - I_{dark}$. The photocurrent is strongly dependent on V_{pro} , where the I_{ph} gradually increases with the increase of gate voltage. The photo responsivity (R) as a critical parameter of photodetector performance, is calculated and plotted as a function of V_{pro} as shown in Figure 27(b). R is defined as the photocurrent generated by per unit power of incident light on the effective area of a photodetector:

$$R = I_{ph} / (P_{density} \cdot S)$$

The photo responsivity displays nearly linear dependence on the programming gate, progressively increasing from $2 \times 10^6 \text{ AW}^{-1}$ ($V_{pro} = -10 \text{ V}$) to $1.2 \times 10^7 \text{ AW}^{-1}$ ($V_{pro} = -80 \text{ V}$). This extraordinary photo responsivity is comparable to or even larger than the results of recently reported ultrasensitive BP photodetectors, indicating BP/BN heterostructure as a promising candidate for photodetector application.

Example 3 – MoTe₂/BN heterostructure

Certain embodiments relate to photoinduced non-volatile and programmable electron doping in MoTe₂ FET based on a multilayer MoTe₂/BN heterostructure. The electron doping effect in MoTe₂ is highly robust, as reflected by its long retention time exceeding 14 days. On the other hand, the doping effect can be conveniently erased and programmed by tuning the polarity of the photodoping gate exerted on BN, indicating its reversibility. Figure 28(a) shows the optical microscopy image of a trilayer MoTe₂ FET with metal contact of Ti/Au (5nm/80nm), on top of the BN flake. The MoTe₂ and BN flakes were characterized by Raman spectra (Figure 33) and Atomic Force Microscopy (AFM) measurement (Figure 34). The transfer curves ($I_{sd}-V_g$) of the MoTe₂ device before and after photodoping in linear scale are shown in Figure 28(b).

- The pristine MoTe₂ device shows a typical hole-dominated ambipolar transport behavior, consistent with previous reports. To photodope the MoTe₂ FET, the device is illuminated by a light pulse (duration 3 mins, wavelength 405 nm, intensity 20 mW cm⁻²) under negative photodoping gate (V_{pd}). After the
- 5 photodoping process at $V_{pd} = -5$ V, the on-current in electron regime is strongly increased, which indicates an electron doping effect in the MoTe₂. Moreover, the on-current in electron regime almost reaches the same level as that of the hole regime, demonstrating a more symmetric and balanced ambipolar characteristic in the MoTe₂ device. With higher photodoping gate
- 10 ($V_{pd} = -20$ V), the current of the electron side is further enhanced, evolving beyond the hole side, indicating an electron-transport dominated ambipolar behavior. These results demonstrate that photodoping can effectively improve the electron transport in the MoTe₂ device, thereby inducing either a more balanced ambipolar or even electron-dominant transport behavior.
- 15 The mechanism of the photoinduced electron doping in the MoTe₂ device is shown in Figure 28(c), which is proposed by the excitation of the mid-gap donor-like states (defects) in the BN flake. It is to note that the donor-like energy levels are mainly distributed close to the middle of the BN bandgap, which is illustrated by the spectra dependent characteristics in Figure 35.
- 20 Figure 35 demonstrates the relationship between the photodoping rate and photon energy by using an exo light source configured with a monochromator. The photodoping rate (D) is defined as the enhancement of electron concentration in MoTe₂ device by per unit power of incident light in a unit time:

$$D = \frac{\Delta n}{(\Delta t \cdot \frac{P}{A})}$$

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where $\Delta n = n_{dope} - n_{pristine}$, $n_{pristine}$ is the electron concentration in the pristine MoTe₂, and n_{dope} is the electron concentration in MoTe₂ after photodoping. Δt is the light illumination time, P/A is the power density of incident light. The

photodoping rate increases rapidly when the photon energy exceeds ~ 2.7 eV, which is consistent with the trend observed in the graphene/h-BN heterostructure. The spectra dependence indicates that the major donor-like energy levels are distributed close to the middle of the BN bandgap. Moreover, the photodoping rate keeps increasing with increasing the photon energy from ~ 2.7 eV to ~ 3.06 eV in a broad range, suggesting that such donor-like energy levels form a broad distribution within the BN bandgap.

When the MoTe₂/BN heterostructure is illuminated by light, the electrons occupying the donor-like states in the BN bandgap are excited to the conduction band. These photon-excited electrons can transfer into MoTe₂ under an external electric field (applying the negative V_{pd}), leaving positive charges localized in the mid-gap of BN. The localized positive charges can weaken the external electric field exerting on BN during the doping process. The elimination of the effective electric field in BN symbolizes the termination of the doping process. The transfer curve is nearly maintained after 3 mins light illumination (Figure 36), suggesting the completion of the photodoping process. It is noted that the positive charges mainly distribute deep in the BN flake after photodoping, which is supported by the hysteresis measurement in Figure 37.

Figure 37 shows the transfer curves of pristine and photodoped (at $V_{pd} = -30$ V, -50 V, -70 V and 3 mins light illumination) MoTe₂/BN device under both forward (V_g sweeps from -80 V to 50 V) and backward (V_g sweeps from 50 V to -80 V) gate sweeps. The forward and backward transfer curves almost coincide for the photodoped device at each V_{pd} , indicating the weak hysteresis of the device. Moreover, such weak hysteresis is comparable to that of the pristine MoTe₂ device. These results indicate that the positive charges in close proximity to the MoTe₂ channel are nearly eliminated after 3 mins photodoping, which therefore strengthens the transport property and reduces the hysteresis of the MoTe₂ device. These results also further support a conclusion that the positively charged defects distribute deep in the BN flake.

These positive charges are stored in BN even after removing the negative gate and switching off the light, which serve as an effective local gate exerting on MoTe₂ and results in a stable electron doping effect in MoTe₂ (Figure 28(d)). Light illumination can also induce the intrinsic photocurrent in the MoTe₂ flake, which is demonstrated in Figure 38.

Figure 38(a) shows an optical image of the newly-fabricated MoTe₂/h-BN heterostructure.

Figure 38(b) demonstrates the time dependent photoresponse of the heterostructure at $V_{pd} = -50$ V and $V_{sd} = 0.1$ V. When the device is illuminated under light, the hole transport current first drops dramatically, followed by a stabilization as prolonging the illumination time to 3 mins. The decay of the hole transport current is mainly due to the generation of positive charges in BN during photodoping. These positively charged defects can effectively screen the electric field induced by the negative backgate exerting on the MoTe₂, which, in turn, results in the decrease of the hole transport current in the MoTe₂ device. When the light is switched off, the current drops again. It is proposed that the second drop is due to the decay of the intrinsic photocurrent in MoTe₂ in the absence of illumination. The photocurrent is estimated to be ~ 0.06 nA from the inset of Figure 38(b). These results indicate that light illumination not only excites the donor-like states and produces positive charges in h-BN, but also induces the intrinsic photocurrent in MoTe₂. The positive charges are stored in BN even after removing the negative gate and switching off the light, which serve as an effective local gate exerting on MoTe₂ and result in a stable electron doping effect in MoTe₂, as shown in the transfer characterization in Figure 38(c). In contrast, the intrinsic photocurrent in MoTe₂ disappear immediately when the light is off. Therefore, any non-negligible influence from the intrinsic photoresponse in MoTe₂ after photodoping is not expected.

The present inventors also investigated the photoresponse of the MoTe₂ device on a bare SiO₂ substrate (Figure 38(d)). When the light is on, the current increases sharply, demonstrating the clear intrinsic photoresponse of

the device under illumination (Figure 38(e)). The photocurrent of ~ 0.16 nA is comparable to the device on BN. Figure 38(f) compares the transfer characteristic of the device before and after 3 mins light illumination at $V_g = -50$ V. The transfer curve is almost maintained after illumination, suggesting that the photoresponse in MoTe₂ does not introduce any doping effect and change the transfer characteristic of the MoTe₂ device.

Nevertheless, such photocurrent immediately disappears once the light is off, which does not introduce any doping effect and change the transfer characteristic of the MoTe₂ device. The *in-situ* Raman characterization was carried out to investigate whether other effects, such as gate-bias stress, lattice distortion, and oxidation occurred during photodoping, as shown in Figure 39. After photodoping for 3 mins, no obvious peak shift or broadening for all characteristic peaks of MoTe₂ was observed, and no additional Raman peak emerged, implying that photodoping does not introduce any additional non-negligible effects in the MoTe₂ flake.

The electron doping level in MoTe₂ can be modulated by the photodoping gate. Figure 29(a) demonstrates the evolution of transfer characteristics of MoTe₂ device with increasing V_{pd} from -10 V to -70 V in logarithmic scale. The transfer curve of the pristine device presents a current minimum at ~ 4 V. As V_{pd} gradually increases to -70 V, the current minimum progressively moves to ~ -70 V. This suggests a significant gate-tunable electron doping effect in MoTe₂. To quantitatively evaluate the effectiveness of the doping process, the electron concentration (n_e) in the linear transport regime after photodoping under different V_{pd} can be determined using the formula:

$$n = -\frac{C_g(V_g - V_{th})}{e}$$

where C_g is the capacitance per unit area for the back gate, comprising 300 nm SiO₂ and 14.5 nm BN, $\sim 1.1 \times 10^{-8}$ F cm⁻². V_{th} is the threshold voltage for electron transport. Figure 29(b) shows the electron concentration at $V_g = 40$ V as a function of V_{pd} . In the pristine MoTe₂ device, the electron concentration is

derived to be $2.9 \times 10^{11} \text{ cm}^{-2}$, which increases to $5.8 \times 10^{11} \text{ cm}^{-2}$ after photodoping under $V_{\text{pd}} = -10 \text{ V}$. With further increasing the V_{pd} to -70 V , the electron concentration is largely increased to $2.8 \times 10^{12} \text{ cm}^{-2}$, nearly tenfold that of the pristine MoTe_2 . The larger V_{pd} facilitates the formation of higher
 5 concentration of localized positive charges in BN, which induces more effective electron-doping and greater electron concentration in the MoTe_2 device. The electron mobility (μ_e) with respect to V_{pd} is also investigated and plotted in Figure 29(b). The field effect electron mobility is calculated using the equation:

$$\mu = \frac{L}{WC_g V_{\text{sd}}} \frac{dI_{\text{sd}}}{dV_g}$$

where dI_{sd} / dV_g represents the slope extracted from the linear regime of the electron transport, L and W are the length and width of the conduction channel respectively. Intriguingly, the photodoped MoTe_2 device demonstrates a strong enhancement of electron mobility, from $1.1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for pristine
 15 MoTe_2 to $10.2 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ after doping at $V_{\text{pd}} = -70 \text{ V}$. It is proposed that the mobility enhancement is mainly due to the reduction of Schottky barrier width between MoTe_2 and metal contacts after photodoping. The electron doping pulls MoTe_2 Fermi level towards its conduction band, which reduces the Schottky barrier width for electron injection, thereby leading to the improved
 20 electron mobility. The $I_{\text{sd}} - V_{\text{sd}}$ output curves become much more linear at the low V_{sd} regime and demonstrate near-ideal ohmic behavior after photodoping, as shown in Figure 40, which suggests the reduction of the contact resistance as well as the Schottky barrier width for electron transport.

The $I_{\text{sd}} - V_{\text{sd}}$ output characteristics of the pristine MoTe_2 device are shown in
 25 Figure 40(c). The $I_{\text{sd}} - V_{\text{sd}}$ curves are nonlinear at small V_{sd} regime, even with a back-gate voltage of $V_g = 50 \text{ V}$ where the contact regions are electrostatically doped, indicating a clear Schottky contact behavior of the MoTe_2 device for electron injection. After photodoping at $V_{\text{pd}} = -50 \text{ V}$, the current is significantly enhanced by over one order of magnitude at each
 30 positive gate. Moreover, the $I_{\text{sd}} - V_{\text{sd}}$ curves become much more linear at the

low V_{sd} regime and demonstrate near-ideal ohmic behavior, which suggests the reduction of the contact resistance as well as the Schottky barrier width for electron transport after photodoping.

Non-volatility is an important feature in doping technique, which allows the retention of doping effect in doped material in the absence of external perturbation. Figure 29(c) exhibits the evolution of transfer characteristics of the doped MoTe_2 device ($V_{pd} = -70$ V) as prolonging the retention time up to 14 days. The on-state current in the electron regime is retained with only slight decline, and the current minimum demonstrates weak shift after two weeks. The electron concentration and mobility were extracted and plotted as a function of retention time in Figure 29(d), where these two parameters nearly remain unchanged over 14 days. The transfer characteristics at $V_{pd} = -10$ V, -30 V, and -50 V were also investigated, demonstrating the similar retention behavior (Figure 41). These results illustrate an outstanding non-volatility property of the photodoped MoTe_2 device. The long retention time in the MoTe_2 device can be attributed to two factors, namely, the highly localized positive charges in BN after doping, and the potential barrier between MoTe_2 and BN. The positive charges in BN serve as a highly stable local gate to maintain the electron doping in MoTe_2 . In addition, due to the high potential barrier between BN and MoTe_2 , the electrons in MoTe_2 are unable to transfer back into BN without external assistance (e.g. external electric field and light illumination), thus reducing the possibility of charge recombination. This ensures the stability of the positive charges in BN and the long retention time of the doped MoTe_2 device.

In addition to non-volatility, programmability is another important characteristic which enables the flexible fabrication of logic devices. The electron doping effect in MoTe_2 can be erased, indicating the programmable nature of the photodoping technique. The erasing operation is realized by applying positive gate on the MoTe_2/BN heterostructure under light illumination, as shown in Figure 42(a). In this process, the ionized positive defects in BN are filled by photon-excited electrons from BN valence band,

generating large quantity of holes. Attributing to the external electric field, the generated holes in BN move to MoTe₂. Consequently, the localized positive charges in BN disappear and the device returns to its original transport behavior after erasing (Figure 42(b)). Figure 29(e) and 29(f) display the repeatability of electron concentration and mobility at different $V_{pd} = -10$ V, -30 V, -50 V, and -70V for 20 dope/erase cycles, respectively. The electron concentration and mobility only fluctuate slightly through the 20 cycles at different V_{pd} . The deviations from the average values of the electron concentration and mobility for each V_{pd} are less than 15%, demonstrating the excellent programmability of the photodoped MoTe₂ device.

Example 4 – homogeneous p-n junction

The photoinduced electron doping in MoTe₂ provides the opportunity to fabricate a homogeneous p-n junction with an arbitrary doping pattern, substantially in accordance with the device 200 shown in Figure 2. More importantly, unlike the traditional SCTD technique which requires photolithography together with photoresist to spatially control the doping profile of TMDs, the realization of a homogeneous p-n junction employing photodoping technique is photoresist-free, since the TMDs can be selectively doped through controlling the TMDs/BN heterostructure configuration or light illumination region. Scanning kelvin probe microscopy (SKPM) measurements were carried out for the pristine and photodoped MoTe₂ flake with half located on BN and another half on SiO₂, as shown in Figure 30(a). The SKPM measurements were performed using Bruker Dimension Icon SPM in PeakForce Tapping Mode through highly doped Si tips (PFQNE-AL) in ambient condition. Figure 30(b) exhibits the AFM height image of the heterostructure, with BN thickness around ~14.2 nm. The SKPM image of pristine MoTe₂ flake (before photodoping) is demonstrated in Figure 30(c). The contact potential difference (CPD) between the sample and the AFM tip in the SKPM image is given by:

$$CPD = \frac{(\Phi_{\text{sample}} - \Phi_{\text{tip}})}{e}$$

Where Φ_{sample} and Φ_{tip} are the work function of the sample and the tip, respectively. e is the elementary charge. The CPD difference of the MoTe₂ flakes on SiO₂ and BN substrates is around ~27 mV before photodoping (Figure 30(d)), which is possibly due to the interface trap charges on the SiO₂ substrate. After photodoping at $V_{\text{pd}} = -50$ V for 3 mins (405 nm light with intensity of ~20 mW cm⁻²), the CPD of the MoTe₂ flake on SiO₂ is almost unchanged, while the CPD of the MoTe₂ flake on BN demonstrates a remarkable reduction by nearly ~150 mV (Figure 30(e) and 30(f)). This indicates that the Fermi level of the photodoped MoTe₂ moves closer to its conduction band, revealing an increase of electron concentration and the n-type doping effect in the photodoped MoTe₂, in good agreement with the device measurement results as discussed with reference to Figure 29. Moreover, the potential difference of the MoTe₂ flakes on SiO₂ and BN substrates reaches up to ~177 mV after photodoping, revealing a clear band bending and the generation of MoTe₂ homo-junction at the SiO₂/BN interface. The potential difference is much larger than that of the WSe₂ homo-junction (~55 mV) achieved by helium ion irradiation, and comparable to that of the CVD grown WS₂/WSe₂ heterostructure (~113 mV), as well as the lateral WSe₂ junction (~200 mV) achieved by H₂ plasma treatment induced degenerated n-type doping.

Figure 31(a) shows a schematic of a homogeneous MoTe₂ p-n junction achieved by controlling the MoTe₂/BN heterostructure configuration. Half of the MoTe₂ flake is transferred on BN substrate, with another half on SiO₂. During the photodoping process, the MoTe₂ flake on BN is electron-doped, while the flake on SiO₂ retains its hole-dominated transport behavior, thereby forming a non-volatile homogeneous p-n junction at the homo-interface. Figure 31(b) shows the optical microscopy image of the MoTe₂ p-n junction. To realize the steep p-n homojunction, the device was photodoped under $V_{\text{pd}} = -50$ V. Figure 31(c) exhibits the typical rectification characteristics ($I_{\text{sd}}-V_{\text{sd}}$) of the MoTe₂ diode under gate voltage from -65 V to -51 V with 2 V step in linear and logarithmic (inset) scale. As V_{g} increases from -65 V to -57 V, the currents in both the negative and positive bias regimes decline rapidly. Note that the

current at the negative bias drops much faster than that at the positive side, thereby yielding a remarkable improvement of the rectification ratio (the ratio between the forward current at $V_{sd} = 2$ V and the reverse current at $V_{sd} = -2$ V). When further increasing V_g from -57 V to -51 V, the forward current

5 continues to decrease while the reverse current almost keeps unchanged, resulting in a decline of the rectification ratio. As shown in Figure 43(a), the rectification ratio experiences a significant enhancement when increasing V_g from -65 V to -57 V, peaking at 1.7×10^4 , followed by a gradual decrease. The gate dependent rectification behavior is mainly attributed to the tunability of

10 the built-in potential barrier across the photodoped and undoped MoTe_2 boundary by applying external electric field. As shown in Figure 43(b) and 43(c), the homogeneous junction of the half-doped MoTe_2 junction evolves from p-p, across p-n, and finally to n-n when positively sweeping the back gate.

15 In Figure 43, the transfer curve is divided into four distinct regimes by a hump with two valleys through tuning the backgate. The homogeneous p-n junction is formed in a single MoTe_2 flake after spatially controlling the photodoping region. Through tuning the backgate, the carrier concentrations in the two different channels are further modulated, which thereby induces the tunability

20 of the built-in potential barrier at the homo-interface. The four regimes correspond to the four different junction profiles, that is, p+p, pn-, p-n and nn+ junction, as shown in the energy band diagram. In regime I, the Fermi level of MoTe_2 is pulled down towards the valence band under a large negative backgate, resulting in a remarkable accumulation of holes in the undoped

25 MoTe_2 channel as well as the hole conduction in the doped channel. With increasing the backgate, the Fermi level gradually shifts up into the bandgap and the electron concentration in the doped MoTe_2 channel is strongly enhanced, which leads to the formation of either pn- (regime II) or p-n (regime III) junction at the interface. In these two regimes, the built-in

30 potential barrier at the interface is largely improved, thereby inducing the significant enhancement of rectification ratio. When further increasing the backgate, the Fermi level progressively moves into the conduction band and

the electron concentrations in both MoTe₂ channels are greatly enriched, thus inducing the nn+ junction profile (regime IV).

The I_{sd} - V_{sd} at $V_g = -53$ V in both linear and logarithmic scale is plotted in Figure 31(d). The reverse current is as low as $\sim 10^{-11}$ A, which is advantageous
 5 for low-power electronics. When the bias is switched to the positive regime, the current demonstrates a sharp increase up to $\sim 10^{-7}$ A, which is a hallmark of diode behavior. By linear fitting the current onset in logarithm scale, the ideality factor η is extracted to be ~ 1.13 , exhibiting a near-ideal p-n junction. Such near-ideal MoTe₂ diode coupling with the large rectification ratio is
 10 advantageous in high performance and photoresist-free TMDs p-n junction.

Example 5 – homogeneous MoTe₂ inverter

In addition to p-n junction, a homogeneous MoTe₂ inverter can also be achieved by spatially controlling the doping of an MoTe₂ channel using a photodoping technique. Figure 32(a) shows the schematic of an MoTe₂ inverter
 15 with two channels in series. The inverter of Figure 32(a) is of similar configuration to the device 300 of Figure 3, for example.

Through controlling the light illumination region, the two channels can be selectively doped. The left channel presents n-type transport behavior after photodoping, while the right channel retains its original p-type transport. The
 20 three metal contacts on MoTe₂ sequentially serve as ground GND , output signal V_{OUT} , and power supply V_{DD} , respectively. To improve the performance of the inverter, few-layer graphene (Gr) may be used as the bottom gate to provide the input signal V_{IN} . Figure 32(b) shows the optical microscopy image of the fabricated MoTe₂ inverter. The device is nearly free of interfacial bubbles
 25 and residues after the dry transfer processes (Figure 44), indicating the high quality of the inverter with clean interfaces. A fine-focused laser beam with spot diameter ~ 3 μm was used to spatially control the doping of the MoTe₂ channel. As shown in the transfer characteristics in Figure 45, the electron transport in the doped MoTe₂ channel (at $V_{pd} = -1$ V) is significantly enhanced,
 30 while the undoped MoTe₂ preserves hole-dominated transport behavior. Figure

- 32(c) shows the output characteristic of the homogeneous MoTe₂ inverter as a function of V_{IN} at $V_{DD} = 1$ V, 2V, and 3V respectively. The output curves are clearly divided into three demonstrative regimes of an inverter: the "high state" for high V_{OUT} , "steep slope" for the sharp decrease of V_{OUT} , and "low state" for low V_{OUT} . To evaluate the performance of the inverter, the gain is extracted from the slope of the output characteristic (gain = dV_{OUT} / dV_{IN}) at the three different V_{DD} (Figure 32(d)). The gain follows a Dirac- δ function with respect to the V_{IN} , in which the highest value occurs at the steepest region in the output curve. The gain reaches up to 18 at small $V_{DD} = 1$ V. With further increasing the V_{DD} to 2 V and 3 V, the gain is remarkably enhanced to 42 and 98 respectively, which is among the highest values reported on 2D materials based homo-inverter. The subthreshold swings of the undoped and doped MoTe₂ channels are as small as 178 mV dec⁻¹ and 126 mV dec⁻¹ respectively, ensuring the fast switching between the high state and low state for the MoTe₂ inverter with the high gain. Static power consumption is another important factor for complementary inverter, which is exhibited in Figure 46. Figure 46(b) shows the V_{OUT} - V_{IN} curves and the static power consumption with a V_{DD} supplying from 0.1 V to 3 V. The static power consumption is calculated by the formula: $P = V_{DD} \times I_{DD}$. The V_{OUT} - V_{IN} curve shows sharp logic inversion, and the power consumption shows typical peak behavior as a function of V_{IN} . The peak powers were extracted and plotted versus V_{DD} in Figure 46(c). The power consumption gradually decreases with decreasing the V_{DD} , from several μ W at $V_{DD} = 3$ V to several tens of pW at $V_{DD} = 0.1$ V. It is noted that the power can be as low as 370 pW when the V_{DD} is reduced to 0.1 V.
- The static power consumption gradually decreases with reducing V_{DD} , from several μ W at $V_{DD} = 3$ V to several tens of pW at $V_{DD} = 0.1$ V. It is noted that the power consumption can be as low as 370 pW when V_{DD} is reduced to 0.1 V, which is comparable to other TMDs based inverters.

In summary, the present inventors have demonstrated photoinduced electron doping in MoTe₂ devices based on the MoTe₂/BN heterostructure configuration. The photon-generated electrons from the mid-gap donor-like states in BN

transfer into MoTe₂ under negative gate, leading to the storage of localized positive charges in BN bandgap. These positive charges can serve as effective local gate, which results in the electron doping effect in MoTe₂. Such doping effect can be erased by tuning the polarity of the photodoping gate under light illumination. In the erasing process, the localized positive charges stored in BN recombine with the photo-excited electrons from the BN valence band, thereby eliminating the local gating effect and restoring the original transport behavior of MoTe₂. The photodoping effect has been written and erased for 20 cycles with only slight deviation of the electron transport behavior between each cycle, suggesting the excellent repeatability. On the other hand, in the absence of external perturbation, the photodoping effect in MoTe₂ is retained for over 14 days, illustrating its robust non-volatility. Moreover, the electron transport properties, including the electron concentration and mobility in MoTe₂ device, can be precisely modulated through adjusting the photodoping gate. The electron doping profile in MoTe₂ device can also be spatially controlled, making it possible to fabricate homogeneous p-n junction and inverter. The MoTe₂ p-n junction is realized by configuring the MoTe₂/BN heterostructure, in which the diode exhibits a near-unity ideality factor of ~ 1.13 with a rectification ratio of $\sim 1.7 \times 10^4$. On the other hand, through controlling the illumination region on MoTe₂ channel, the MoTe₂ inverter is achieved with a remarkable gain of ~ 98 at $V_{DD} = 3$ V. The discovery of photodoping technique in 2D TMDs provides a simple method to achieve TMDs based non-volatile and programmable complementary electronic devices in high performance, which paves the way for the application of 2D TMDs in future photoresist-free logic electronics.

Example 6 - Fabrication of 2D MoTe₂/BN and MoTe₂/BN/graphene heterostructures

The hybrid structure of MoTe₂ and BN was achieved by a dry transfer method in a glovebox (Ar atmosphere). Firstly, a few-layer BN flake was mechanically exfoliated onto a 300 nm SiO₂/Si substrate. An MoTe₂ flake exfoliated on a transparent polydimethylsiloxane (PDMS) substrate was then aligned on the

BN flake using an optical microscope. After the alignment, the PDMS film was pressed on the Si substrate for ~ 2 minutes followed by a slow lift up, during which the MoTe_2 flake was transferred onto the BN flake. The $\text{MoTe}_2/\text{BN}/\text{graphene}$ heterostructure was fabricated by the same method in glovebox. A graphene flake was exfoliated on SiO_2/Si substrate firstly, followed by the dry transfer of BN and MoTe_2 flakes in sequence. After the dry transfer, the MoTe_2/BN or $\text{MoTe}_2/\text{BN}/\text{graphene}$ heterostructures on SiO_2/Si substrate was spin-coated by PMMA in the same glovebox for device fabrication. The electrodes were patterned by standard electron beam lithography (EBL) in high vacuum ($\sim 10^{-6}$ mbar), followed by developing in MIBK/IPA (1:3) solution in glovebox. The sample was then loaded in a thermal evaporator in high vacuum ($\sim 10^{-7}$ mbar) to deposit metal contacts of Ti/Au (5nm/80nm). After that, the sample was immersed in acetone solution for several hours to lift off the PMMA layer in glovebox. After lift-off, the as-made devices were wire-bonded onto a leaded chip carrier (LCC) in air immediately, then loaded in a custom-designed high vacuum chamber ($\sim 10^{-7}$ mbar).

Example 7 - Electrical characterization of the 2D FET, p-n junction, and inverter

All the devices were characterized in a high vacuum chamber ($\sim 10^{-7}$ mbar). All the fabricated devices were also stored in the high vacuum chamber after measurements. The electrical measurements were conducted by using an Agilent 2912A source measure unit. A micro-sized laser beam with wavelength 405 nm was used to modulate the photodoping effect. The light intensity of laser beam was calibrated by THORLABS GmbH (PM 100A) power meter.

It will be appreciated that many further modifications and permutations of various aspects of the described embodiments are possible. Accordingly, the described aspects are intended to embrace all such alterations, modifications, and variations that fall within the spirit and scope of the appended claims.

Throughout this specification and the claims which follow, unless the context requires otherwise, the word "comprise", and variations such as "comprises"

and “comprising”, will be understood to imply the inclusion of a stated integer or step or group of integers or steps but not the exclusion of any other integer or step or group of integers or steps.

The reference in this specification to any prior publication (or information
5 derived from it), or to any matter which is known, is not, and should not be taken as an acknowledgment or admission or any form of suggestion that that prior publication (or information derived from it) or known matter forms part of the common general knowledge in the field of endeavour to which this specification relates.

CLAIMS

1. A semiconductor device, comprising:
 - a gate electrode and a gate dielectric that is a photosensitive material
 - 5 and/or is disposed adjacent to a photosensitive material;
 - a channel layer at least partly contacting the photosensitive material to form a heterojunction region, the channel layer being formed from a two-dimensional semiconductor material; and
 - at least one pair of electrodes between which at least part of the
 - 10 channel layer extends, at least partly in the heterojunction region, to thereby form a transport channel of the field effect transistor.
2. A semiconductor device according to claim 1, wherein the channel layer is formed from a two-dimensional direct bandgap semiconductor material.
- 15 3. A semiconductor device according to claim 1 or claim 2, wherein the photosensitive material has a bandgap containing one or more mid-gap states that are excitable by optical radiation.
- 20 4. A semiconductor device according to claim 3, wherein the photosensitive material is boron nitride (BN) or a metal oxide film.
5. A semiconductor device according to any one of the preceding claims, wherein the two-dimensional semiconductor material is a transition metal dichalcogenide.
- 25 6. A semiconductor device according to claim 5, wherein the transition metal dichalcogenide is MoTe_2 or WSe_2 .
- 30 7. A semiconductor device according to any one of claims 1 to 4, wherein the two-dimensional semiconductor material is phosphorene.
8. A semiconductor device according to any one of the preceding claims,

wherein the channel layer is a monolayer of the two-dimensional semiconductor material, or comprises multiple layers of the two-dimensional semiconductor material.

- 5 9. A semiconductor device according to any one of the preceding claims, wherein the back gate comprises a graphene layer.
10. A semiconductor device according to any one of the preceding claims, wherein the channel layer partially contacts the photosensitive material
10 and partially contacts the gate dielectric.
11. A method of fabricating a semiconductor device, comprising:
forming a back gate on a substrate, the back gate comprising a back gate electrode and a gate dielectric, wherein the gate dielectric is a
15 photosensitive material and/or is disposed adjacent to a photosensitive material;
applying a channel layer to at least part of the photosensitive layer to form a heterojunction region, the channel layer being formed from a two-dimensional semiconductor material; and
20 forming electrodes on at least the photosensitive material, whereby at least part of the channel layer extends, at least partly in the heterojunction region, between two of the electrodes to thereby form a transport channel of the field effect transistor.
- 25 12. A method according to claim 11, wherein the channel layer is formed from a two-dimensional direct bandgap semiconductor material.
13. A method according to claim 11 or claim 12, wherein the photosensitive material has a bandgap containing one or more mid-gap states that are
30 excitable by optical radiation.
14. A method according to claim 13, wherein the photosensitive material is boron nitride (BN) or a metal oxide film.

15. A method according to any one of claims 11 to 14, wherein the two-dimensional semiconductor material is a transition metal dichalcogenide.
- 5 16. A method according to claim 15, wherein the transition metal dichalcogenide is MoTe_2 or WSe_2 .
17. A method according to any one of claims 11 to 16, wherein the two-dimensional semiconductor material is phosphorene.
- 10 18. A method according to any one of claims 11 to 17, wherein the channel layer is a monolayer of the two-dimensional semiconductor material, or comprises multiple layers of the two-dimensional semiconductor material.
- 15 19. A method according to any one of claims 11 to 18, wherein the back gate comprises a graphene layer.
- 20 20. A method according to any one of claims 11 to 19, wherein the channel layer partially contacts the photosensitive material and partially contacts the gate dielectric.

AMENDED CLAIMS

received by the International Bureau on 28 November 2019 (28.11.2019)

CLAIMS

1. A semiconductor device, comprising:
 - a gate electrode and a gate dielectric that is a photosensitive material
 - 5 or is disposed adjacent to a photosensitive material;
 - a channel layer at least partly contacting the photosensitive material to form a heterojunction region, the channel layer being formed from a two-dimensional semiconductor material; and
 - at least one pair of electrodes between which at least part of the
 - 10 channel layer extends, at least partly in the heterojunction region, to thereby form a transport channel of the semiconductor device.
2. A semiconductor device according to claim 1, wherein the channel layer is formed from a two-dimensional direct bandgap semiconductor material.
- 15 3. A semiconductor device according to claim 1 or claim 2, wherein the photosensitive material has a bandgap containing one or more mid-gap states that are excitable by optical radiation.
- 20 4. A semiconductor device according to claim 3, wherein the photosensitive material is boron nitride (BN) or a metal oxide film.
5. A semiconductor device according to any one of the preceding claims, wherein the two-dimensional semiconductor material is a transition metal dichalcogenide.
- 25 6. A semiconductor device according to claim 5, wherein the transition metal dichalcogenide is MoTe_2 or WSe_2 .
- 30 7. A semiconductor device according to any one of claims 1 to 4, wherein the two-dimensional semiconductor material is phosphorene.
8. A semiconductor device according to any one of the preceding claims,

wherein the channel layer is a monolayer of the two-dimensional semiconductor material, or comprises multiple layers of the two-dimensional semiconductor material.

- 5 9. A semiconductor device according to any one of the preceding claims, wherein the gate electrode is in contact with a graphene layer.
10. A semiconductor device according to any one of the preceding claims, wherein the channel layer partially contacts the photosensitive material
10 and partially contacts the gate dielectric.
11. A method of fabricating a semiconductor device, comprising:
forming a back gate on a substrate, the back gate comprising a
back gate electrode and a gate dielectric, wherein the gate dielectric is a
15 photosensitive material or is disposed adjacent to a photosensitive
material;
applying a channel layer to at least part of the photosensitive layer
to form a heterojunction region, the channel layer being formed from a
two-dimensional semiconductor material; and
20 forming electrodes on at least the photosensitive material, whereby
at least part of the channel layer extends, at least partly in the
heterojunction region, between two of the electrodes to thereby form a
transport channel of the semiconductor device.
- 25 12. A method according to claim 11, wherein the channel layer is formed from
a two-dimensional direct bandgap semiconductor material.
13. A method according to claim 11 or claim 12, wherein the photosensitive
material has a bandgap containing one or more mid-gap states that are
30 excitable by optical radiation.
14. A method according to claim 13, wherein the photosensitive material is
boron nitride (BN) or a metal oxide film.

15. A method according to any one of claims 11 to 14, wherein the two-dimensional semiconductor material is a transition metal dichalcogenide.
- 5 16. A method according to claim 15, wherein the transition metal dichalcogenide is MoTe_2 or WSe_2 .
17. A method according to any one of claims 11 to 16, wherein the two-dimensional semiconductor material is phosphorene.
- 10 18. A method according to any one of claims 11 to 17, wherein the channel layer is a monolayer of the two-dimensional semiconductor material, or comprises multiple layers of the two-dimensional semiconductor material.
- 15 19. A method according to any one of claims 11 to 18, wherein the back gate comprises a graphene layer.
- 20 20. A method according to any one of claims 11 to 19, wherein the channel layer partially contacts the photosensitive material and partially contacts the gate dielectric.

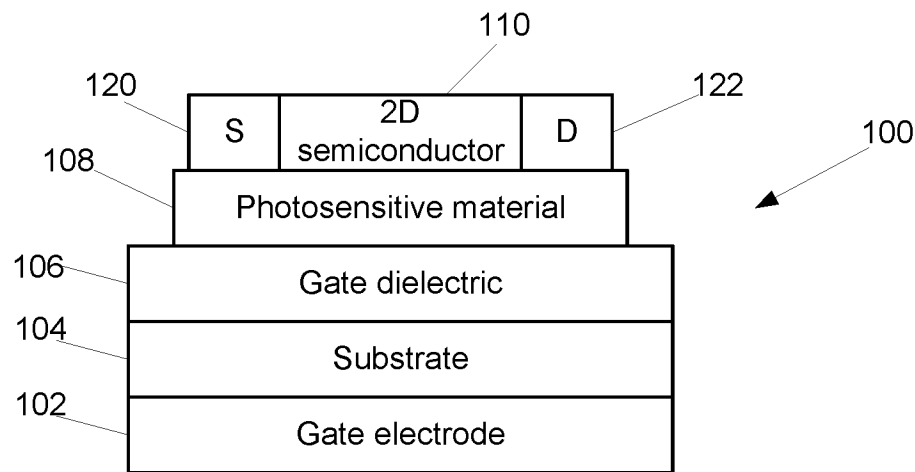


FIGURE 1

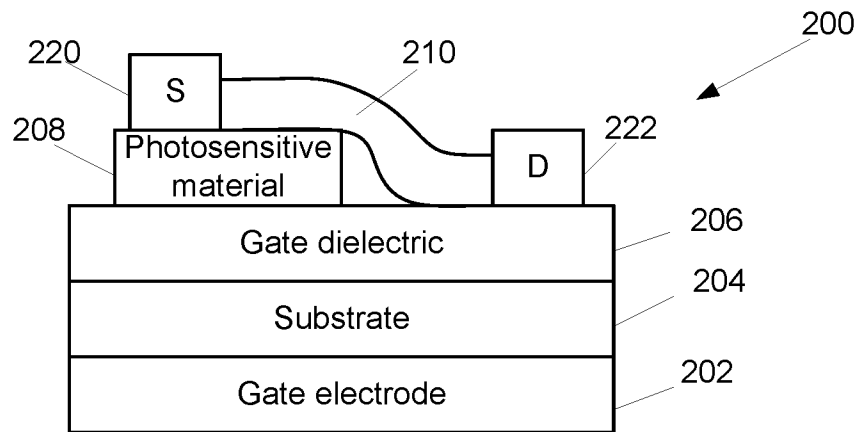


FIGURE 2

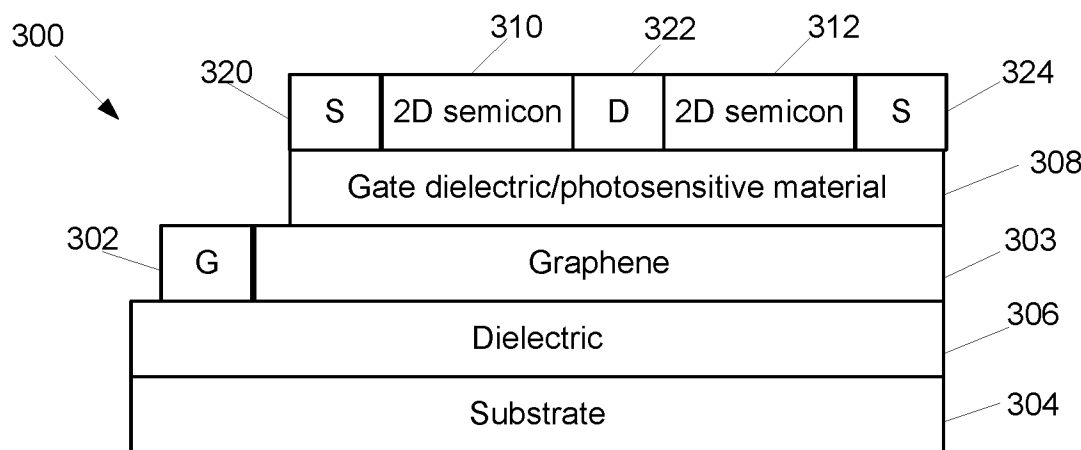


FIGURE 3

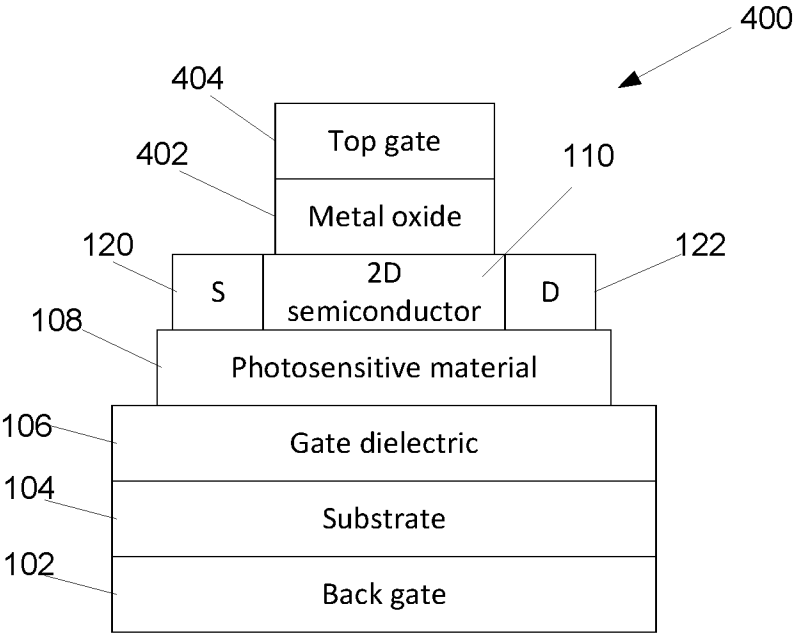


FIGURE 4

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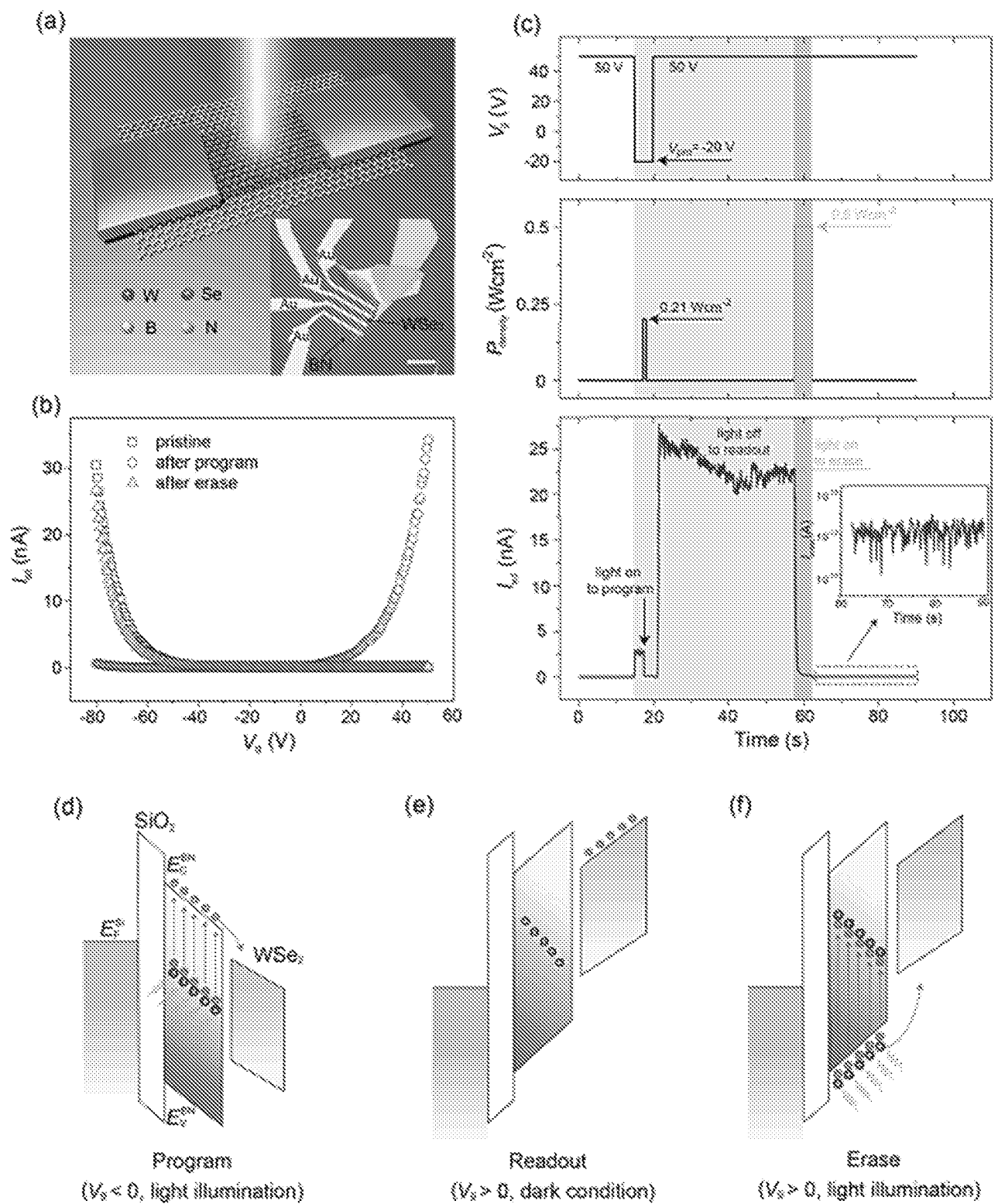


FIGURE 5

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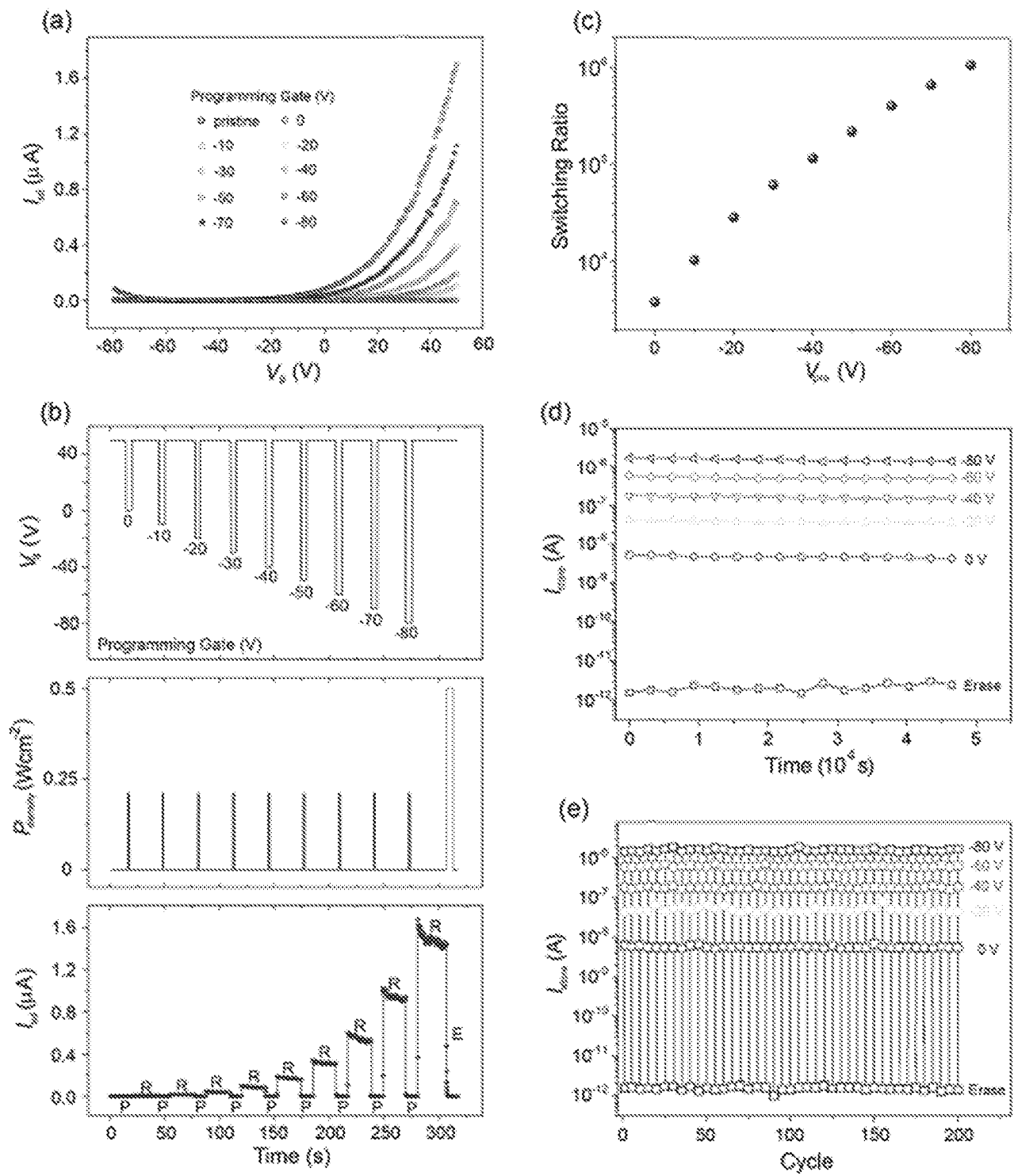


FIGURE 6

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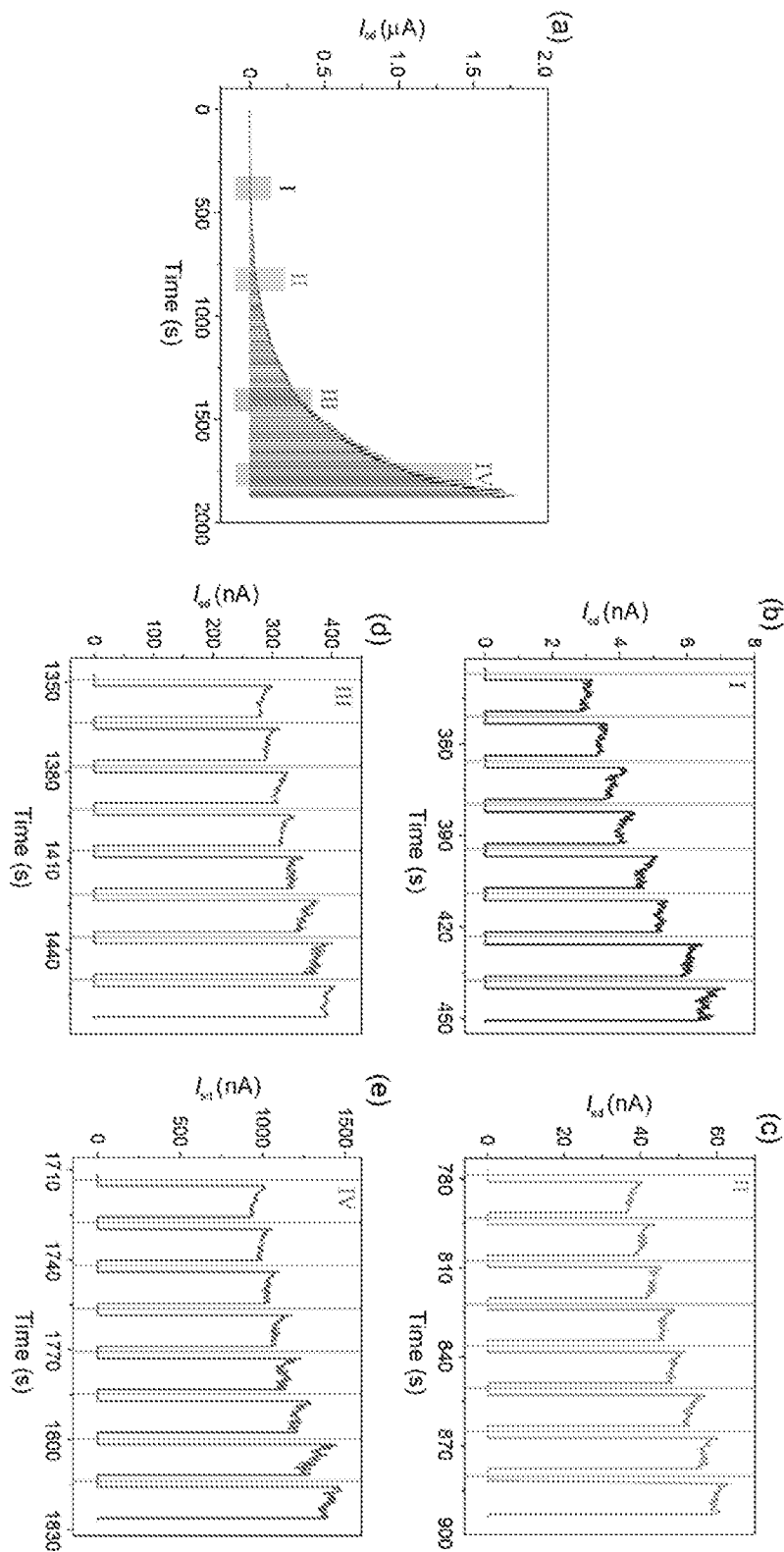


FIGURE 7

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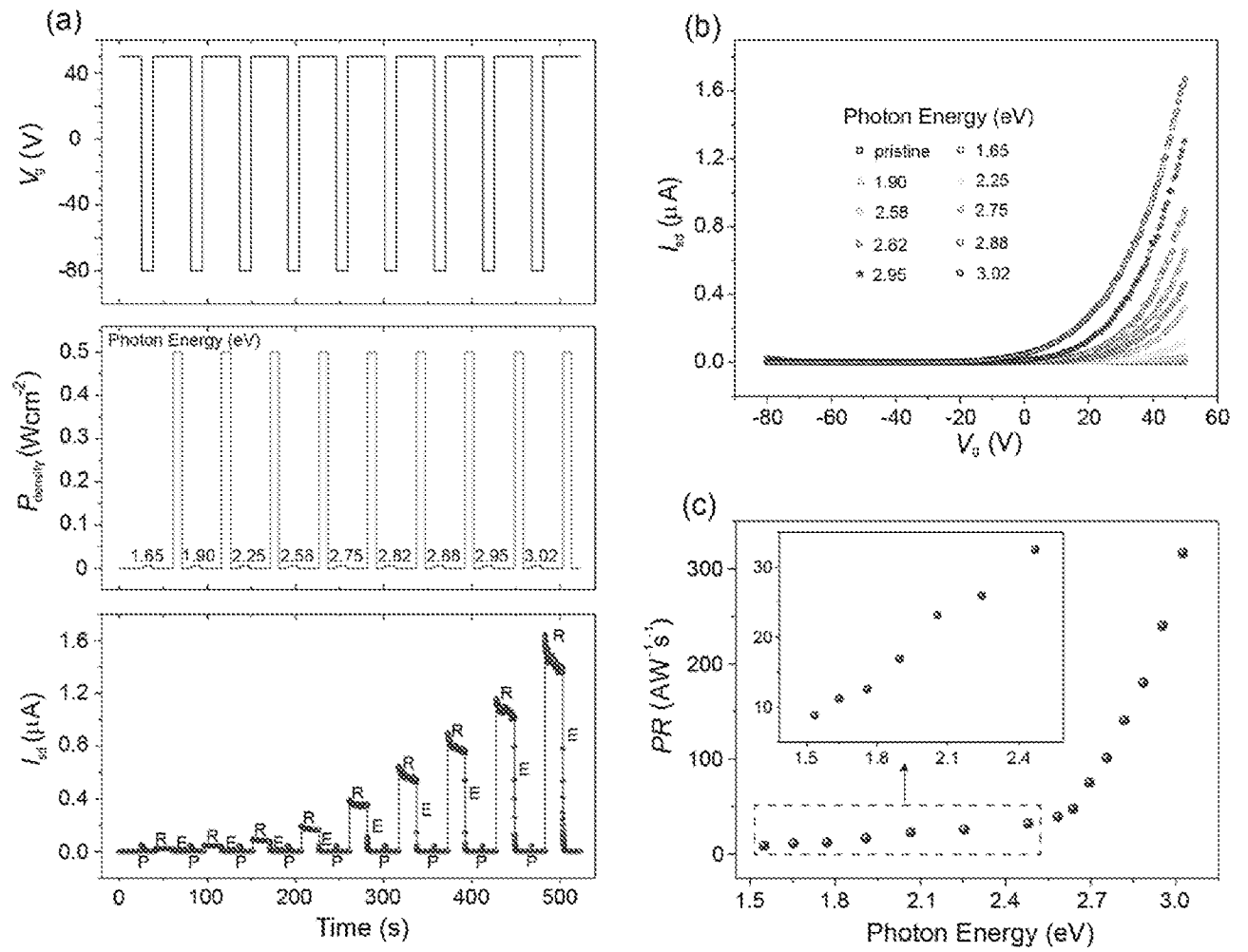


FIGURE 8

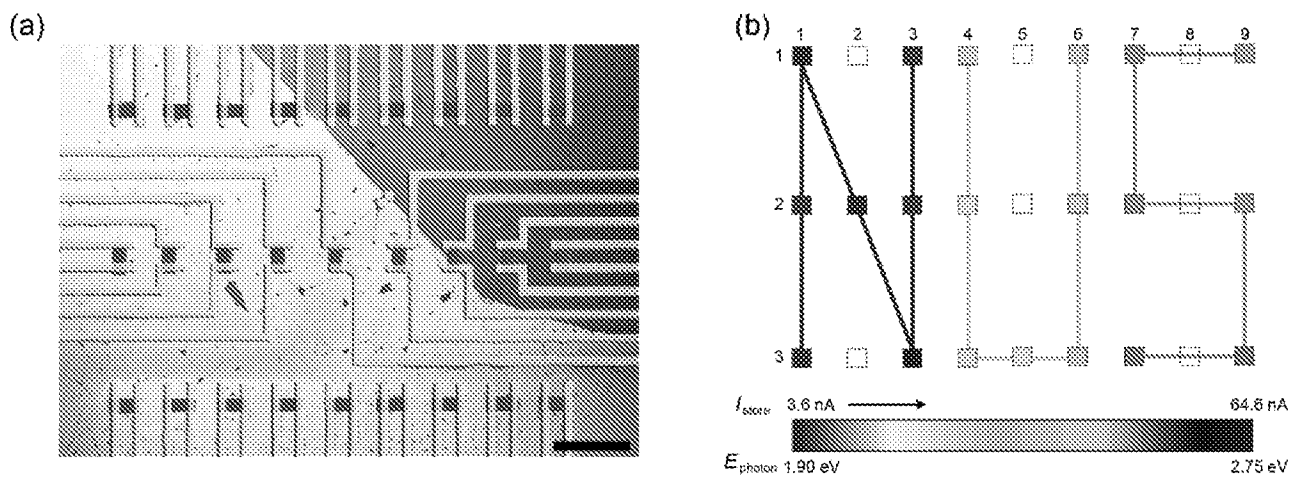


FIGURE 9

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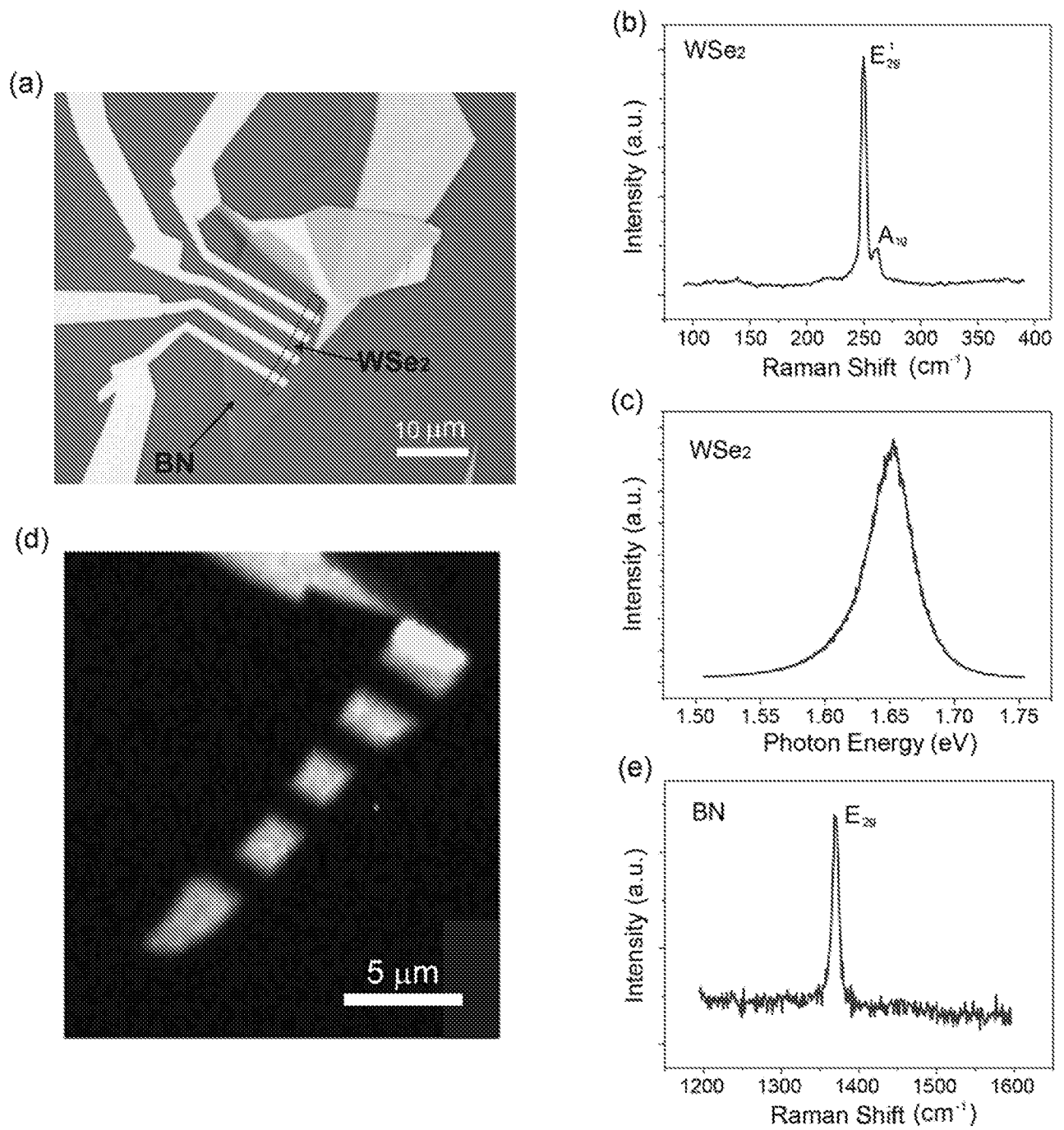


FIGURE 10

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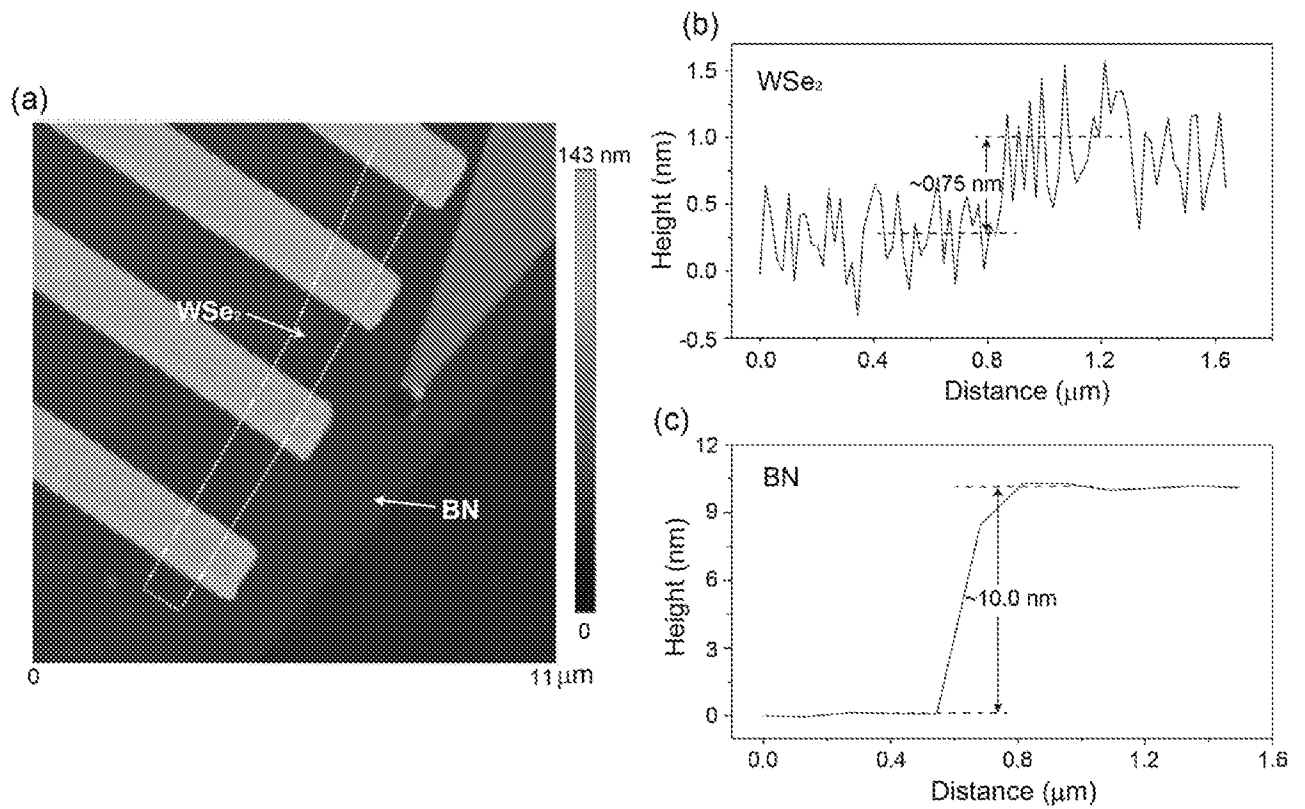


FIGURE 11

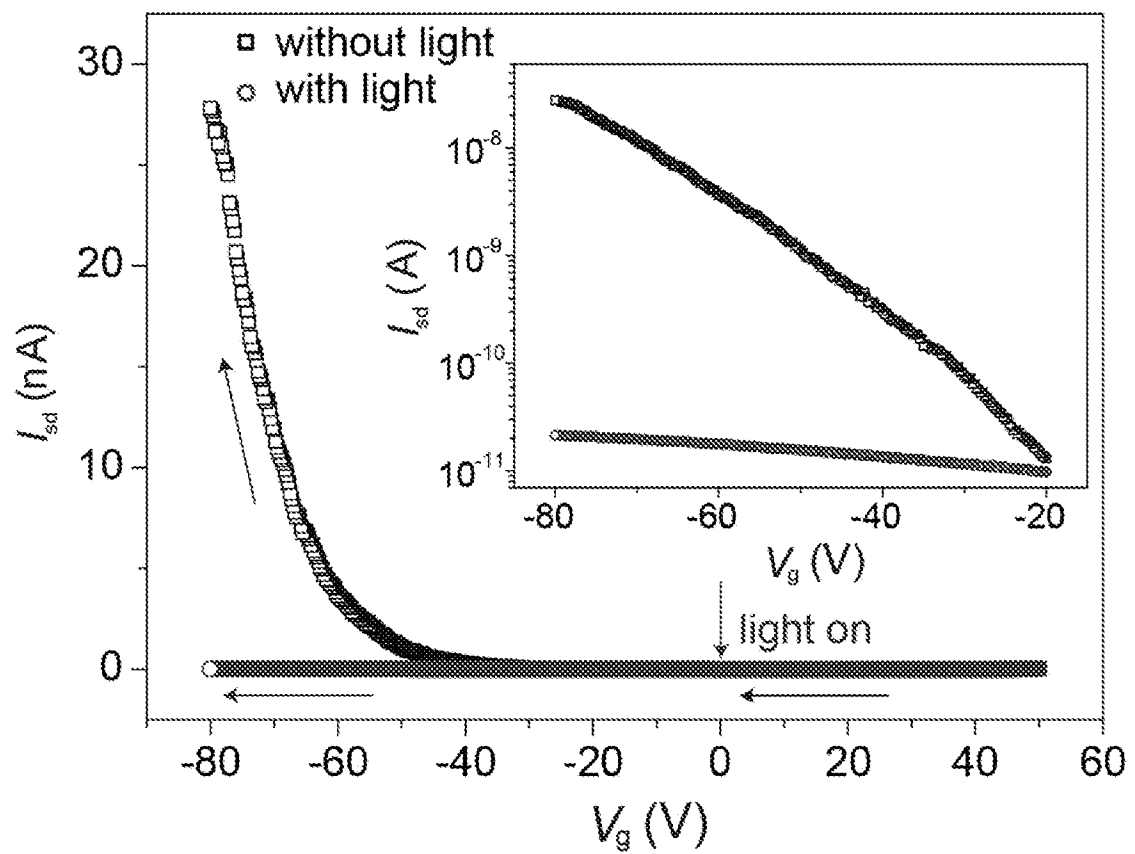


FIGURE 12

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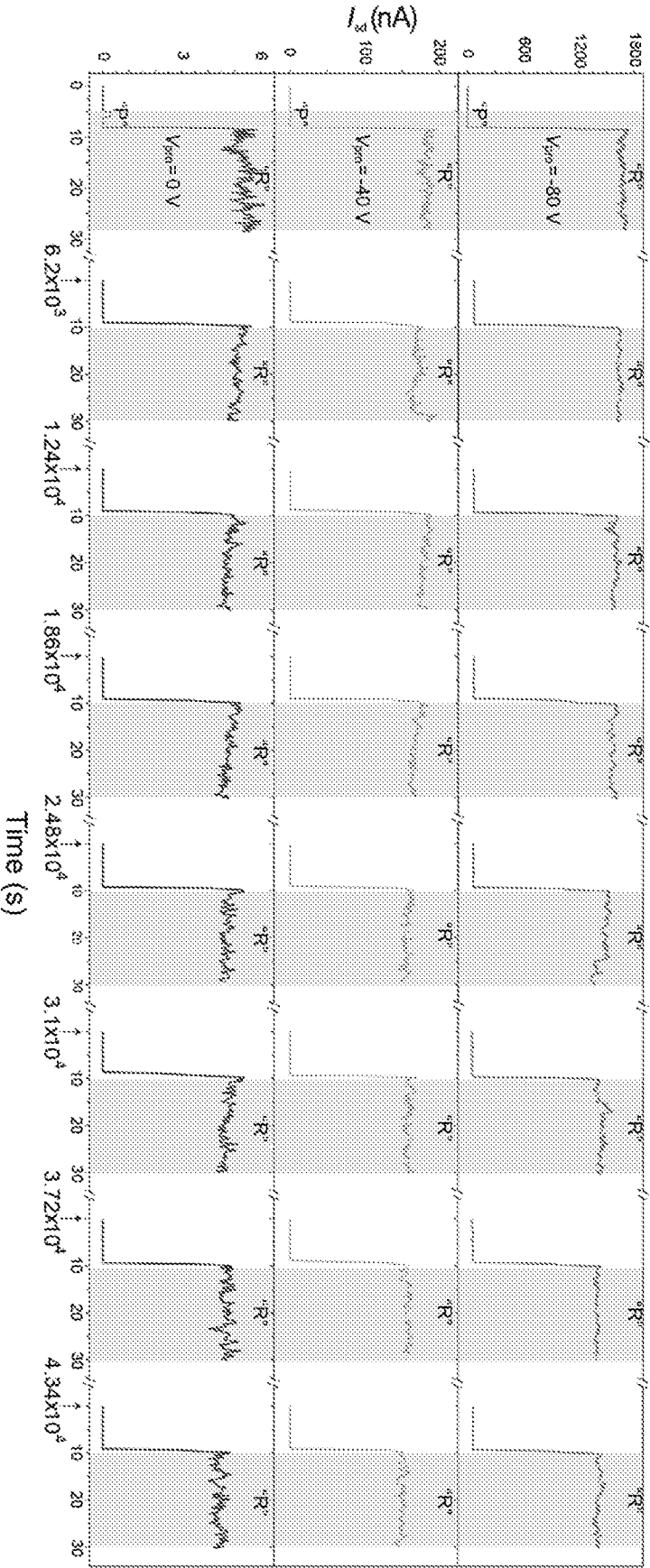


FIGURE 13

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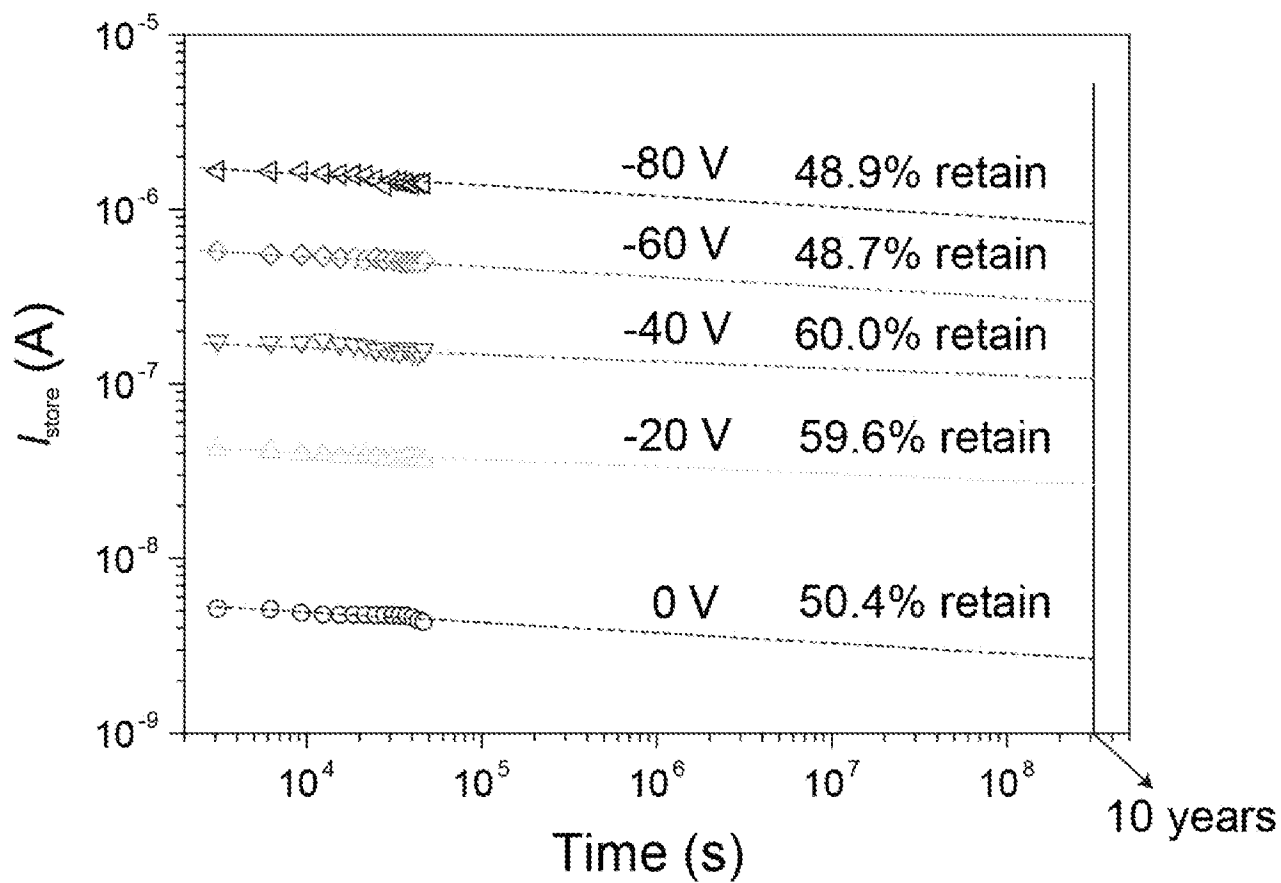


FIGURE 14

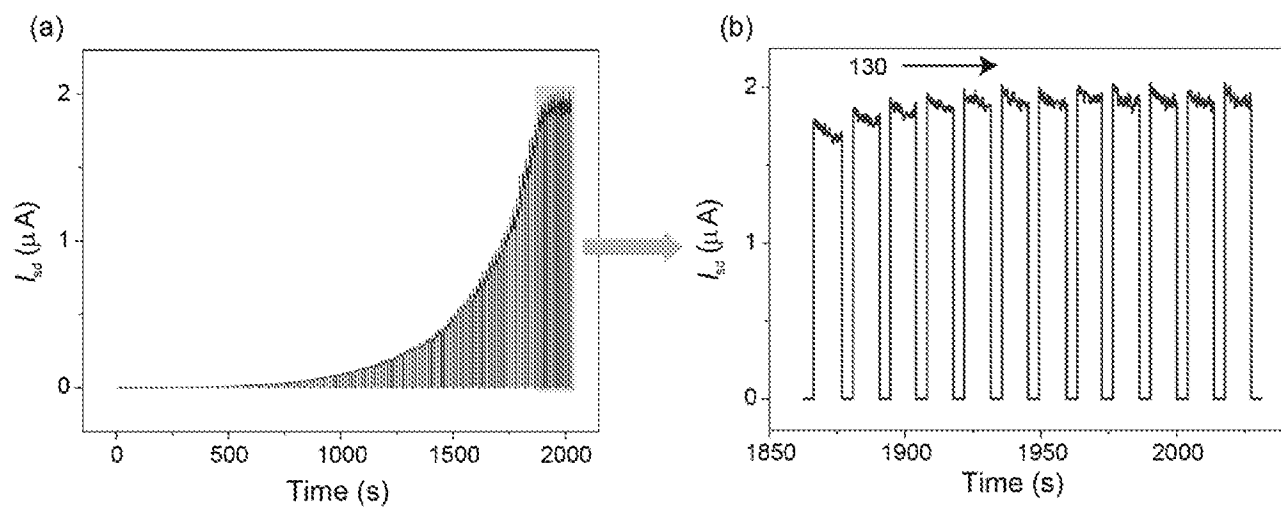


FIGURE 15

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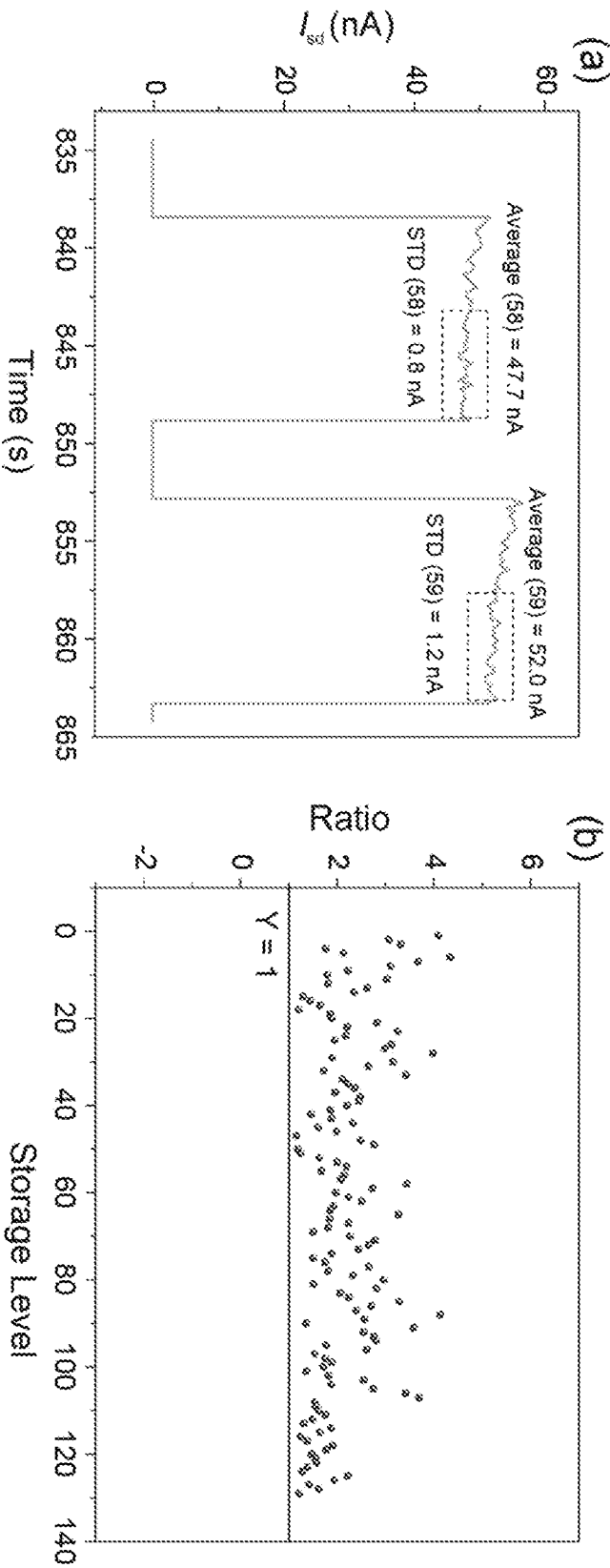


FIGURE 16

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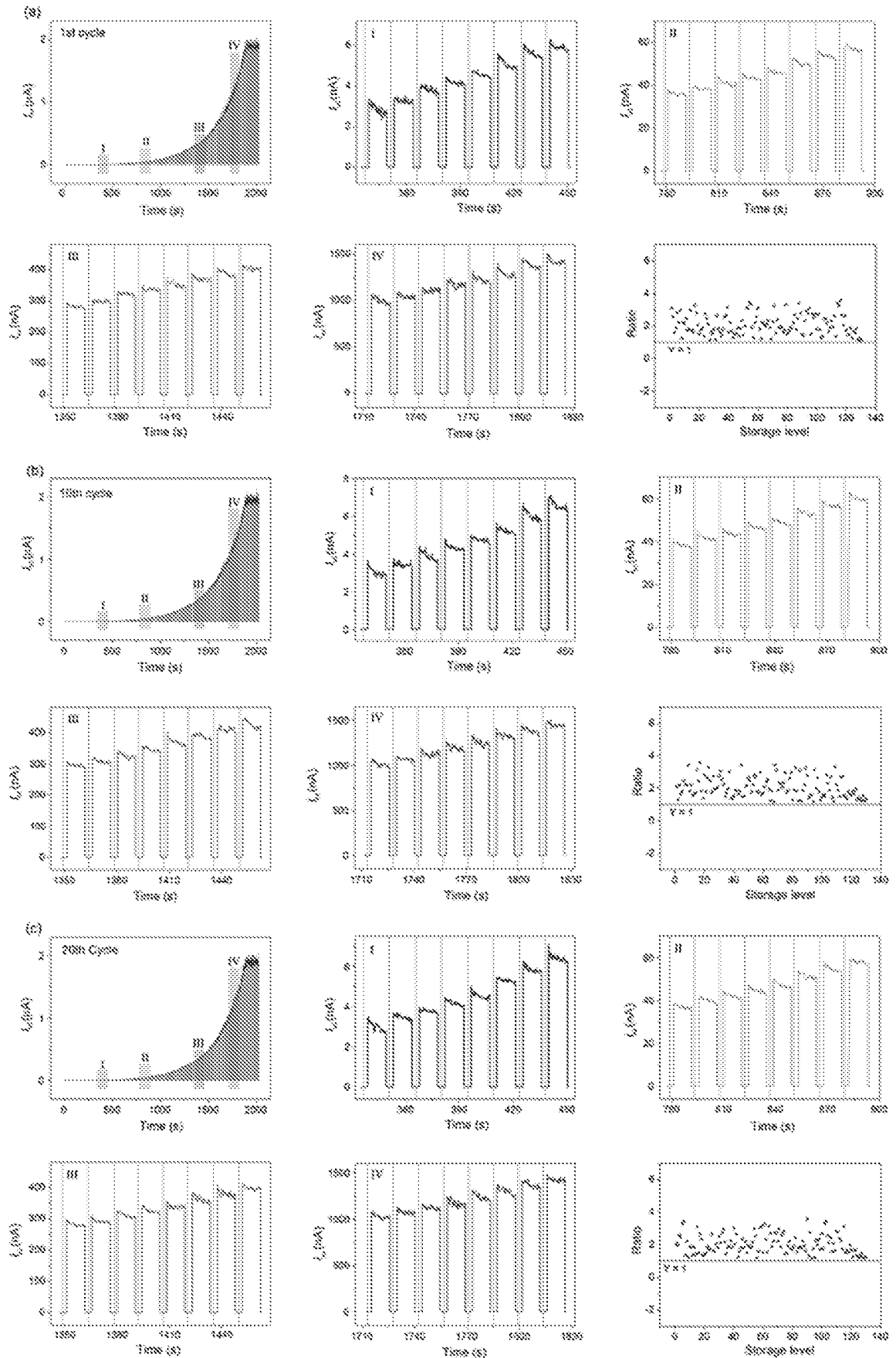


FIGURE 17

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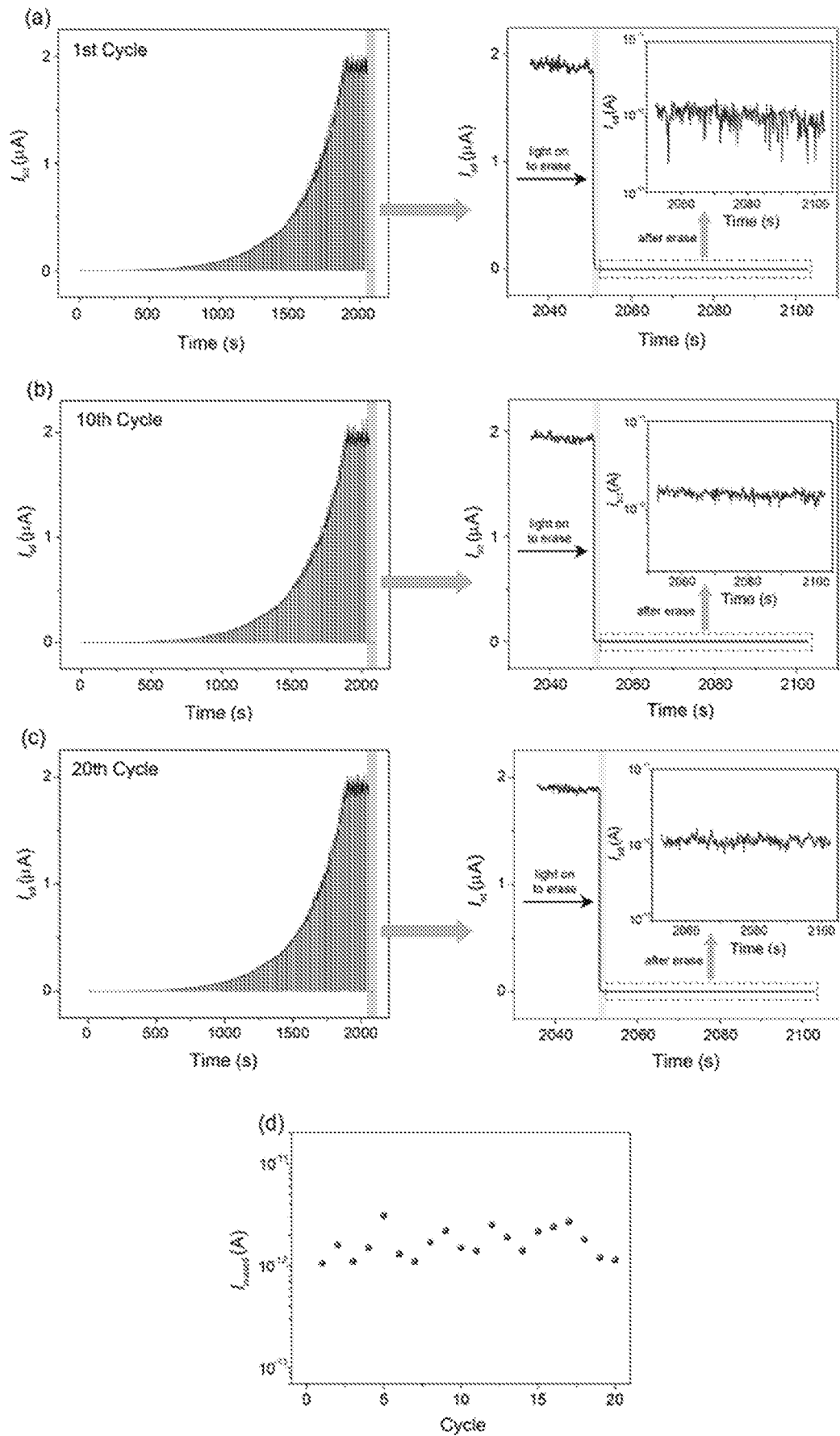


FIGURE 18

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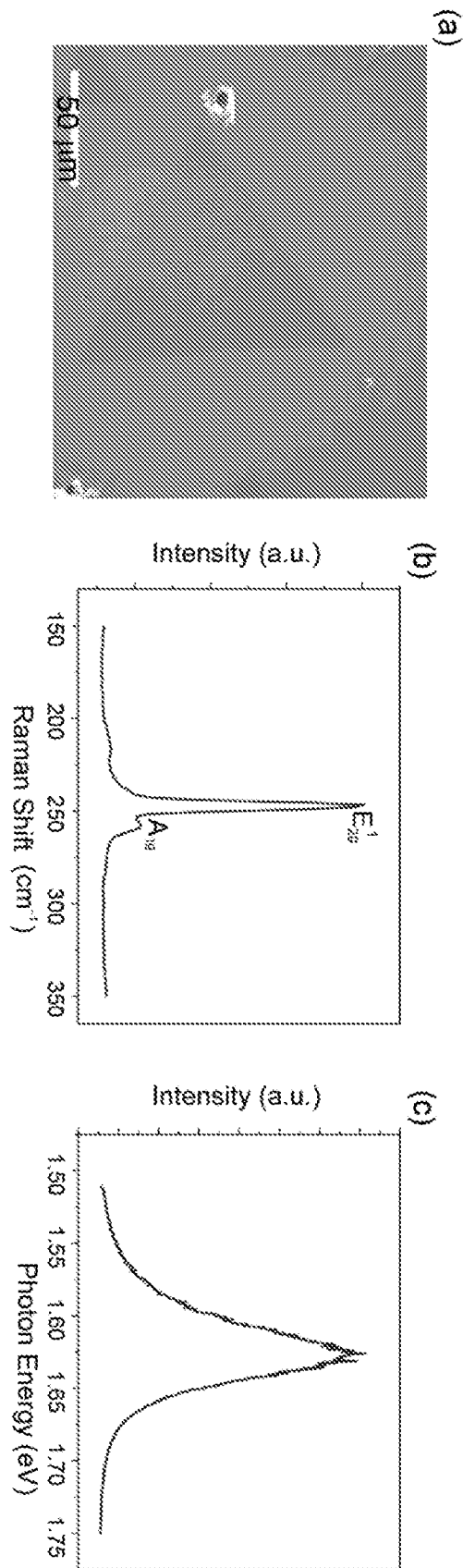


FIGURE 19

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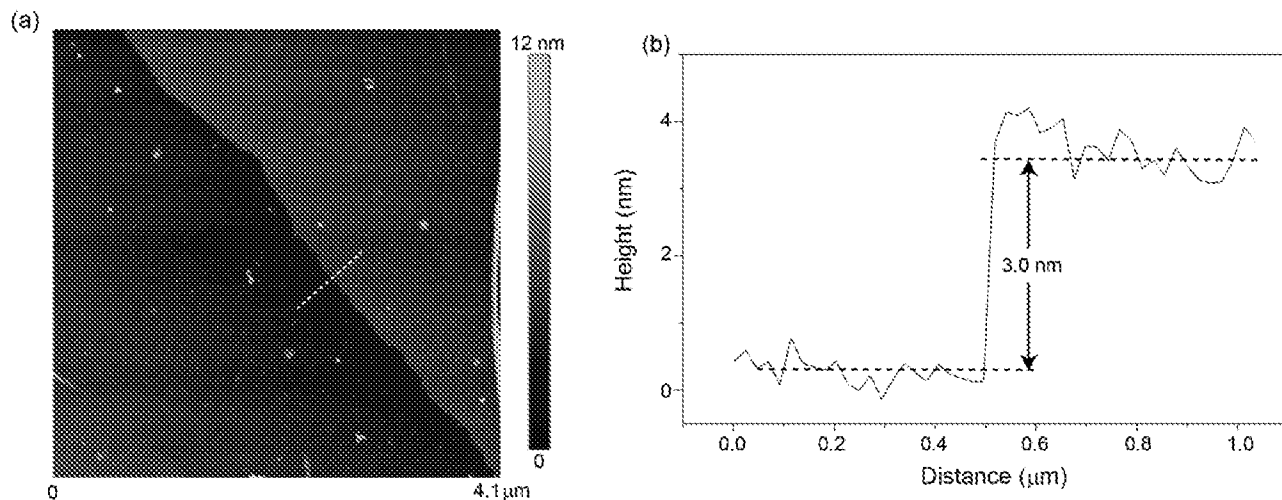


FIGURE 20

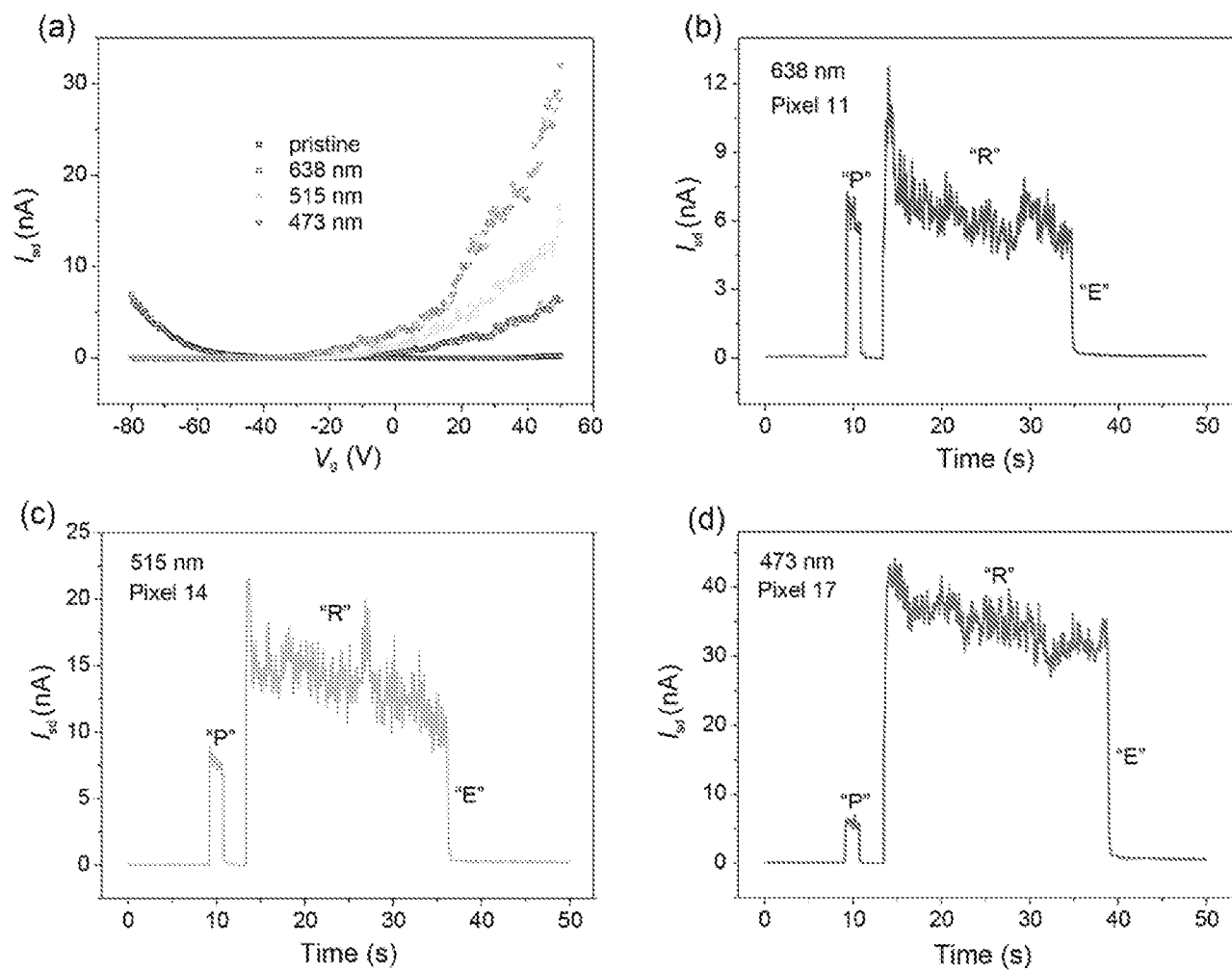


FIGURE 21

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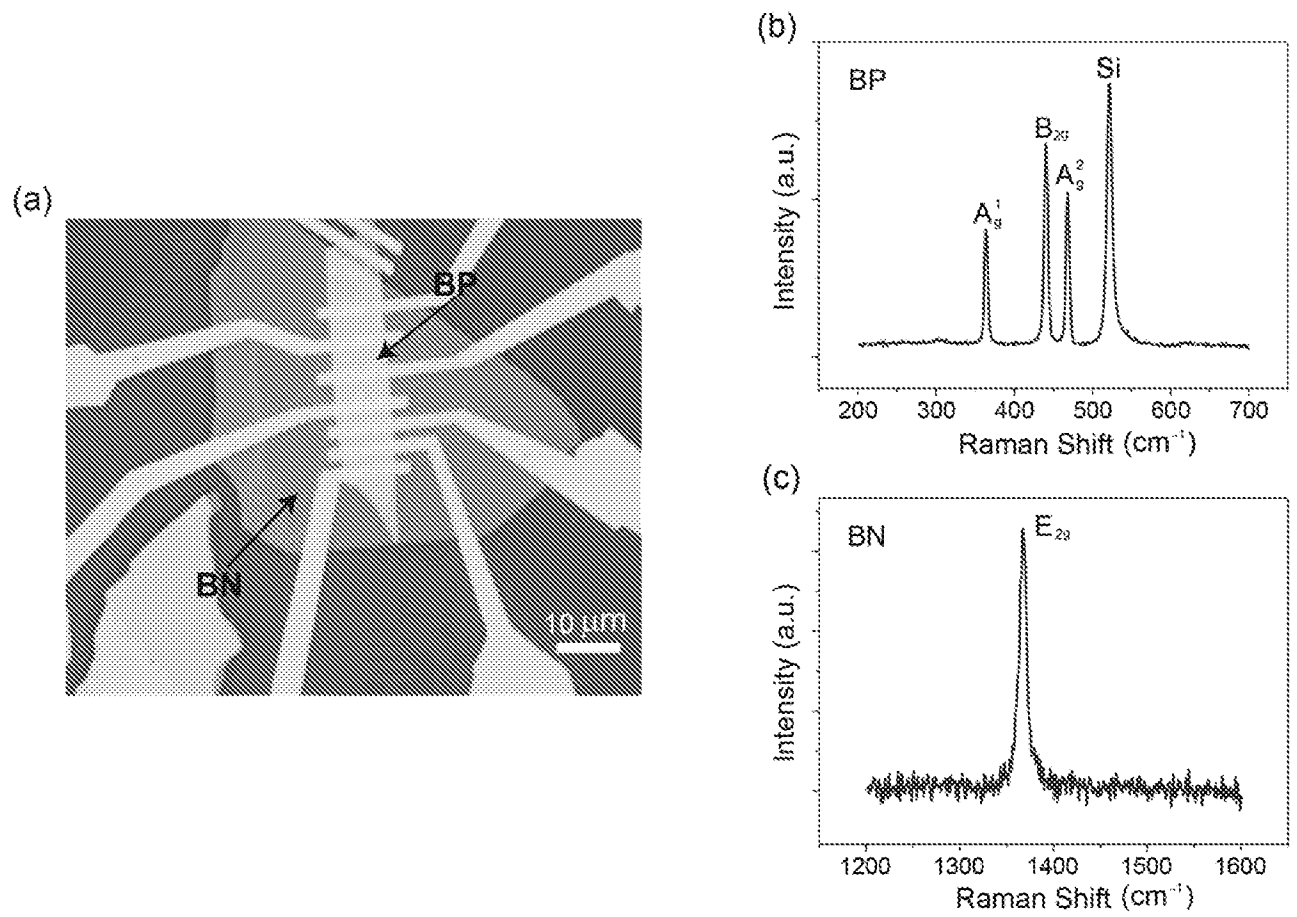


FIGURE 22

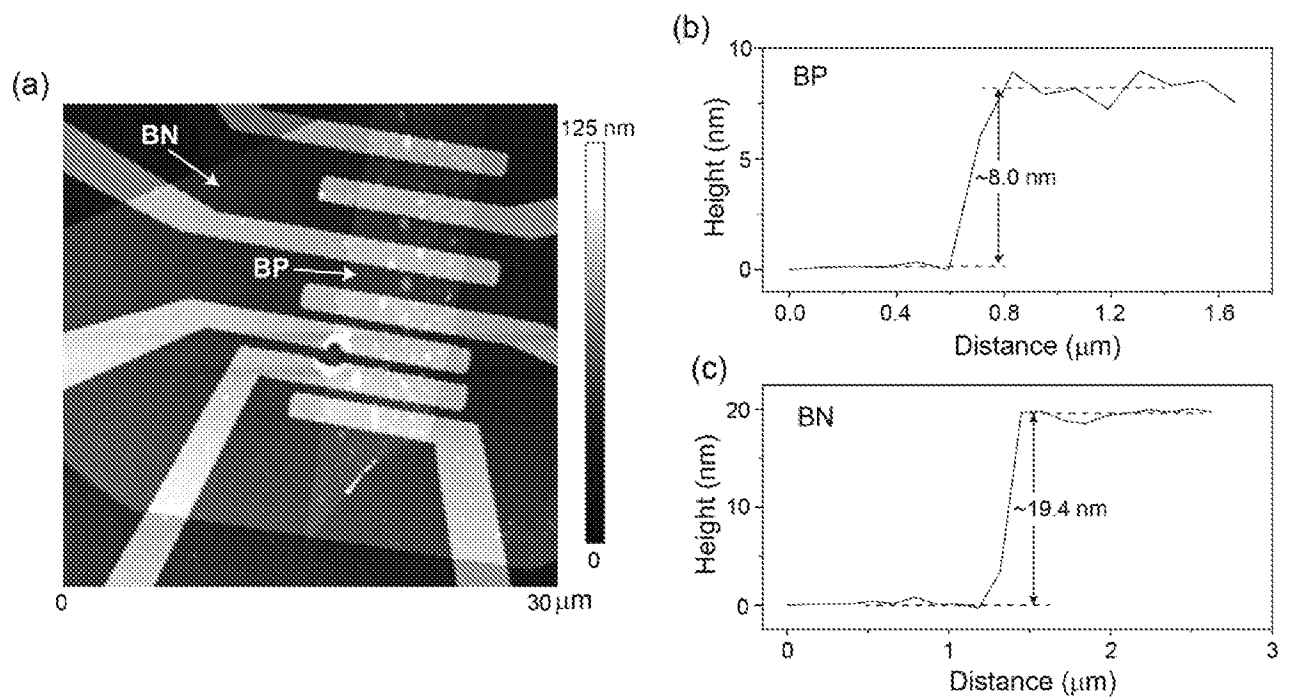


FIGURE 23

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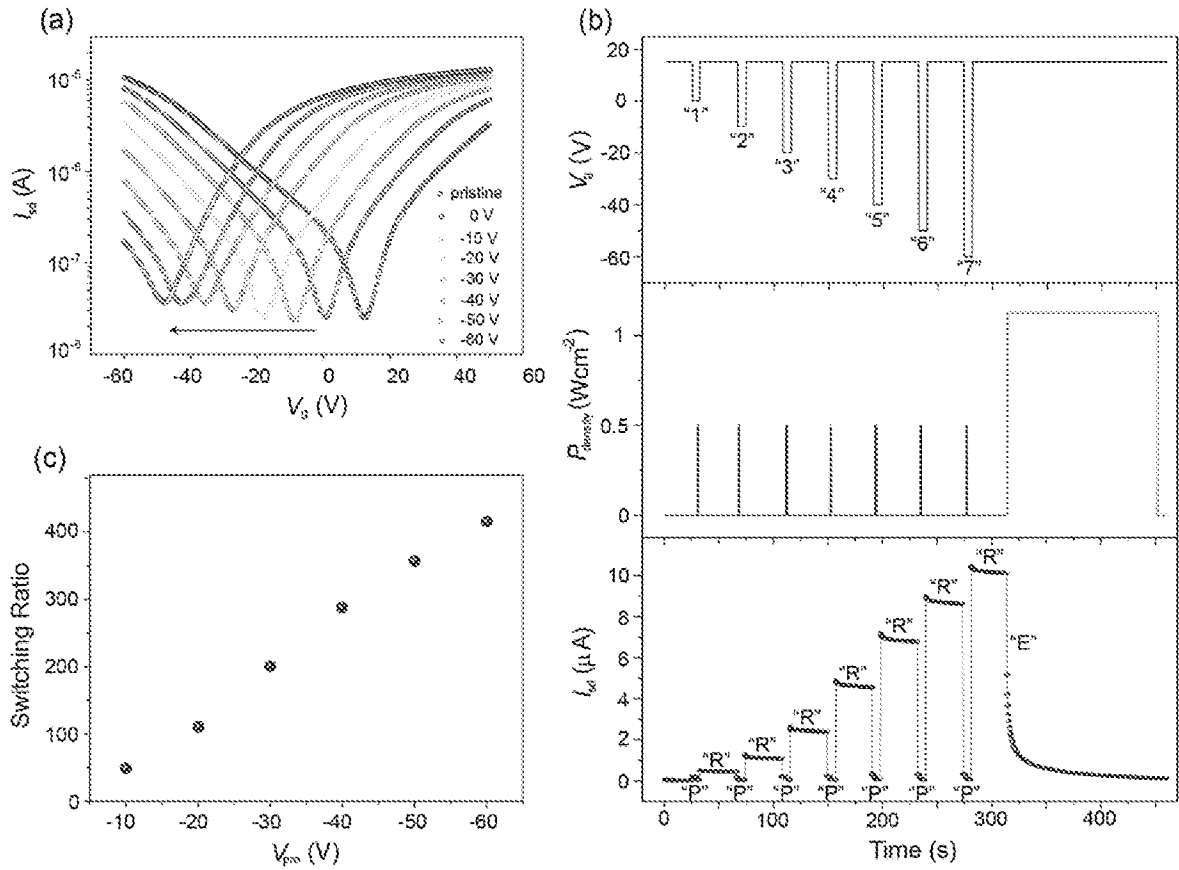


FIGURE 24

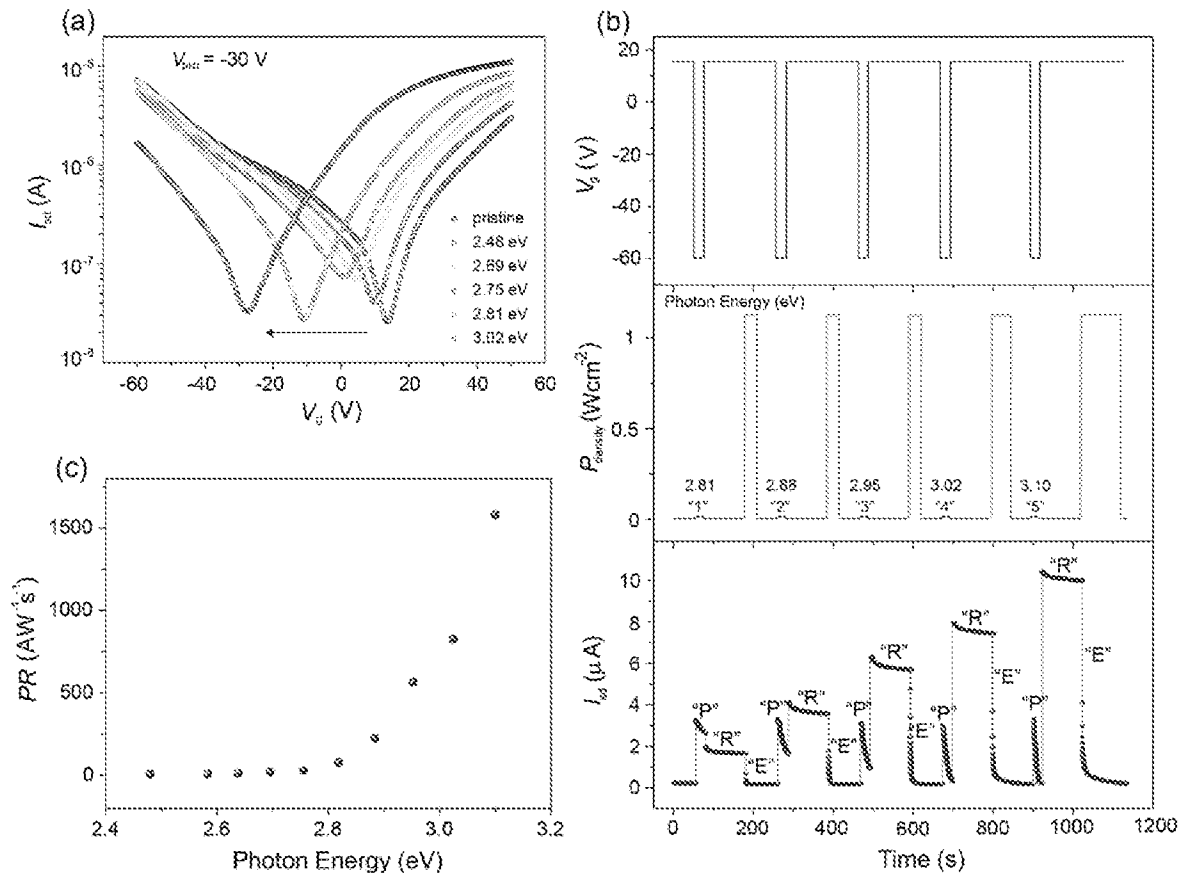


FIGURE 25

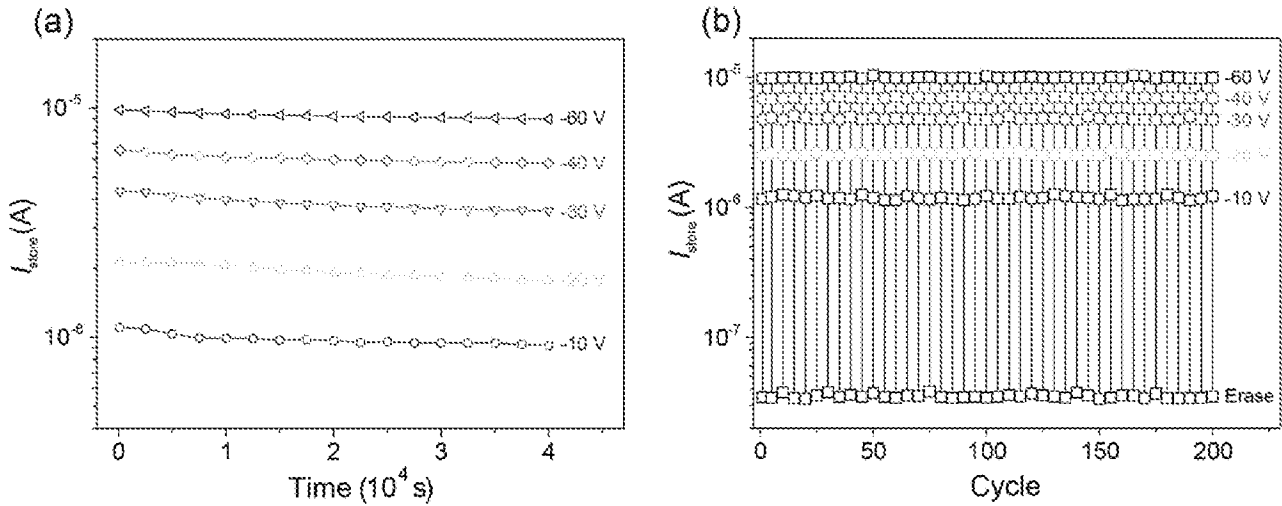


FIGURE 26

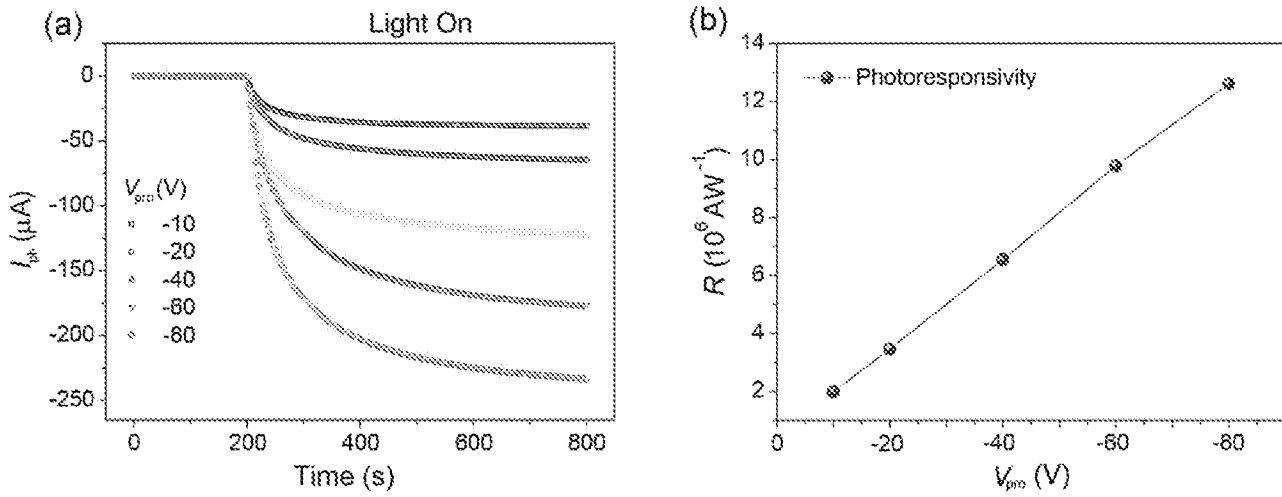


FIGURE 27

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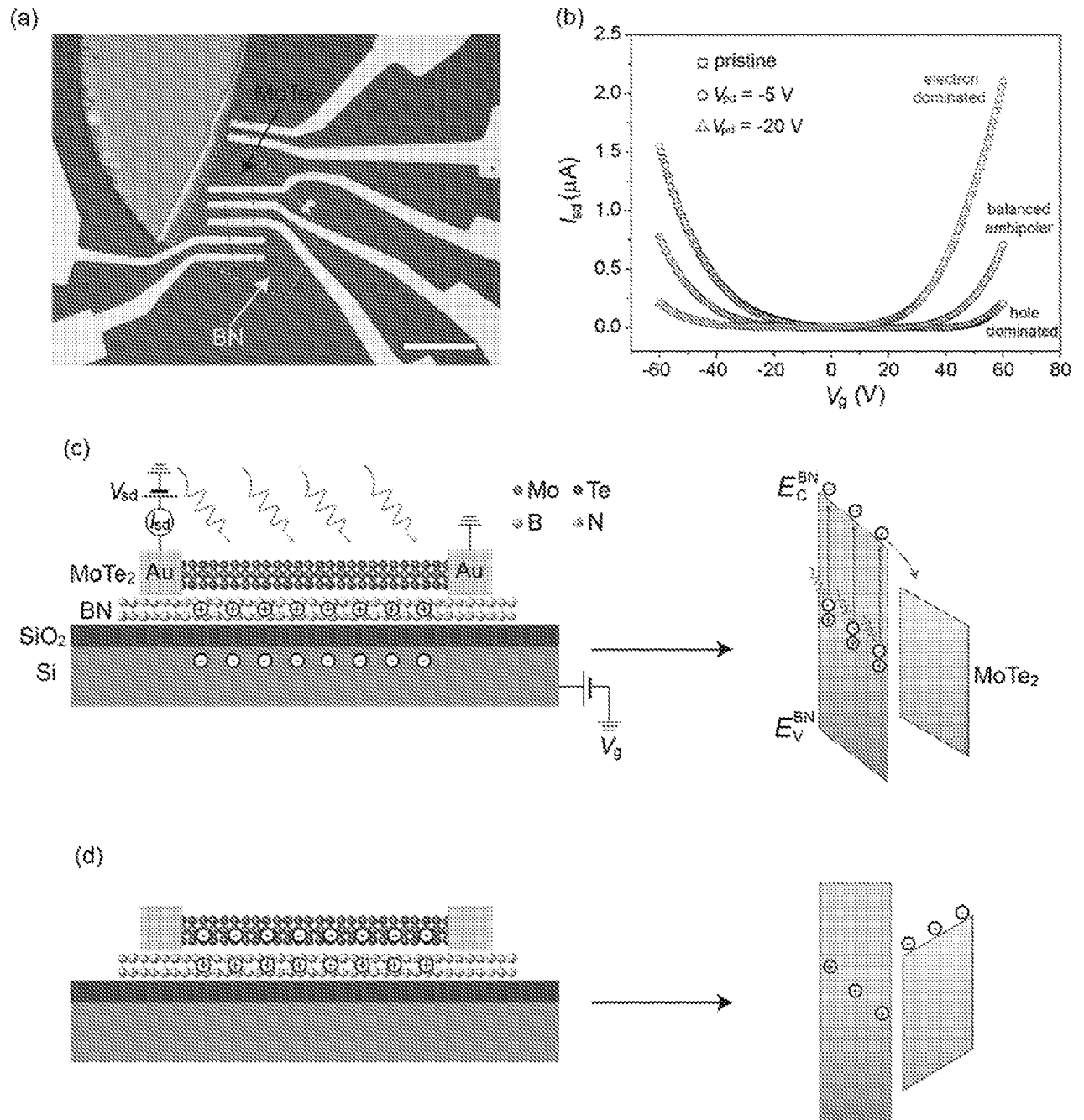


FIGURE 28

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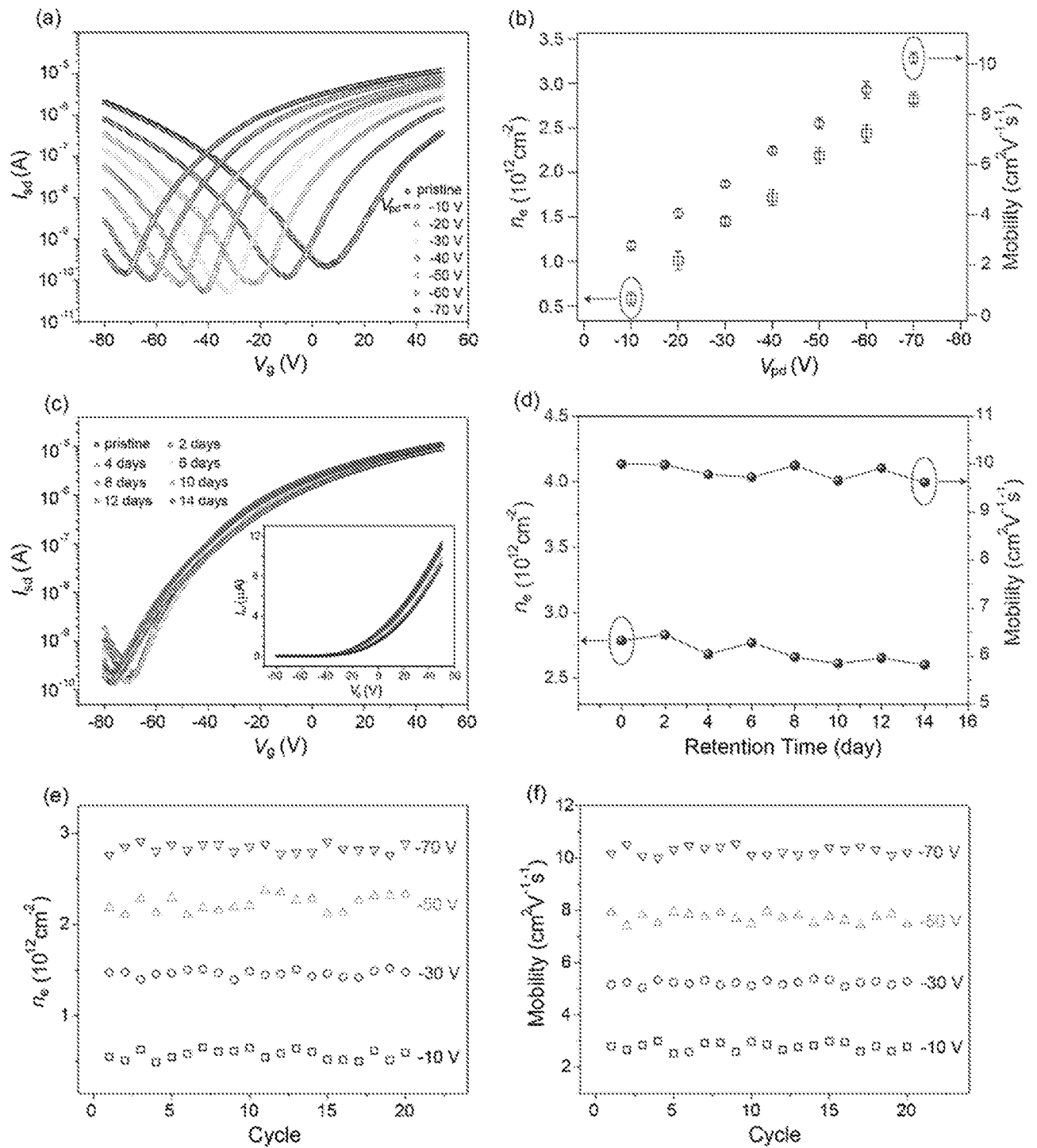


FIGURE 29

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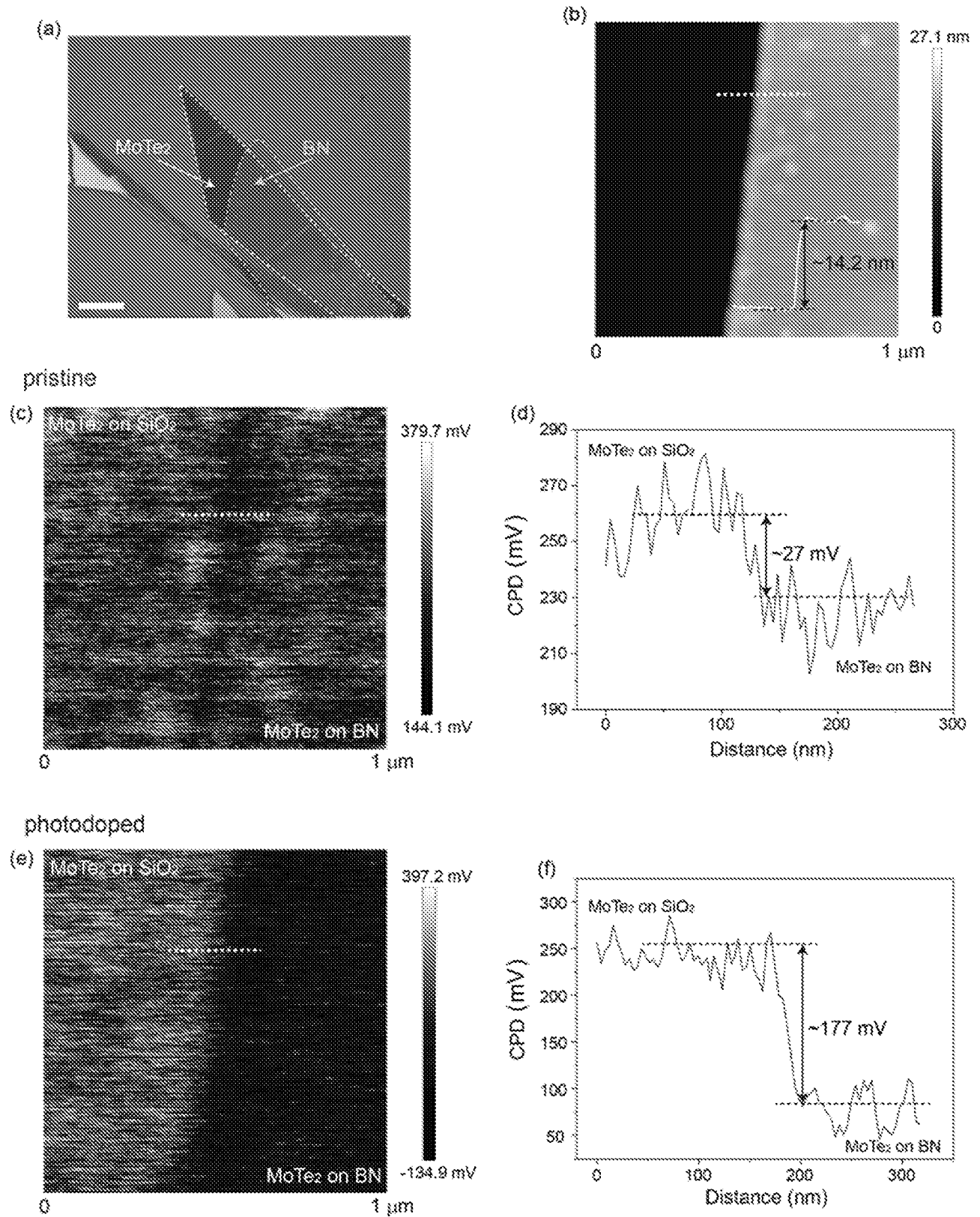


FIGURE 30

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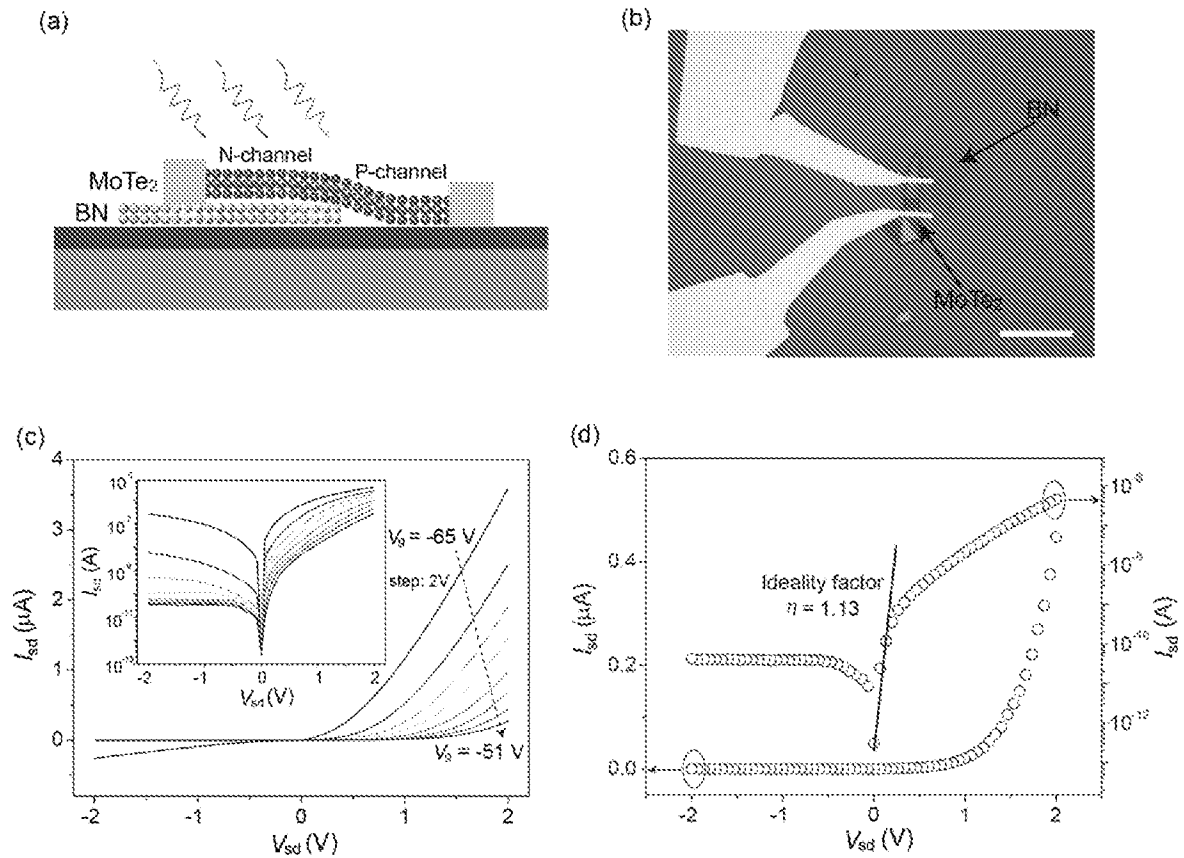


FIGURE 31

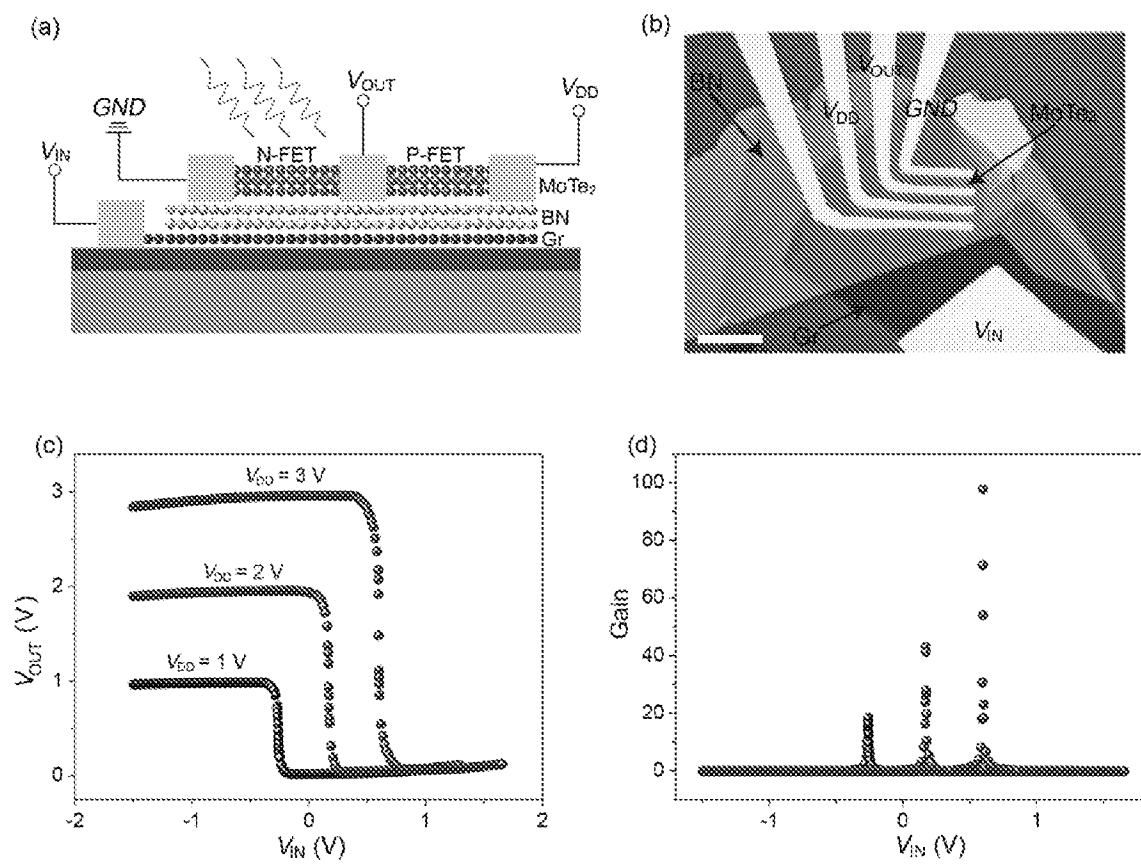


FIGURE 32

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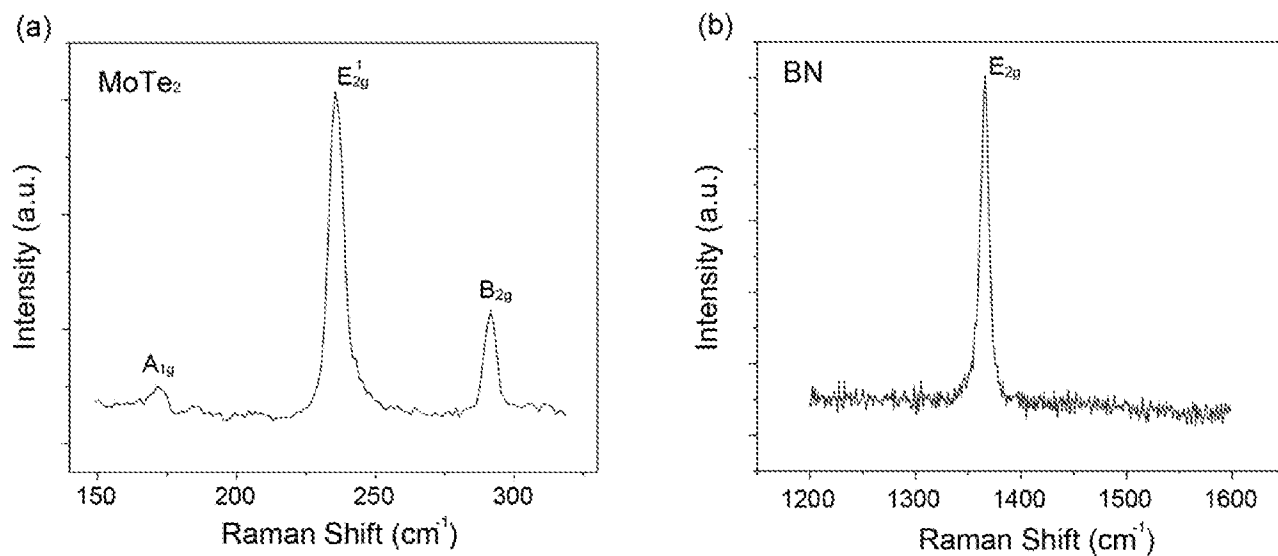


FIGURE 33

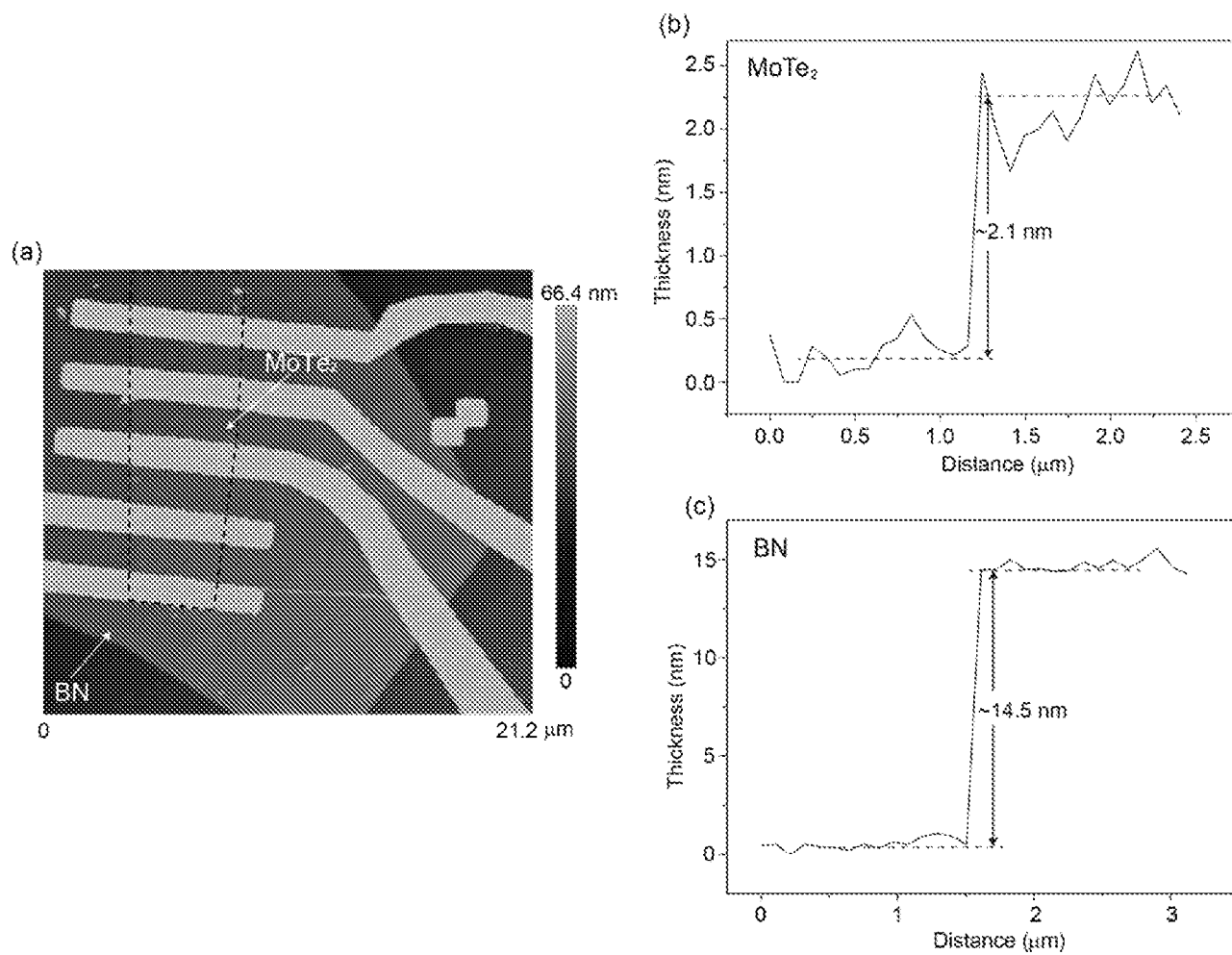


FIGURE 34

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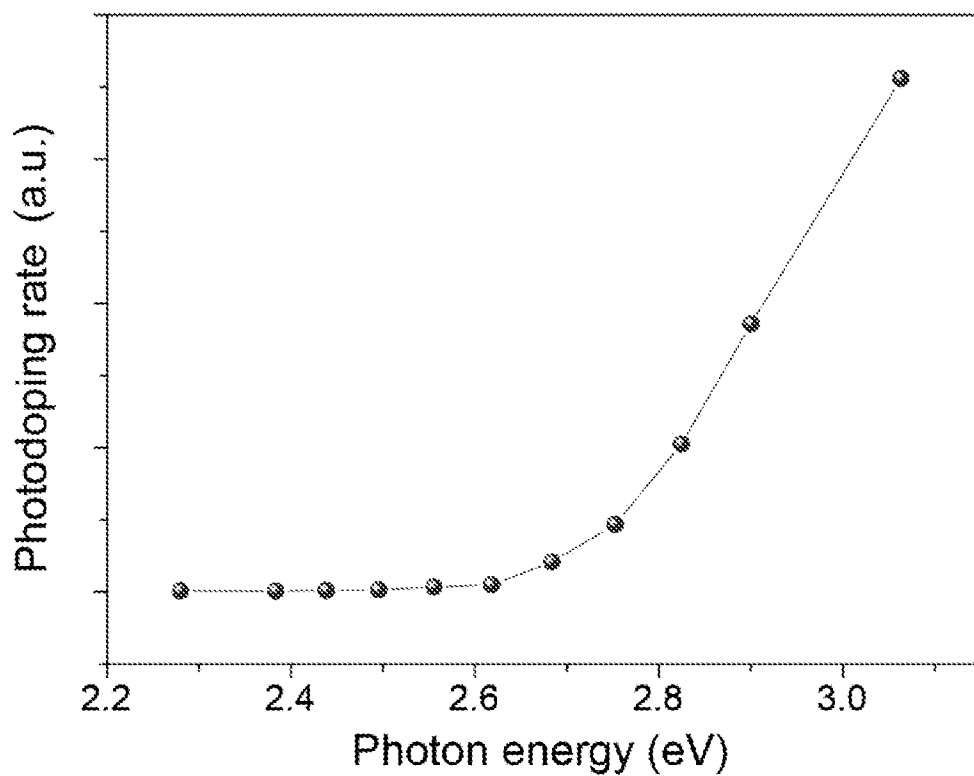


FIGURE 35

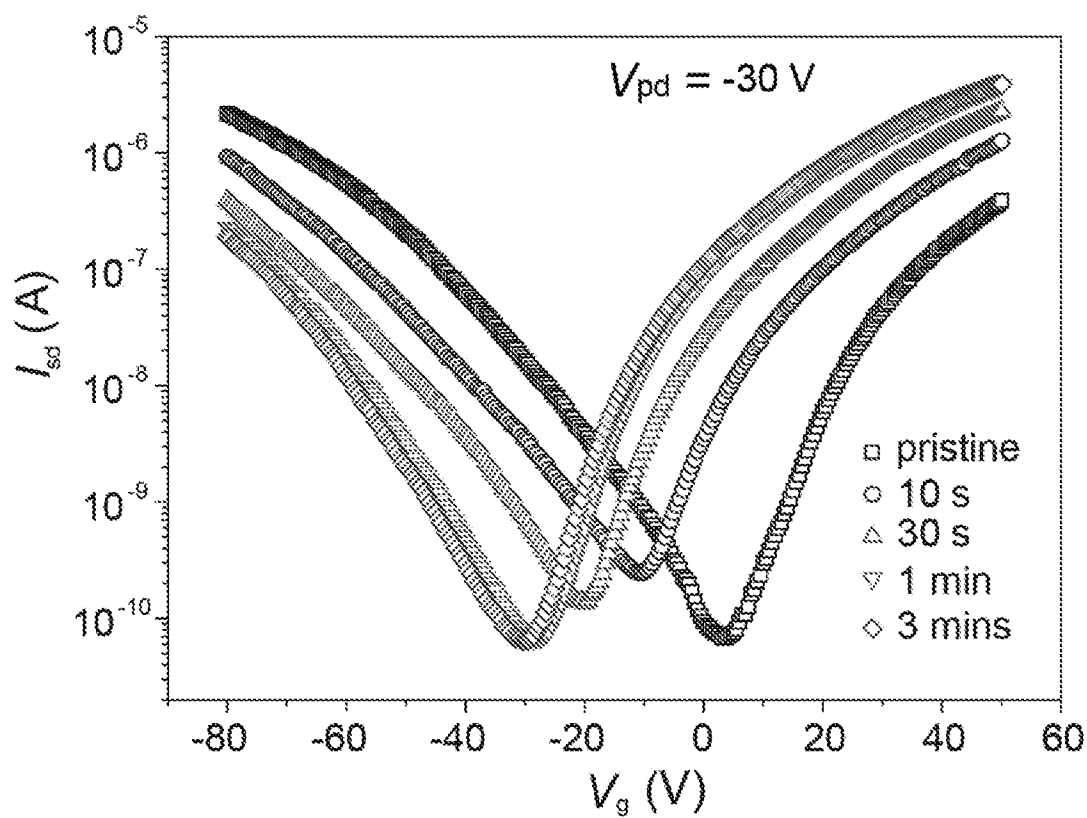


FIGURE 36

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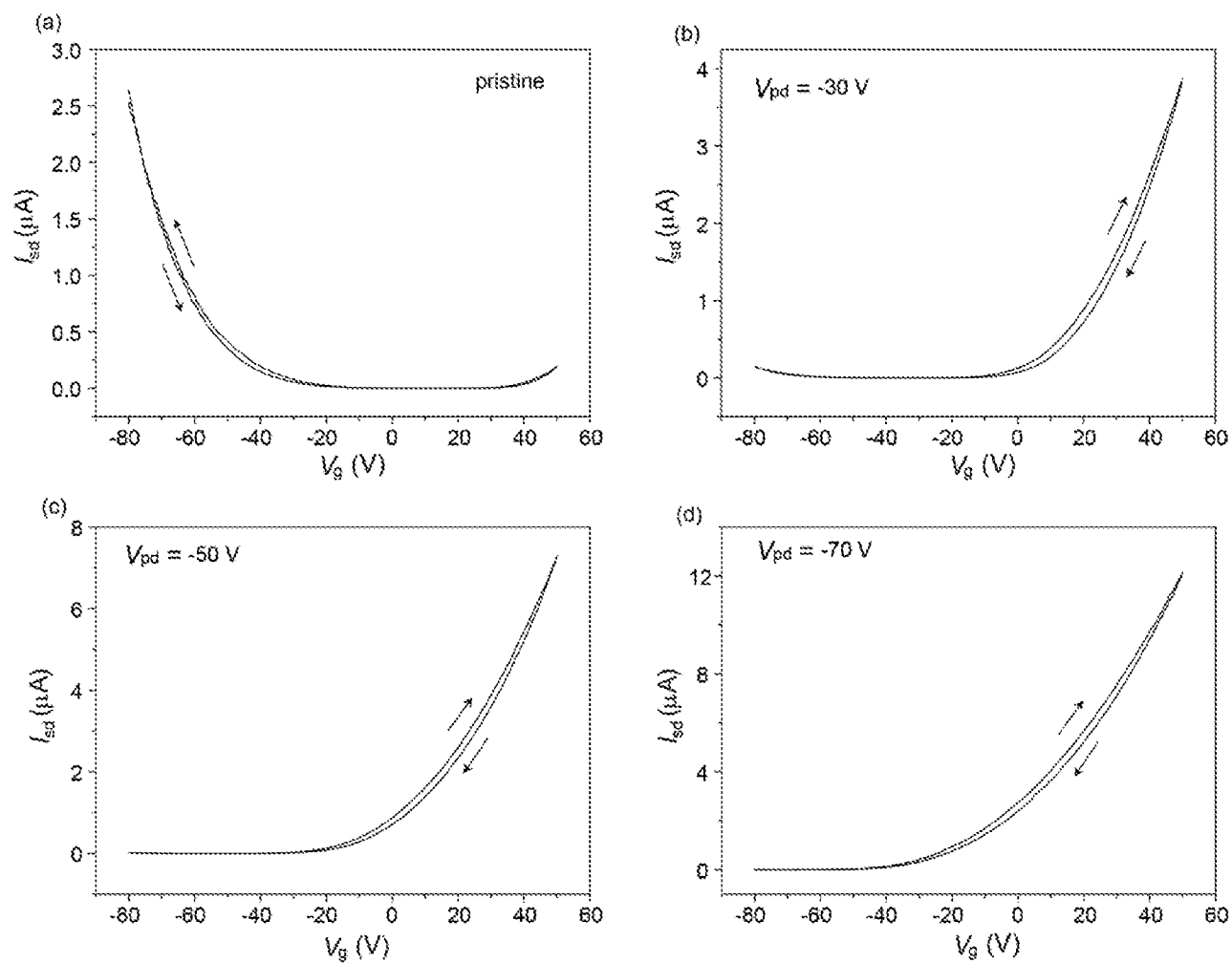


FIGURE 37

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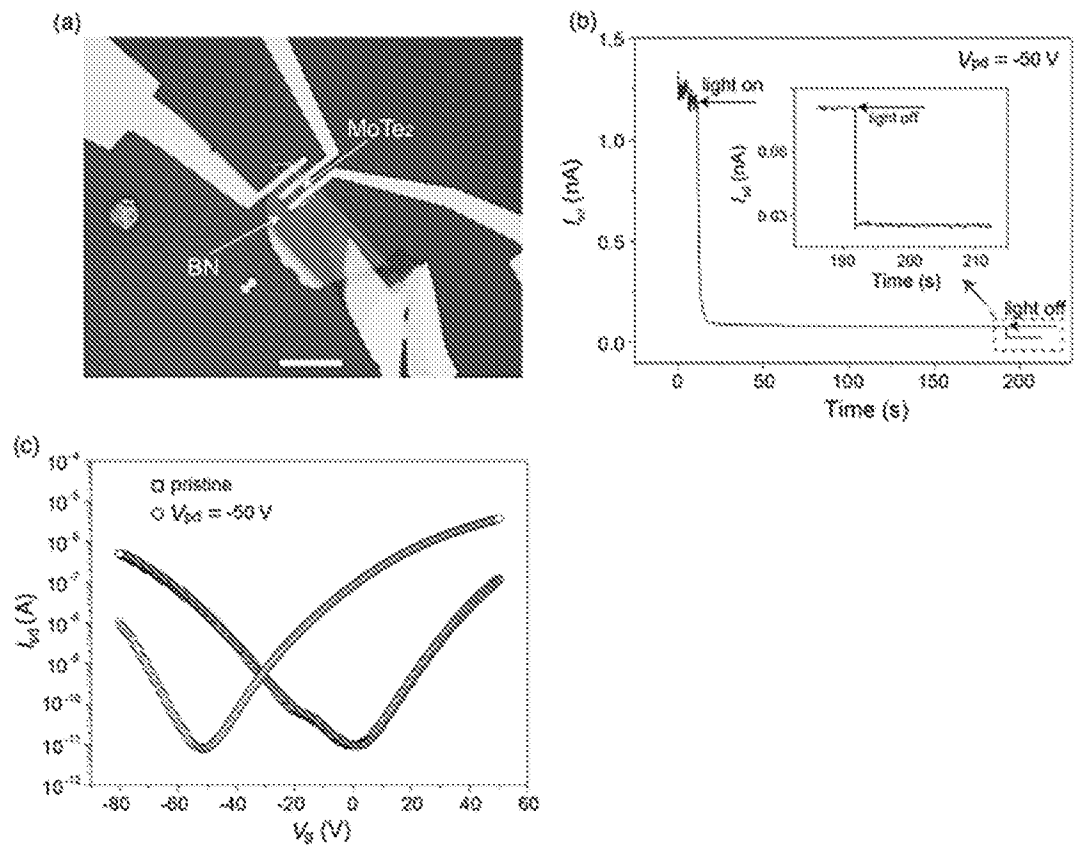
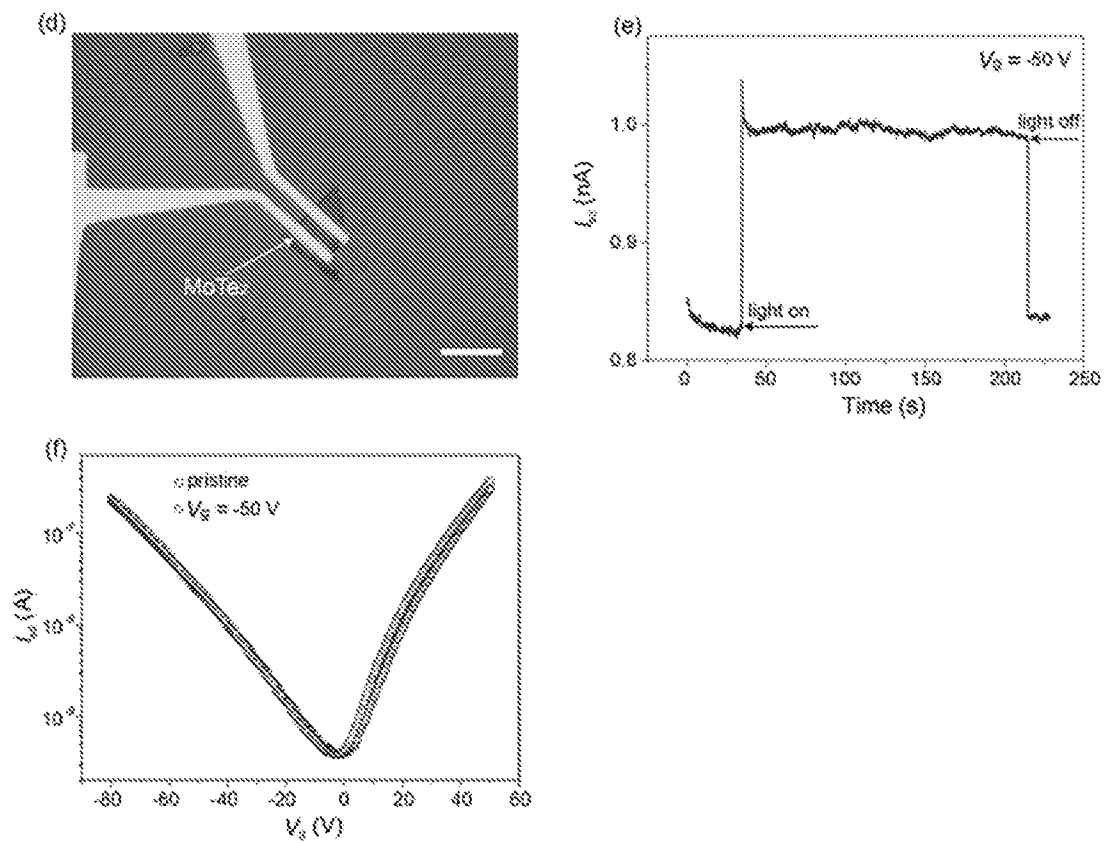
MoTe₂ on BNMoTe₂ on SiO₂

FIGURE 38

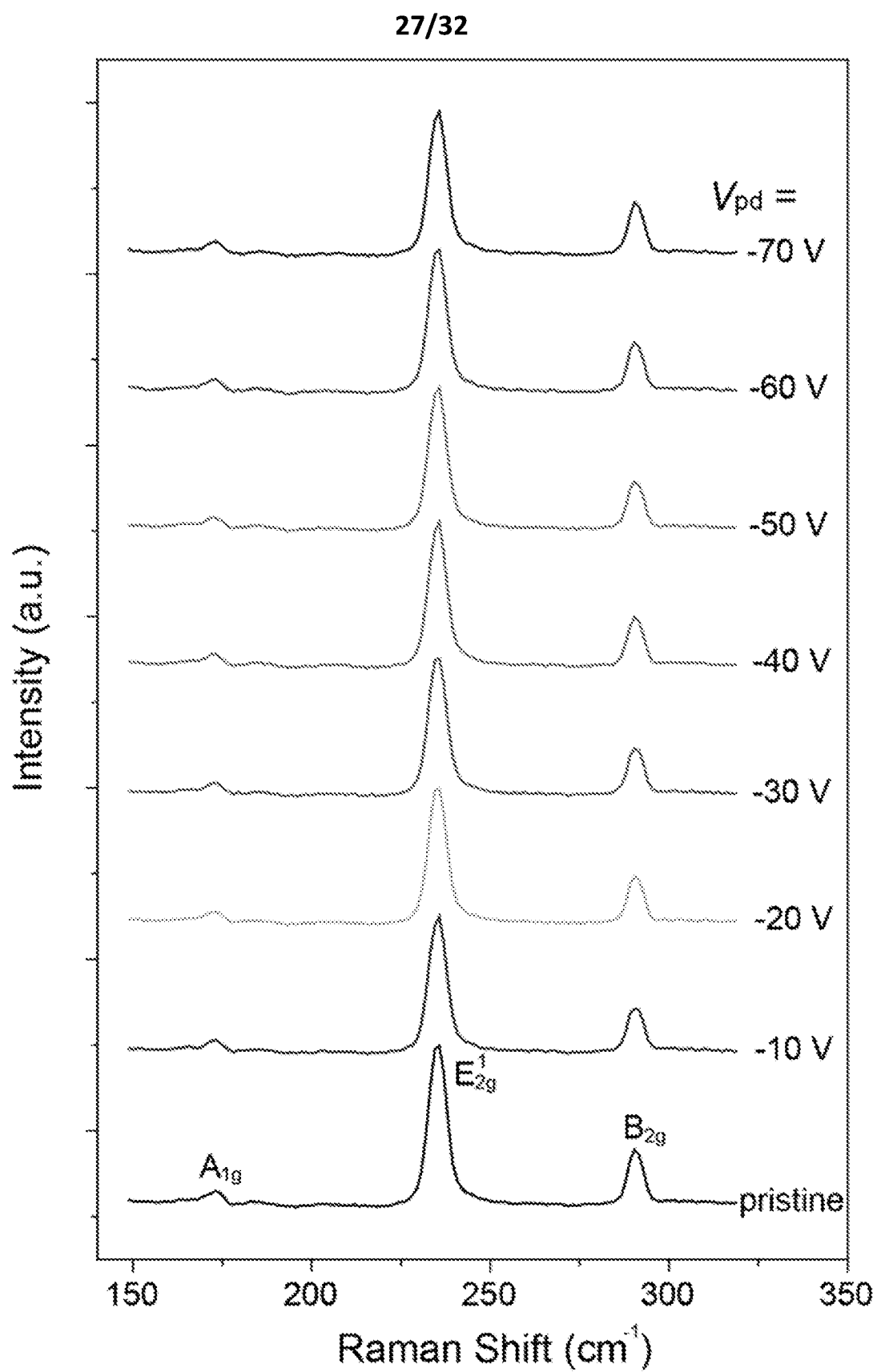


FIGURE 39

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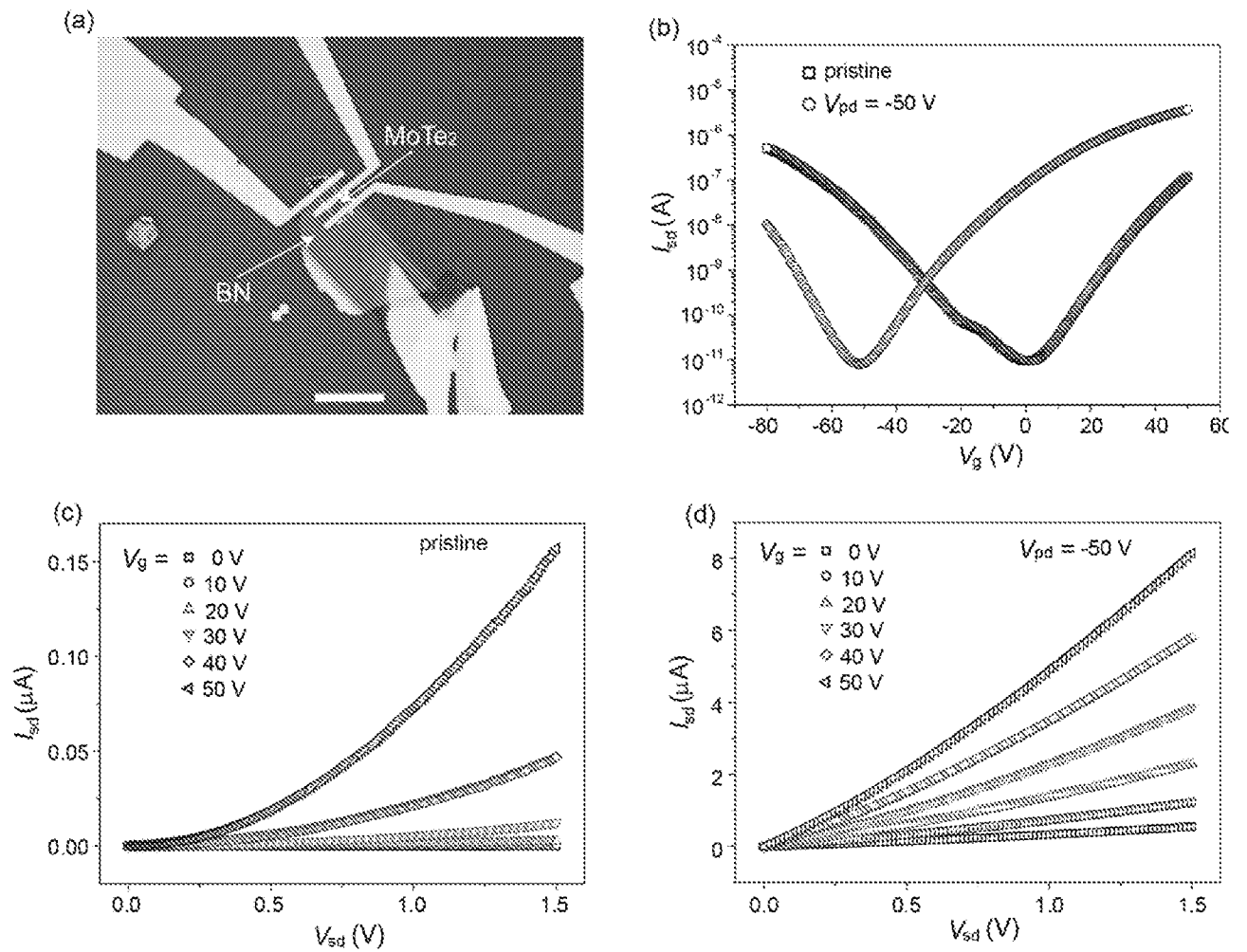


FIGURE 40

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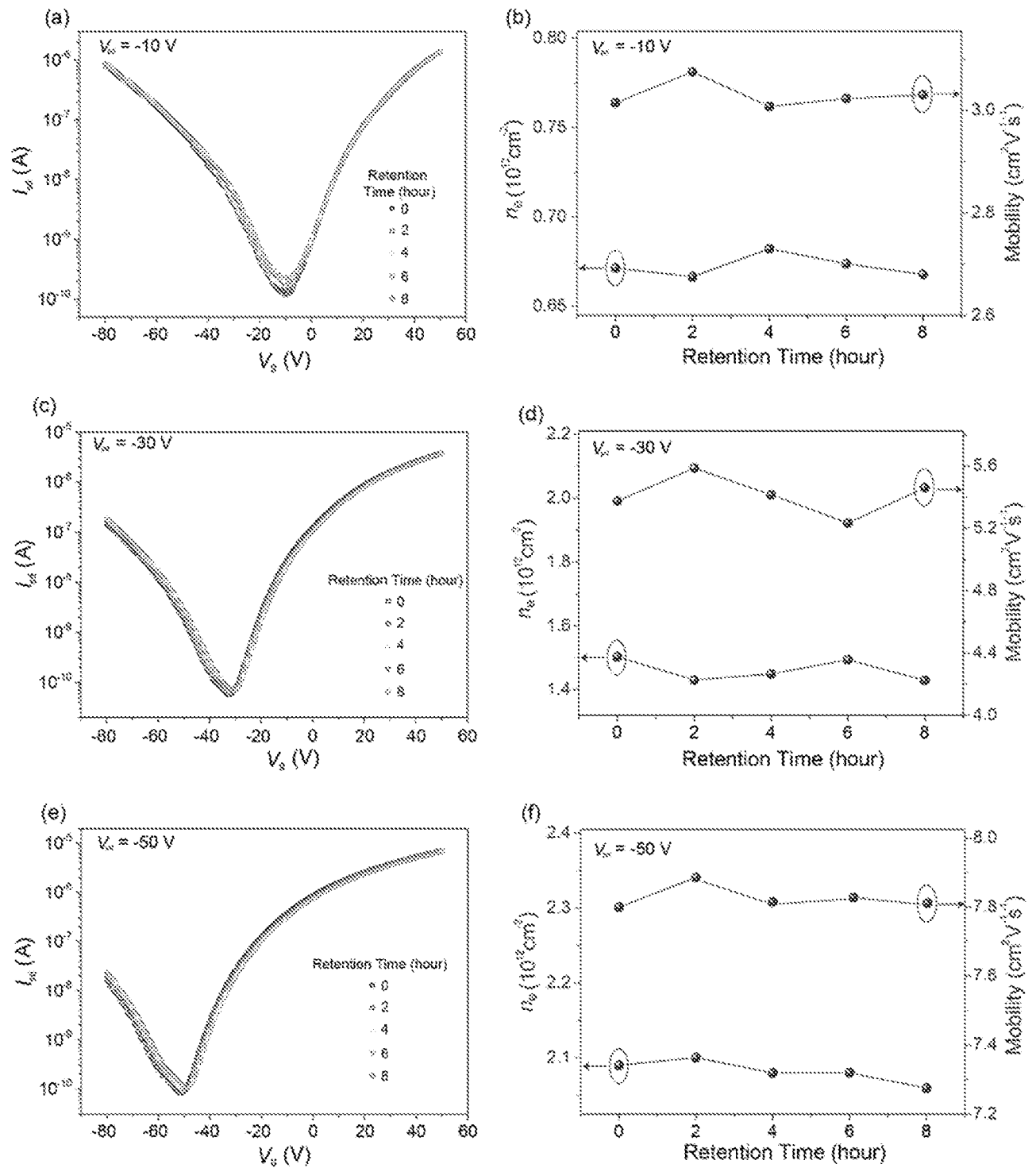


FIGURE 41

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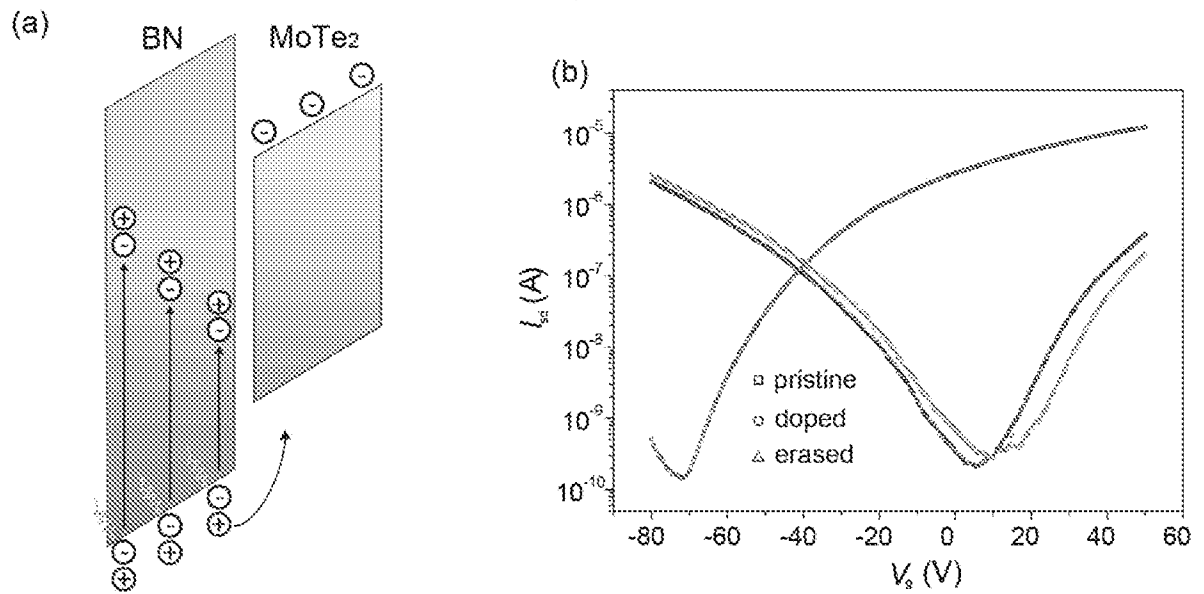


FIGURE 42

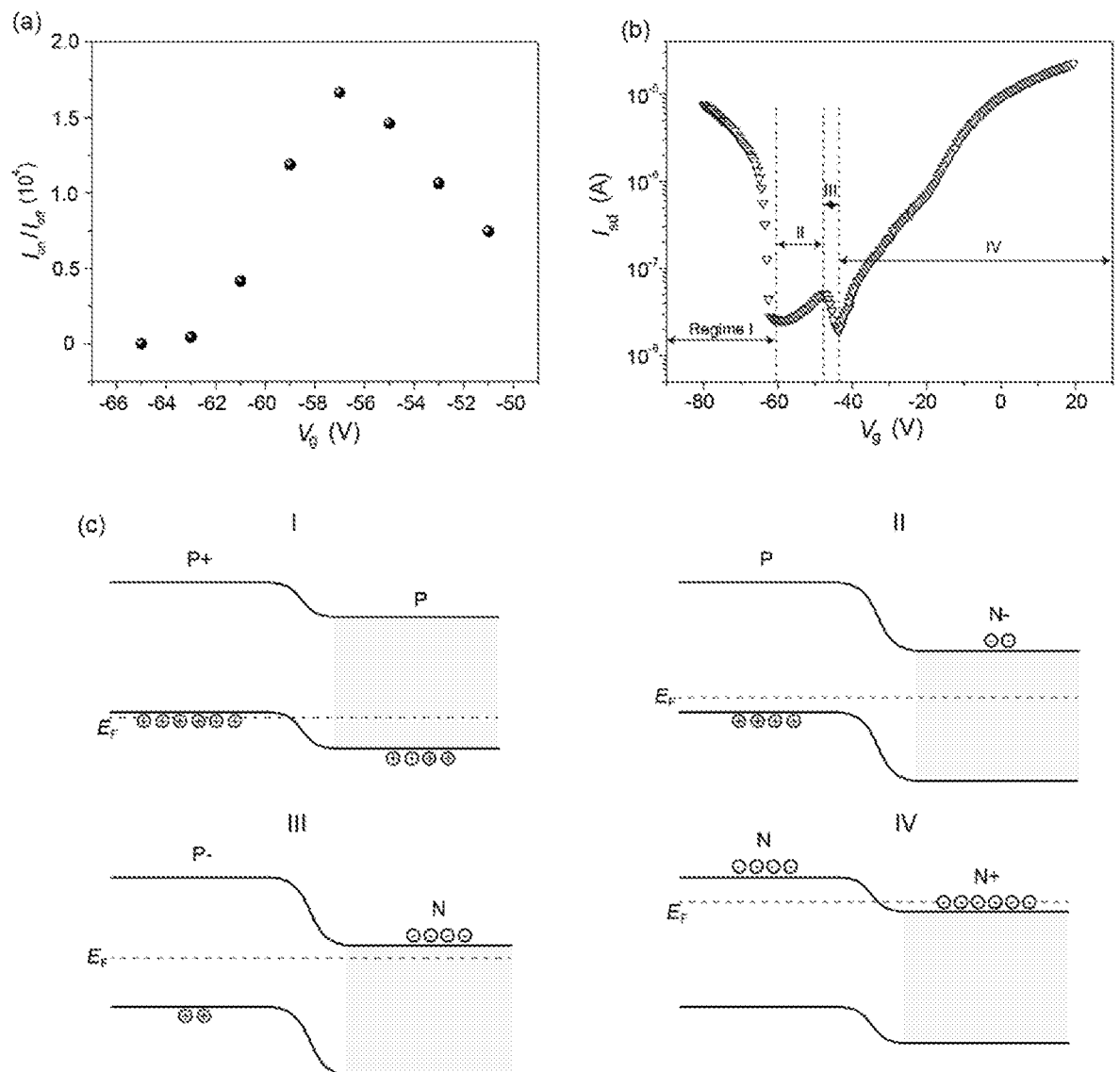


FIGURE 43

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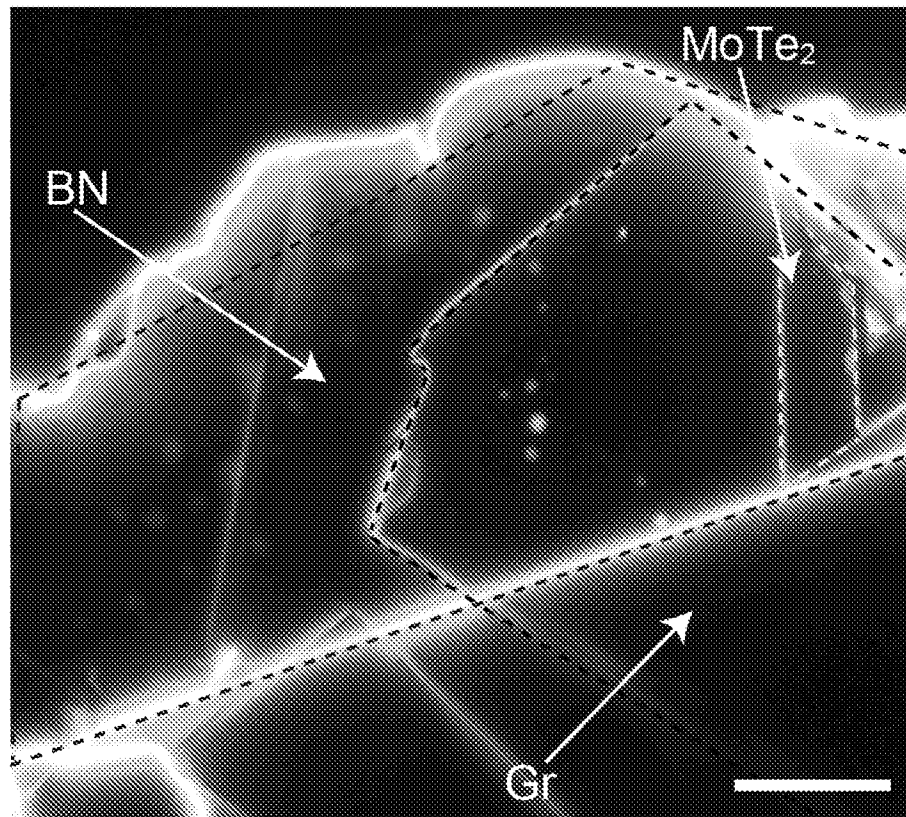


FIGURE 44

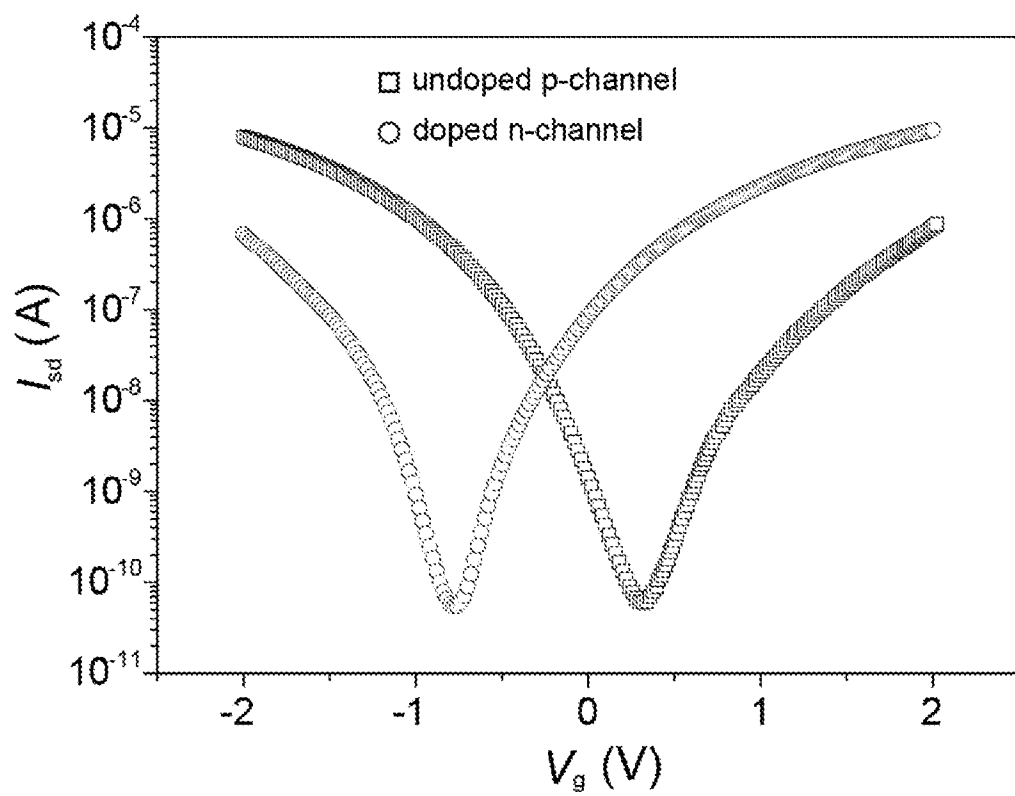


FIGURE 45

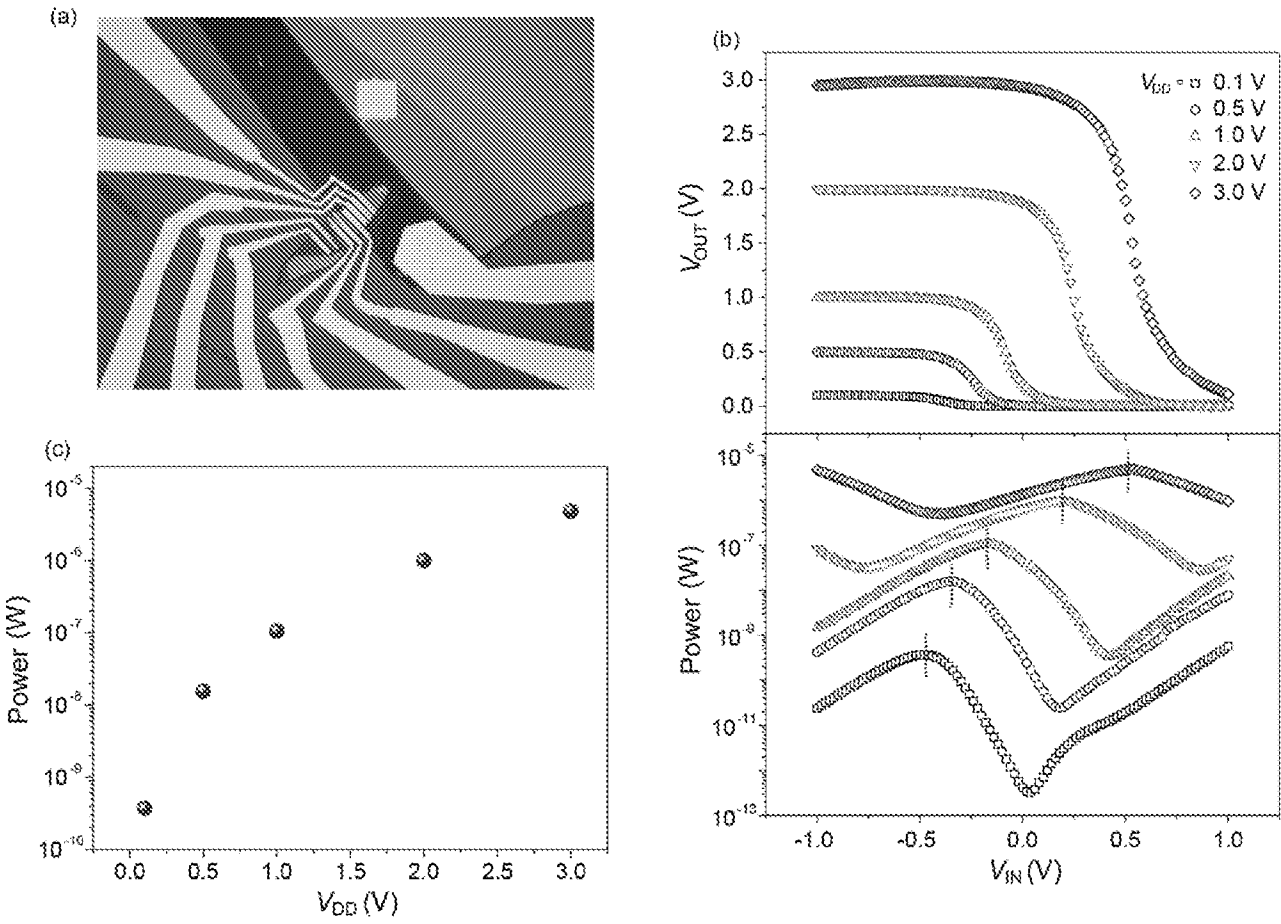


FIGURE 46

INTERNATIONAL SEARCH REPORT

International application No.

PCT/SG2019/050365

A. CLASSIFICATION OF SUBJECT MATTER

See Supplemental Box

According to International Patent Classification (IPC)

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/00; H01L 31/00; B82Y 10/00; B82Y 20/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

FAMPAT: source, drain, gate, two-dimensional, channel, heterojunction, transistor, transition metal dichalcogenide, hexagonal boron nitride, mid-gap, optoelectronic memory, phosphorene, molybdenum, graphene, van der waals, back gate, 源极, 漏极, 栅极, 异晶结构, 异质结构, 二维, 氮化硼, 光敏, 存储器 and related search keywords. Deepdyve and the internet: FET, 2D material, back gate, hBN, optoelectronic memory, monolayer and heterostructure.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ROY K. ET AL., Graphene-MoS ₂ hybrid structures for multifunctional photoresponsive memory devices. <i>Nature Nanotech.</i> , 20 October 2013, Vol. 8, pages 826-830 [Retrieved on 2019-08-13] <DOI: 10.1038/NNANO.2013.206> Entire document	1-20
X	Interlayer exciton optoelectronics in a 2D heterostructure p-n junction. 3 January 2017 [Retrieved on 2019-08-13 from https://arxiv.org/ftp/arxiv/papers/1701/1701.00802.pdf] Pages 2-3; figures 1-3	1-20
X	CN 109004016 A (NATIONAL CENTER FOR NANOSCIENCE & TECHNOLOGY CHINA) 14 December 2018 Pages 2-3, 7, 10; figure 1a of the machine translation	1-20

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search

13/08/2019

(day/month/year)

Date of mailing of the international search report

20/08/2019

(day/month/year)

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Singapore 408533

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Eunice Leong (Dr)

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/SG2019/050365

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	LI D. ET AL., Two-dimensional non-volatile programmable p-n junctions. <i>NATURE NANOTECH.</i> , 12 June 2017, Vol. 12, pages 901-907 [Retrieved on 2019-08-13] <DOI: 10.1038/NNANO.2017.104> Entire document	1-20
A	WANG F. ET AL., Progress on electronic and optoelectronic devices of 2D layered semiconducting materials. <i>SMALL</i> , 8 June 2017, Vol. 13, pages 1604298 [Retrieved on 2019-08-13] <DOI: 10.1002/SMLL.201604298> Entire document	

INTERNATIONAL SEARCH REPORT

International application No.

PCT/SG2019/050365

Supplemental Box (Classification of Subject Matter)

Int. Cl.

H01L 29/786 (2006.01)

H01L 29/267 (2006.01)

H01L 31/10 (2006.01)

B82Y 10/00 (2011.01)

B82Y 20/00 (2011.01)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/SG2019/050365

Note: This Annex lists known patent family members relating to the patent documents cited in this International Search Report. This Authority is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
CN 109004016 A	14/12/2018	NONE	