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[Continued on next page]

(54) Title: MEMRISTOR ARRAY WITH ACTIVE MEMRISTORS

(57) Abstract: In one example in accordance with the present disclosure a memristor device is described. The device includes an active memristor to be set to one of a plurality of states. The device also includes a state controller to program the state of the active memristor. The state defines a current-voltage relationship for the active memristor. The state controller also sets an operating point for the active memristor around which an input signal oscillates. The resistance of the active memristor defines an amplitude modulation of the input signal and the reactance of the active memristor defines a phase delay of the input signal.

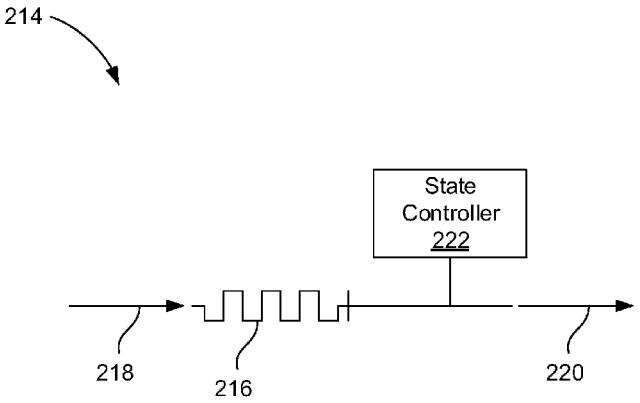

Fig. 2A

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MEMRISTOR ARRAY WITH ACTIVE MEMRISTORS

BACKGROUND

[0001] Memristors are devices that can be programmed to different states by applying a programming energy, for example, a voltage or current pulse. The programming energy generates a combination of electric field and thermal effects that are to modulate the conductivity of both non-volatile switch and non-linear select functions in a switching element. After programming, the state of the memristor remains stable over a specified time period and the state is thus readable. Memristor elements can be used in a variety of applications, including non-volatile solid state memory, programmable logic, signal processing, control systems, pattern recognition, and other applications.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The accompanying drawings illustrate various examples of the principles described herein and are a part of the specification. The illustrated examples are given merely for illustration, and do not limit the scope of the claims.

[0003] Fig. 1 is a diagram of a computing system for operating a memristor array of active memristors, according to one example of the principles described herein.

[0004] Figs. 2A and 2B are diagrams of a memristor device with an active memristor, according to one example of the principles described herein.

[0005] Fig. 3 is a flowchart of a method for operating a memristor device with an active memristor, according to another example of the principles described herein.

[0006] Fig. 4 is a diagram of a crossbar memristor array with active memristors, according to another example of the principles described herein.

[0007] Fig. 5 is a flowchart of a method for operating a memristor device with an active memristor, according to another example of the principles described herein.

[0008] Fig. 6 is a diagram of an electronic device with a memristor array with active memristors, according to one example of the principles described herein.

[0009] Throughout the drawings, identical reference numbers designate similar, but not necessarily identical, elements.

DETAILED DESCRIPTION

[0010] Electronic device usage within society is becoming more and more common place such that their use is becoming ubiquitous in society. As the use of electronic devices becomes more widespread, user demand leads development for faster, stronger, and more efficient electronic devices. Moreover, faster, stronger, and more efficient electronic devices may lead to unforeseen uses for electronic devices.

[0011] To address this rising demand for improved electronic device processing, artificial neural networks, such as spiking neural networks, may be implemented. Spiking neural networks attempt to imitate the neuron synapses in the human brain. Generally speaking, the spiking neural network incorporates time as well as neuronal and synaptic state, from which computational function may emerge in the neural network. Particularly, spiking neural networks operate on the basis that neurons generate spikes at a particular time based on the state of the neuron and that the time a spike is received impacts neuron function. When a neuron generates a spike, the spike travels to other neurons, which may adjust their states based on the time that

the spike is received. Thus a spiking neural network improves the capability by not only having a data value represented by the magnitude of an electrical signal, but also by when the electrical signal is received. Such spiking neural networks may be promising as a low energy and high performance computational topology as encoding data through spike timing can carry more bits of information than other digital encoding methods. However, while such networks offer increased processing potential, the implementation of such spiking neural networks may be inefficient.

[0012] For example, spiking neural networks compute synaptic weights, or signal amplitudes, and also control transmission delay. This additional level of control may increase the complexity and expense in implementing or simulating spiking neural networks in electronic devices.

[0013] The devices and methods of the present specification and appended claims address this and other issues. Specifically, the memristor device disclosed herein may integrate synapse design with a controllable transmission delay and signal amplitude modulation.

[0014] Specifically, the present specification describes a memristor device. The memristor device includes an active memristor that is set to one of a plurality of states and has a dynamic resistance and a dynamic reactance within a state. The memristor device also includes a state controller to program the state of the active memristor, the state defining a current-voltage relationship for the active memristor. The state controller also sets an operating point for the active memristor around which an input signal oscillates. The resistance of the active memristor defines an amplitude modulation of the input signal and the reactance of the active memristor defines a phase delay of the input signal.

[0015] The present specification also describes a crossbar array. The crossbar array includes a number of row lines and a number of column lines intersecting the row lines to form a number of junctions. A number of transmission lines of the crossbar array are coupled to the number of row lines to pass a vector of input signals along the number of row lines. A row line is to receive an individual input signal of the vector of input signals. The crossbar

array also includes a number of active memristors coupled between the row lines and the column lines at the junctions. The active memristors are to be set to a state by a forming signal, modify the amplitude of the input signal based on a resistance of the active memristor, and delay the transmission of the input signal based on the reactance of the active memristor.

[0016] The present specification describes a method for operating a memristor device with variable transmission delay. In the method an active memristor in a memristor array is set to have one of a plurality of states. The active memristor is also set to have an operating point around which an input signal oscillates.

[0017] Certain examples of the present disclosure are directed to a system and method for operating an active memristor array that provides a number of advantages not previously offered including 1) providing the increased processing potential of an artificial neural network such as a spiking neural network; and 2) providing compact and efficient timing and weight processing using a single active memristor. However, it is contemplated that the devices and methods disclosed herein may prove useful in addressing other deficiencies in a number of technical areas. Therefore the systems and devices disclosed herein should not be construed as addressing just the particular elements or deficiencies discussed herein.

[0018] As used in the present specification and in the appended claims, the term “a number of” or similar language is meant to be understood broadly as any positive number including 1 to infinity; zero not being a number, but the absence of a number.

[0019] In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present systems and methods. It will be apparent, however, to one skilled in the art that the present apparatus, systems, and methods may be practiced without these specific details. Reference in the specification to “an example” or similar language indicates that a particular feature, structure, or characteristic described in connection with that example is included as described, but may not be included in other examples.

[0020] Turning now to the figures, Fig. 1 is a diagram of an electronic device (100) for operating a memristor array (110) of active memristors having variable transmission delay, according to one example of the principles described herein. The electronic device (100) may be any device that is capable of executing data processing operations. Examples of electronic devices (100) include laptop computers, personal digital assistants (PDAs), mobile devices, notebooks, tablets, gaming systems, smartphones, and mobile devices among other electronic devices (100).

[0021] To achieve its desired functionality, the electronic device (100) includes various hardware components. Among these hardware components may be a number of processors (101), a number of data storage devices (102), a number of peripheral device adapters (103), and a number of network adapters (104). These hardware components may be interconnected through the use of a number of busses and/or network connections. In one example, the processor (101), data storage device (102), peripheral device adapters (103), and a network adapter (104) may be communicatively coupled via a bus (105).

[0022] The processor (101) may include the hardware architecture to retrieve executable code from the data storage device (102) and execute the executable code. The executable code may, when executed by the processor (101), cause the processor (101) to implement at least the functionality of operating the memristor array (110) within the electronic device (100). In the course of executing code, the processor (101) may receive input from and provide output to a number of the remaining hardware units.

[0023] The data storage device (102) includes a number of modules. The modules refer to program instructions for performing a designated function. The computer program code of the data storage device (102) causes the processor (102) to execute the designated function of the modules.

[0024] The modules refer to a combination of hardware and program instructions to perform a designated function. The modules may be hardware. For example, the modules may be implemented in the form of electronic circuitry (e.g., hardware). For example, the modules may be hardware components,

such as chip components, integrated circuit components, etc., and the modules may be hardware modules on the hardware component. Each of the modules may include its own processor, but one processor may be used by all the modules. For example, each of the modules may include a processor and memory. Alternatively, one processor may execute the designated function of each of the modules.

[0025] In a further example, the modules may be a combination of software and hardware. For example, the modules may be a set of machine readable instructions that is stored on a hardware device.

[0026] The data storage device (102), for example via the modules, may store data such as executable program code that is executed by the processor (101) or other processing device. As will be discussed, the data storage device (102) may specifically store computer code representing a number of applications that the processor (101) executes to implement at least the functionality described herein.

[0027] The data storage device (102), specifically the modules, may include a computer readable medium, a computer readable storage medium, or a non-transitory computer readable medium, among others. For example, the memory may be, an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system, apparatus, or device, or any suitable combination of the foregoing. More specific examples of the computer readable storage medium may include, for example, the following: an electrical connection having a number of wires, a portable computer diskette, a hard disk, a random access memory (RAM), a read-only memory (ROM), an erasable programmable read-only memory (EPROM or Flash memory), a portable compact disc read-only memory (CD-ROM), an optical storage device, a magnetic storage device, or any suitable combination of the foregoing. In the context of this document, a computer readable storage medium may be any tangible medium that can contain, or store computer usable program code for use by or in connection with an instruction execution system, apparatus, or device. In another example, a computer readable storage medium may be any non-transitory medium that can

contain, or store a program for use by or in connection with an instruction execution system, apparatus, or device.

[0028] The data storage device (102) may include various types of memory modules, including volatile and nonvolatile memory. For example, the data storage device (102) of the present example includes Random Access Memory (RAM) (106), Read Only Memory (ROM) (107), and Hard Disk Drive (HDD) (108) memory. Many other types of memory may also be utilized, and the present specification contemplates the use of many varying type(s) of memory as may suit a particular application of the principles described herein. In certain examples, different types of memory may be used for different data storage needs. For example, in certain examples the processor (101) may boot from Read Only Memory (ROM), maintain nonvolatile storage in the Hard Disk Drive (HDD) memory, and execute program code stored in Random Access Memory (RAM).

[0029] The device (100) also includes a voltage source (112) to apply voltages to the memristor array (110). The voltages applied may be writing voltages to program the memristors in the memristor array (110) by forcing the memristor into a particular state, which state has a particular current-voltage relationship. For example, an active memristor in a first state may have a first current-voltage relationship and an active memristor in a second state may have a second current-voltage relationship. The state to which an active memristor is set is indicated by the processor (101). In a further regard, the voltage source (112) may apply a rewriting voltage to clear the state of the memristors in the memristor array (110) such that the memristors may be re-programmed.

[0030] The device (100) also includes an active memristor array (110) that includes a number of memristors to carry out operations. A memristor is a device that retains its state even after electrical energy, i.e., a voltage or a current is removed from the memristor. For example, if charge flows in one direction through a circuit, the resistance of that component of the circuit will increase. If charge flows in the opposite direction in the circuit, the resistance will decrease. If the flow of charge is stopped by turning off the applied voltage, the component will “remember” the last resistance that it had, and when the flow

of charge starts again the resistance of the circuit will be what it was when it was last active. A memristor is a resistor device whose resistance can be changed.

[0031] Memristors in a memristor array (110) take many forms. One example is a metal-insulator-metal structure where the memristor includes a first conductive electrode a second conductive electrode and a switching element placed between the conductive electrodes. The first and second conductive electrodes may be formed of an electrically conductive material such as AlCu, AlCuSi, AlCuSi, TaAl, TiN, HfN, AlN, Pt, Cu, and WSiN. In some examples the first and second electrode are formed of the same material, and in other examples the second electrode is formed of a different material than the first electrode.

[0032] The switching element may be formed of a switching oxide, such as a metallic oxide. Specific examples of switching oxide materials may include magnesium oxide, titanium oxide, zirconium oxide, hafnium oxide, vanadium oxide, niobium oxide, tantalum oxide, chromium oxide, molybdenum oxide, tungsten oxide, manganese oxide, iron oxide, cobalt oxide, copper oxide, zinc oxide, aluminum oxide, gallium oxide, silicon oxide, germanium oxide, tin dioxide, bismuth oxide, nickel oxide, yttrium oxide, gadolinium oxide, and rhenium oxide, among other oxides. In addition to the binary oxides presented above, the switching oxides may be ternary and complex oxides such as silicon oxynitride. The oxides presented may be formed using any of a number of different processes such as sputtering from an oxide target, reactive sputtering from a metal target, atomic layer deposition (ALD), oxidizing a deposited metal or alloy layer, etc.

[0033] The state of the memristor may be changed in response to various programming conditions and the memristor is able to exhibit a memory of past electrical conditions. For instance, the memristor may be programmed to have one of a plurality of distinct states. Particularly, the resistance level of the switching element may be changed through application of an electrical field, e.g., through application of a current or voltage, in which the current or voltage may cause mobile dopants in the switching element to move and/or change the

status of conducting channel(s) in the switching element, which may alter the resulting electrical operation of the memristor. That is, for instance, the distinct resistance levels of the switching element, and thus the state of the memristor, may correspond to different programming current levels or voltage amplitudes applied to the switching element. By way of example, the switching element may be programmed to have a higher resistance level through application of an earlier current or voltage level. After removal of the current or voltage, the locations and characteristics of the dopants or conducting channels are to remain stable until the application of another programming electrical field. That is, the switching element remains at the programmed resistance level following removal of the current or voltage. In one example, the memristors in the memristor array (110) may be active memristors such that the array is an active memristor array (110).

[0034] The data storage device (102) includes an active memristor array module (111) that includes hardware and software for operating the active memristor array (110). For example, the active memristor array module (110) may include machine-readable instructions that, when executed by the processor (101), cause the processor (101) to set the state and operating point for memristors in the memristor array (110).

[0035] The hardware adapters (103, 104) in the computing system (100) enable the processor (101) to interface with various other hardware elements, external and internal to the computing device (100). For example, the peripheral device adapters (103) may provide an interface to input/output devices, such as, for example, display device (109), a mouse, or a keyboard. The peripheral device adapters (103) may also provide access to other external devices such as an external storage device, a number of network devices such as, for example, servers, switches, and routers, client devices, other types of computing devices, and combinations thereof.

[0036] The display device (109) may be provided to allow a user of the computing device (100) to interact with and implement the functionality of the computing device (100). The peripheral device adapters (103) may also create an interface between the processor (101) and the display device (109), a printer,

or other media output devices. The network adapter (104) may provide an interface to other computing devices within, for example, a network, thereby enabling the transmission of data between the computing device (100) and other devices located within the network. Examples of display devices (109) include a computer screen, a laptop screen, a mobile device screen, a personal digital assistant (PDA) screen, and a tablet screen, among other display devices (106).

[0037] Including an active memristor array (110) in the electronic device (100) may allow for complex computations, such as those performed in a spiking neural network, to be performed using simple elements such as active memristors.

[0038] Figs. 2A and 2B are diagrams of a memristor device (214) with an active memristor (216), according to one example of the principles described herein. In the memristor device (214), the memristor may be an active memristor (216). As used in the present specification and in the appended claims, an "active memristor" (216) may refer to a memristor that can be set to a number of states and within each state has a variable and dynamic resistance level and a variable and dynamic reactance level. An active memristor (216) in different states may have different current-voltage relationships. For example, in a first state an active memristor (216) may have one current-voltage relationship identified by an I/V curve. In a second state, the same active memristor (216) may have a different current-voltage relationship identified by a different I/V curve. Within each state an active memristor (216) may have a distinct dynamic reactance and dynamic resistance. For example, in a first state, the active memristor (216) may react to a change in voltage differently than when the same active memristor (216) is in a second state.

[0039] An active memristor (216) may exhibit negative differential resistance which allows the memristor (216) to transiently store energy (such as heat) and impose a phase delay on an input signal (218). Put another way an active memristor (216) has a real (resistance) component to impedance and an imaginary (reactance) component to impedance. The resistance of the active memristor (216) allows the active memristor (216) to modulate the amplitude of

an input signal (218) and the reactance of the active memristor (216) allows the active memristor (216) to impose a phase delay on the input signal (218). As the resistance and reactance of an active memristor (216) is dynamic, the effect of an active memristor (216) on an input signal may also change. In other words, the active memristor (216) acts as a function that transforms an input signal by altering its amplitude and by imposing a phase delay. Put yet another way, the output (220) of the memristor device (214) may be a delayed and amplitude-modulated version of the input signal (218). For example, the input signal may be an alternating current that includes a sequence of energy pulses, such a sequence may be referred to as a spike train. In this example, the active memristor (216) may enlarge or shrink the energy pulse and may delay the arrival of the pulses at the output (220).

[0040] As stated above, memristors may be placed into a variety of states. The state that the active memristor (216) is placed into is dependent upon the desired manipulation of the incoming signal.

[0041] An active memristor (216) may be a thermally-formed memristor. In a thermally-formed memristor a current is applied to heat up the memristor. As the memristor heats up, it conducts more current and further heats up. Doing so may generate an active memristor (216) behavior by providing a negative differential resistance, as one example. In another example, this negative differential resistance depends on the time constant for heating and cooling, and thus temporarily stores energy.

[0042] The memristor device (214) may include a state controller (222) to set the state of the active memristor (216). For example, the state controller may set the active memristor (216) to one of a number of states. When in different states, the memristor has different current-voltage relationships. In some examples, the state controller (222) may be a voltage source that applies a voltage value that is greater than a threshold value of the active memristor (216). The threshold voltage being greater forces the active memristor (216) into a particular state. Accordingly, the state controller (222) may be a voltage source (Fig. 1, 112) that applies an energy such as a voltage or a current that is

greater than a threshold voltage or current for the active memristor (216) placing the active memristor (216) into a particular state.

[0043] The state controller (222) may also affect the resistance and reactance of the active memristor (216) by selecting an operating point for the active memristor (216) around which an input signal will oscillate. For example, an operating point may be a DC bias of .8 volts and an AC input will add to that .8 volt value and see the differential resistance around that .8 volt value. Still further, an active memristor (216) in a first state and at a first operating point may impose no phase delay and a first amplitude modulation on an input signal (218). By comparison, the active memristor (216) in the first state and at a second operating point may impose no amplitude modulation and a first phase delay of an input signal (218). The operating point may be selected based on a specific modulation to be applied to the input signal. For example, one operating point may effectuate a large amplitude modulation without any phase delay and another operating point may effectuate a large phase delay without any amplitude modulation. The operating point may be selected based on a specific modulation desired for the input signal. For example, one operating point may effectuate a large amplitude modulation without any phase delay and another operating point may effectuate a large phase delay without any amplitude modulation.

[0044] In other words, the modifying effect of the active memristor (216) is dependent upon the state of the active memristor (216) (i.e., a particular current-voltage relationship as well as the operating point. Accordingly, an active memristor (216) used in an active memristor array (Fig. 1, 110) offers increased functional capability as many different functions can be carried out by a single active memristor (216) as an active memristor (216) can impose a modulation and a phase delay and can impose various modulations and phase delays depending on a state of the active memristor (216) and an operating point for the active memristor.

[0045] In summary, as described above, the active memristor (216) modulates the amplitude of an input signal (218) and also imposes a phase delay on the input signal (218). The degree to which the active memristor (216)

performs these modifications is controlled by the state controller (222) by 1) putting the active memristor (216) into a particular memristor state, and 2) selecting a particular operating point for the active memristor (216) which additionally affects the reactance and resistance of the active memristor (216) as seen by an AC input such as a spike train. In other words, the reactance and resistance of an active memristor (216) are highly tunable such that many different combinations and input signal-modifying behaviors can be selected.

[0046] In some examples, the state controller (222) may be a direct current voltage source that applies a constant voltage to the active memristor (216). For example, a memristor may be set to a particular operating point and state via a direct current form the voltage source (Fig. 1, 112). Doing so may allow a user to select a particular reactance, and corresponding phase delay, and resistance, and corresponding amplitude modulation, as desired for the particular use of the memristor array (Fig. 1, 110).

[0047] As depicted in Fig. 2A, in some examples, the active memristor (216) may be disposed between the input signal (218) and the state controller (222). However, if multiple memristor devices (214) are to be cascaded together, the state controller (222) may be between the input signal (218) and the active memristor (216) as depicted in Fig. 2B. In this example, the active memristor (216) may be coupled to a virtual ground through an operational amplifier (224) such that any downstream memristor devices (214) or memristor arrays (Fig. 1, 110) see a low impedance source and not the complexity of the upstream circuit. Connecting the memristor device (214) to a virtual ground from the operational amplifier (224) facilitates the establishment of the operating point (voltage or current) independently of any memristor devices (214) or memristor arrays (Fig. 1, 110) that are connected downstream. These make the connection of multiple memristor devices (214) simpler, and the connection of multiple memristor devices (214) further emulates the human brain, which is the intent when using a spiking neural network.

[0048] Fig. 3 is a flowchart of a method (300) for operating a memristor device (Fig. 2, 214) with an active memristor (Fig. 2, 216), according to another example of the principles described herein. As a general note, the methods

(300, 500) may be described below as being executed or performed by at least one device, for example, the electronic device (Fig. 1, 100). Other suitable systems and/or computing devices may be used as well. The methods (300, 500) may be implemented in the form of executable instructions stored on at least one machine-readable storage medium of at least one of the devices and executed by at least one processor (Fig. 1, 102) of at least one of the devices. Alternatively or in addition, the methods (300, 500) may be implemented in the form of electronic circuitry (e.g., hardware). While Figs. 3 and 5 depict operations occurring in a particular order, a number of the operations of the methods (300, 500) may be executed concurrently or in a different order than shown in Figs. 3 and 5. In some examples, the methods (300, 500) may include more or less operations than are shown in Figs. 3 and 5. In some examples, a number of the operations of the methods (300, 500) may, at certain times, be ongoing and/or may repeat.

[0049] According to the method (300), an active memristor (Fig. 2, 216) is set (block 301) to have one of a plurality of states. An active memristor (Fig. 2, 216) in different states exhibits different current-voltage relationships. The particular state that an active memristor (Fig. 2, 216) is set to is based on a desired amplitude modulation and phase delay. The amplitude modulation and phase delay may represent a function that an input signal (Fig. 2, 218) is passed through to generate an output (Fig. 2, 220). For example, the processor (Fig. 1, 101) may instruct the state controller (Fig. 2, 222) to pass an energy signal, i.e., voltage or current, to the active memristor (Fig. 2, 216) that is greater than a threshold value for the active memristor (Fig. 2, 216). As the energy signal is greater than the threshold value, the active memristor (Fig. 2, 216) is placed in a particular state.

[0050] The method (300) also includes setting (block 302) an operating point for the active memristor (Fig. 2, 216). The operating point is a bias for a given memristor state, around which any AC input signal (Fig. 2, 218) oscillates and experiences a net resistance and reactance. For example, within a particular state, an active memristor (Fig. 2, 216) at a particular operating point may have different resistance and reactance as compared to the active memristor (Fig. 2, 216) in a different state at the same or different operating

point. The operating point affects the reactance and resistance of an active memristor (Fig. 2, 216) as seen by any AC input. In some examples, the operating point is a baseline direct current voltage. In other words, the active memristor (Fig. 2, 216) is biased to a particular voltage value.

[0051] Fig. 4 is a diagram of a crossbar memristor array (110) with active memristors (216), according to another example of the principles described herein. The array (110) in Fig. 4 may include additional components and some of the components depicted in Fig. 4 may be removed or modified without departing from the scope of the array (110). In some examples, the crossbar memristor array (110) makes up at least a part of an artificial neural network such as a spiking neural network.

[0052] The memristive cross-bar array (110) may include a number of electrically conductive row lines (428-1, 428-2, 428-3) and a number of electrically conductive column lines (430-1, 430-2, 430-3) intersecting the row lines (428-1, 428-2, 428-3) to form a number of junctions. As used in the present specification "-*" refers to a specific instance of an element. For example, (428-1) references first row line. By comparison, a reference number without "-*" refers to a generic element. For example, (428) refers to a non-specific instance of a row line (428). Even though three row lines (428) and four column lines (430) are depicted in Fig. 4, any number of row lines (428) and column lines (430) may be present in the memristive cross-bar array (110). A number of "active memristors" (216) are located at the junctions and electrically couple the row lines (428) to the column lines (430). For simplicity a single instance of an active memristor (216) is identified by a reference number. As described above the active memristors (216) are set to a state by a forming signal (432) , i.e., a voltage or current that is larger than a threshold value for the active memristor (216) that is received from a state controller (Fig. 2, 222). In this set state the active memristor (216) modifies an amplitude of an input signal (218) based on the resistance of the active memristor (216) and delays the transmission of the input signal (218) based on the reactance of the active memristor (216).

[0053] With many active memristors (216) coupled together in a grid-like pattern multiple input values (218-1, 218-2, 218-3) may be simultaneously modified at high density and with minimal control lines. In this fashion, the crossbar array (110) may execute a function on a number of input signals. For example, a vector of input signals (218-1, 218-2, 218-3) may be received by transmission lines coupled to the row lines (428) and may be passed such that each row line (428) receives an individual input signal (218) of the vector of input signals. Each signal is then modulated by the active memristors (216) which modulation affects the outputs which are collected along the columns (430) of the array (110), the difference between the input and output reflective of the function. Accordingly, a desired function can be executed by imposing certain reactance levels and resistance levels to the active memristors (216).

[0054] In some examples, the crossbar array (110) may be one of a plurality of crossbar arrays (110), for example in a spiking neural network such that an output of the crossbar array (110) is passed to other crossbar arrays of the plurality. Accordingly, the inputs of each column may be coupled to a virtual ground through an operational amplifier (224-1, 224-2, 224-3) driving the outputs to facilitate the cascading nature of a plurality of crossbar arrays (110).

[0055] According to an example, the array (110) to provide a spiking neural network. Generally speaking, a spiking neural network may carry much more bits of information than traditional encoding methods, while using the same or smaller amount of energy. As such, the array (110) may provide hardware that enables a spiking neural network having a relatively high power efficiency to be realized.

[0056] Fig. 5 is a flowchart of a method (500) for operating a memristor device (Fig. 2, 214) with an active memristor (Fig. 2, 216), according to another example of the principles described herein. According to the method (500) an active memristor (Fig. 2, 216) is set (block 501) to have one of a plurality of states. This may be performed as described in connection with Fig. 3. An operating point for the active memristor (Fig. 2, 216) is set (block 502), the operating point being a value around which an input signal (Fig. 2, 218) oscillates. This may be performed as described in connection with Fig. 3.

[0057] An input signal (Fig. 2, 218) is received (block 503) at the active memristor (Fig. 2, 216). The input signal (Fig. 2, 218) may be an alternating current signal having a phase and an amplitude. As the input signal (Fig. 2, 218) is received at the active memristor (Fig. 2, 216) the reactance and the resistance of the active memristor (Fig. 216) may modulate the phase delay and the amplitude of the input signal (Fig. 2, 218), respectively. This modulated signal is collected (block 504) as an output from the active memristor (Fig. 2, 216). An output value is determined (block 505) based on the modified amplitude and time of reception (affected by the phase delay) of the output signal. This output value may then be passed onto a processor (Fig. 1, 101) or a subsequent crossbar array (Fig. 1, 110) for further processing.

[0058] Fig. 6 is a diagram of an electronic device (100) with a variable transmission delay memristor array (Fig. 1, 110) with active memristors (Fig. 2, 216), according to one example of the principles described herein. The electronic device (100) includes a processor (101) and a machine-readable storage medium (636). Although the following descriptions refer to a single processor (101) and a single machine-readable storage medium (636), the descriptions may also apply to an electronic device (100) with multiple processors and multiple machine-readable storage mediums. In such examples, the instructions may be distributed (e.g., stored) across multiple machine-readable storage mediums and the instructions may be distributed (e.g., executed by) across multiple processors.

[0059] The processor (101) may include at least one processor and other resources used to process programmed instructions. For example, the processor (101) may be a number of central processing units (CPUs), microprocessors, and/or other hardware devices suitable for retrieval and execution of instructions stored in machine-readable storage medium (636). In the electronic device (100) depicted in Fig. 6, the processor (101) may fetch, decode, and execute instructions (638, 640) for setting the operating characteristics of an active memristor (Fig. 2, 216). As an alternative or in addition to retrieving and executing instructions, the processor (101) may include a number of electronic circuits comprising a number of electronic components for performing the

functionality of a number of the instructions in the machine-readable storage medium (636). With respect to the executable instruction representations (e.g., boxes) described and shown herein, it should be understood that part or all of the executable instructions and/or electronic circuits included within one box may, in alternate examples, be included in a different box shown in the figures or in a different box not shown.

[0060] The machine-readable storage medium (636) represent generally any memory capable of storing data such as programmed instructions or data structures used by the electronic device (100). The machine-readable storage medium (636) may be included in the data storage device (Fig. 1, 102) or any of the modules therein. The machine-readable storage medium (636) includes a machine readable storage medium that contains machine readable program code to cause tasks to be executed by the processor (101). The machine-readable storage medium (636) may be tangible and/or non-transitory storage medium. The machine-readable storage medium (636) may be any appropriate storage medium that is not a transmission storage medium. For example, the machine-readable storage medium (636) may be any electronic, magnetic, optical, or other physical storage device that stores executable instructions. Thus, machine-readable storage medium (636) may be, for example, Random Access Memory (RAM), an Electrically-Erasable Programmable Read-Only Memory (EEPROM), a storage drive, an optical disc, and the like. The machine-readable storage medium (636) may be disposed within the electronic device (100), as shown in Fig. 6. In this situation, the executable instructions may be "installed" on the electronic device (100). Alternatively, the machine-readable storage medium (636) may be a portable, external or remote storage medium, for example, that allows the electronic device (100) to download the instructions from the portable/external/remote storage medium. In this situation, the executable instructions may be part of an "installation package". As described herein, the machine-readable storage medium (636) may be encoded with executable instructions for dual-power reception.

[0061] Referring to Fig. 6, state setting instructions (638), when executed by a processor (101), may cause the electronic device (100) to set an active

memristor (Fig. 2, 216) in an active memristor array (Fig. 1, 110) to one of a plurality of states. Operating point instructions (640), when executed by a processor (101), may cause the electronic device (100) to set an operating point for the active memristor (Fig. 2, 216) around which an input signal (Fig. 2, 218) oscillates.

[0062] In some examples, the processor (101) and machine-readable storage medium (636) are located within the same physical component, such as a server, or a network component. The machine-readable storage medium (636) may be part of the physical component's main memory, caches, registers, non-volatile memory, or elsewhere in the physical component's memory hierarchy. Alternatively, the machine-readable storage medium (636) may be in communication with the processor (101) over a network. Thus, the electronic device (100) may be implemented on a user device, on a server, on a collection of servers, or combinations thereof.

[0063] The electronic device (100) of Fig. 6 may be part of a general purpose computer. However, in alternative examples, the electronic device (100) is part of an application specific integrated circuit

[0064] Aspects of the present system and method are described herein with reference to flowchart illustrations and/or block diagrams of methods, apparatus (systems) and computer program products according to examples of the principles described herein. Each block of the flowchart illustrations and block diagrams, and combinations of blocks in the flowchart illustrations and block diagrams, may be implemented by computer usable program code. The computer usable program code may be provided to a processor of a general purpose computer, special purpose computer, or other programmable data processing apparatus to produce a machine, such that the machine-readable program code, when executed via, for example, the processor (Fig. 1, 102) of the computing system or other programmable data processing apparatus, implement the functions or acts specified in the flowchart and/or block diagram block or blocks. In one example, the computer usable program code may be embodied within a computer readable storage medium; the computer readable storage medium being part of the computer program product. In one example,

the computer readable storage medium is a non-transitory computer readable medium.

[0065] Certain examples of the present disclosure are directed to a system and method for operating an active memristor array as part of, for example, a spiking neural network that provides a number of advantages not previously offered including 1) providing the increased processing potential of an artificial neural network such as a spiking neural network; and 2) providing compact and efficient timing and weight processing using a single active memristor. However, it is contemplated that the devices and methods disclosed herein may prove useful in addressing other deficiencies in a number of technical areas. Therefore the systems and devices disclosed herein should not be construed as addressing just the particular elements or deficiencies discussed herein.

[0066] The preceding description has been presented to illustrate and describe examples of the principles described. This description is not intended to be exhaustive or to limit these principles to any precise form disclosed. Many modifications and variations are possible in light of the above teaching.

CLAIMS

WHAT IS CLAIMED IS:

1. A memristor device comprising:
an active memristor, wherein the active memristor:
is to be set to one of a plurality of states; and
has a dynamic resistance and a dynamic reactance within a state; and
a state controller to:
program the state of the active memristor, wherein the state defines a current-voltage relationship for the active memristor; and
set an operating point for the active memristor around which an input signal oscillates;
wherein:
a resistance of the active memristor defines an amplitude modulation of the input signal; and
a reactance of the active memristor defines a phase delay of the input signal.

2. The memristor device of claim 1, wherein the active memristor is between the input signal and the state controller.

3. The memristor device of claim 1, wherein the state controller is between the input signal and the active memristor.

4. The memristor device of claim 1, wherein an input of the active memristor is coupled to an operational amplifier.

5. The memristor device of claim 1, wherein the input signal is an alternating spike train.

6. The memristor device of claim 1, wherein the state controller is a direct current voltage source to apply a voltage to the active memristor.

7. The memristor device of claim 1, wherein the active memristor has a negative differential resistance.

8. A crossbar array comprising:

a number of row lines;

a number of column lines intersecting the row lines to form a number of junctions;

a number of transmission lines coupled to the number of rows to pass a vector of input signals along the number of row lines, wherein a row line is to receive an input signal for the vector of input signals;

a number of active memristors coupled between the row lines and the column lines at the junctions, the active memristors:

to be set to a state by a forming signal;

modify the amplitude of the input signal based on a resistance of the active memristor; and

delay the transmission of the input signal based on the reactance of the active memristor.

9. The crossbar array of claim 8, wherein the crossbar array is part of a spiking neural network.

10. The crossbar array of claim 8, wherein:

the crossbar array is one of a plurality of crossbar arrays; and

an output of the crossbar array is passed to a second crossbar array of the plurality of crossbar arrays.

11. The crossbar array of claim 8, wherein the number of active memristors are thermally-formed memristors.

12. A method of operating a memristor device, comprising:

setting an active memristor in a memristor array to have one of a plurality of states; and

setting an operating point for the active memristor around which an input signal oscillates.

13. The method of claim 12, further comprising:

applying an input signal to the active memristor, wherein the input signal is:

modulated via a resistance of the active memristor; and

temporally delayed via a reactance of the active memristor;

collecting an output signal from the active memristor; and

determining an output value based on the amplitude and timing of receipt of the output signal.

14. The method of claim 12, wherein the input signal is an alternating current signal.

15. The method of claim 12, wherein the operating point is a baseline direct current voltage.

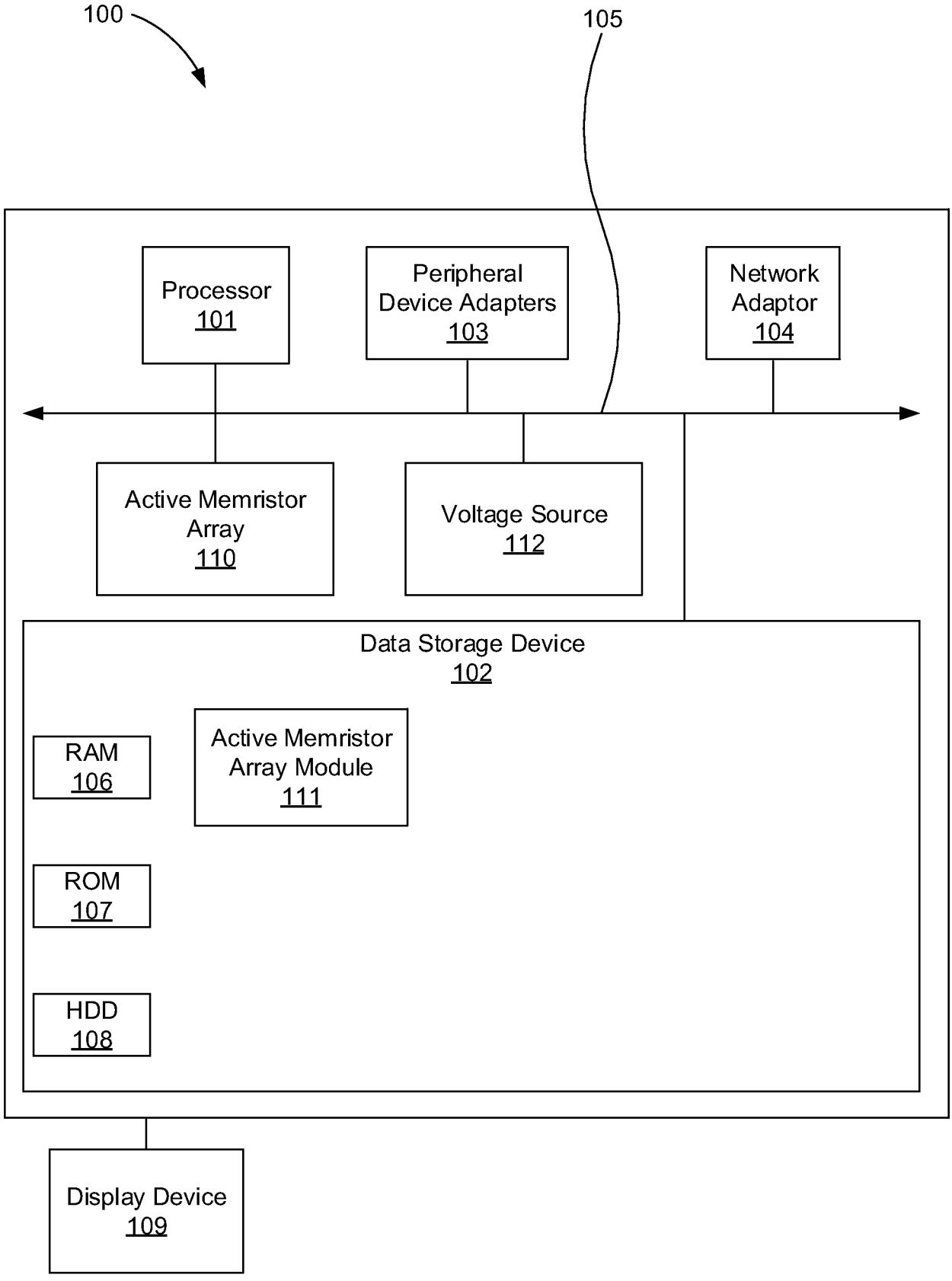
100
105
Processor
101
Peripheral
Device Adapters
103
Network
Adaptor
104
Active Memristor
Array
110
Voltage Source
112
Data Storage Device
102
RAM
106
Active Memristor
Array Module
111
ROM
107
HDD
108
Display Device
109

Fig. 1

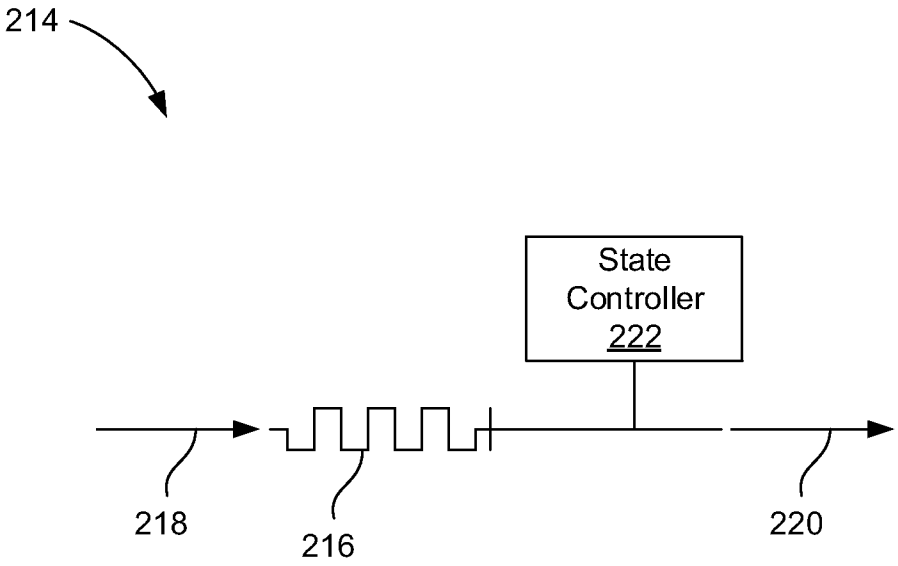
214
State
Controller
222
218
216
220

Fig. 2A

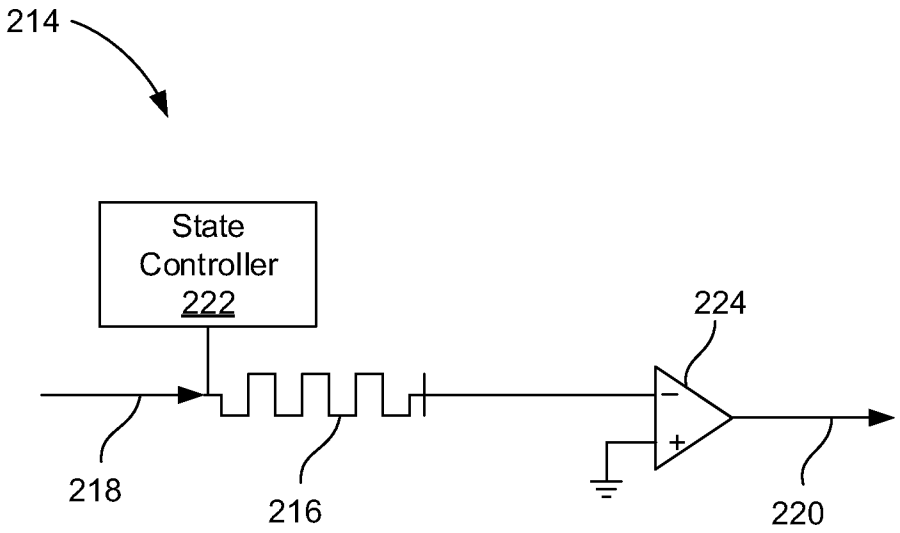
214
State
Controller
222
224
218
216
220

Fig. 2B

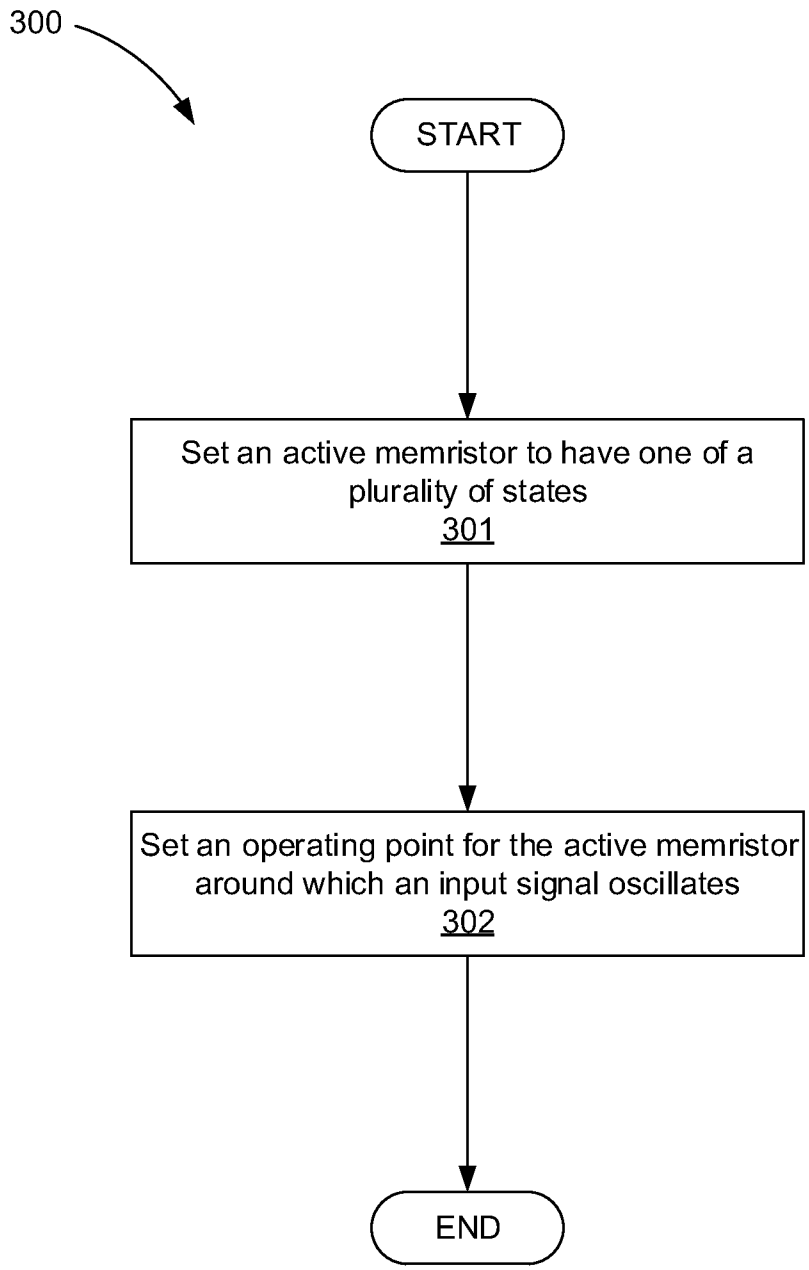
300
START
Set an active memristor to have one of a plurality of states
301
Set an operating point for the active memristor around which an input signal oscillates
302
END

Fig. 3

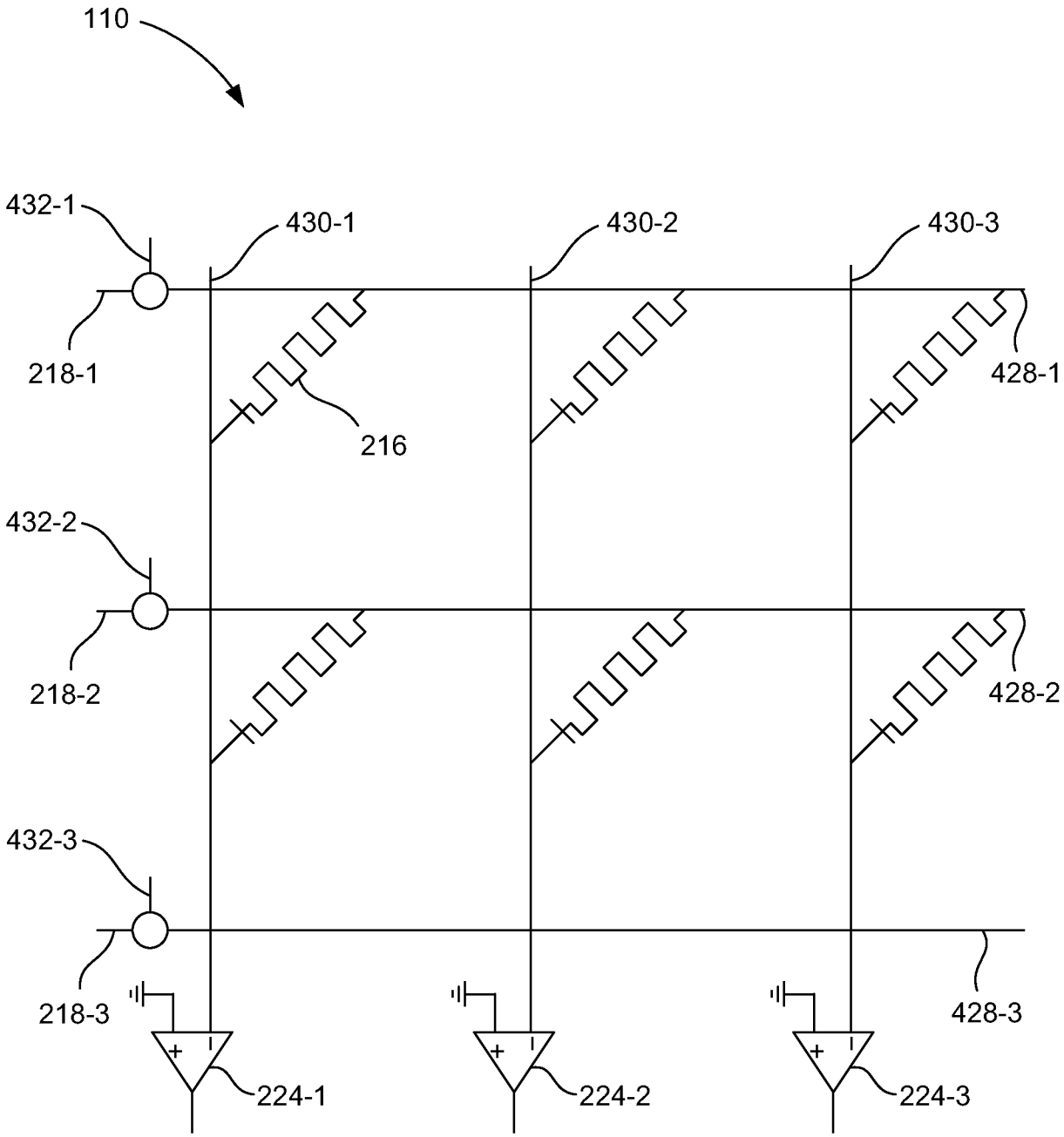
110
432-1
430-1
430-2
430-3
218-1
216
428-1
432-2
218-2
428-2
432-3
218-3
428-3
224-1
224-2
224-3

Fig. 4

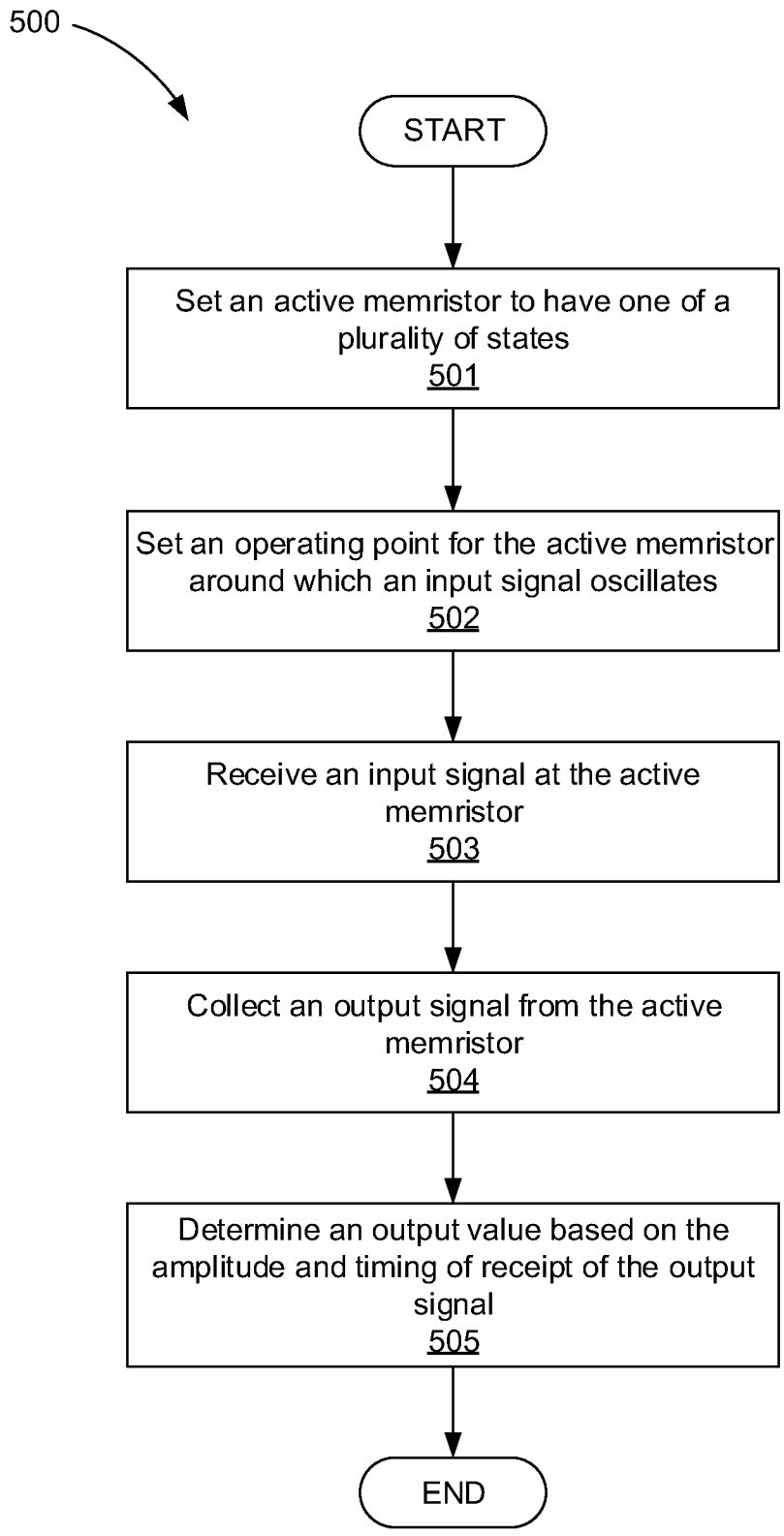
500
START
Set an active memristor to have one of a plurality of states
501
Set an operating point for the active memristor around which an input signal oscillates
502
Receive an input signal at the active memristor
503
Collect an output signal from the active memristor
504
Determine an output value based on the amplitude and timing of receipt of the output signal
505
END

Fig. 5

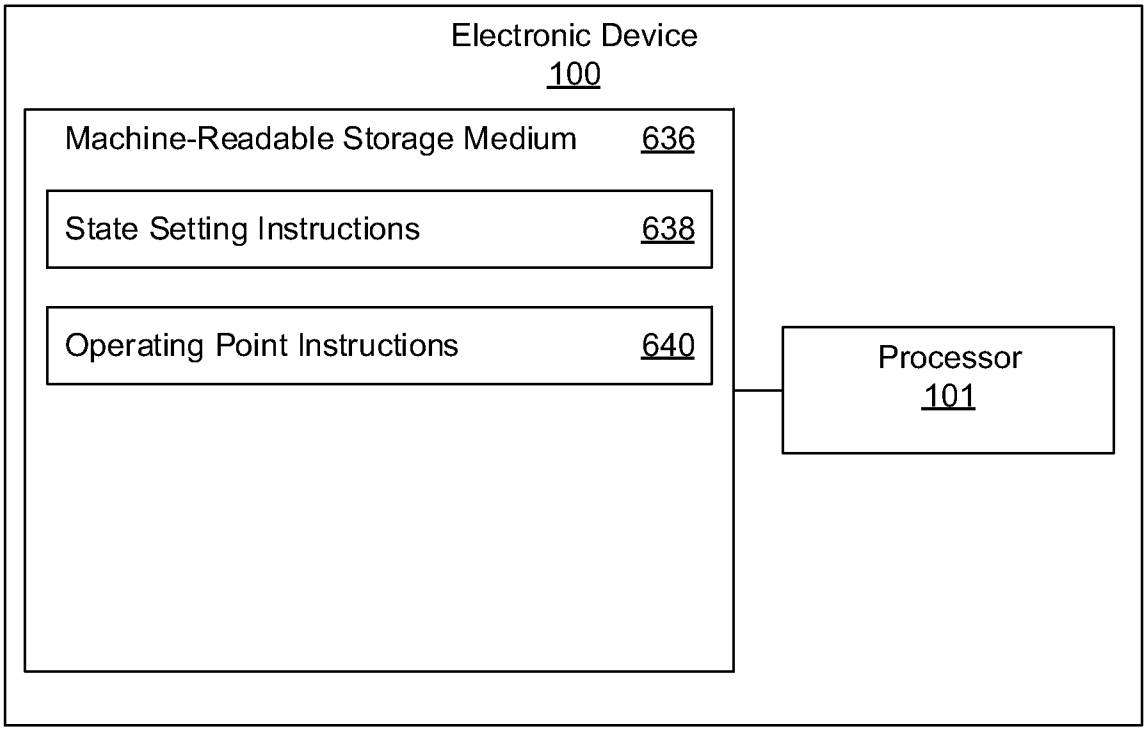
Electronic Device
100
Machine-Readable Storage Medium
636
State Setting Instructions
638
Operating Point Instructions
640
Processor
101

Fig. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/040877

A. CLASSIFICATION OF SUBJECT MATTER

G11C 11/56(2006.01)i, G11C 13/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C 11/56; G06N 3/063; G06N 99/00; G06N 3/04; G06N 3/08; G06N 3/02; H01L 27/24; G11C 13/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: active, set, state, current-voltage, operating, point, input, signal, oscillate, resistance, amplitude, modulation, reactance, spike, crossbar, array, memristor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2012-0011091 A1 (VLADIMIR APARIN et al.) 12 January 2012 See paragraphs [0029], [0034]-[0037], [0039], [0043], [0048]; and figures 1-5.	1-9,12-15
A		10-11
Y	US 2014-0258194 A1 (REGAN BLYTHE TOWAL et al.) 11 September 2014 See paragraphs [0047], [0049], [0053]-[0056], [0059]; and figures 1-2.	1-9,12-15
Y	US 2012-0317063 A1 (JAE YOON SIM et al.) 13 December 2012 See paragraphs [0056]-[0083]; and figure 1.	8-9
A	US 2015-0019468 A1 (ALEX NUGENT et al.) 15 January 2015 See paragraphs [0081]-[0086]; and figure 5.	1-15
A	US 2012-0175583 A1 (ALEX NUGENT) 12 July 2012 See paragraph [0086]; and figure 22.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
03 June 2016 (03.06.2016)	**03 June 2016 (03.06.2016)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/040877

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		WO 2012-006465 A1	12/01/2012
US 2014-0258194 A1	11/09/2014	WO 2014-138202 A1	12/09/2014
US 2012-0317063 A1	13/12/2012	EP 2718933 A1	16/04/2014
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		WO 2012-169726 A1	13/12/2012
US 2015-0019468 A1	15/01/2015	None	
US 2012-0175583 A1	12/07/2012	US 9104975 B2	11/08/2015