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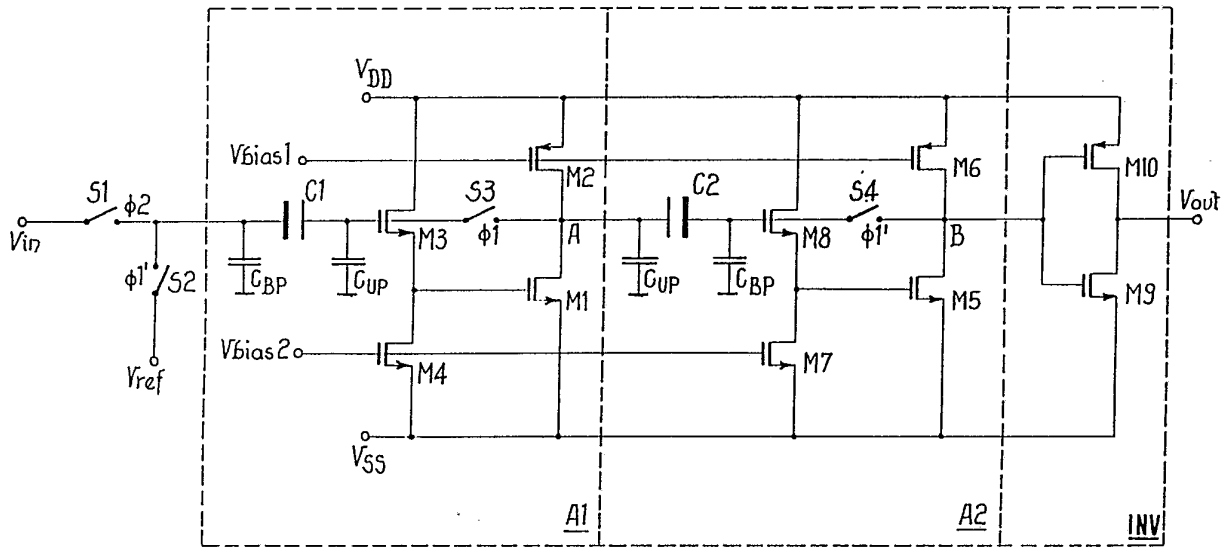

(57) Abstract

The comparator circuit of the autozeroed type, for implementation in CMOS technology, includes two identical cascaded amplifier stages (A1, A2), and one final stage at which output a square-wave signal, representing the times during which the input signal (Vin) is higher than the reference signal (Vref), is present. Each one of the two amplifier stages (A1, A2) includes an inverter (M1, M2; M5, M6) driven by a follower circuit (M3, M4; M7, M8).

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"LOW POWER DISSIPATION AUTOZEROED COMPARATOR CIRCUIT"

DESCRIPTION

The present invention relates to a low power dissipation autozeroed comparator circuit suitable for CMOS integration.

As known, a comparator circuit receives at its input a constant reference signal and a signal generally variable in time, and produces a square-wave signal representing the times during which the level of the variable signal is higher (or lower) than the threshold represented by the reference signal.

The operation of an autozeroed comparator occurs in two times or phases, an autozero phase Φ1 where the circuit initial conditions are resetted, and phase Φ2 where the input signal Vin is compared to the reference signal Vref.

Comparators are used in a variety of digital processing systems requiring a conversion interface.

CMOS comparators with autozero-phase designed through switched capacitors (SC) tecnique, are already well known.

Fig. 1 shows a known circuit of this type, consisting of two cascaded autozeroed inverters, followed by a so-called latch L. The basic structure, shown inside the dotted section, includes two transistors MA1 and MA2, n channel and p channel respectively, connected in series between two voltages V_{DD} and V_{SS}, whose gates are shorted.

To the gates common node one of plates of comparator input capacitor C1, is connected. Two switches S1 and S2 are foreseen to connect alternatively and subsequently the other plate of capacitance C1 to an input voltage Vin and to a reference voltage Vref, respectively.

The gates common node is connected to capacitance C2 of the subsequent stage through a switch S3, this stage being alike to the previous one and formed by components C2, MA3, MA4 and S4.

In autozero operation (during which the switch S3 is closed) the two transistors MA1 and MA2 are biased in the saturation range with high voltage between gate and source V_{GS} equal to approx $(V_{DD} - V_{SS})/2$.

This condition causes a high bias current Ip to flow through the transistors MA1 and MA2 and, consequently a considerable power dissipation.

One of the objects of the present invention is therefore to eliminate or at least to limit this disadvantage of the present known autozeroed comparators, and in particular to realize a low power dissipation circuit, suitable for integration in CMOS technology.

Another object of the invention is to propose a comparator having improved performances, in particular able to obtain an advantageous compromise between operation

speed and power dissipation, together with improved sensitivity performances.

These objects are achieved with the comparator of this invention thanks to the characteristics which form the object of claim 1. Further favourable characteristics result from the sub-claims.

The invention shall be now described referring to the preferred, but not limiting, realization forms, illustrated in the enclosed figures, where:

Fig. 1 shows an example of comparator according to the known technique;

Fig. 2 shows a schematic of the comparator according to the invention;

Fig. 3 shows the timing of phase or clock signals; and

Fig. 4 shows a realization variant of the single gain stage of comparator according to the invention.

Fig. 1 refers to a comparator according to the known technique which has already been examined briefly and shall not therefore be furtherly described.

Fig. 2 shows a schematic of the comparator according to the invention, consisting of a three stage cascade A1, A2 and INV. Stages A1 and A2 are essentially alike and realize the gain required for the operation, while the INV stage is an inverter stage employed to square the outgoing waveform Vout. According to a not shown realization

variant, INV stage could be replaced by a latch whose function is to store the voltage at node B on the edge of an appropriate control phase.

Each of the two stages A1 and A2 includes four transistors, M1-M4 and M5-M8, respectively. Being the two stages essentially identical, stage A1 only shall be described in detail.

This stage includes an inverter circuit (transistors M1 and M2) driven by a follower circuit formed by transistors M3 and M4, shown in Fig. 2 as n channels. An autozeroed CMOS switch S3 is connected between these two circuits; its control clock or phase signal is described below.

Switch S3 is closed when phase Φ1 is active (high) and conventionally, in the Figures, each controlled switch is marked also by a phase signal, meaning by that the switch results being closed when this phase signal is high.

Stage A1 needs two supply voltages V_{DD} and V_{SS}, and also two bias voltages, Vbias1 and Vbias 2 for the gates of M2 and M4 transistors, respectively. M3 gate is connected to a plate of the comparator input capacitance C1, whose other plate is connected, selectively and subsequently, to the input voltage Vin and to the reference voltage Vref. In Fig. 2 stray capacitances of C1 plates labelled C_{BP} and C_{UP}

are also highlighted, and the same for capacitance C2 of stage A2.

Connections between C1 and voltages Vin and Vref are assured via the controlled switches S1 and S2, respectively. More in detail, the switch S1 is closed when phase Φ2 is high, while the switch S2 is controlled by a Φ1′ signal. As can be seen in Fig. 3, Φ1′ is a replica of phase Φ1 where the opening edge has a delay equal to τ compared to the same edge for phase Φ1. However, this delay is such to uphold the transition in the disoverlap range between Φ1 and Φ2.

The output of stage A1 is withdrawn at the common node A of M1 and M2 drain terminals. As already pointed out, the connection between M3 gate and output node A is provided via switch S3 controlled by phase Φ1.

Stage A2 is cascaded to the previous one and is alike. A2 stage output is withdrawn at node B common to M5 and M6 drain terminals. The connection between M8 gate and output node B takes place via switch S4 controlled by phase Φ1′.

The inverter stage INV consists of two transistors M9 and M10 and this stage needs to generate an output waveform with very steep transition edges between high logic level and low logic level.

The comparator circuit operates as follows.

During phase Φ1 the comparator autozero is carried out (S3 and S4 switched on) as well as the charging of the input capacitance C1 to the reference level (S2 switched on). Being phases Φ1 and Φ1′ simultaneous, the autorezero operation is carried out on both gain stages A1 and A2.

The autozero is introduced to have all the transistors of the two stages A1 and A2 led again to the linear operation range, between a switching phase and the subsequent one. At the end of this operation, the circuit resets in the initial bias conditions, imposing a voltage value equal to approximately $(V_{DD} - V_{SS})/2$ at nodes A and B. By this operation the values of input and output voltages of each gain stage result equal between them and equal to the half of swing range voltage.

This equal distance of output voltages (intermediate ones in each single stage) from both final logic levels allows to balance the response times (and therefore the speed) of the comparator for input signals higher and lower, of a same quantity than the reference voltage.

The autozero phase is requested also to compensate the comparator offset, approximately egual to the offset of the first stage A1 since the offset charge stored on capacitor C2 of stage A2, referred to the input of the comparator, is divided by the gain of the first stage and therefore highly attenuated.

In the comparator, measures are taken to minimize voltage peaks in input capacitor C1, due to the clockfeedthrough charge injection at the end of phase Φ1.

This charge injection has to be reduced as much as possible since it is amplified by the gain of both stages A1 and A2 and can originate a false switching of the output towards one of the two possible logic states, depending on the charge sign. The contribution of this charge tends to originate an asymmetrical behaviour of the comparator, accelerating one transition and delaying the other one.

To reduce this charge, CMOS switches S3 and S4 are adequately sized and S4 is also controlled by phase Φ1' whose opening edge is slightly delayed in respect with the one of signal Φ1 controlling S3.

Thus, when S3 is open, S4 remains still closed for the time τ, and the charge injected towards C2 sees low impedance towards the output, entering C2 and traducing an offset voltage equal to (Q/C2) for the stage A2, where (Q) is the clockfeedthrough charge. The charge injected towards C1 sees a low impedance path towards Vref and entrs C1.

When after the delay τ S4 opens too, the charge injected towards A charges the parasitic capacitance of C2 (C_{BP}). Due to the fact that the voltage drop produced is inversely proportional to such parasitic capacitance, it is preferred to connect the bottom plate of C2 to the gate of

M8 as shown in Fig. 2. In this way there is also the advantage to avoid a too high capacitive load at node A which would originate a slowing down of stage A1.

Similarly, the charge deriving from the delayed opening of S2 charges the parasitic capacitance (C_{BP}) at the input of stage A1 to which the bottom plate of C1 is connected in order to avoid a partition of the input signal between C1 and the stray capacitance at M3 gate.

During phase Φ2 , switch S1 connecting C1 to the input voltage Vin, is closed and the comparison between this voltage and the reference precharged in C1 takes place.

In stages A1 and A2 according to the invention, the follower transistor (M3, M8 respectively) allows biasing the corresponding gain transistors (M1, M5 respectively) in the saturation area, characterized by a low drop voltage between gate and source, with an ensuring reduction of the bias current Ip. Making reference to stage A!, the gain of each stage can be expressed as follows:

$$G = \frac{gm1}{gds1 + gds2}$$

where gm1 is the transconductance of the gain transistor, equal to:

$$\sqrt{2\mu C_{ox}(W/L)I_p},$$

and gds1 and gds2 are the channel conductances of the gain transistor and of the load transistor, respectively.

Thus G is proportional to $1/\sqrt{Ip}$, consequently, the possibility to perform a low bias current operation helps the realization of a high gain and therefore of a good sensitivity.

At fixed bias current to meet the low dissipation specification, the switching speed can be assured through an adequate sizing of transistors M1 and M5, respectively; in fact speed is proportional to gm1, which in its turn depends on $\sqrt{Ip(W/L)}$, where W is the width and L is the length of the gain transistor. The gain required for the correct toggling of the comparator is assured by the cascade of the two gain stages.

The final inverter stage INV is constantly unbalanced and not affecting therefore the total power dissipation.

According to a further realization form partially shown in Fig. 4, the comparator circuit can include a further follower stage including transistors M11 and M12 driving transistor M2. A similar follower stage is introduced to drive transistor M6, thus obtaining an increase of the gain of each stage and of the switching speed.

Moreover it must be noticed that the optimization between operation speed and circuit power dissipation

according to the invention enables also an improvement of sensitivity performance, thanks to the gain enhancement deriving from a lower stationary current.

CLAIMS

1. Autozeroed comparator circuit, including a first amplifier stage (A1) whose input can be selctively connected to an input voltage (Vin) and to a reference voltage (Vref); a second amplifier stage (A2) connected to the output of this last, and a final stage at which output a rectangular signal is present, representing the times during which the input signal (Vin) is higher than the reference signal (Vref), characterized by the fact that the two amplifier stages (A1; A2) are identical and each one includes an inverter (M1, M2; M5, M6) driven by a follower circuit (M3, M4; M7, M8).

2. Comparator circuit according to claim 1, characterized by the fact that said first amplifier stage (A1) includes an input capacitance (C1) having a selectively and not simultaneously connectable plate, via two controlled input switches (S2, S1), to the reference voltage (Vref) and to the input voltage (Vin), respectively, and a first controlled switch (S3) between the follower transistor (M3) and the output (A) of said first stage (A1).

3. Comparator circuit according to claim 1, characterized by the fact that said second stage (A2) has a second controlled switch (S4) between the follower

transistor (M8) and the output (B) of said second stage (A2).

4. Comparator circuit according to claim 3, characterized by the fact that said first controlled switch (S3) of the first amplifier circuit (A1) is closed when a first phase signal (Φ1) is high during which the autozero operation occurs.

5. Comparator circuit according to claim 4, characterized by the fact that said controlled input switch (S1) for the connection to the input voltage (Vin) is closed when a second phase signal (Φ2) is active, subsequent in time to said first phase signal (Φ1).

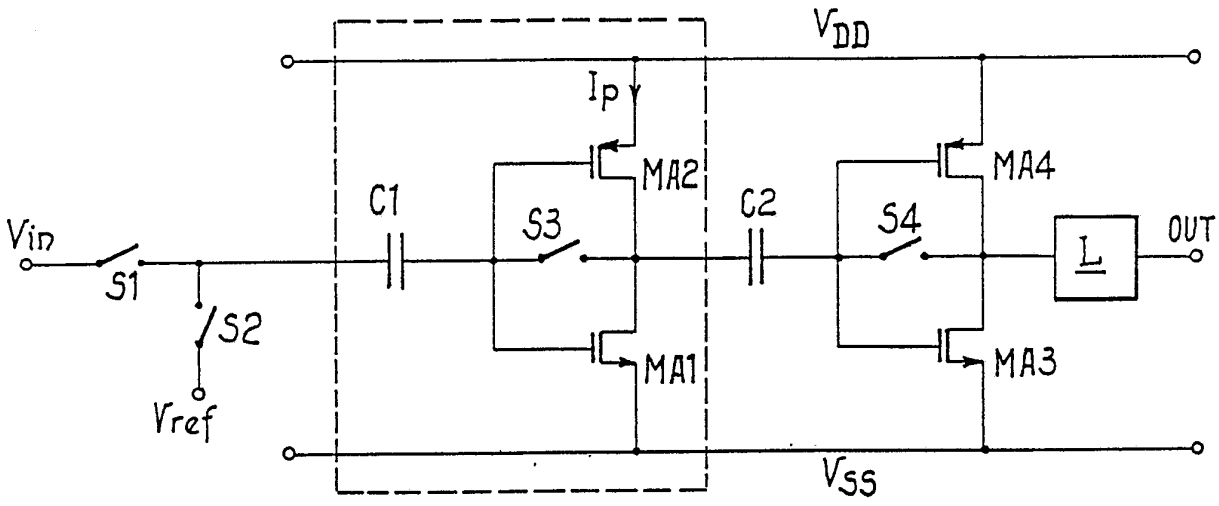
6. Comparator circuit according to claim 4 or 5, characterized by the fact that said controlled input switch (S2) for the connection to the reference voltage (Vref) and said second controlled switch (S4) of the second amplifier circuit (A2) are controlled by a phase signal (Φ1') remaining active for a longer time compared to said first phase signal (Φ1), but not superimposing to said second phase signal (Φ2).

7. Comparator circuit according to claim 1, characterized by the fact that said follower circuit (M3, M4; M7, M8) is realized with n channel CMOS transistors.

8. Comparator circuit according to claim 1, characterized by the fact that said follower circuit (M3, M4; M7, M8) is realized with p channel CMOS transistors.

9. Comparator circuit according to claim 1, characterized by the fact to have a further inverter circuit (M11, M12) between said first follower circuit (M3, M4; M7, M8) and the first inverter (M1, M2; M5, M6).

Fig.1



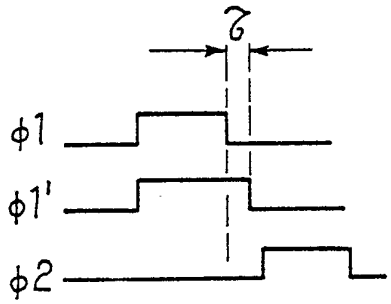
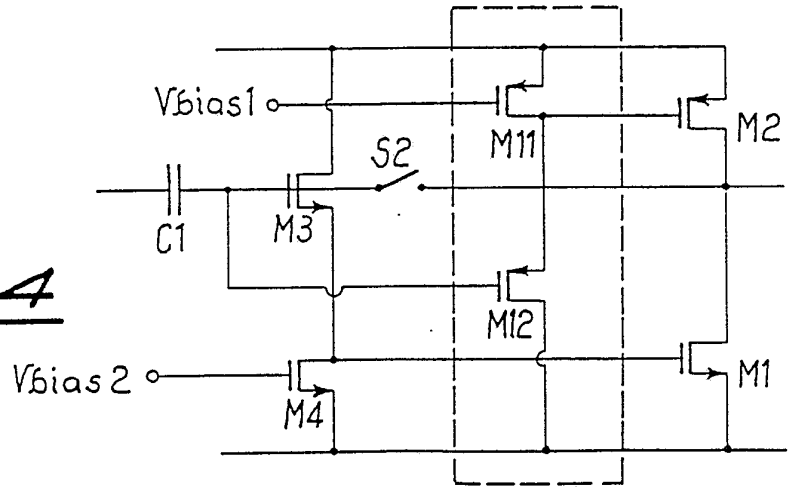


Fig.3

Fig.4



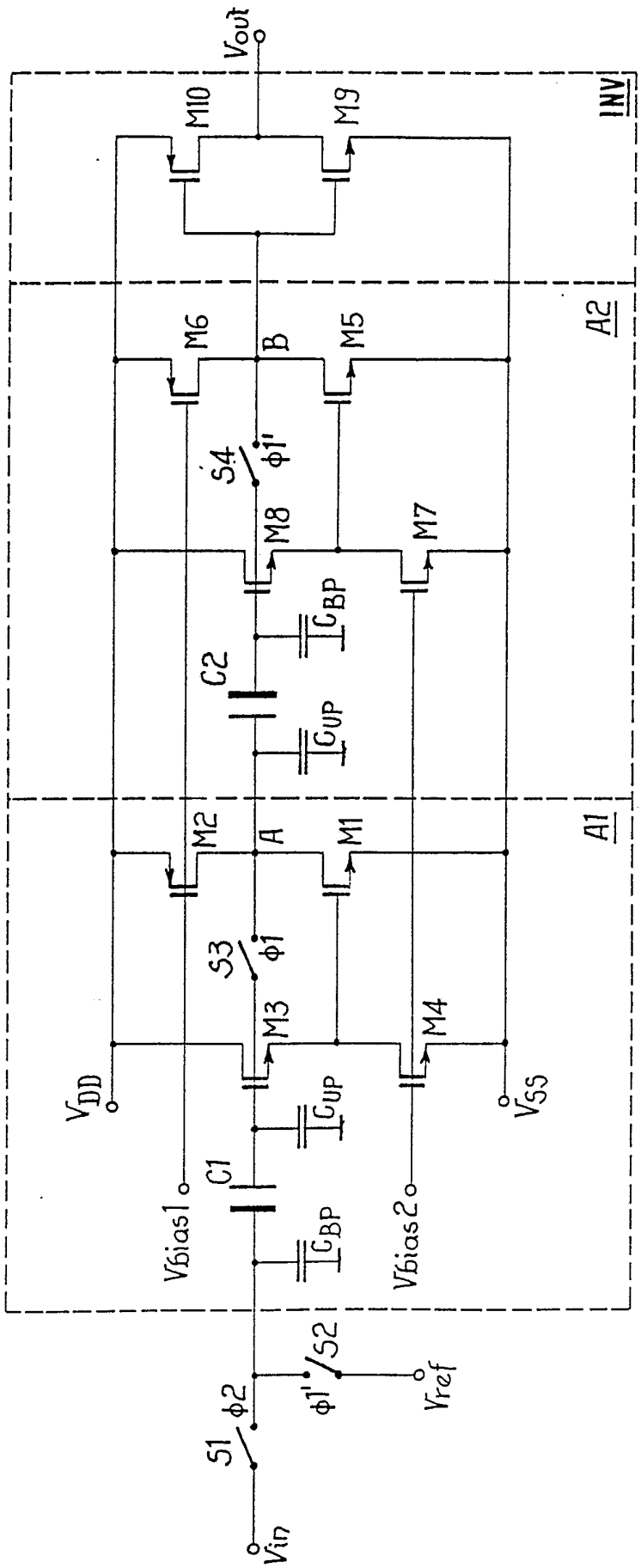

Vout
INV
M10
M9
A2
M6
B
M5
S4
φ1'
M8
M7
CBP
C2
CUP
A1
M2
A
M1
S3
φ1
M3
M4
VDD
VSS
CUP
C1
CBP
Vbias1
Vbias2
S2
φ1'
Vref
S1
φ2
Vin

Fig.2

INTERNATIONAL SEARCH REPORT

International Application No PCT/EP 91/00920

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl.5 H 03 K 5/24

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl.5	H 03 K H 03 F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
A	PATENT ABSTRACTS OF JAPAN, vol. 12, no. 158 (E-608)[3005], 13 May 1988, & JP-A-62 271 518, (SONY CORP) 25 November 1987, see the whole abstract	1-9
A	PATENT ABSTRACTS OF JAPAN, vol. 12, no. 101 (E-595)[2948], 2 April 1988, & JP-A-62 232 215 (SONY CORP.) 1 April 1986, see the whole abstract	1-9
A	EP-A-0 240 830 (K.K. TOSHIBA) 14 November 1987, see figures 1-21	1-9
A	US-A-3 676 702 (Mc GROGAN Jr.) 11 July 1972, see figure 3	1

° Special categories of cited documents : [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
30-08-1991	24 SEP 1991
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	Mme N. KUIPER

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. EP 9100920 SA 47403

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 13/09/91
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A- 0240830	14-10-87	JP-A- 62228172	07-10-87
		US-A- 4760287	26-07-88
US-A- 3676702	11-07-72	None	