July 21, 1964 T. A. BRENDLE 3,141,969

METHOD OF AND APPARATUS FOR PERFORMING COMPUTATIONS

Filed May 3, 1960 2 Sheets-Sheet 1

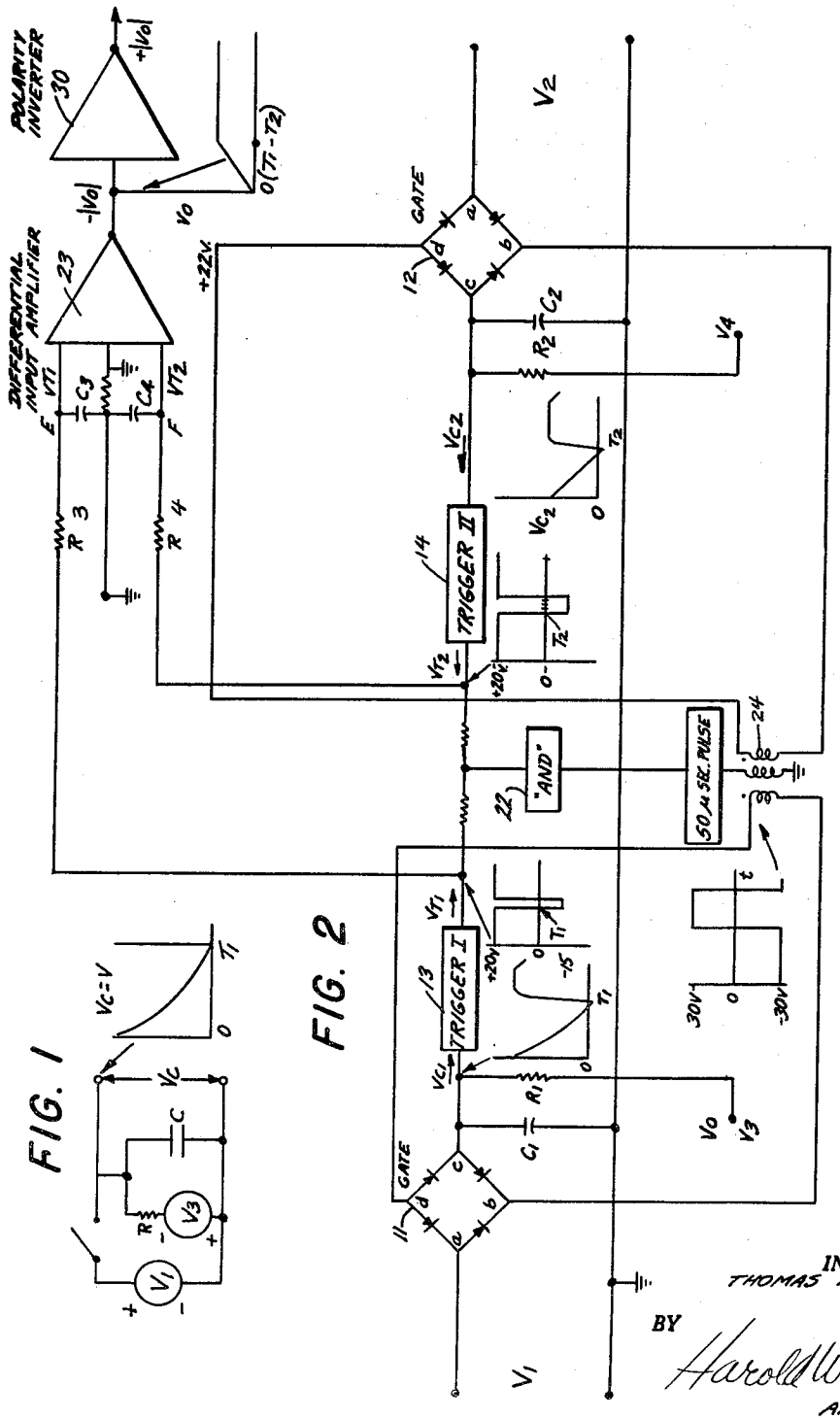

FIG. 1

FIG. 2

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FIG. 3

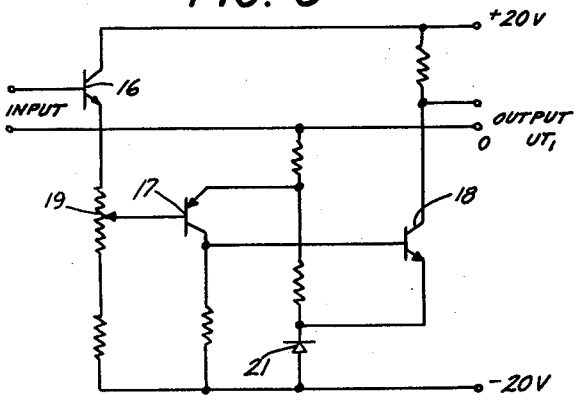


FIG. 7

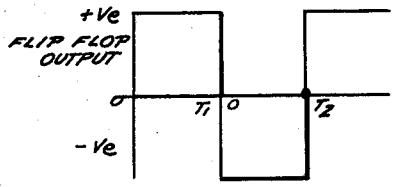
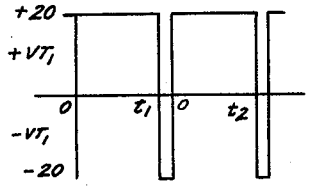


FIG. 6



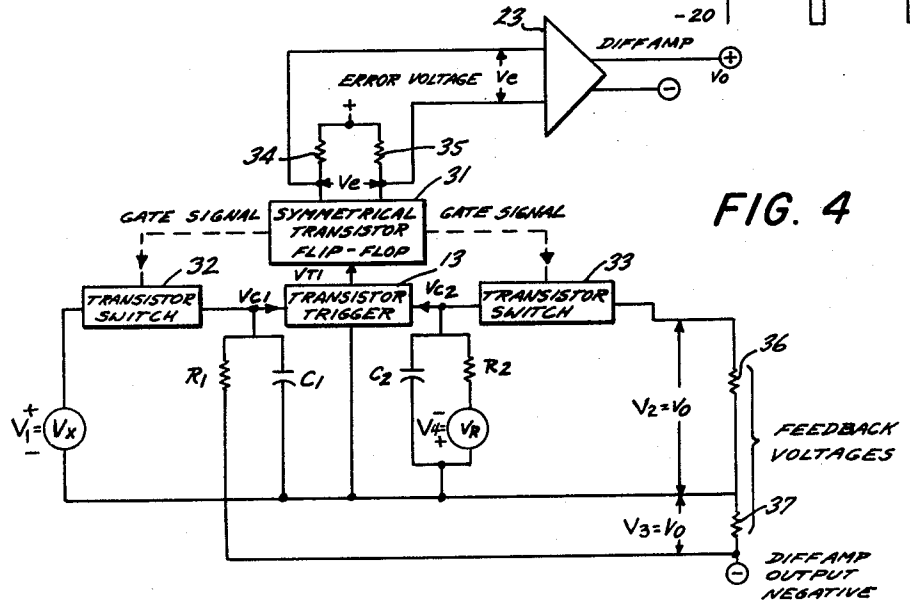


FIG. 4

FIG. 5

TRIGGER INPUT		TRIGGER OUTPUT VT1		FLIP FLOP	
Vc1	Vc2	ON	OFF	SWITCH 32	SWITCH 33
+	+		⊓	CLOSED	CLOSED
+	+		⊓	OPEN	CLOSED
ZERO	+	⊔		CLOSED	OPEN
ZERO	ZERO		⊓	CLOSED	CLOSED

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METHOD OF AND APPARATUS FOR PERFORMING COMPUTATIONS

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Filed May 3, 1960, Ser. No. 26,474
2 Claims. (Cl. 235—193)

This invention relates to a method of and apparatus for performing computations. More particularly this invention relates to a method of and apparatus for performing a multiplicity of different types of computations.

An object of this invention is to provide a method of and apparatus for performing a multiplicity of computations such as finding logarithms, extracting square roots, summations, divisions and multiplication in which time is utilized as an independent variable.

A further object of this invention is to provide a method of and apparatus for performing a multiplicity of different computations utilizing first order time constant networks.

Yet another object of this invention is to provide a method of and apparatus for duplicating the relationships which hold when the expression $V1/V3=V2/V4$ utilizing first order time standard networks and solving the general equation $V1(V2+V4)-V2(V1+V3)=0$.

Another object of this invention is to provide a method of and apparatus for duplicating the relationships which hold when the quantity $V1/V3$ equals the quantity $V2/V4$ as intervals of elapsed time and utilizing the intervals of elapsed time to perform a multiplicity of computations.

Still another object of this invention is to provide a method of and apparatus for performing a multiplicity of computations utilizing time standard networks arranged in an automatic, null balance closed loop system.

The method of duplicating the relationships which hold when the quantity $V1/V3$=the quantity $V2/V4$ utilizing this invention may include the steps of charging a voltage storage device on a transient between a voltage potential V1 and a voltage potential V3, and interrupting the transient charge when the voltage in the voltage storage device passes through an arbitrary value such as zero, at which instant the time interval of charge T of the voltage storage device equals

$$\frac{V1}{V1+V3}$$

the relationships desired to be duplicated.

The method of performing a multiplicity of analog computations with quantities represented by voltages V1, V2, V3 and V4 utilizing an elapsed time of charge T of a voltage storage device may include the steps of charging a first voltage storage device on a transient between a voltage potential V1 and a voltage potential V3, interrupting the transient charge as the voltage on said first voltage storage device passes through zero, at which instant the time interval of charge T1 of said first voltage storage device equals

$$\frac{V3}{V1+V3}$$

charging a second voltage storage device on a transient between a voltage potential V2 and a voltage V4, interrupting the transient charge as the voltage on said second voltage storage device passes through zero, at which instant the time interval of charge $T2$ equals

$$\frac{V4}{V2+V4}$$

comparing the time intervals T1 and T2 and simultaneously generating an error voltage equal to the difference between said time intervals and adjusting at least one of the voltages V1, V2, V3 and V4 until $T1=T2$ and the error voltage is zero whereby the value of the adjusted voltage equals the required function.

A basic computer circuit for duplicating the relationships which hold when $V1/V3=V2/V4$ may include a time standard network such as a first order RC (Resistor-Capacitor) or RL network (Resistor-Inductor) connected in series with a source of voltage or current V3. A switch or gate connects or disconnects an unknown voltage V1 across the capacitor C of an RC network, for instance. When the gate is closed the voltage V1 is transferred to the capacitor and when the gate is opened, the capacitor charges on a transient between the voltages V1 and V3. Electrical means connected to the time standard network interrupts the transient charge of the voltage Vc on the capacitor as the voltage Vc passes through an arbitrary value such as zero. At the instant the voltage Vc equals zero the time of charge T equals

$$R1C1 \log \frac{V3}{V1+V3}$$

the relationships to be duplicated.

A closed loop, null balance computer for making computations utilizing the relationship between the period or elapsed charging time and voltage existing across a first order RC network may include first and second basic computer networks R1C1 and R2C2 respectively connected in a null balance, pulse repetition system. Gating means connect and disconnect to first RC network, R1C1, with a source of voltage to charge the capacitor on a transient between the voltages V1 and V3. A voltage trigger comparator receive the output voltage Vc across the capacitor and interrupts the transient charge at the instant Vc equals zero. The elapsed time of charge T1 equals

$$RC \log \frac{V1}{V1+V3}$$

In a similar manner the second RC network R2C2 is charged on a transient between voltages V2 and V4. A voltage comparator trigger interrupts the transient charge as it passes through zero. The time of charge equalling

$$R2C2 \log \frac{V4}{V2+V4}$$

A differential amplifier connected to the voltage comparator triggers compares and generates an output voltage proportional to the difference between the time intervals T1 and T2 which equals the desired function of the voltages V1, V2, V3 and V4, and which when fed back into the networks R1C1 and R2C2 for at least one of the voltages V1, V2, V3 and V4 balances the computer, at which time $T1=T2$.

These and many other objects will become apparent from the following description of an embodiment of the invention taken in view of the following drawings in which:

FIG. 1 is an electrical schematic of the invention illustrating a basic computer network.

FIG. 2 is an electrical schematic of the invention showing a closed loop, null balance computer circuit.

FIG. 3 is an electrical schematic of a voltage comparator trigger used in the computer circuit shown in FIG. 2.

FIG. 4 is an electrical schematic of a modified version of the invention shown in FIG. 2 including a flip flop controlled switching system.

FIG. 5 is a chart illustrating the logic of the operation of the switching system of the computer shown in FIG. 4.

FIG. 6 is a diagram illustrating the waveform of the output voltage VT1 of the voltage comparator trigger shown in FIG. 4.

FIG. 7 is a diagram illustrating the output voltage of the symmetrical flip flop utilized in the computer circuit shown in FIG. 4.

The principle of operation of this invention is based on the condition that if $V1/V3$ equals $V2/V4$ then the following relations hold:

$$(1) \qquad \frac{V1}{V3}+1=\frac{V2}{V4}+1$$

$$(2) \qquad \frac{V1+V3}{V3}=\frac{V2+V4}{V4}$$

$$(3) \qquad \frac{V1+V3}{V1}=\frac{V2+V4}{V2}$$

which is the general computer equation

$$(4) \qquad V2(V1+V3)-V1(V2+V4)=0$$

A multiplicity of computations may be performed utilizing the aforementioned relationships. For instance the above relationships (1–4) may be utilized to find the square root of a quantity represented by a voltage Vx as follows:

Assuming $V1=Vx$, $V2=Vo$, $V3=Vo$ and $V4=Vr$ and inserting these values into (4) yields

$$(5) \qquad Vo(Vx+Vo)-Vx(Vo+Vr)=0$$

or

$$(6) \qquad Vo^2=VxVr$$

or

$$(7) \qquad Vo=\sqrt{Vx}$$

Vr being unity. This is the desired result.

Similarly many other computations such as multiplication, summations, finding logarithms etc. may be performed utilizing the relationships (1–4) by choosing the proper values for the quantities V1, V2, V3 and V4, once the relationships (1–4) have been duplicated.

Referring to FIG. 1 a basic computer network for duplicating the relationships which hold when $V1/V3=V2/V4$ is shown. The basic computer network comprises, for instance, a first order RC time standard network which comprises a resistor R, a capacitor C and an adjustable voltage source V3. An unknown voltage $V1$ is connected across the capacitor through a solid state switch or gate which is opened and closed by suitable means not shown.

The switch or gate is closed for a conduction interval just long enough for the voltage V1 to be transferred to the capacitor C at which time the voltage Vc across the capacitor C equals the voltage V1. At the end of the charging interval and when the switch gate is opened, a transient current I_t will start to flow in the RC time standard network. The differential equation describing the network when the switch is open is:

$$V1+V3=RI+1/C\int Idt$$

The transient current I_t is expressed as follows:

$$(8) \qquad I_t=\frac{V3}{R}e-\frac{T}{RC}$$

When VC, the voltage across the capacitor C, equals zero this reduces to the following:

$$(9) \qquad I_t=\frac{V3}{R}e-\frac{T}{RC}$$

substituting this value into (8) gives

$$(10) \qquad \frac{V3}{R}=\frac{V1+V3}{R}e-\frac{T}{RC}$$

solving for T,

$$(11) \qquad T=RC\log\frac{V3}{V1+V3}$$

since RC is a constant

$$(12) \qquad T=K\log\frac{V3}{V1+V3}$$

the exact relationship required.

Referring to FIG. 2 an analog computer circuit for performing a multiplicity of computations utilizing the relationships represented by the elapsed time of charge T1 of a first order RC time standard network is shown. The computer circuit comprises a pair of similar first order RC time standard networks R1C1 and R2C2 connected in a closed loop, null balance, pulse repetition system.

Before describing the circuit shown in FIG. 2 in detail the operation of the computer will first be briefly described.

As stated the principle of operation of the computer is based on certain relationships (Equations 1–3) which it has been shown can be duplicated electrically as the charging time interval T of a capacitor C arranged in a circuit as shown in FIGURE 1. By employing two networks R1C1 and R2C2 two respective charging time intervals T1 and T2 may be obtained. By employing voltages V1 and V3 with the network R1C1 the time interval required for the capacitor C1 to charge from the voltage V1 through zero is expressed as follows:

$$(13) \qquad T1=K\log\frac{V3}{V1+V3}$$

Similarly the charging time interval required for the capacitor C2 of the network R2C2 to charge from a voltage V2 through zero is expressed as follows:

$$(14) \qquad T2=K\log\frac{V4}{V2+V4}$$

A voltage comparator trigger **13** shown in detail in FIG. 3 interrupts the transient charge of the capacitor C1 at the instant the output voltage VC1 of the capacitor C1 reaches zero. At that instant the trigger trips "on" swinging its output voltage VT1 from a positive to a negative value. Similarly a voltage comparator trigger **14** trips "on" and interrupts the transient charge of the capacitor C2 at the instant the output voltage VC2 of the capacitor C2 reaches zero. When both of the triggers **13** and **14** have tripped on, an And circuit **22** pulses four-diode gates **11** and **12** to again transfer the voltages V1 and 2 to the networks R1C1 and R2C2. At this time the gates are opened and the charging time intervals T1 and T2 are again compared.

A differential amplifier **23** compares the trigger voltages VT1 and VT2 and generates a voltage Vo which is proportional to the difference between the respective time intervals T1 and T2. The voltage Vo thus generated is fed back into the networks for one or more of the voltages V1, V2, V3 or V4 in the Equations 13 and 14. Since cycling of the computer is continuous, the time intervals T1 and T2 will continue to be compared and the voltages Vo adjusted until T1 equals T2 and the closed loop computer circuit is balanced. At this time the voltage Vo reaches a steady state and equals the required function of the voltages V1, V2, V3 and V4. By feeding the voltage Vo in the networks R1C1 and R2C2 for one or more of the voltages V1, V2, V3 and V4 the computer may be utilized to perform a multiplicity of computations such as square root extraction, division, multiplication, summations and finding logarithms.

Referring now to FIG. 2 the input voltage V1 is applied to the network R1C1 across a capacitor C1 and ground through a conventional four-diode gate **11**. A resistor R1 is connected to a voltage source V3 and the capacitor C1 forming an RC time standard network R1C1. In a similar fashion an input voltage V2 is applied to the network R2C2 across a capacitor C2 and ground through a conventional four-diode gate **12**, while a resistor R2 is connected to a voltage source V4 and the capacitor C2 forming an RC time standard network R2C2.

As described in FIG. 1, the voltages V1 and V2 respectively are transferred to the capacitors C1 and C2 when the gates **11** and **12** open for the correct con-

duction intervals. The operation of the gates **11** and **12** is conventional and only the operation of gate **11** need be described in detail.

The gate **11** is a four-diode bridge having four corners **11***a*–**11***d*. The voltage V1 is connected to the opposite corners **11***a*–*c*, and is transferred to the capacitor C1 when a positive voltage pulse appears across the opposite corners **11***b* and *d*. During this interval the gate **11** is open. When the positive voltage across the corners **11***b* and *d* goes negative the gate **11** closes. The gate **12** is opened in a similar fashion to transfer the voltage V2 to the capacitor C2.

Upon a closing of the gates **11** and **12** respectively, the output voltages VC1 and VC2 of the capacitors C1 and C2 which are connected to identical voltage comparator triggers **13** and **14**, respectively, discharge on a transient toward zero. The voltage comparator trigger **13** which is essentially a high gain amplifier trips "on" and interrupts the transient discharge of the voltage VC1 as it passes through zero as is clearly shown in FIG. 2. An output voltage VT1 of the trigger **13** swings from a positive value to a negative value at the instant the voltage VC1 passes through zero. The elapsed time interval of charge T1 of the capacitor C1 is as expressed in Equation 13.

The voltage comparator trigger **14** trips "on" in a similar fashion, interrupting the transient charge of the voltage VC2 as it passes through zero as shown in FIG. 2. The charging time interval T2 of the capacitor C2 is as expressed in Equation 14. An output voltage VT2 of the trigger **14** also swings from a positive value to a negative value at the instant VC2 passes through zero.

The voltage comparator trigger **13** which is identical with the voltage comparator trigger **14** is shown in detail in FIG. 3 and comprises transistors **16**, **17** and **18**, interconnected and suitably powered to form a high gain amplifier which produces a constant amplitude pulse when the input voltage VC1 is negative or zero.

The output voltage VT1 of the trigger **13** is shown in FIG. 2 and is a high positive value during the interval when the capacitor C1 is discharging between V1 and zero. When the voltage VC1 is positive, the trigger is in an "off" state and the transistors **17** and **18** are nonconducting.

When the input voltage VC1, which is applied to the base electrode of the transistor **16**, passes through zero, the transistor **17** connected to the emitter of the transistor **16** through a trigger level resistor **19** is arranged to conduct. The exact value of voltage VC1 at which the transistor **17** conducts may be adjusted by varying the setting of the trigger level resistor **19**.

The transistor **18** remains cut off until the potential at the collector electrode of the transistor **17** exceeds the bias applied to the emitter electrode of the transistor **18** by a level diode **21**. This occurs as VC1 passes through zero volts. At that instant the transistor **18** conducts, tripping the trigger **13** to the "on" state. The output voltage VT1 is instantaneously changed from a positive value such as +20 v. to a negative value such as a −20 v. for example. The output voltage VT1 remains at a constant negative value until the gate **11** is opened and the voltage V1 is again transferred to the capacitor C1.

As stated the operation of the triggers **13** and **14** is identical, differing only in the trigger input voltage (VC1 or VC2) employed and the output voltage derived (VT1 or VT2).

The output voltages VT1 and VT2 are equal in amplitude and opposing when the triggers **13** and **14** are both "on" or "off," and the voltage across the trigger outputs is zero. When the triggers **13** and **14** are in different states (either "on" or "off"), the voltages VT1 and VT2 are adding and the polarity of the resultant voltage across the trigger outputs is ±40 volts depending upon which of the triggers **13** or **14** trips first as determined by the length of the respective time intervals T1 and T2.

The output voltages VT1 and VT2 of the triggers **13** and **14**, respectively, are connected to a conventional "and" circuit **22** and to a differential amplifier **23** to complete the closed loop, balanced network computer circuit.

The "And" circuit **22** is a coincidence circuit having two or more inputs to each of which is applied a pulse of common polarity such as VT1 and VT2 and a single output. A pulse appears at the output of the "And" circuit **22** only when identical pulses (VT1 and VT2) are applied to both inputs. Thus when VT1 and VT2 are both negative, the "And" circuit **22** pulses both gates **11** and **12** through a transformer **24** to open the gates and again transfer the voltages V1 and V2 to the capacitors C1 and C2, respectively. The complete cycle of the voltages VC1 and VC2 is illustrated in FIG. 2.

Referring to FIG. 2 the output voltage VT1 of the trigger **13** is applied to the differential amplifier **23** and across a capacitor C3 to ground through an input R3 while the output voltage VT2 of the trigger **14** is applied to the differential amplifier **23** and across a capacitor C4 to ground through an input resistor R4. During conditions of balance, that is when the opposing voltages VT1 and VT2 which are equal in amplitude are both positive or negative, the voltage VEF across the capacitors **26** and **28** (points E and F in FIG. 2) is zero and will remain zero until one of the triggers **13** or **14** trips and the triggers are in an opposite state. When this occurs, because of the capacitors C3 and C4, the voltage VEF will rise as an exponential function of time, its polarity indicating which trigger **13** or **14** has tripped.

The differential amplifier **23**, which may be of conventional design and need not be described in detail, has a very high common mode rejection ratio and conducts only during the intervals when VT1 and VT2 are opposite in polarity producing an output voltage V*o* which is a linear function of the voltage VEF. A polarity inverter **30** such as a pair of center grounded dropping resistors or a grounded cathode vacuum tube circuit, for instance, is connected to the differential amplifier and reverses the polarity of V*o*, thus providing both a negative and positive V*o* output.

As stated, the output voltage V*o* of the differential amplifier is a linear function of the voltage VEF and it rises until the triggers **13** and **14** are again in the same state at which time the voltage VEF returns to approximately zero. The rate of increase of the output voltage V*o* of the differential amplifier **23** is determined by the time constants R3C3 and R4C4 of the input impedance to the differential amplifier **23**. The amplitude of the voltage V*o* is thus determined by the length of time the voltage comparator triggers **13** and **14** are in different states.

Since the triggers **13** and **14** are both in the "off" state when the voltages VC1 and VC2 are positive (the instant the gates **11** and **12** are closed) and reverse to the "on" state only when the voltages VC1 and VC2 pass through zero, the amplitude of the voltage V*o* at any instant is proportional to the difference between the respective charging times T1 and T2 that it takes for the capacitors C1 and C2 to charge between the voltages V1 and V3 and V2 and V4, respectively. That is:

$$(15)\quad Vo=K(T1-T2)=Ko\left(\frac{V3}{V1+V3}-\frac{V4}{V2+V4}\right)$$

When both of the triggers **13** and **14** have tripped "on" the "And" circuit **22** pulses the gates **11** and **12**, resetting them and commencing a new cycle.

The adjusted voltage V*o* is fed back into the networks R1C1 and R2C2 for one or more of the voltages V1, V2, V3 or V4 depending upon which computation is to be performed. As the computer circuit cycles the voltage VEF is reduced to approximately zero, at which time the time intervals T1 and T2 are approximately equal. Uti-

lizing the relationships which hold when $V1/V3=V2/V4$ and the circuit of FIG. 2 a multiplicity of computations can be performed by choosing the proper designations and values for the voltages V1, V2, V3 and V4.

Square Root Extractions

To extract the square root of a number represented by a voltage Vx for instance the closed loop, null balance, computer network is arranged as follows:

(16) $V1=Vx$ the unknown voltage
(17) $V2=+Vo$
(18) $V3=-Vo$
(19) $V4=-Vr$ (reference voltage)

Assuming $Vx=9$, Vo equals zero initially, R1C1 equals R2C2 and the gates **11** and **12** are open, the operation of the circuit is as follows:

The capacitors C1 and C2 will charge to the voltages Vx and Vo, respectively, at which time an "And" circuit output pulse will be discontinued, closing the gates **11** and **12**. The voltage comparator triggers **13** and **14** will remain in the "off" state until the input voltages VC1 and VC2 pass through zero. The times required for the capacitors C1 and C2 to charge to zero are T1 and T2, respectively where

(20) $$T1=R1C1\log\left(\frac{Vo}{Vo+Vx}\right)$$

or

$$K\log\left(\frac{Vo+1}{Vx}\right)$$

and

(21) $$T2=R2C2\log\left(\frac{Vr}{Vr+Vo}\right)$$

or

$$K\log\left(\frac{1+Vr}{Vo}\right)$$

Since the quantity K in both equations is equal, $T1=T2$ reduces to

(22) $$\frac{Vx+Vo}{Vo}=\frac{Vo+Vr}{Vr}$$

which reduces to

(23) $$Vo=\sqrt{VxVr}$$

and when

$$Vr=1$$

(24) $$Vo=\sqrt{Vx}$$

or

$$Vo=\sqrt{V1}$$

Note that Vr may be any value desired to give the proper amplification factor for Vo.

In the example, since Vx is 9 and Vo is zero or at a minimum operation voltage for the differential amplifier **23**, T1 is greater than T2. The voltage comparator trigger **14** will trip instantaneously and the voltage VT2 will go negative. At that instant, the voltage VEF will start from zero and increase exponentially as a function of time until the trigger **13** trips and the voltage VT1 goes negative.

The output voltage Vo of the differential amplifier because of the time constants R3C3 and R4C4 increases linearly during the time interval ($T1-T2$) to a value of 3 volts. At the instant the voltage VT1 goes negative the "And" circuit **22** will pulse the gates **11** and **12** through the transformer **24** to again open the gates and charge the capacitors C1 and C2, respectively, for a next cycle of operation.

During the next cycle of operation, the circuit will be balanced, T1 equals T2, and the voltage Vo will remain constant. It is to be noted that by varying the time constant of the input impedance to the differential amplifier **23**, the slope and thus the amplitude of the voltage Vo may be varied. In this event the computer circuit will continue to cycle and compare the respective time intervals T1 and T2 until the voltage Vo is adjusted to the proper value and the time intervals T1 and T2 are made equal. At that instant the computer circuit is balanced and Vo equals the required function of the voltages V1, V2, V3 and V4.

In this instance the time constants R3C3 and R4C4 of the input impedance to the differential amplifier **23** are chosen so that the slope of the output voltage Vo is such that the time intervals T1 and T2 are made equal and the computer circuit is balanced in one cycle of operation. Thus, the respective charging time intervals T1 and T2 are simultaneously compared and made equal to provide a symmetric, null balance closed loop, computer circuit.

Division or Ratio

To perform the computation of division such as Vx/Vy using the computer circuit of FIG. 2, assume the following:

(25) $V1=Vx$
(26) $Vy=V3$
(27) $Vr=V2$

and

(28) $Vo=V4$

The operation of the circuit is the same as for extracting square roots, and

(29) $$T1=R1C1\log\frac{Vy}{Vg+Vx}$$

and

(30) $$T2=R2C2\log\frac{Vr}{Vo+Vr}$$

when the respective voltages VC1 and VC2 pass through zero. Adjusting the voltage Vo until T1 equals T2 and solving for Vo, yields

(31) $$\frac{Vr}{Vo+Vr}=\frac{Vy}{Vy+Vx}$$

which reduces to

(32) $$Vo=\frac{Vx}{Vy}\text{ or }V1/V3$$

the desired function. The differential amplifier **23** increases the output voltage Vo linearly during the interval when the triggers **13** and **14** are in opposite states to the correct value so that the computer network is again balanced. During the next cycle of operation T1 equals T2, the voltage VEF remains zero and Vo is not changed.

Summations

To find the sum of the quantities $Vx+Vy+Vz$, for example, using the null balanced computer circuit of FIG. 2, assume the following:

(33) $V1=Vx$
(34) $V2=Vo$
(35) $V3=Vy$

and

(36) $V4=-Vz$

Again solving for T1 and T2 when the voltages VC1 and VC2 pass through an arbitrary value of voltage VA where $VA<(Vo-Vz)$

(37) $$T1=R1C1\log\frac{A}{Vx+Vy}$$

and

$$T2=R2C2\log\frac{A}{-Vz+Vo} \tag{38}$$

which when

$$T1=T2 \tag{39}$$

reduces to

$$Vo=Vx+Vy+Vz \tag{40}$$

or

$$Vo=V1+V3+V4$$

the desired relationship. Again the differential amplifier **23** responds to the difference between the time intervals T1 and T2 to adjust the voltage V*o* and balance the RC time standard networks R1C1 and R2C2. It is to be noted that the transient voltages VC1 and VC2 across the capacitors **C1** and **C2**, respectively, need not be interrupted at the instant they reach zero but may be interrupted at some arbitrary value such as VA in this instance.

Obviously, the above circuit can be utilized to find the sum of a greater number of figures by using the voltage V*o* in two or more of the balanced networks in a progressive relationship.

Multiplication

To multiply the quantities V*x* and V*y* for instance using the null balanced computer network of FIG. 2, assume the following:

$$V1=Vx \tag{41}$$
$$V2=Vr \tag{42}$$
$$V3=Vo \tag{43}$$

and

$$V4=Vy \tag{44}$$

Solving for T1 and T2 when the voltages VC1 and VC2 pass through zero

$$T1=R1C1\log\frac{Vo}{Vx+Vo} \tag{45}$$

and

$$T2=R2C2\log\frac{Vy}{Vy+Vr} \tag{46}$$

Making V*r* unity and $T1=T2$ gives

$$Vo=VyVx \tag{47}$$

which is the desired result. It is to be noted that when $Vx=Vy$, the circuit may square the unknown quantity. The differential amplifier **23** responds to the difference between the time intervals T1 and T2 and simultaneously adjusts the voltage V*o* to the correct value to balance the RC time standard networks R1C1 and R2C2.

Referring now to FIG. 4, a simplified schematic of a modified version of the computer circuit of FIG. 2 is shown. The modified computer circuit includes the RC time standard networks R1C1 and R2C2, the operation of which is identical to that previously described. The voltages VC1 and VC2 in this instance, however, are connected to a single voltage comparator trigger **13**. The voltage comparator trigger **13** is set to trip from the "off" to the "on" state when either of its two inputs VC1 or VC2 is zero or negative and resets when both of its inputs VC1 and VC2 are positive. As before described the output VT1 of the trigger **13** is either positive or negative. The output voltage VT1 is shown in FIG. 5 as a series of sharp pulses which are determined by the voltages VC1 and VC2 charging from a positive value through zero. The pulsating output voltage VT1 of the voltage comparator trigger **13** is connected to a conventional symmetrical flip flop **31** which in turn controls a pair of switches **32** and **33**. The switches **32** and **33** may be transistorized and act as SPDT switches. They are placed in opposite positions, switch **32** being closed and switch **33** open or vice versa. The switches **32** and **33** are pulsed from one position to the other by the symmetrical flip flop **31** which responds to the pulses in the output voltage VT1 of the voltage comparator trigger **13**. The logic of the operation of the circuits as shown in FIG. 6 illustrates the manner in which the switches are opened and closed by the flip flop **31** as the voltages VC1 and VC2 charge through zero from the voltages V1 and V2, respectively.

A differential amplifier **23** having the proper input impedance as previously described is connected to the symmetrical flip flop **31** across a pair of collector resistors **34** and **35**. The output voltage of the flip flop **31** is of constant amplitude either positive or negative which is determined by the state of voltage comparator trigger **13**.

The differential amplifier **23** is arranged to operate on the average voltage output V*e* of the symmetrical flip flop **31**. Thus when the time intervals T1 and T2 are equal, the average value of the error voltage V*e* is zero and the output voltage V*o* of the differential amplifier **23** remains constant. When the time intervals T1 and T2 are different, the differential amplifier **23** will adjust the value of the voltage V*o* accordingly until T1 equals T2 and the error voltage V*e* is zero. The polarity of the output voltage V*o* of the differential amplifier **23** is inverted across the dropping resistors **36** and **37**.

As shown, the circuit of FIG. 4 is arranged to take the square of a quantity V*x*. In this instance assume the following:

$$V1=Vx \tag{48}$$
$$V2=Vo \tag{49}$$
$$V3=0 \tag{50}$$

and

$$V4=Vr \tag{51}$$

In operation with the power off the transistor switches **32** and **33** are closed transferring the voltages V1 and V2 to the capacitors **C1** and **C2**, respectively. The instant the transistor switches **32** and **33** are energized, the symmetrical flip flop **31** by its inherent feedback trips on to open one of the switches, for instance, switch **32** and close switch **33**. At that instant the voltage VC1 of the capacitor **C1** will start on a transient charge toward the voltage V*o*. As the voltage VC1 passes through zero the voltage comparator trigger **13** will trip "on" to pulse the symmetrical flip flop **31** and reverse the position of the switches **32** and **33**. That is, the switch **32** now closes and the switch **33** opens.

At that instant, both inputs VC1 and VC2 to the voltage comparator trigger **13** are positive and the voltage comparator trigger **13** will reset to the "off" state. At that time, however, the voltage VC2 of the capacitor **C2** is charging from the voltage V*o* toward zero and at the instant the voltage VC2 reaches zero the voltage comparator trigger **13** will again fire "on" to pulse the symmetrical flip flop **31** and again reverse the state of the switches **32** and **33** to initial a next cycle of operation.

Each time the trigger **13** pulses the flip flop **31**, an output voltage V*e* of the flip flop **31** swings between a positive and negative value resulting in a pulsating output as shown in FIG. 7.

Since the waveform of the voltage V*e* is symmetrical the average value of the error voltage V*e* is zero when the time interval T1 and T2 are equal and varies as a function of the difference between the respective time intervals T1 and T2.

A differential amplifier **23** which has a high common mode rejection ratio operates on the average value of the error voltage V*e* to produce a voltage V*o*, which is applied to the dropping resistors **36** and **37** and inserted into the computer circuit as voltages V2 and V3, in this instance. The circuit will cycle and continuously compare the time intervals T1 and T2 until the differential

amplifier adjusts the voltage Vo to the value which forces the error voltage Ve to zero. At this time the following equations hold:

$$T1=T2 \tag{52}$$

or

$$\frac{Vo}{Vx+Vo}=\frac{Vr}{Vo+Vr} \tag{53}$$

Solving Equation 53 yields,

$$Vo=\sqrt{Vx} \tag{54}$$

which is the required function of the input voltage Vx. Thus, in the modified closed loop, null balance computer circuit of FIG. 4 the time intervals T1 and T2 are determined separately and then compared to produce an error voltage Ve equal to the difference between the respective time intervals T1 and T2. In the null balance closed loop computer circuit of FIG. 2 the gates **11** and **12** are closed at the same instant allowing the capacitors **C1** and **C2** to charge toward zero simultaneously to determine the respective time intervals T1 and T2.

It is to be noted, however, that the circuit of FIG. 4 may also be arranged to perform the computations of division, multiplication and summation by the proper selection and insertion of voltages into the circuit for the values V1, V2, V3 and V4. Further, the circuit of FIG. 2 as well as FIG. 4 may be utilized to find logarithms by disconnecting the differential amplifier in each case and using the error voltage Ve or VEF directly.

A preferred embodiment of the invention has been shown, but obviously numerous alterations and modifications may be made in the light of the above teachings. Accordingly, it is to be expressly understood that the spirit and scope of the invention is to be limited only by the spirit and scope of the appended claims.

I claim:

1. A closed loop null-balance computing circuit for generating an output voltage Vo as a function of input voltages V1, V2, V3, V4, at least one of the latter voltages being $\pm Vo$, said computing circuit comprising:

(a) two like input circuits, one receiving V1 and V3 as input voltages and delivering output voltages VT1, the other receiving V2 and V4 as input voltages and delivering output voltage VT2, the following organization of the first input circuit also applying to the second input circuit with V2 substituted for V1, V4 for V3, and VT2 for VT1, said first input circuit including:

($a1$) a gate receiving at its input V1,

($a2$) means for applying spaced gating pulses to said gate for gating V1 through,

($a3$) a time constant network receiving as energizing potential V3 and the through-gated V1, and producing output potential which is substantially V1 while a gating pulse is applied to said gate, and which relaxes from V1 towards V3 upon closure of the gate,

($a4$) a trigger receiving the latter output signal as trigger input signal, for generating VT1 in form of a two-level trigger output voltage pulse train, the trigger output voltage transferring from the first level to the second level when the trigger input voltage attains a predetermined value while relaxing towards V3, and retransferring to said first level as the trigger input voltage recovers to substantially V1,

said computing circuit further comprising:

(b) pulse generating means responsive to coincidence of second levels of VT1 and VT2 for generating said gating pulses and delivering them via the mentioned pulse applying means to the input circuit gates,

(c) differential integrating means receiving VT1 and VT2 as input voltages and building up Vo as the time integral of their difference, and

(d) means for applying $\pm Vo$ to at least one of said input circuits to constitute it at least one of the four voltages V1, V2, V3, V4, whereby to force the first level durations of VT1 and VT2 substantially to coincidence, whence Vo assumes a value corresponding to the computed result.

2. A computer circuit according to claim 1, wherein the gating pulse generating means produces gating pulses having uniform width and having separation that is variable in accordance with the time difference of first level durations of VT1 and VT2.

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