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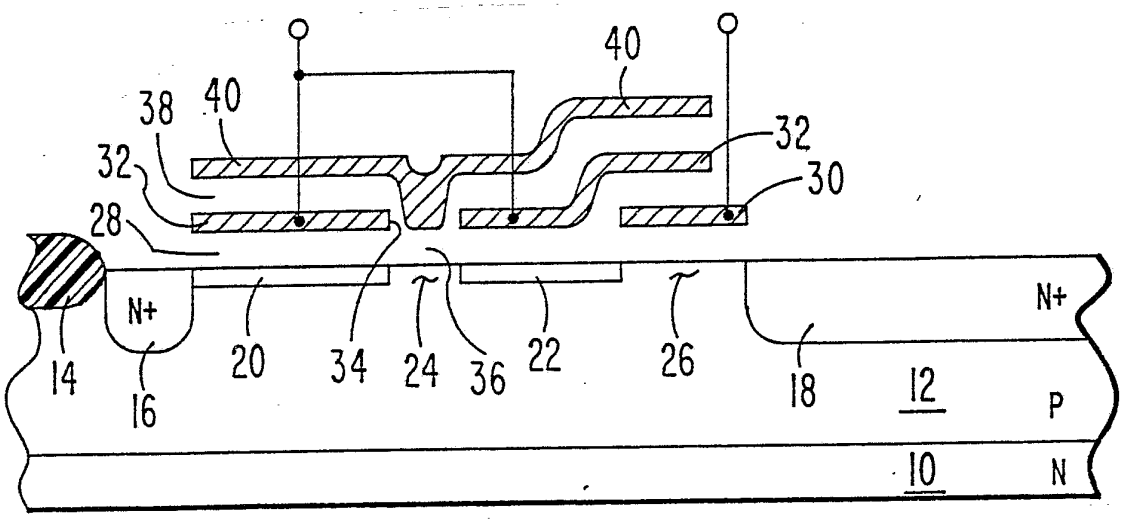

(57) Abstract

A novel, nonvolatile floating-gate memory structure wherein the floating-gate member (40) is substantially shielded from the substrate (10) by the control-gate member (32). The control-gate member (32) is provided with a pair of apertures (34, 48), through which portions of the floating-gate member (40) extend. One aperture (48) serves as means for 'writing' and 'erasing', while the other aperture (34) serves as means for 'reading'.

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AN ELECTRICALLY ALTERABLE, NONVOLATILE FLOATING GATE MEMORY DEVICE

This invention relates, in general, to semiconductor memory devices and more particularly, to electrically alterable, nonvolatile floating-gate memory devices.

The microprocessor-based systems, as well as the related arts, have long required electrically alterable, read-only memory (EAROM) elements that were nonvolatile, and many devices incorporating such elements have, to some extent, filled this need. However, as the computer arts have become more complex in nature and have required higher speeds and greater capacity, there now exists the need for a high-density memory device that may be easily programmed or "written" and, as the occasion arises, to reprogram ("erase" and "rewrite") the device in the field. To this end, devices are presently available to design engineers that exhibit nonvolatile characteristics but, as will be discussed, they have inherent shortcomings that are overcome by the subject invention.

One such device resides in the family of Floating Gate Avalanche Metal Oxide Semiconductor (FAMOS) devices. The advantage of this type of device resides in the fact that it is independent of any outside current to maintain the stored information in the event that power is lost or interrupted. Since this device is independent of any outside power, there is also no need to refresh the device, which feature results in a significant savings in power.

The floating-gate family of devices usually has source and drain regions of a given conductivity type, formed in a substrate of the opposite conductivity type, at the surface thereof. Between the source and drain regions, and on the surface of the substrate, a gate structure is formed by first forming a thin, insulating layer of gate oxide on the surface of the substrate followed by the formation of a conductive layer (the floating gate). This is followed by a second insulating layer which completely surrounds the floating gate and insulates it from the remainder of the device. A second

conductive layer (usually referred to as the control gate) is formed over the second insulating layer (in the region of the floating gate) to complete the gate structure. Such devices are exemplified in U. S. Letters Patent 3,500,142 issued to D. Kahng on March 10, 1970. The major drawback of these devices resides in the fact that high fields are required to produce the necessary avalanche breakdown in order for charge to be placed on the floating gate. Further, to erase the charge appearing on the floating gate, the entire device must be provided with a transparent window so that it may be flooded with energy in the ultraviolet or x-ray portion of the spectrum. Thus, it is extremely difficult to erase a single "word" without erasing all the charge on the device, then requiring that the entire device be completely reprogrammed. Further, the erasing step required an extremely long period of exposure time, of the order of about 30 to 45 minutes, with the device or chip removed from the equipment.

In recent years, the art has progressed to the point where nonvolatile floating-gate read-only memory devices have been produced which are electrically alterable. One such memory cell has been described in detail in an article entitled "16-K EE-PROM Relies on Tunneling for Byte-Erasable Program Storage" by W. S. Johnson, et al., ELECTRONICS, February 28, 1980, pp. 113-117. In this article, the authors describe a "Floating-Gate Tunnel Oxide" structure wherein a cell, using a polycrystalline silicon (polysilicon) floating-gate strucutre, is charged with electrons (or holes) through a thin oxide layer positioned between the polycrystalline silicon gate and the substrate using the Fowler-Nordheim tunneling mechanism. An elevation view of a typical device is described and shown in FIGURE 1 of the article, wherein the floating-gate member represents the first polycrystalline silicon level. However, by using this type of structure wherein the floating gate (the first-level polycrystalline silicon since it is closest to

the substrate) is covered by and insulated from a second polycrystalline silicon level, an excessively high floating gate-to-substrate capacitance is produced. A certain area of floating gate is necessary in order to maintain close coupling between the first and second polycrystalline silicon levels. It has been found that some manufacturers etch away portions of the first polycrystalline silicon level, in order to reduce the capacitance between the floating gate and the substrate, without substantially reducing the capacitance between the first and second polycrystalline silicon levels.

A novel configuration of floating-gate memory device has been described wherein the floating gate comprises a second polycrystalline silicon level rather than the traditional first polycrystalline silicon level, in order that the second-level polycrystalline silicon floating gate be shielded from the substrate. The first-level polycrystalline silicon is provided with an aperture, and the second-level floating gate is made to extend through the aperture so that only a relatively small area of the second-level floating gate is coupled to the substrate for the write and erase functions. Such a structure reduces the otherwise high floating gate-to-substrate capacitance.

The nonvolatile memory cell of the present invention is provided with a shielded floating-gate structure using the Fowler-Nordheim tunneling mechanism to charge the floating gate. The layer shielding the floating gate from the substrate covers the entire channel region except where it provides a "read window" through which the floating gate is coupled to the channel region. The net result is an improved read efficiency.

In the drawing:

FIGURE 1 is a plan view of an electrically alterable, nonvolatile floating-gate memory device made in accordance with the teaching of the present invention;

FIGURE 2 is a cross-sectional view of the novel memory device taken along line 2-2 of FIGURE 1; and

FIGURE 3 is a cross-sectional view of the novel memory device taken along line 3-3 of FIGURE 1.

FIGURES 1, 2 and 3 show a P type well 12 formed in an N type substrate 10. Source and drain regions 16 and 18, respectively, are formed at the surface of the P type well 12 with conductivity-modifying ions of a type opposite to that of the P type well 12. Within the P type well 12, and positioned between the source and drain regions 16 and 18, respectively, is a channel region comprising source-extension portion 20 and floating-source portion 22, each of which have conductivity modifiers therein sufficient to form N-type depletion regions. The depletion-region portions 20 and 22 are separated by a read-channel portion 24, while the depletion-region portion 22 and the drain region 18 are separated by a word line-channel portion 26. At the surface of the P type well 12 are field oxide regions 14, which define the limits of the active regions consisting of source and drain regions 16 and 18, respectively, depletion-region portions 20 and 22, and channel portions 24 and 26. A polycrystalline silicon (polysilicon) layer 30, the word line 30, is positioned above the channel region, so as to be aligned with word-line channel portion 26, and is insulated therefrom by a layer 28 of silicon oxide having a thickness of about 1000 Angstroms. In the drawing, the cross-hatching for the insulating layers existing between the word line 30, P type well, etc. has been omitted for the sake of clarity. Positioned above the remainder of the channel region is a polycrystalline silicon layer 32, which serves as a shield and control gate and has a read-window aperature 34 therein aligned with the read-channel portion 24. Shield or control-gate member 32 is separated and insulated from the surface of the P type well 12 by means of the insulating layer 28, which has a thickness of about 1000 Angstroms. Typically, this layer 28 may be silicon oxide. A polycrystalline silicon layer 40, representing the floating-gate layer, is positioned above the polycrystalline silicon control-gate member 32 and has

a portion thereof extending through the read-window aperture 34. The floating-gate layer 40 is insulated from the control gate member 32 by, for example, a silicon oxide insulating layer 38 having a thickness of about 2500 Angstroms, while the extended portion of the floating-gate layer 40, through the read-window aperture 34, is insulated from the surface of the channel region by an insulating layer 36 having a thickness of about 1000 Angstroms. The area where the floating-gate layer 40 couples to the substrate 10 (at the P type well 12), through the read-window aperture 34, is herein referred to as the read window.

As shown in FIGURE 1, the surface of the control-gate member 32 is shown generally to be "U" shaped, with the opening of the "U", as defined by the read-window aperture 34, representing the read window. An aperture 48, together with an N type doped region 50 (FIGURE 3), represents a "write" and "erase" window.

As shown in FIGURE 1 (symbolically shown in FIGURE 3), a contact 42 is the means for electrically connecting a metal program line 44 to the polycrystalline silicon control-gate member 32 so that, when the voltage shown in the accompanying table is applied to the line 44, the same voltage will be applied also to the control-gate member 32. A contact 56 is the drain contact providing an electrical, ohmic contact between the metal line 46 and the doped drain region 18. As shown in FIGURE 3, the metal line 44, as well as the metal drain line 46, is separated and insulated from the floating-gate layer 40 by means of an insulating layer 54 having a thickness of about 6000 Angstroms.

The write/erase functions are provided by means of the aperture 48 located in the shield member 32, with the aperture 48 positioned over the write/erase N type doped region 50. The floating-gate layer 40 has a portion that extends through the aperture 48 in shield member 32 and is insulated from the surface of the channel

region by means of an insulating layer 52, which has a thickness of about 90-120 Angstroms.

The following table shows the potentials which are applied to the various elements of the device herein described, in order to erase, write and read any charge on the floating-gate layer 40. In the table, the various potentials shown under the columns entitled "ERASE", "WRITE", and "READ" are applied to those elements shown under the column entitled "ELEMENT".

ELEMENT	ERASE	WRITE	READ
Drain (18)	+20v	0v	+5v
Source (16)	+20v	0v	+0v
Control gate (32)	0v	+20v	+5v
P-Well (12)	0v	0v	0v
Word Line (30)	+20v	+20v	+5v

Thus, as shown in the above table, to "erase" the device, a 20 volt signal is initially applied to the drain region 18, the source region 16 and the word line 30, while the control-gate member 32 and the P type well 12 are maintained at 0 volts. This "erase" cycle will place a positive charge on the floating-gate layer 40, which puts the read-channel portion 24 in a low-threshold (high-conduction) state. In the high-conduction state, with the read-channel portion 24 inverted and the depletion-region portions 20 and 22 conductive, it should be obvious now that there will be no electron flow between the source region 16 and the drain 18 unless the proper "read" voltage is applied to the word line 30, in order to invert the word line-channel portion 26. This provides a convenient method of checking the device to determine if it is, in fact, erased. To "write", a 20 volt signal is applied to the control-gate member 32 and the word line 30, and 0 volts is applied to the drain and source regions 18 and 16, respectively, and the P type well 12. This, in effect, places a negative charge on the floating-gate layer 40, which places the read-channel portion 24 in a high-threshold (low-conduction) state. In the low-conduction state, the negative charge on the floating-gate layer 40 prevents the read-channel portion 24 from being inverted, and no conduction can take place between the depletion-region portions 20 and 22 or between the source and drain regions 16 and 18, respectively. To "read" the device, that is, to determine whether the cell is in a high-threshold or a low-threshold state, 5 volts is placed on the drain region 18, the program line 44 and

the word line 30, while the source region and the P type well 12 are placed at 0v. The indication of conduction will signify the presence of a low-threshold (high-conduction) state.

While the present device has been described in terms of multiple layers of polycrystalline silicon, it should not be so limited. It should now be obvious to those skilled in the art that various other conductive layers, such as layers formed of refractory metals, refractory metal silicides, etc., or any combination thereof, may be used in place of the polycrystalline silicon layers 30, 32 and 40.

CLAIMS:

1. A floating-gate memory device including a body of semiconductor material of a first conductivity type having first and second doped regions of a second conductivity type formed in the semiconductor body at the surface thereof, the first and second doped regions spaced from each other to define a channel region therebetween in the semiconductor body for supporting current flow between the first and second doped regions, a first conductive layer insulated from the body of the semiconductor material, and a second conductive layer positioned over both the channel region and the first conductive layer and insulated therefrom, the first conductive layer having a first aperture therein into which the second conductive layer extends, characterized in that:

a first portion of the channel region, adjacent the first doped region (16), has a pair of depletion-type regions (20, 22) formed in the semiconductor body (12) at the surface thereof and spaced from each other to define a first channel portion (24) therebetween;

a second aperture (34) is disposed in the first layer (32) of polycrystalline silicon, and is aligned with the first channel portion (24), a portion of the second conductive layer (40) extending into said second aperture (34);

a second channel portion (26) is disposed adjacent the second doped region (18) and occupys the remainder of the channel region; and

a third conductive layer (30) is positioned over and insulated from the second channel portion (26).

2. The floating-gate memory device of Claim 1 wherein:

the first and second doped regions (16, 18) are source and drain regions, respectively; and

one (20) of the pair of depletion regions (20, 22) is adjacent to the source region (16).

3. The floating-gate memory device of Claim 2 wherein:

the first conductive layer (32) is a control gate;

the second conductive layer (40) is a floating gate; and

the third conductive layer (30) is a word line.

4. The floating-gate memory device of Claim 3 wherein:

the control gate (32) and the word line (30) are each insulated from the surface of the channel region by a layer (28) of silicon oxide having a thickness of about 1,000 Angstroms; and

the portion of the floating gate (40) that extends into the second aperture (34) in the control gate (32) is insulated from the channel region by a layer (36) of silicon oxide having a thickness of about 1,000 Angstroms.

5. The floating-gate memory device of Claim 4 wherein:

the body (12) of semiconductor material is a well region (12) of the first conductivity type formed in a substrate (10) of the second conductivity type.

6. The floating-gate memory device of Claim 5 wherein:

the material of the first, second and third conductive layers (32, 40 and 30) is selected from the group consisting of doped polycrystalline silicon, a refractory metal and a refractory metal silicide.

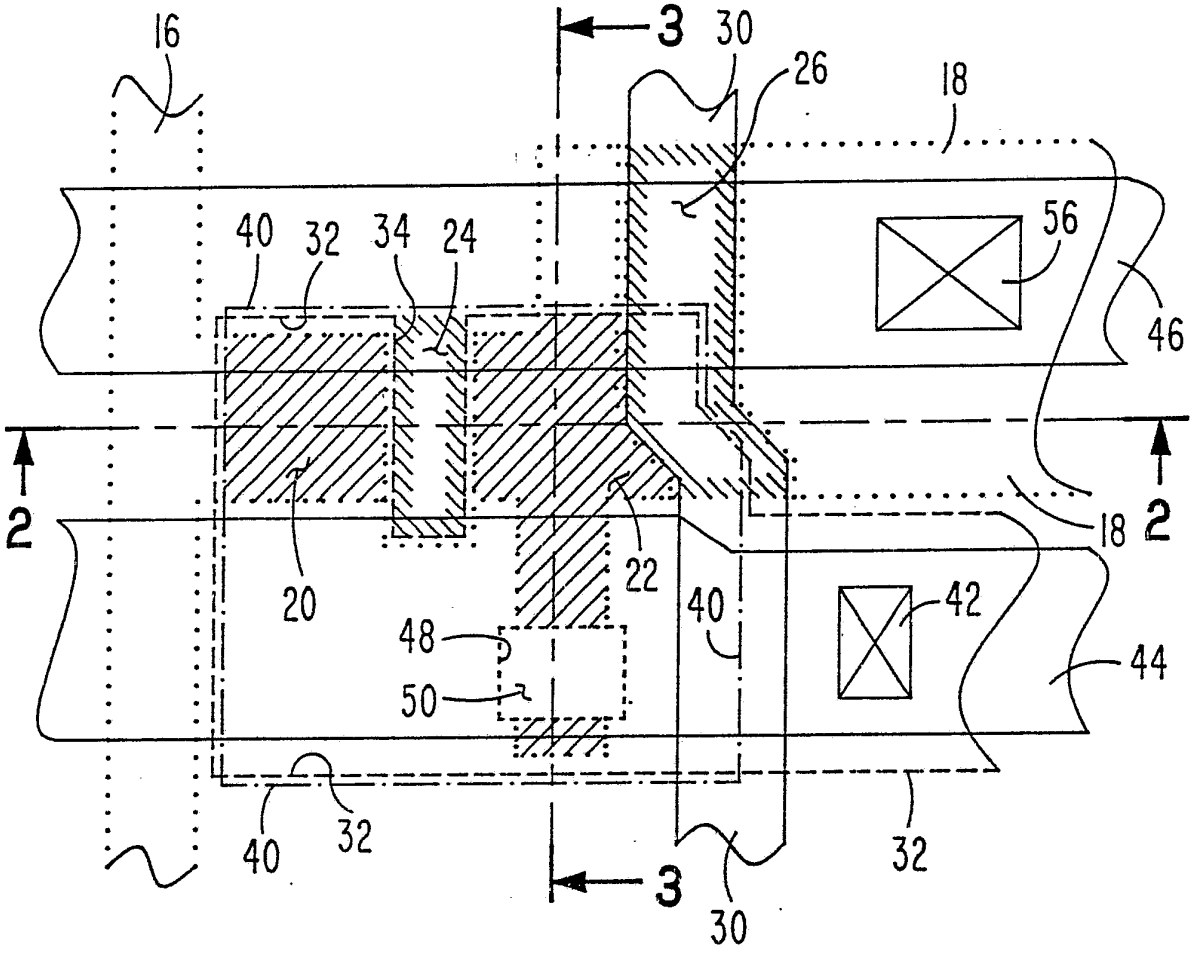

Fig. 1

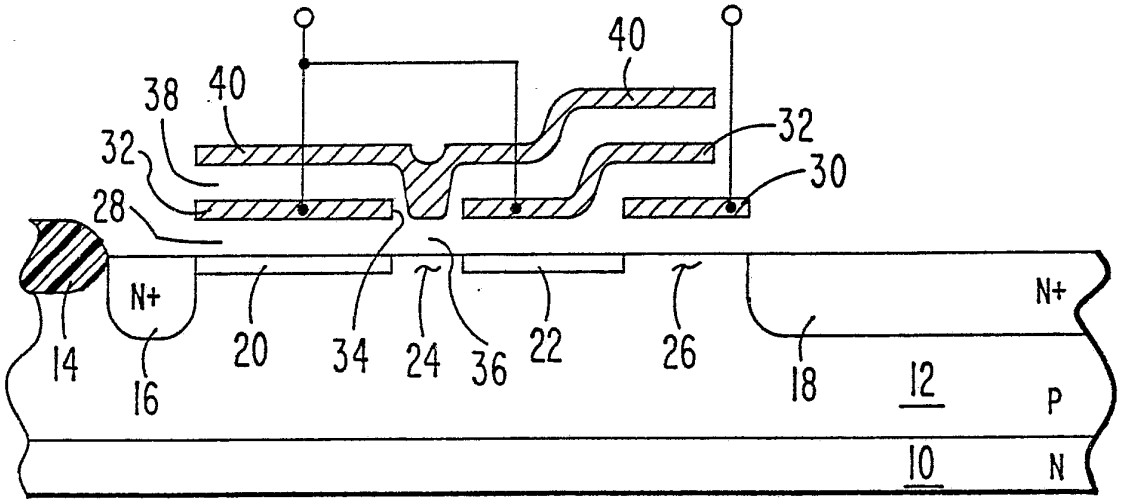

Fig. 2

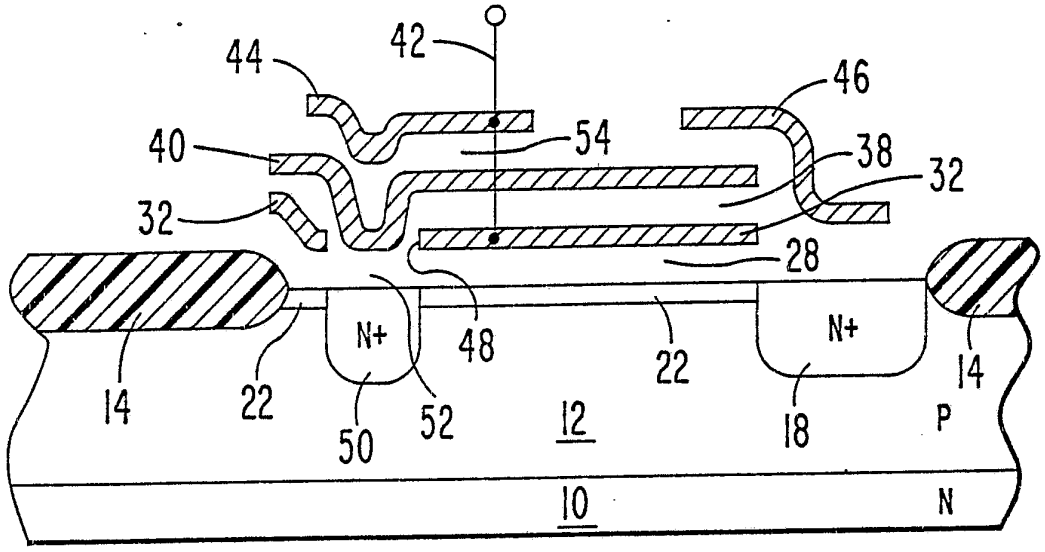

Fig. 3

INTERNATIONAL SEARCH REPORT

International Application No PCT/US83/00295

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.[3] H01L 29/78, 27/02; G11C 11/34
U.S. CL. 357/23VT, 41; 365/185

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
US	357/23VT, 41 465/185

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	US, A, 4,099,196 (SIMKO) 4 July 1978	
A,P	US, A, 4,336,603 (KOTECHA ET AL) 22 June 1982	
A	US, A, 4,203,158 (FROHMAN-BENTCHKOWSKY) 13 May 1980	
A	US, A, 3,825,946 (FROHMAN-BENTCHKOWSKY) 23 July 1974	

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IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
23 May 1983	07 JUN 1983
International Searching Authority [1]	Signature of Authorized Officer [20]
ISA/US	Gene Munson