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SIGNAL SLICER CIRCUIT

Filed March 30, 1965

FIG. 1

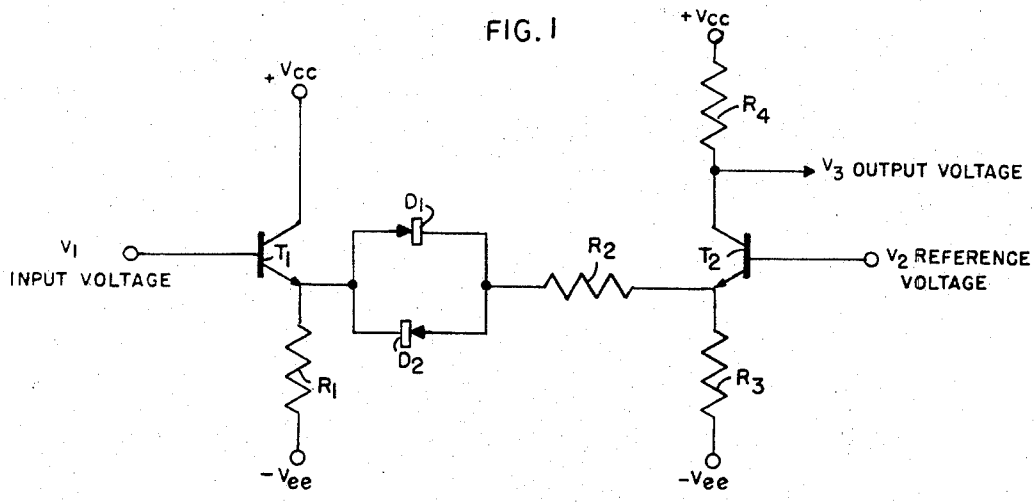
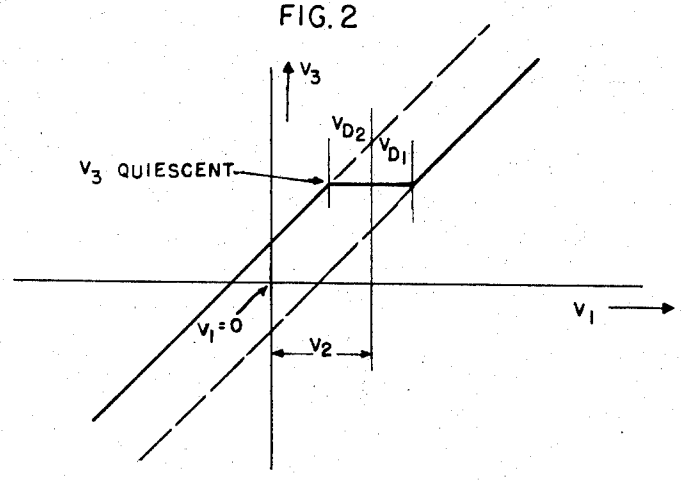


FIG. 2



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SIGNAL SLICER CIRCUIT

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ABSTRACT OF THE DISCLOSURE

A signal slicer circuit is disclosed. The emitters of two transistors are coupled through a pair of oppositely poled parallel connected diodes. An input voltage is applied to the base of the first transistor and a reference voltage is applied to the base of the second transistor. The output voltage is taken at the collector of the second transistor. The magnitude and polarity of the reference voltage determines what portion of the input signal will be removed or sliced out. Any portion of a given input signal can be removed by selecting the proper reference voltage.

This invention relates to a signal slicer circuit, and more particularly to a transistorized circuit for slicing or eliminating a portion of a signal.

For any one of numerous reasons it may be necessary or desirable to eliminate a portion of an input signal. The most common reason for eliminating part of an input signal is noise suppression. Noise suppression or elimination is generally accomplished by the use of a clipper circuit. This type of circuit clips-off the peaks of the input signals. If one wishes to remove some portion other than the peaks of a given input signal, he can not utilize the standard clipper circuit. A signal slicer circuit must be used.

I have invented a new transistorized circuit that is capable of removing any portion of a given input signal. The portion of the signal removed is determined by a reference voltage.

Therefore, an object of my invention is to provide a signal slicer circuit.

Another object of my invention is to provide a circuit for attenuating a signal over a small region in the vicinity of a fixed reference voltage.

A further object of my invention is to provide a circuit for eliminating any predetermined portion of a signal.

The above mentioned and other objects will be evident from the following detailed description when read with the accompanying drawing wherein:

FIG. 1 shows a preferred embodiment of my invention and;

FIG. 2 is a graph showing the relationship of output voltage to input voltage.

Referring now to FIG. 1, the emitter of a first transistor T_1 is coupled to the emitter of a second transistor T_2 by means of a pair of parallel connected, oppositely poled, diodes D_1 and D_2 and a resistor R_2. A bias voltage of $-V_{ee}$ is applied to the emitter of transistor T_1 through a resistor R_1 and to the emitter of transistor T_2 through a resistor R_3. Resistors R_1 and R_3 have the same value of resistance. A bias voltage of $+V_{cc}$ is applied to the collectors of both transistors T_1 and T_2. An input voltage V_1 is applied to the base of transistor T_1 and the output voltage V_3 is taken at the collector of transistor T_2. The resistor R_4 is a load resistor. A reference voltage V_2 is applied to the base of transistor T_2. Diodes D_1 and D_2 are identical diodes.

If reference voltage V_2 is some positive value, as indicated in FIG. 2, output voltage V_3 will remain fixed at the

value labelled V_3 quiescent in FIG. 2 so long as input voltage V_1 remains within the range

$$V_2-V_{D2}<V_1<V_2+V_{D1}$$

(where V_{D1} and V_{D2} are the forward voltage drops of diodes D_1 and D_2 respectively). Output voltage V_3 remains at this fixed value because diodes D_1 and D_2 do not conduct when input voltage V_1 lies within the above given range.

Now should input voltage V_1 become more negative than V_2-V_{D2}, current will flow through diode D_2. Its magnitude will be

$$\frac{[V_2-V_{D2}]-|V_1|}{r_{D2}+R_2}$$

and its direction will be from the emitter of transistor T_2 toward the emitter of transistor T_1 (r_{D2} is the slope of the I–V curve for D_2). This current will be drawn out of the collector supply of transistor T_2 causing a change in output voltage V_3.

$$\therefore V_3=V_3 \text{ quiescent}-\frac{[V_2-V_{D2}]-|V_1|}{r_{D2}+R_2}R_3$$

Similarly, should input voltage V_1 become more positive than V_2+V_{D1}, current will flow through diode D_1. Its magnitude will be

$$\frac{|V_1|-[V_2+V_{D1}]}{r_{D1}+R_2}$$

and its direction will be from the emitter of transistor T_1 toward the emitter of transistor T_2 (r_{D1} is the slope of the I–V curve for diode D_1). This current ultimately flows into the collector supply of transistor T_2 causing a change in output voltage V_3

$$\therefore V_3=V_3 \text{ quiescent}+\frac{|V_1|-[V_2+V_{D1}]}{r_{D1}+R_2}R_3$$

From the above discussion and from FIG. 2 it is apparent that as input voltage V_1 increases from a negative value to a positive value, output voltage V_3 follows the input voltage in a linear fashion until the magnitude of the input voltage approaches the magnitude of reference voltage V_2. As input voltage V_1 increases from V_2-V_{D2} to V_2+V_{D1}, output voltage V_3 remains constant. When input voltage V_1 exceeds V_2+V_{D1}, output voltage V_3 again follows the input voltage in a linear fashion.

Reference voltage V_2 can have any value. It can be negative, zero or positive. The magnitude of the reference voltage is, of course, limited by the power handling capabilities of the circuit components and the maximum value of the input voltage.

If reference voltage V_2 is zero, my slicer will take out a slice of input voltage V_1 that is symmetrical about the Y-axis of FIG. 2. Similarly, a negative reference voltage will cause the output voltage to remain constant when the input voltage lies within the range of V_2+V_{D2} to V_2-V_{D2}. Thus, my slicer circuit can remove any given portion of an input signal by merely changing the value of the reference voltage applied to the base of transistor T_2. It should also be noted that the input voltage can be either a direct or an alternating voltage.

The foregoing disclosure relates to a preferred embodiment of my invention. Numerous modifications or alterations may be made thereto without departing from the spirit and scope of the invention as set forth in the appended claims.

What is claimed is:

1. A signal slicer circuit comprising: a first active element having first, second and third electrodes; a second active element having first, second and third electrodes;

means to apply an input signal to said second electrode of said first active element; means to apply a reference voltage to said second electrode of said second active element; output terminal means connected to the third electrode of said second active element; a first diode having an anode and a cathode; a second diode having an anode and a cathode; means to connect said anode of said first diode and said cathode of said second diode to said first electrode of said first active element; a resistor; means to connect said resistor between said first electrode of said second active element and said anode of said second diode and said cathode of said first diode; means to apply a positive bias voltage to said third electrodes of both said first and second active elements; and means to apply a negative bias voltage to said first electrodes of both said first and second active elements.

2. A signal slicer circuit comprising: a first transistor having at least a base electrode and an emitter electrode; a second transistor having an emitter electrode, a base electrode and a collector electrode; means to apply an input signal to said base electrode of said first transistor; means to apply a reference voltage to said base of said second transistor; means to derive an output signal from said collector electrode; first and second oppositely poled parallel connected diodes; a resistor; means to connect said diodes between said emitter of said first transistor and said resistor; and means to connect said resistor between said diodes and said emitter of said second transistor.

3. A signal slicer circuit comprising: a first transistor having an emitter electrode, a base electrode and a collector electrode; a second transistor having an emitter

electrode, a base electrode and a collector electrode; means to apply an input signal to said base electrode of said first transistor; means to apply a reference voltage to said base of said second transistor; a source of negative bias voltage; a first resistor connected between said negative bias voltage and said emitter of said first transistor; a second resistor connected between said negative bias voltage and said emitter of said second transistor; a positive bias voltage; means to connect said positive bias voltage to said collector of said first transistor; a third resistor connected between said positive bias voltage and said collector of said second transistor; output terminal means connected at the junction of said third resistor and said collector of said second transistor; a first diode having an anode and a cathode; a second diode having an anode and a cathode; a fourth resistor having first and second terminals; means to connect said anode of said first diode and said cathode of said second diode to said emitter of said first transistor; means to connect said cathode of said first diode and said anode of said second diode to said first terminal of said fourth resistor; and means to connect said second terminal of said fourth resistor to said emitter of said second diode.

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