United States Patent

Harwood

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[54] CREDIT CARD FOR INFORMATION VERIFICATION SYSTEMS

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[52] **U.S. Cl.** **340/149,** 340/166

[51] **Int. Cl.** **H04q 3/00,** H04q 5/00

[58] **Field of Search** ..... 340/166, 149, 149 A

[56] **References Cited**

UNITED STATES PATENTS

3,202,980	8/1965	Stone	340/324.1
3,387,265	6/1968	Smeiman	340/149 A
2,914,746	11/1959	James	340/149 A
3,154,761	10/1964	O'Gorman	340/149 A
3,430,200	2/1969	Barney	340/149 A
3,508,031	4/1970	Cooper	340/149 A

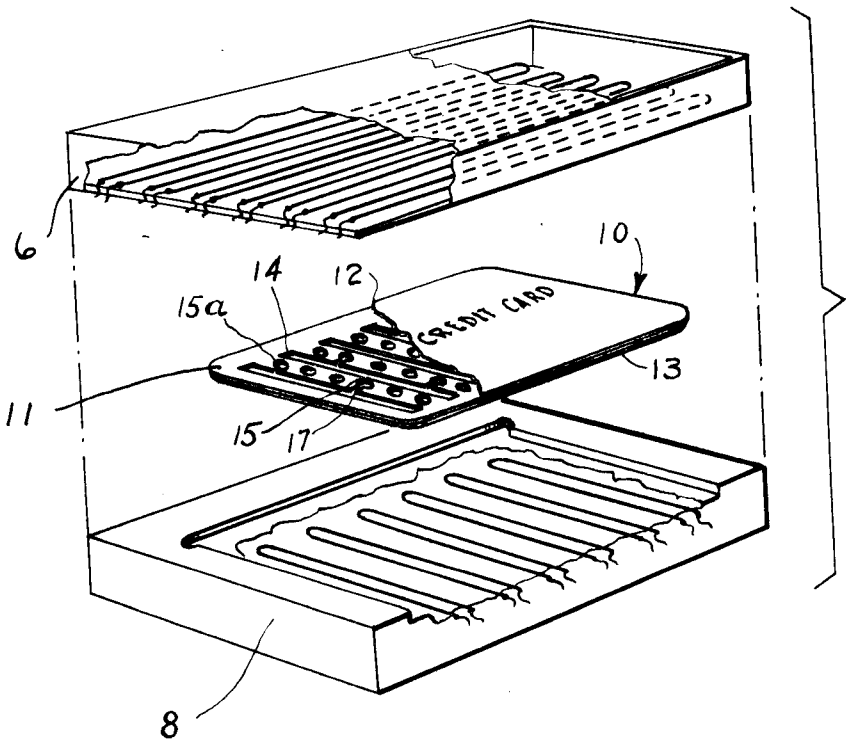
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[57] **ABSTRACT**

A memory unit comprising a pair of printed circuit boards, each board containing a plurality of loop circuits. The circuits on one board are formed parallel with a given X-axis and the circuits on the other board are parallel with a given Y-axis. The two boards are disposed in close proximity to each other so that their respective circuits effectively intersect and are adapted to receive between them a metallic plate having formed therein rows of holes some of which are connected to apertures by means of slots in the plate according to the encoded information desired. The holes not so connected relative to the slotted holes inhibit voltage induction at the intersections of the X- and Y-loop circuits where the unslotted holes are located.

2 Claims, 8 Drawing Figures



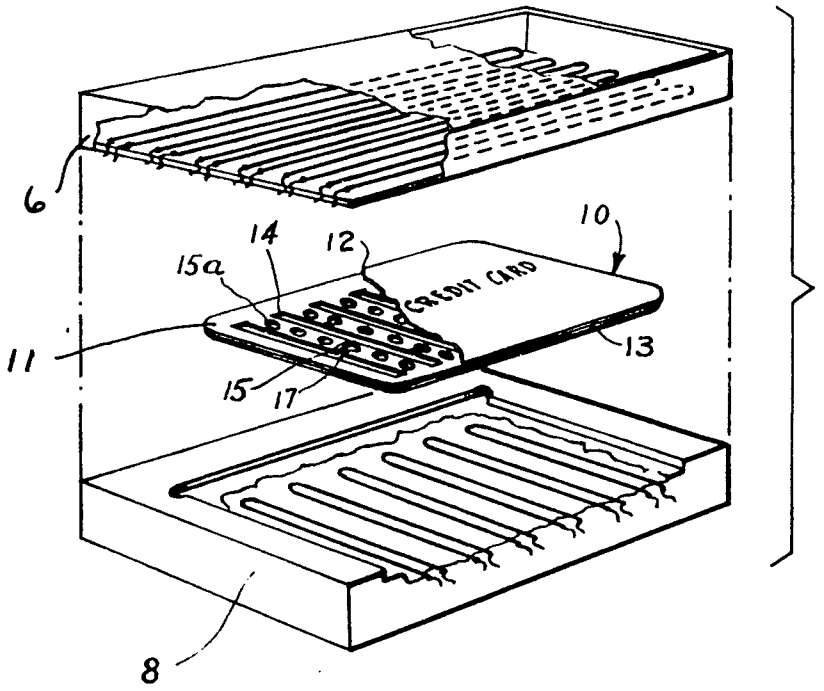


Fig. 1

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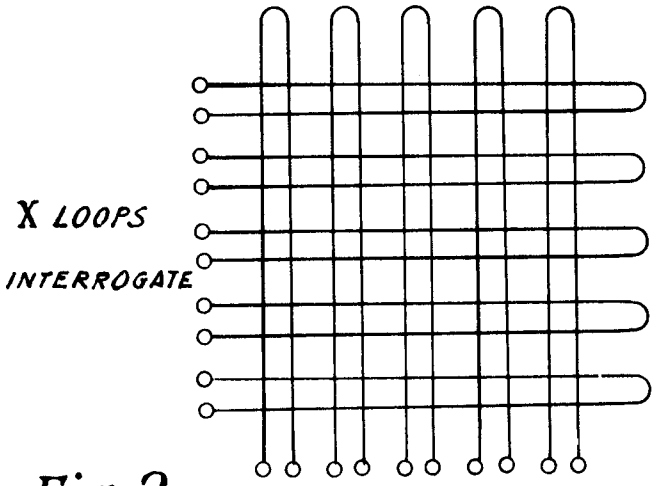


Fig. 2

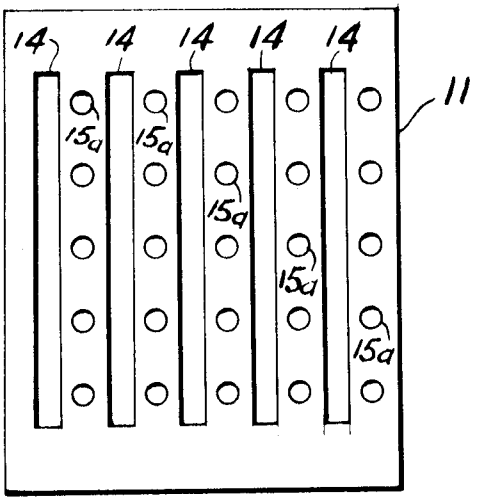


Fig. 3

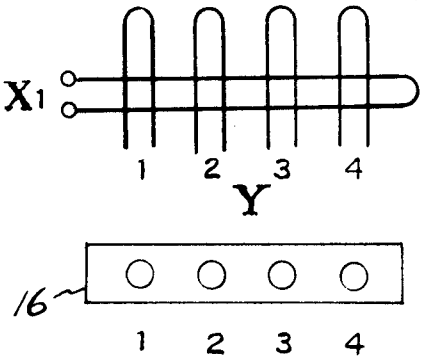


Fig. 4

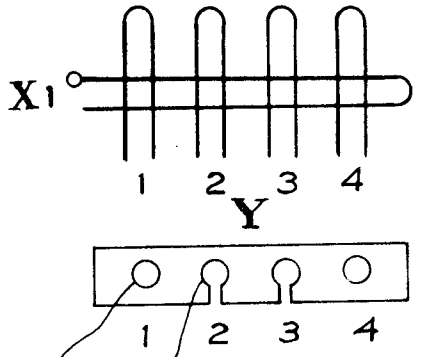


Fig. 5

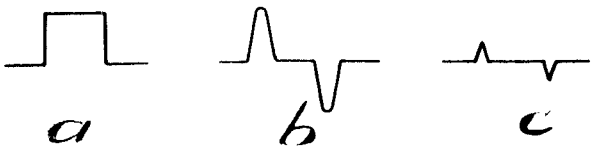


Fig. 6

CREDIT CARD FOR INFORMATION VERIFICATION SYSTEMS

This invention relates to computing systems having memory components and in particular to the memory components themselves as a device for storing information evoked for desired application in the presence of selected interrogation signals.

A memory component is contemplated which permits of a technique for scanning and reaching out encoded information which is presented, by way of example, on identification, credit or other type cards used to give information of value to persons responsible for clearing others for security, extending credit, etc. The cards themselves are uniquely configurated and are adapted for use especially with the memory unit disclosed herein.

In general the memory unit functions electromagnetically to afford information on command. The information is scanned by a series of signal pulses placed in a set of separate, printed circuits each corresponding to a binary number. The readout signals occur on a similar array of separate, printed circuits which are adapted to be electromagnetically coupled to the first set of circuits depending on the encoded information stored in the card disposed proximate the two sets. Circuitry including amplifiers, a strobe device for detecting the desired level of output and a buffer register for comparing the produced information for particular application purposes are used to process the output of the memory but constitute no part of the present invention.

One object of the invention is to provide a memory unit adapted to scan and read out information which is otherwise secure.

There follows a more detailed description of one embodiment of the invention taken in conjunction with the accompanying drawing, in which

FIG. 1 is a perspective view of the assembly the principal components of which are shown separated for purposes of clarification.

FIG. 2 is a diagrammatic view of the coupled grid circuits comprising separate interrogate and read loops.

FIG. 3 illustrates the encoded metal lamination of the encoder card.

FIG. 4 is an explanatory diagram showing an encoder strip and loop output circuits with a single interrogate loop.

FIG. 5 is a similar explanatory diagram illustrating an encoder strip having a different code pattern from that shown in FIG. 4.

FIGS. 6*a*, *b*, and *c* are interrogate and read out pulse diagrams.

Referring to the drawings, the memory unit assembly consists essentially of interrogate printed circuit board **6** and read printed circuit board **8**, there being disposed between the boards an encoded card **10**. The printed circuits of the board **6** are separate loops parallel to the X-axis whereas the loop circuits on the board **8** are parallel to the Y-axis as shown diagrammatically in FIG. **2**. Where the circuits are disposed proximate to each other, as shown in FIG. **2**, it is seen that an inductive coupling is provided at the intersection of each X-loop and Y-loop enabling a current pulse through the X-loops to induce a voltage in the Y-loops. The X-loops may be regarded as interrogate loops and the Y-loops as read loops. Multiple X-loops are provided where it is necessary to read out more than one binary number.

The encoded card **10** is in the form of a metal, nonmagnetic plate **11** having suitable conductive properties disposed intermediate outer layers **12** and **13** fabricated of nonconductive material. Thus, the encoded information cannot be detected by unaided visual scanning and the outer laminations provide electrical insulation between and across the boards. There is formed in the plate a series of elongated apertures **14** and between the apertures rows of holes selectively connected by slots **17** to an adjacent aperture (FIG. **1**). The slotted holes **15** and the unslotted holes **15***a* are distributed in a pattern according to the information content required. The purpose of the metal plate **11** between the printed circuit boards is to selectively inhibit or permit the coupling of the X-loops and the Y-loops at the intersections by means of the unslotted and slotted holes in the plate.

To explain the operation of the memory, a single X-loop intersecting with four Y-loops are formed on printed circuit boards with a metal plate **16** having a row of four unslotted holes formed at the intersections and disposed intermediate the boards. In FIG. **4** the plate is shown separated from the boards for reasons of clarity. If a current is passed through the X-loop little or no voltage will be induced in the Y-loops as the metal plate will serve as a shorted secondary turn dissipating most of the energy. If, however, the holes at positions **2** and **3** are slotted to the edge of the plate, see FIG. **5**, the shorted turn is removed at these positions. When this X-loop is interrogated, voltage will be induced in Y-loops **2** and **3** but not in **1** and **4**. In this manner binary information is generated, a "one" being represented by a slotted hole and a "zero" by an unslotted hole.

If one row of holes is considered as a storage location in which one binary number is stored, then a current pulse applied to the interrogate loop associated with this location will cause the number to be read out in parallel on the read loop output circuits.

There is shown in FIG. **6***a* an interrogate pulse of approximately 1 microsecond in duration. In FIG. **6***b* is shown a relatively high-amplitude read pulse "one" and in **6***c* a relatively low-amplitude read pulse "zero."

The number of interrogate and read loops is chosen to suit the requirements of the system of which the memory unit is a component. Various embodiments of the invention may be effected by persons skilled in the art without departing from the scope and principle thereof as defined in the appended claims.

What is claimed is:

1. A credit card, comprising:

a substantially flat, nonconductive body portion; and

a substantially flat metallic strip, disposed in a coded area discretely within the body portion of said card, having a plurality of longitudinally shaped slots forming parallel conductors therebetween with segments selectively formed of different resistance values, said parallel conductors including a plurality of apertures disposed along their length, said apertures being selectively open circuited and short circuited.

2. A credit card, comprising:

a substantially flat nonconductive body portion; and

at least one substantially flat, metallic strip disposed in a coded area discreetly within the body portion of said card, having spaced-apart flat conductors with segments selectively formed of different resistant values, and a plurality of spaced-apart apertures, said apertures being selectively open circuited and short circuited.

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