US 20030141108A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2003/0141108 A1

Enomoto et al. (43) Pub. Date: Jul. 31, 2003

(54) SINGLE-SIDED CIRCUIT BOARD AND METHOD FOR MAUFACTURING THE SAME

(75) Inventors: **Ryo Enomoto**, Gihu (JP); **Yasuji Hiramatsu**, Gihu (JP)

Correspondence Address:
Welsh & Katz, Ltd.
Thomas W. Tolpin
22nd Floor
120 South Riverside Plaza
Chicago, IL 60606 (US)

(73) Assignee: **IBIDEN CO., Ltd.**, Gihu (JP)

(21) Appl. No.: **10/358,933**

(22) Filed: **Feb. 5, 2003**

Related U.S. Application Data

(62) Division of application No. 09/453,636, filed on Dec. 3, 1999, now Pat. No. 6,518,513.

(30) **Foreign Application Priority Data**

Jun. 6, 1997 (JP) 9-165291

Dec. 10, 1998 (WO) 98/56220

Publication Classification

(51) **Int. Cl.**[7] **H05K 1/11**

(52) **U.S. Cl.** **174/262**

(57) **ABSTRACT**

Holes (**40***a*) are formed with a laser beam through an insulating substrate (**40**) on which a metallic layer (**42**) is formed and via holes (**36***a*) are formed by filling up the holes (**40***a*) with a metal (**46**). After the via holes (**36***a*) are formed, a conductor circuit (**32***a*) is formed by etching the metallic layer (**42**) and a single-sided circuit board (**30**A) is formed by forming projecting conductors (**38***a*) on the surfaces of the via holes (**36***a*). The projecting conductors (**38***a*) on the circuit board (**30**A) are put on the conductor circuit (**32***b*) of another single-sided circuit board (**30**B) with adhesive layers (**50**) composed of an uncured resin in-between and heated and pressed against the circuit (**32***b*). The projecting conductors (**38***a*) get in the uncured resin by pushing aside the resin and are electrically connected to the circuit (**32***b*). Since single-sided circuit boards (**30**A, **30**B, **30**C, and **30**D) can be inspected for defective parts before the boards (**30**A, **30**B, **30**C, and **30**D) are laminated upon one another, only defectless single-sided circuit can be used in the step of lamination.

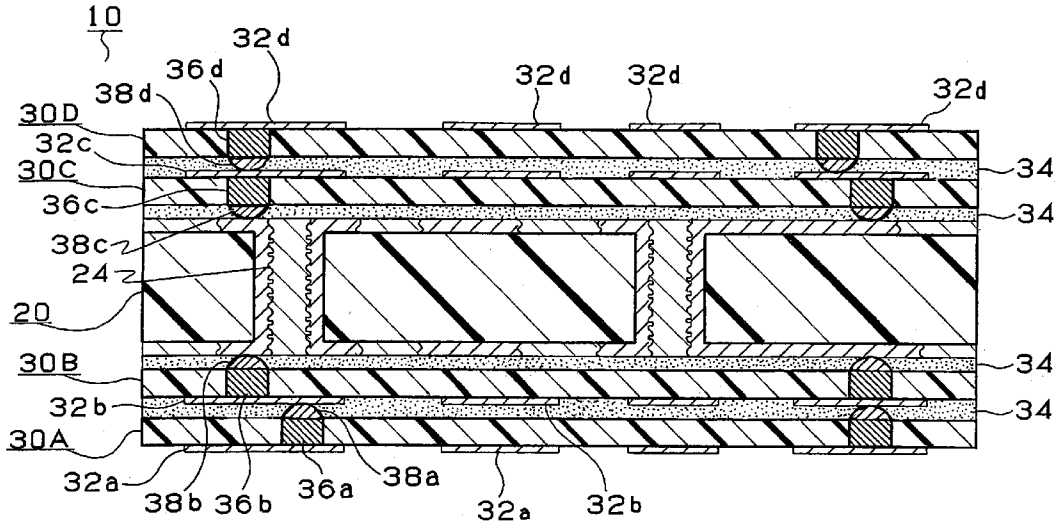


Fig. 1

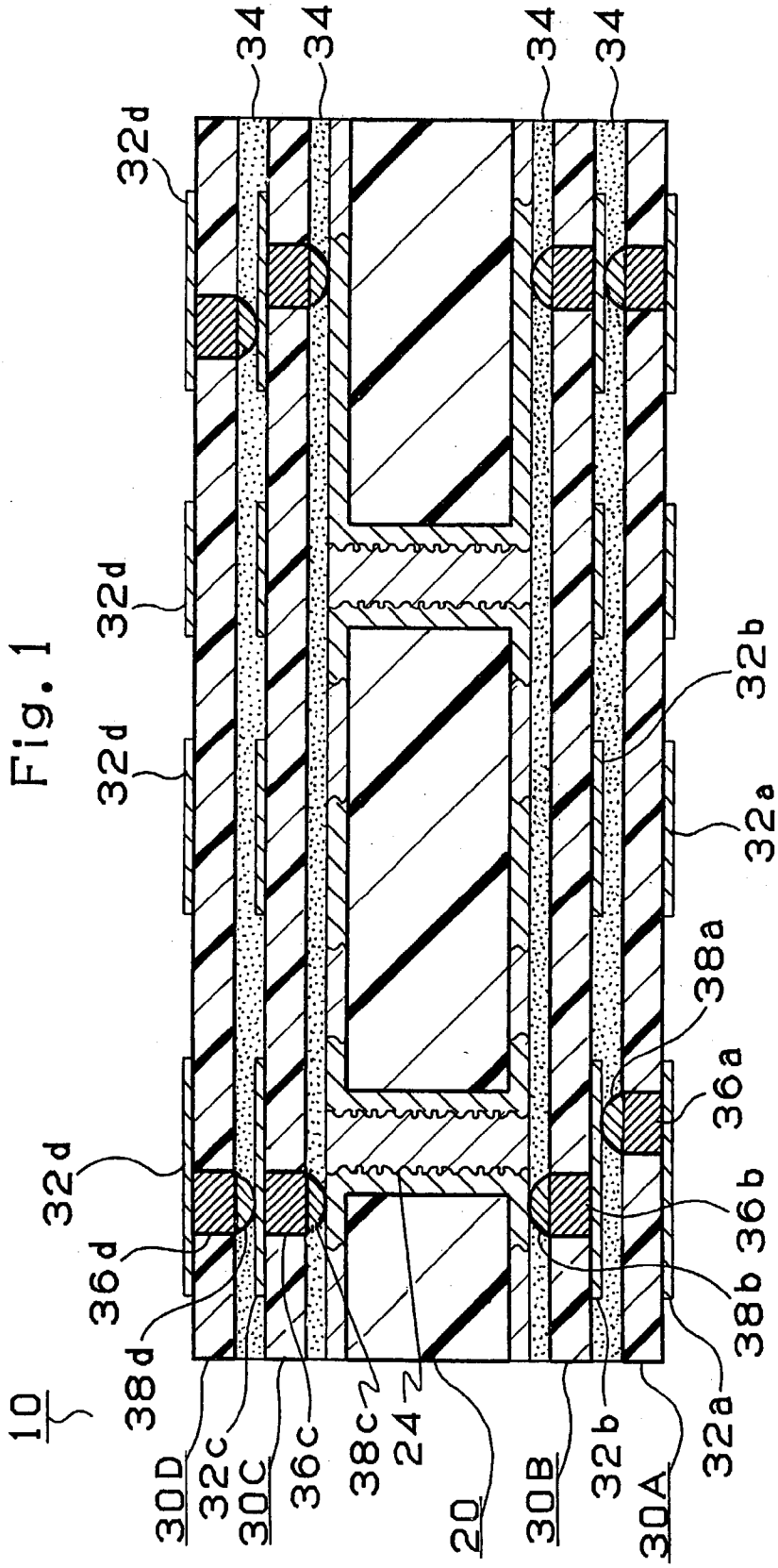

34
34
34
34
32d
32d
32d
32d
32b
32a
38a
36a
36b
38b
32d
36d
38d
10
30D
32c
30C
36c
38c
24
20
30B
32b
30A
32a
38b
36b

Fig. 2

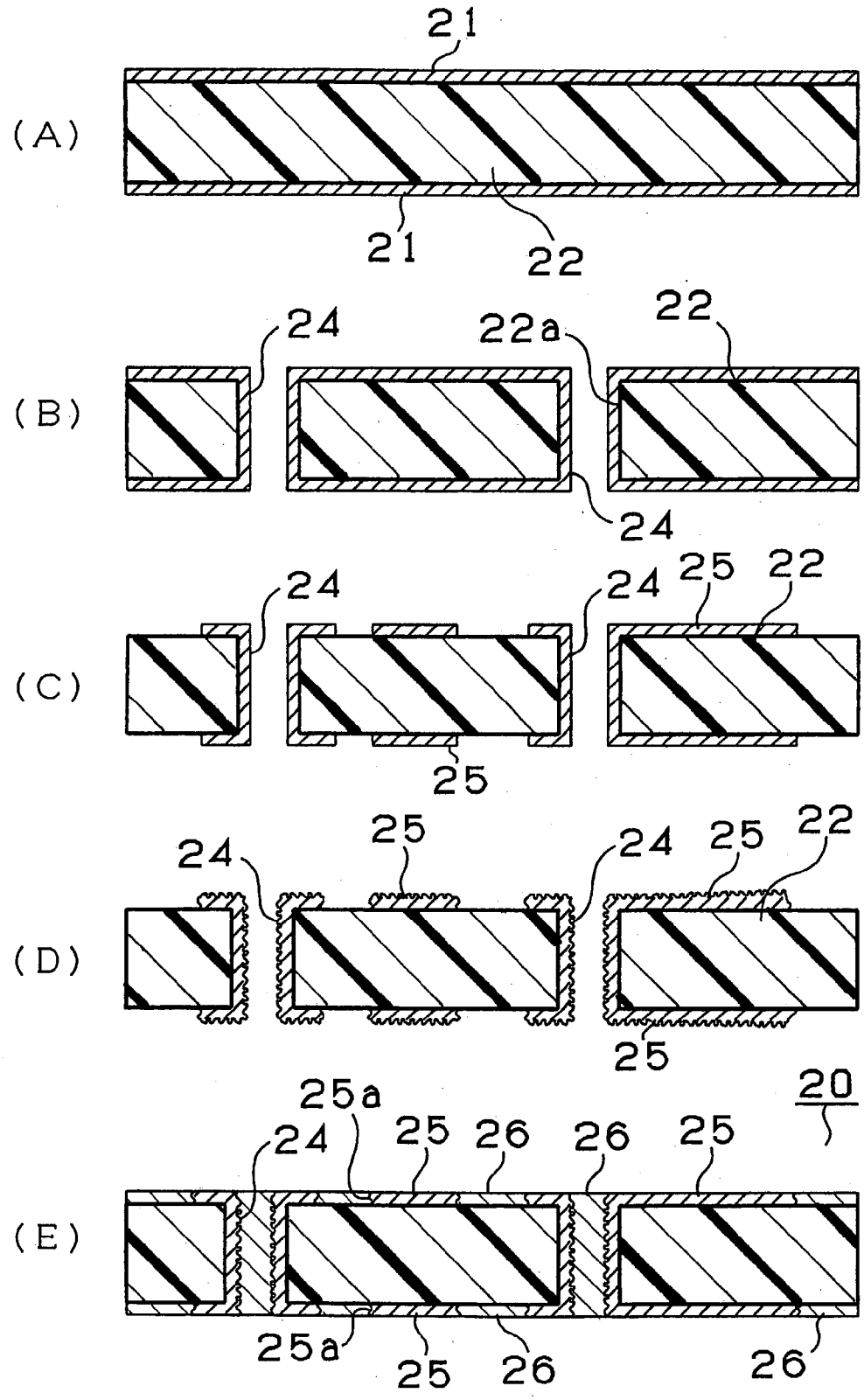

(A)
21
21
22
(B)
24
22a
22
24
(C)
24
24
25
22
25
(D)
24
25
24
25
22
25
(E)
20
25a
24
25
26
26
25
25a
25
26
26

Fig. 3

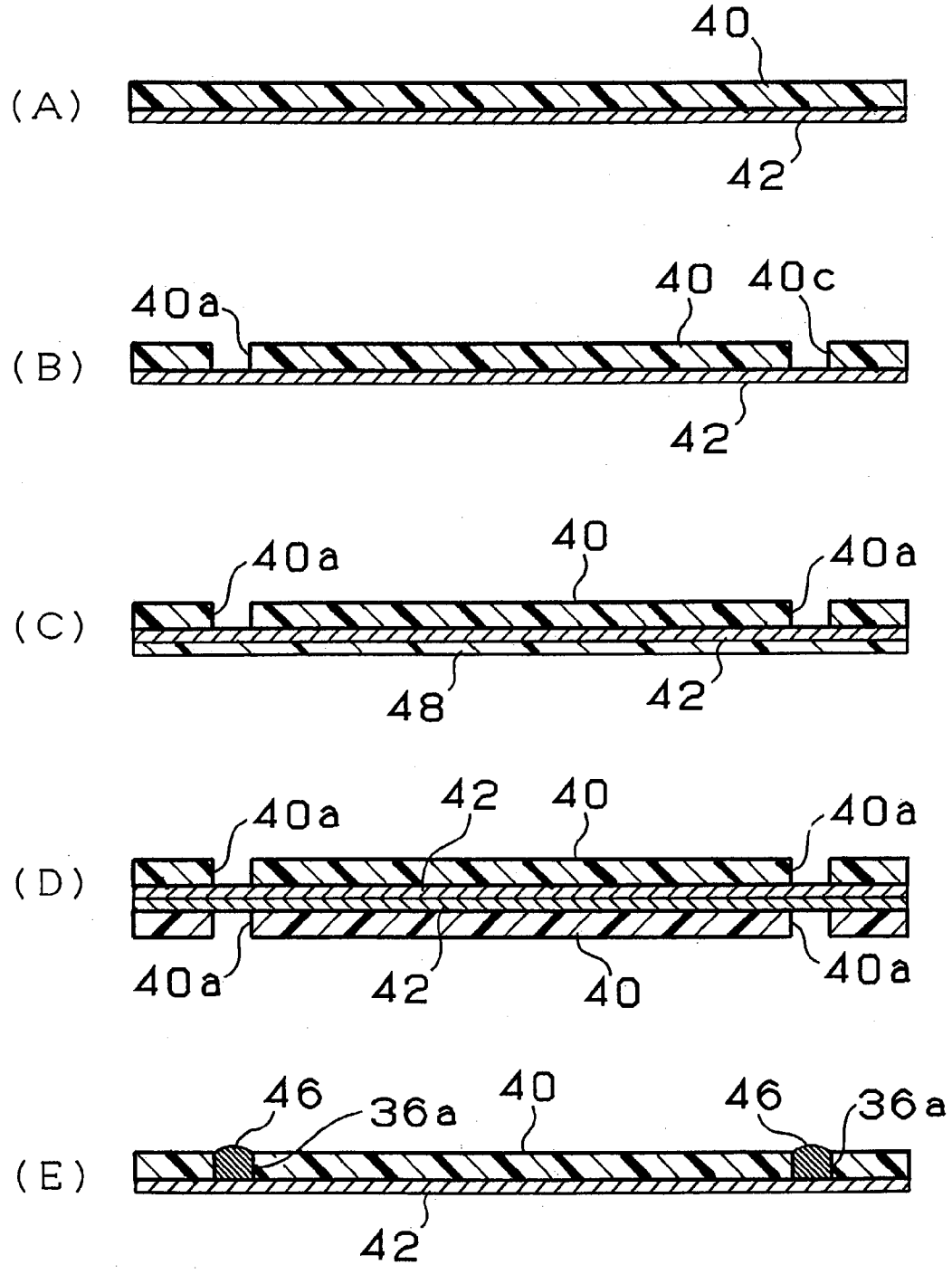

(A)
40
42
(B)
40a
40
40c
42
(C)
40a
40
40a
48
42
(D)
40a
42
40
40a
40a
42
40
40a
(E)
46
36a
40
46
36a
42

Fig. 4

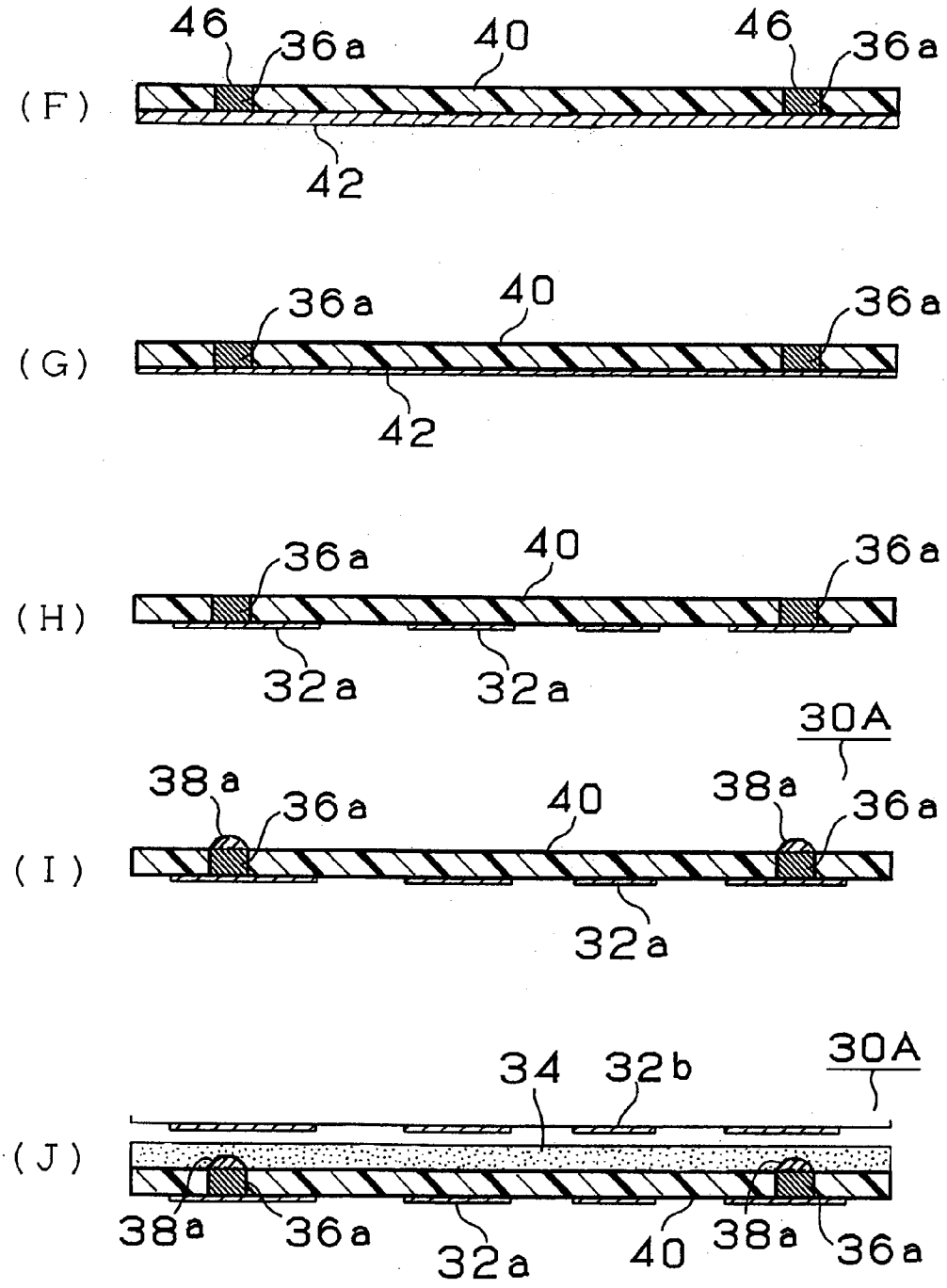

(F)
46
36a
40
46
36a
42
(G)
36a
40
36a
42
(H)
36a
40
36a
32a
32a
30A
(I)
38a
36a
40
38a
36a
32a
30A
(J)
34
32b
38a
36a
32a
40
38a
36a

Fig. 5

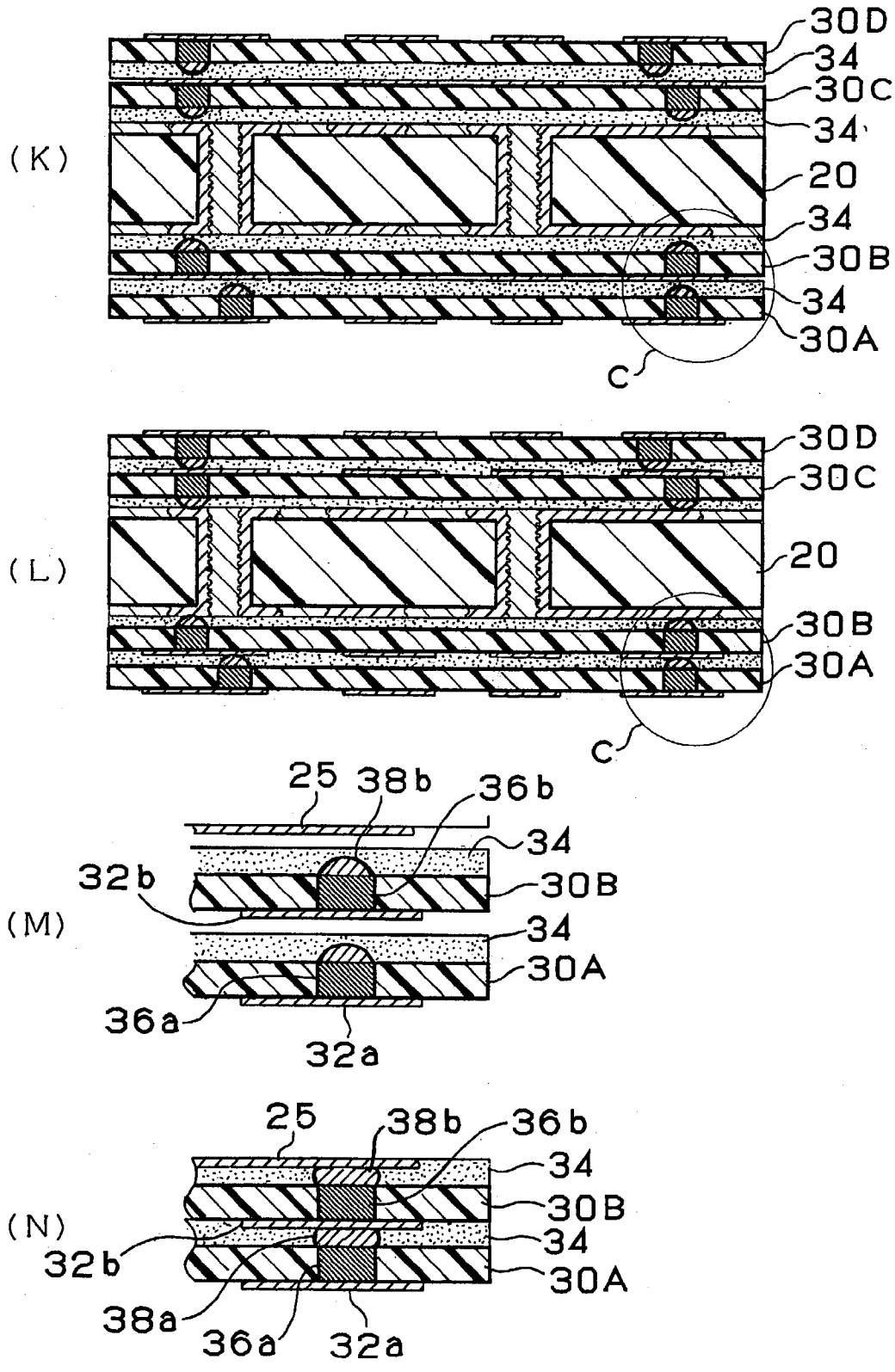

(K)
30D
34
30C
34
20
34
30B
34
30A
C
(L)
30D
30C
20
30B
30A
C
(M)
25
38b
36b
34
32b
30B
34
30A
36a
32a
(N)
25
38b
36b
34
30B
32b
34
30A
38a
36a
32a

Fig. 6

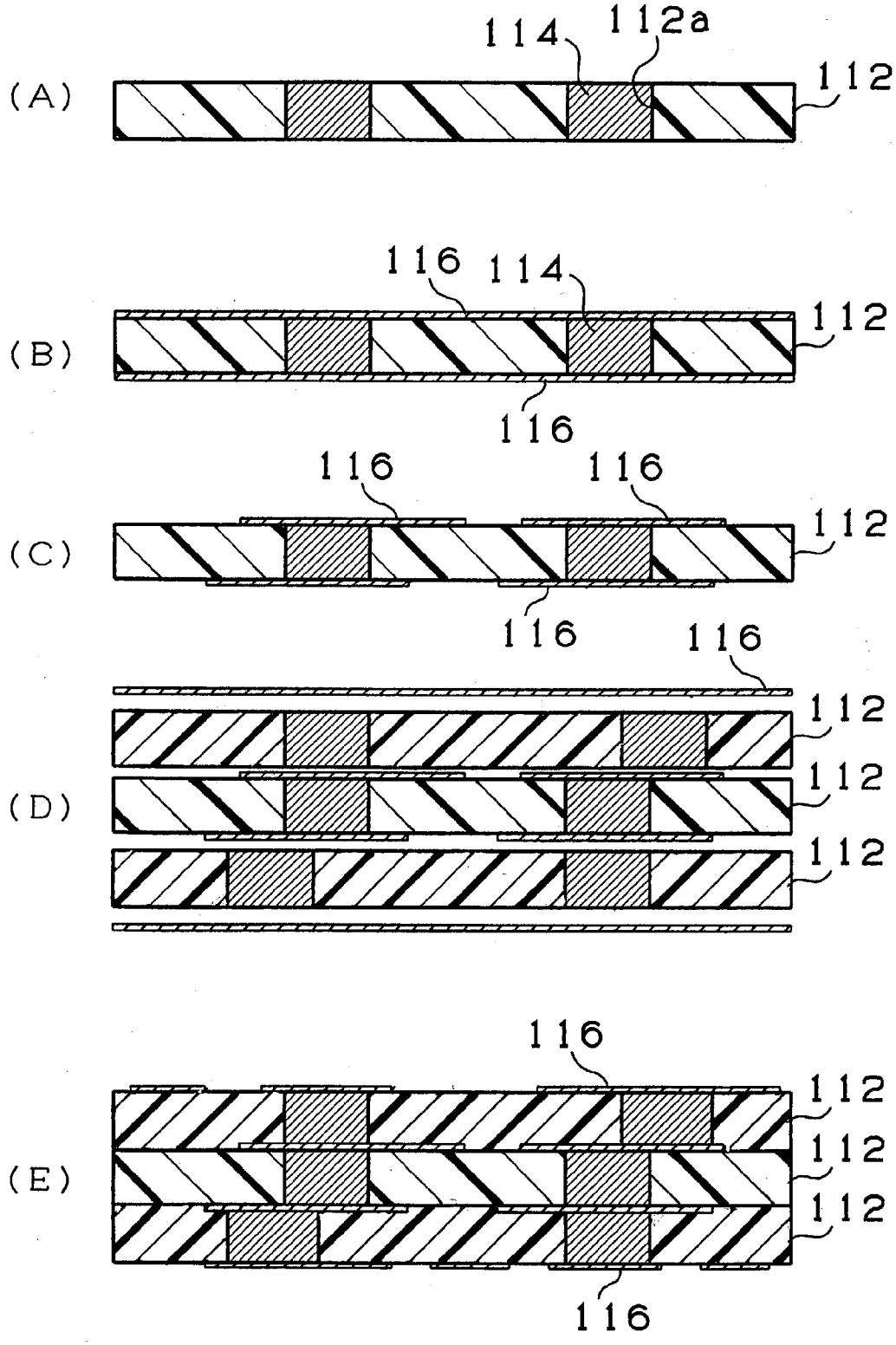

(A)
114
112a
112
(B)
116
114
112
116
(C)
116
116
112
116
116
(D)
116
112
112
112
(E)
116
112
112
112
116

Fig. 7

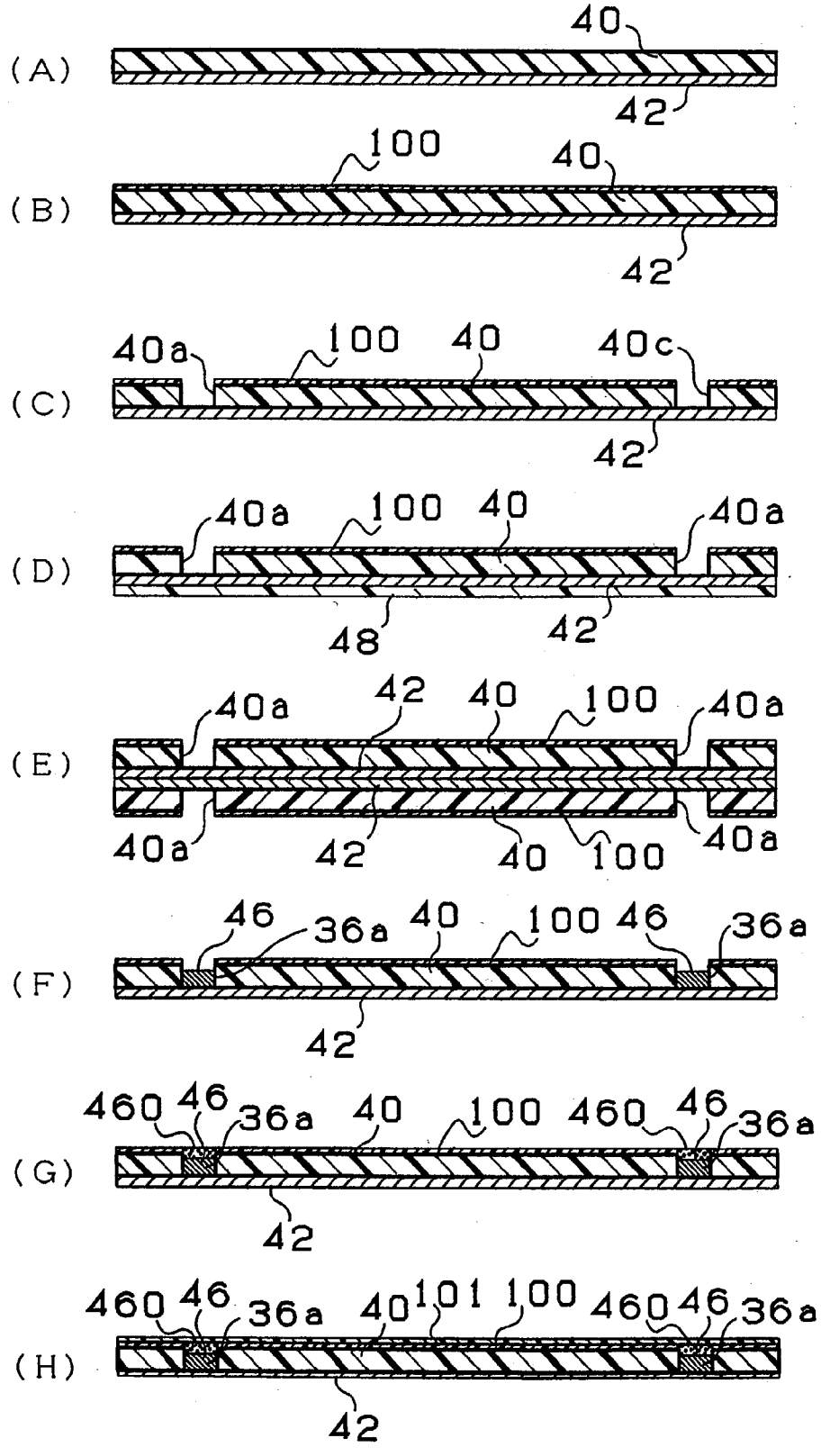

(A)
40
42
(B)
100
40
42
(C)
40a
100
40
40c
42
(D)
40a
100
40
40a
48
42
(E)
40a
42
40
100
40a
40a
42
40
100
40a
(F)
46
36a
40
100
46
36a
42
(G)
460
46
36a
40
100
460
46
36a
42
(H)
460
46
36a
40
101
100
460
46
36a
42

Fig. 8

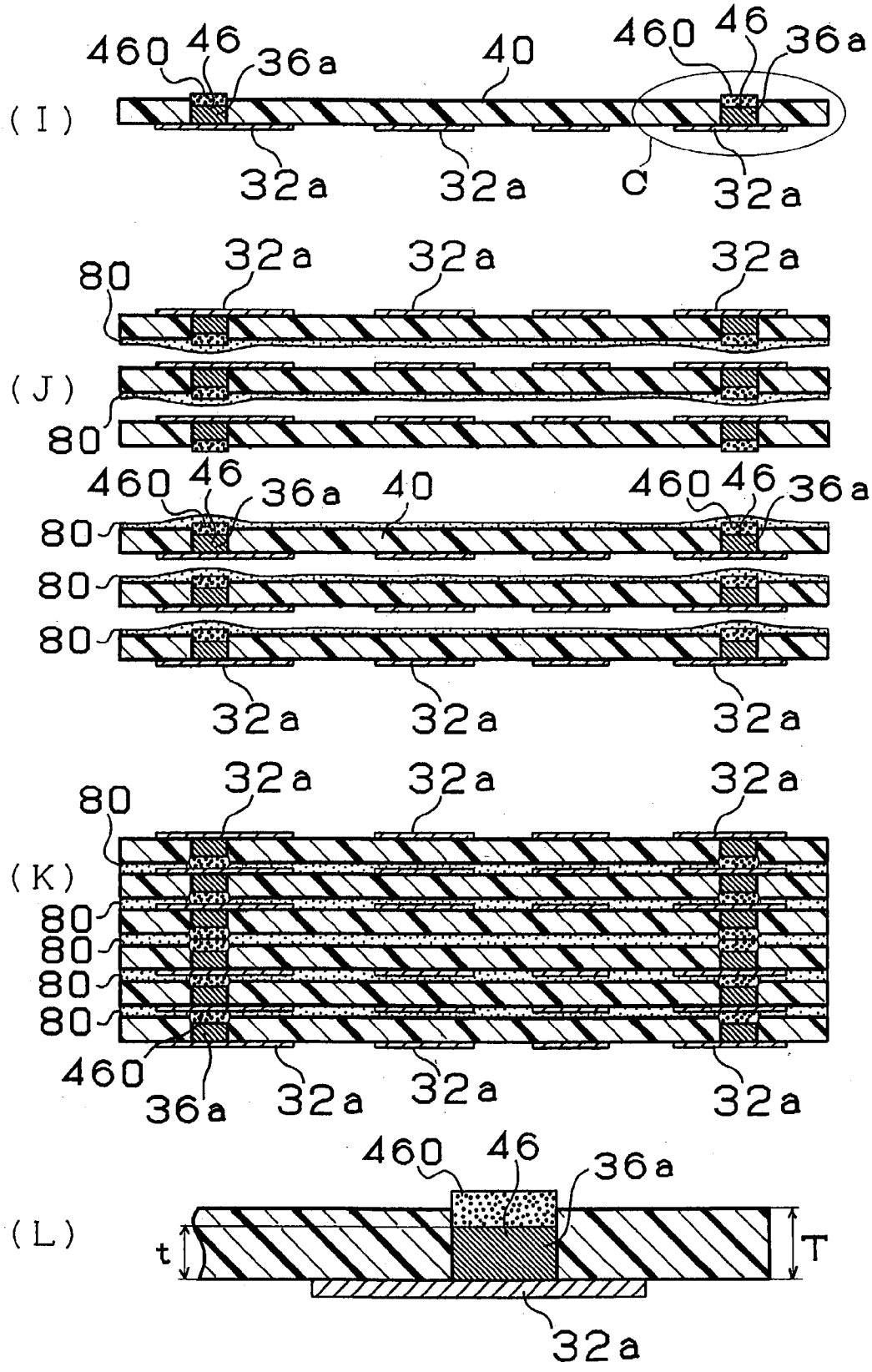
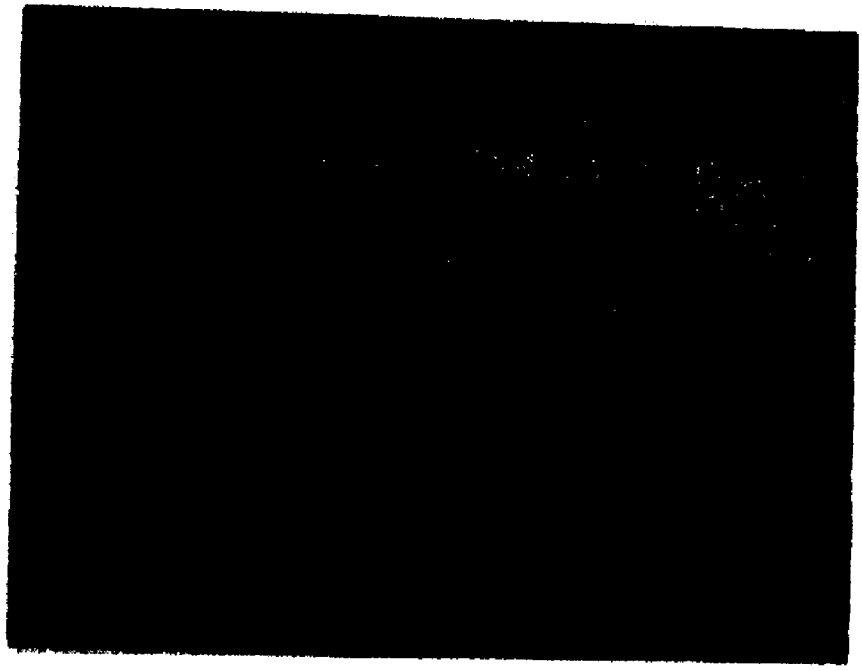

(I)
460
46
36a
40
460
46
36a
32a
32a
C
32a
(J)
80
32a
32a
32a
80
(K)
460
46
36a
40
460
46
36a
80
80
80
32a
32a
32a
80
80
80
80
460
36a
32a
32a
32a
(L)
460
46
36a
t
T
32a

Fig. 9



SINGLE-SIDED CIRCUIT BOARD AND METHOD FOR MAUFACTURING THE SAME

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a single-sided circuit board and a manufacturing method therefor, and more particularly to a single-sided circuit board used for manufacture of a multilayer printed circuit board having an interstitial via hole (IVH) structure and a manufacturing method therefor.

[0003] 2. Description of the Related Art

[0004] A conventional multilayer printed circuit board is constituted by a laminate obtained by alternately laminating copper-clad laminates and prepregs. The laminate has a surface on which a surface wiring pattern has been formed. Moreover, an internal wiring pattern is formed between interlayer insulating layers. Through holes are, by punching formed in the direction of the thickness of the laminate to establish the electric connections among internal wiring patterns or among internal wiring patterns and the surface wiring patterns.

[0005] The multilayer printed circuit board having the above-mentioned through hole structure must have regions for forming the through holes. Therefore, the density at which elements are mounted cannot be easily raised. As a result, there arises a problem in that the multilayer printed circuit board having the through hole structure cannot easily address needs for considerable reductions in the sizes of the portable electronic apparatuses, realizing narrow pitch packages and practical use of MCM.

[0006] As an alternative to the foregoing multilayer printed circuit board having the through hole structure, a multilayer printed circuit board has recently received attention which is formed into a full-thickness interstitial via-hole (IVH) structure which is able to easily address raising of the density.

[0007] The multilayer printed circuit board having the full-thickness IVH structure is a printed circuit board having a structure in which via holes for electrically connecting conductive layers to one another are formed in each of the interlayer insulating layers which constitute the laminate. That is, the foregoing printed circuit board has the via holes (buried via holes or blind via holes) which do not penetrate the substrate on which the circuit is formed and which electrically connect the internal wiring patterns to one another or the internal wiring patterns and the surface wiring patterns to one another. Therefore, the multilayer printed circuit board having the IVH structure is free from a necessity of specially forming regions for forming the through holes. Therefore, arbitrary layers can freely be connected to one another through small via holes. As a result, size reduction, high density and high-speed propagation of signals can be easily realized.

[0008] The multilayer printed circuit board having the IVH structure is manufactured by a process arranged, for example, as shown in **FIG. 6**.

[0009] Initially, a material having a structure in which an aramide nonwoven fabric cloth is impregnated with epoxy resin is employed as prepreg **112**. Then, an operation for forming holes in the prepreg **112** is performed by using carbon dioxide gas laser. Then, conductive paste **114** is enclosed in obtained hole portions **112***a* (see **FIG. 6**(A)).

[0010] Then, copper foil **116** is laminated on each of the two sides of the prepreg **112**, and then heat and pressure are applied to the prepreg **112** having the copper foil **116** by heat pressing. Hence it follows that the epoxy resin and the conductive paste of the prepreg **112** are hardened so that the electrical connection between the two copper foil members **116** on the two sides of the prepreg **112** is established (see **FIG. 6**(B)).

[0011] Then, the copper foil **116** on each side is patterned by an etching method so that a hard and double-sided substrate having via holes is obtained (see **FIG. 6**(C)).

[0012] Then, the obtained double-sided substrates are used as core layers to form a multilayer structure. Specifically, the prepreg and copper foil are sequentially laminated on the two sides of the foregoing core layer while the prepreg and the copper foil are being aligned. Then, heat pressing is again performed, and then the uppermost copper foil **116** is etched. Thus, a four-layer substrate is obtained (see FIGS. **6**(D) and **6**(E)). When a structure having a large number of layers is formed, the foregoing process is repeated. Thus, a six-layer substrate or an eight-layer substrate can be obtained.

[0013] The foregoing conventional technique, however, must repeat the laminating process using heat pressing and the process for patterning the copper foil by performing the etching operation. Therefore, the manufacturing process becomes too complicated and considerable time is required to complete the manufacturing operation.

[0014] If the multilayer printed circuit board having the IVH structure which can be obtained by the above-mentioned manufacturing method encounters only one defective portion (only one defective process) in the patterning operation during the manufacturing process, the overall circuit board, which is the final product, becomes a defective product. Hence it follows that the manufacturing yield deteriorates excessively.

[0015] To overcome the above-mentioned problems, an object of the present invention is to provide a high-density multilayer printed circuit board having the IVH structure which can be efficiently manufactured and which permits a satisfactory high manufacturing yield.

DISCLOSURE OF THE INVENTION

[0016] To achieve the above-mentioned object, a single-sided circuit board in the present invention is structured as follows. A single-sided circuit board according to the present invention is characterized in that an insulating base member on either side of which a conductive circuit is formed, wherein said insulating base member has non-penetrating holes which reach said conductive circuit, via holes are formed by enclosing electrolytic plating in said non-penetrating holes, projecting conductors made of conductive paste or metal having a low melting point are formed on the surfaces of said via holes formed on the surface of said insulating base member opposite to the surface on which said conductive circuit has been formed.

[0017] In accordance with the more preferred teaching of the present invention, said non-penetrating holes are characterized by being completely filled with electrolytic plating.

[0018] In accordance with the more preferred teaching of the present invention, said non-penetrating holes are characterized by being filled with the electrolytic plating to an average depth of 50% or higher of the depth of said non-penetrating holes and lower than 100% of the same.

[0019] In accordance with the more preferred teaching of the present invention, said insulating base member is characterized as an organic insulating member.

[0020] In accordance with the more preferred teaching of the present invention, said electrolytic plating is characterized as copper electrolytic plating.

[0021] In accordance with the more preferred teaching of the present invention, said insulating member is characterized as a single-sided copper-clad laminate.

[0022] A method of manufacturing a single-sided circuit board according to the present invention is characterized by at least comprising the steps (1) to (4):

[0023] (1) forming non-penetrating holes which reach a metal layer by a laser process in a insulating base member having said metal layer formed on either side thereof;

[0024] (2) enclosing electrolytic plating into said non-penetrating holes formed in step (1) to form via holes;

[0025] (3) forming a conductive circuit by etching said metal layer; and

[0026] (4) forming projecting conductors made of conductive paste or metal having a low melting point on the surfaces of said via holes formed on the surface of said insulating base member to the surface on which said conductive circuit has been formed so that a single-sided circuit board is obtained.

[0027] A method of manufacturing a single-sided circuit board according to the present invention is characterized by at least comprising the steps (1) to (3):

[0028] (1) forming non-penetrating holes which reach a metal layer by a laser process in a insulating base member having said metal layer formed on either side thereof;

[0029] (2) enclosing electrolytic plating into said non-penetrating holes formed in step (1) to form via holes and forming projecting conductors made of conductive paste or metal having a low melting point on the surfaces of said via holes formed on the surface of said insulating base member opposite to the surface on which said conductive circuit has been formed; and

[0030] (3) etching metal layer to form a conductive circuit so that a single-sided circuit board is obtained.

[0031] A method of manufacturing a single-sided circuit board in accordance with the more preferred teaching of the present invention is characterized in that said step (1) is performed such that a film is bonded to insulating base member having the metal layer formed on either side thereof and non-penetrating holes which penetrate said film and said insulating base member to reach said metal layer are formed by a laser process.

[0032] A method of manufacturing a single-sided circuit board in accordance with the more preferred teaching of the present invention is characterized in that said insulating base member is an organic insulating base member.

[0033] A method of manufacturing a single-sided circuit board in accordance with the more preferred teaching of the present invention is characterized in that said insulating base member is a single-sided copper cladding laminate.

[0034] A method of manufacturing a single-sided circuit board in accordance with the more preferred teaching of the present invention is characterized in that said electrolytic plating is copper electrolytic plating.

[0035] A method of manufacturing a single-sided circuit board in accordance with the more preferred teaching of the present invention is characterized in that said projecting conductors are formed by printing conductive paste.

[0036] A method of manufacturing a single-sided circuit board in accordance with the more preferred teaching of the present invention is characterized in that said projecting conductors are formed by printing metal paste having a low melting point, plating of metal having a low melting point or immersion of metal having a low melting point into molten solution.

[0037] The single-sided circuit board according to the present invention is arranged such that the single-sided circuit boards each having a conductive circuit which incorporates a predetermined wiring pattern formed thereon are previously and individually manufactured.

[0038] These single-sided circuit boards are laminated to other substrates through an adhesive layer and are integrated by the heat pressing. Therefore, inspection for detecting whether or not the conductive circuit or the like has a defective portion can be performed before the single-sided circuit boards are laminated. Hence it follows that only single-sided circuit boards free from any defect can be used in the laminating process. That is, the manufacturing method is able to reduce defects in the manufacturing process. As a result, the multilayer printed circuit board having the IVH structure can be manufactured with a high manufacturing yield.

[0039] The method of manufacturing a multilayer printed circuit board having the IVH structure used the single-sided circuit board according to the present invention is not required to repeat the heating press operation while the prepreg is being laminated as distinct from the conventional technique. That is, the present invention enables the heat pressing operation to be completed at a time such that a plurality of the single-sided circuit boards are laminated through the adhesive agents placed on the single-sided circuit boards. Therefore, the manufacturing method according to the present invention is free from a necessity for repeating the laminating process, in which the complicated heat press is performed, and the patterning process. Hence it follows that the multilayer printed circuit board having the IVH structure can efficiently be manufactured.

[0040] In the present invention, formation of the non-penetrating holes in the organic insulating substrate is performed by laser machining. The structure of the present invention is able to eliminate the necessity of forming holes in the organic adhesive agent, an organic insulating substrate

and an adhesive agent by performing a laser process. That is, after holes have been formed in the organic insulating substrate by performing the laser process, the organic adhesive layer can be formed on the single-sided circuit substrate or the substrate having the conductor circuit.

[0041] That is, the single-sided circuit board according to the present invention is structured such that the projecting conductors inserted into the organic adhesive layer during the heat pressing establish the connection of the conductor circuits. Therefore, previous formation of the conducting hole in the organic adhesive layer is not required. The organic adhesive layer may be formed at the final heat pressing process. As a result, the desmear process, which is performed after the hole has been formed, may be performed before the formation of the organic adhesive layer. Hence it follows that the desmear process does not erode the adhesive layer.

[0042] Also, the adhesive layer can be formed on the single-sided circuit board or the substrate having the conductive circuit after the non-penetrating hole has been formed in the insulating base member by performing the laser process and the non-penetrating hole has been filled with the electrolytic plating. Therefore, the electrolytic plating solution and the adhesive layer are not made contact with each other. As a result, the erosion and contamination of the adhesive layer with the plating solution can be prevented.

[0043] Since the adhesive layer is not hardened until the heat pressing process which is the final process is performed, the organic adhesive layer easily deteriorates owing to the desmear process and the plating solution. The present invention is characterized in that the foregoing problem can be prevented and a reliable substrate can be easily formed.

[0044] Furthermore, projecting conductors made of conductive paste or metal having a low melting point are formed on the surfaces of via holes formed on the surface of said insulating base member opposite to the surface on which conductive circuit has been formed. Therefore, since conductive paste or metal having a low melting point is deformed during the heat pressing and uneven height of the electric plating can be absorbed, the multilayer printed circuit board, whereby the defective connection can be prevented which is highly reliable in connection, is obtained.

[0045] Moreover, according to the single-sided circuit board of the present invention, a necessity for previously forming a conducting hole in the adhesive layer can be eliminated. Therefore, defective conduction caused from deviation in the positions of the hole in the adhesive layer and the projecting conductors provided for the organic insulating base member can be prevented.

[0046] In the single-sided circuit board according to the present invention, the projecting conductors are formed on the via holes filled with the electrolytic plating. Therefore, electrical connection between the upper and lower conductive layers in the multilayer printed circuit substrate can be easily established by penetrating the relatively thin organic adhesive layer. Therefore, the height and the diameter of each projecting conductor can be reduced. Hence it follows that the pitch between adjacent projecting conductors can be shortened. Therefore, the pitch between adjacent via holes can also be shortened. As a result, addressing to the raising of the density can be permitted. Since the via holes are filled with the electrolytic plating, the resistance value between the upper and the lower conductor layers can be lowered.

[0047] Techniques for connecting the upper and lower conductors to each other by penetrating the resin insulating layer of the multilayer printed circuit board have been disclosed in Japanese Patent Laid-Open No. 7-14628, Japanese Patent Laid-Open No. 7-106756, Japanese Patent Laid-Open No. 7-231167, Japanese Patent Laid-Open No. 8-172270 and Japanese Patent Laid-Open No. 8-288649. The foregoing techniques are different from the technique with which the projecting conductors are formed on the via holes filled with the electrolytic plating. Therefore, the effect of the present invention cannot be obtained.

BRIEF DESCRIPTION OF DRAWINGS

[0048] **FIG. 1** is a vertical cross sectional view showing a multilayer printed circuit board according to an embodiment of the present invention;

[0049] **FIG. 2** is a diagram showing a process for manufacturing a core substrate which constitutes the multilayer printed circuit board according to the embodiment of the present invention;

[0050] **FIG. 3** is a diagram showing a process for manufacturing a single-sided circuit board which constitutes the multilayer printed circuit board according to the embodiment of the present invention;

[0051] **FIG. 4** is a diagram showing a process for manufacturing the single-sided circuit board which constitutes the multilayer printed circuit board according to the embodiment of the present invention;

[0052] **FIG. 5** is a diagram showing a process for manufacturing the multilayer printed circuit board according to the embodiment of the present invention;

[0053] **FIG. 6** is a diagram showing a process for manufacturing a conventional multilayer printed circuit board;

[0054] **FIG. 7** is a diagram showing a process for manufacturing the core substrate which constitutes the multilayer printed circuit board according to the embodiment of the present invention;

[0055] **FIG. 8** is a diagram showing a process for manufacturing the core substrate which constitutes the multilayer printed circuit board according to the embodiment of the present invention; and

[0056] **FIG. 9** is an enlarged photograph showing a metal structure of the cross section of a via hole in the multilayer printed circuit board according to the embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0057] A single-sided circuit board and a multilayer printed circuit board and a manufacturing method therefor used single-sided circuit board according to an embodiment of the present invention will now be described with reference to the drawings.

[0058] **FIG. 1** shows a vertical cross section of a multilayer printed circuit board having a full-thickness IVH

structure. A multilayer printed circuit board **10** is a multilayer printed circuit board incorporating a core substrate **20** disposed in a central portion of the multilayer printed circuit board **10** and single-sided circuit boards **30**A, **30**B, **30**C and **30**D of the present invention, two substrates of which are formed on the upper surface of the core substrate **20** and the lower surface of the same, respectively.

[**0059**] Conductive circuits **32***a*. **32***b*, **32***c* and **32***d* each having a predetermined pattern are formed on the surfaces of the corresponding single-sided circuit boards **30**A, **30**B, **30**C and **30**D. Adhesive layers **34** are formed on other surfaces of the same. The core substrate **20** and the single-sided circuit boards **30**A, **30**B, **30**C and **30**D are bonded to one another through the adhesive layers **34**. The single-sided circuit boards **30**A, **30**B, **30**C and **30**D have corresponding via holes **36***a*, **36***b*, **36***c* and **36***d* formed by enclosing electrolytic copper plating. Projecting conductors (hereinafter called "bumps") **38***a*, **38***b*, **38***c* and **38***d* made of metal, such as solder or an indium alloy or conductive paste, are formed on the foregoing via holes (the surfaces of the via holes opposite to the surfaces on which the conductive circuits are formed).

[**0060**] That is, in the multilayer printed circuit board **10**, a conductive circuit **32***a* of the lowermost single-sided circuit board **30**A is connected to a bump **38***a* through the via hole **36***a*. The bump **38***a* is made to contact with a conductive circuit **32***b* of the single-sided circuit board **30**B to establish the connection between the two circuits. The bump **38***b* connected to the conductive circuit **32***b* through the via hole **36***b* is made to contact with the through hole **24** (a via hole is made after multilayer structure is formed) of the core substrate **20** so that conduction is realized. The through hole **24** of the core substrate **20** is connected to the bump **38***c* of the upper single-sided circuit board **30**C. The conductive circuit **32***c* connected to the bump **38***c* through the via hole **36***c* is connected to the bump **38***d* of the uppermost single-sided circuit board **30**D. The bump **38***d* is connected to the conductive circuit **32***d* through the via hole **36***d*. An electronic element, such as a bear chip, can be mounted on either surface or two surfaces of the uppermost single-sided circuit board **30**D. Thus, the conductive circuit **32***a* of the lowermost single-sided circuit board **30**A of the multilayer printed circuit board and the chip element (not shown) mounted on the conductive circuit **32** of the uppermost single-sided circuit board **30**D are connected to each other through the via holes **36***a*, **36***b*, **36***c* and **36***d*. The foregoing via holes constitute interstitial via holes.

[**0061**] The method of manufacturing the multilayer printed circuit board **10** using single-sided circuit board according to the present invention will now be continued. A method of manufacturing the core substrate **20** will now be described with reference to **FIG. 2**.

[**0062**] The core substrate may be a known rigid substrate, such as an epoxy resin substrate having a glass cloth base member or a BT (Bismaleimide-Triazine) resin substrate having a glass cloth base member.

[**0063**] Specifically, in process (A) shown in **FIG. 2, a** starting material is copper-clad laminates incorporating a substrate **22** which is made of BT (Bismaleimide-Triazine) resin and which has two sides on each of which copper foil **21** is bonded. In process (B), holes **22***a* serving as through holes are formed in the substrate **22** by punching, and then electroless plating is performed so that the inner surfaces of the holes **22***a* are applied with copper plating. Thus, through holes **24** are formed.

[**0064**] In process (C), etching resist (not shown) is previously applied, and then an etching process is performed to remove unnecessary portions of the copper foil **21**. As a result, a predetermined conductive circuit **25** is formed.

[**0065**] In process (D), the surfaces of the conductive circuit **25** and the through holes **24** are subjected to blacking-reducing process so as to be coarsened.

[**0066**] In process (E), resin **26** which must be enclosed is uniformly applied by using a roll coater, and then the resin which must be enclosed is hardened. Then, the resin which must be enclosed is ground with a belt sander or the like until the conductive circuit **25** is exposed on the surface. As a result, a core substrate **20** having two flat surfaces is manufactured.

[**0067**] The core substrate **20** is brought to a state in which the inside portion of the through holes **24** and two sides **25***a* of the conductive circuit **25** are coarsened. As a result, the adhesiveness between the conductive circuit **25** and the resin **26** which must be enclosed can be improved. Hence it follows that occurrence of a crack can be prevented which occurs in the adhesive layer **34** described with reference to **FIG. 1** and which starts at the interface between the conductive circuit **25** and the resin **26** which must be enclosed.

[**0068**] Description of the method of manufacturing the single-sided circuit board **30** according to the present invention will now be continued with reference to **FIGS. 3 and 4**. In process (A) shown in **FIG. 3**, an insulating base member **40** having a metal layer **42** formed on either surface thereof is used as a starting material. The insulating base member **40** must be an organic insulating base member. Specifically, it is preferable that a base member is selected from rigid laminates including an aramide nonwoven fabric cloth-epoxy resin base member, a glass cloth epoxy resin base member, an aramide nonwoven fabric cloth-polyimide base member and a bismaleimide-triazine resin base member or films including a polyphenylene (PPE) film and a polyimide (PI) film.

[**0069**] It is preferable that the insulating base member **40** is a rigid laminated base member. In particular, it is preferable that a single-sided circuit board is employed. The reason for this lies in that displacement of the positions of the wiring pattern and the via holes can be prevented during handling which is performed after the metal layer **42** has been etched. That is, excellent accuracy of the position can be realized.

[**0070**] The metal layer **42** formed on the insulating base member **40** may be copper foil. The copper foil may be subjected to a matting process in order to improve the adhesiveness. The single-sided circuit board is a substrate which can be obtained by heat-pressing a laminate of prepreg and copper foil, the prepreg being in the form of a B-stage constituted by causing a glass cloth to be impregnated with thermosetting resin, such as epoxy resin, phenol resin or bismaleimide-triazine resin. The single-sided circuit board is a rigid substrate which can easily be handled and which is an advantage substrate from the viewpoint of cost reduction. Metal may be evaporated on the surface of the

insulating base member **40**, followed by forming a metal layer by performing electrolytic plating.

[**0071**] The thickness of the insulating base member **40** is 10 μm to 200 μm, preferably 15 μm to 100 μm. The optimum thickness is 20 μm to 80 μm to maintain insulating characteristics. If the thickness is smaller than the above-mentioned ranges, the strength is decreased excessively to perform easy handling. If the thickness is too large, formation of small via holes is inhibited and enclosing of the conductive material cannot easily be performed.

[**0072**] The thickness of the metal layer **42** is 5 μm to 35 μm, preferably 8 μm to 30 μm, and more preferably 12 μm to 25 mm. If the thickness is too small, a hole attempted to be formed by a laser process as described later is undesirably formed into a through hole. If the thickness is too large, a fine pattern cannot be formed by the etching process.

[**0073**] Then, the laser irradiation process is performed to form non-penetrating holes **40**a in the insulating base member **40** (process (B)). The laser processing machine may be a carbon dioxide gas laser processing machine, an UV laser processing machine or an excimer laser processing machine. It is preferable that the caliber of the laser processing machine is 20 μm to μm. The carbon dioxide gas laser processing machine exhibits high processing speed, enabling the cost of the process to be reduced. Therefore, the foregoing laser processing machine is a most suitable machine from a viewpoint of industrial use. Therefore, the foregoing laser processing machine is a most suitable machine for the present invention. When the carbon dioxide gas laser processing machine is employed, resin existing in the non-penetrating hole **40***a* and slightly melted onto the surface of the metal layer **42** is easily left. Therefore, it is preferable that a desmear process is performed to maintain the reliability of the connection.

[**0074**] Then, an electrolytic plating is enclosed in the non-penetrating holes **40***a* formed by the laser process so that via holes **36***a* are formed (process (E)). As an alternative to this, conductive paste may be enclosed or a portion of electrolytic plating may be enclosed, followed by enclosing conductive paste into a residual portion. The electrolytic plating may be, for example, copper, gold, nickel or solder plating. Most suitable electrolytic plating is copper electrolytic plating. In this case, the formation of the bumps can be performed simultaneously with the process.

[**0075**] The conductive paste may be conductive paste made of metal particles made of one or more materials selected from silver, copper, gold, nickel and solder. As the metal particles, a material may be employed which is obtained by coating the surfaces of the metal particles with different metal. Specifically, metal particles may be employed which are obtained by coating the surfaces of copper particles with noble metal selected from gold and silver.

[**0076**] It is preferable that the conductive paste is organic conductive paste obtained by adding thermosetting resin, such as epoxy resin, phenol resin or polyphenylene sulfide (PPS), to the metal particles.

[**0077**] In this embodiment, the small holes each having a diameter of 20 μm to 150 μm are formed by the laser process and enclose the electrolytic plating, which is an advantage since air bubbles easily release compared with the enclosure of the conductive paste.

[**0078**] The electrolytic plating is performed as the lead for the metal layer **42** formed on the insulating base member **40**. Since the metal layer **42** is formed on the overall surface of the insulating base member **40**, the density of the electric field can be uniform. In this embodiment, the non-penetrating holes are completely enclosed by electrolytic plating. Therefore, the non-penetrating holes can be enclosed with the electrolytic plating such that a uniform height is realized. It is preferable that the surface of the metal layer **42** in each of the non-penetrating holes **40***a* is subjected to an activating process using acid or the like. When plating is performed, it is preferable that deposition of the electrolytic plating on the surface of the metal layer **42** provided for the organic insulating base member **40** is prevented by applying a mask **48** on the metal layer **42** in process (C). As an alternative to this, in process (D), two insulating base members **40** are laminated and brought into hermetic contact with each other to prevent contact with the plating solution during the electrolytic plating process.

[**0079**] After the electrolytic plating has been completed, a portion of the electrolytic plating (metal **46**) projecting over the non-penetrating holes **40***a* may be removed by grinding or the like to flatten the surface in process (F) shown in **FIG. 4**. The grinding process may be performed by using a belt sander or by buffing.

[**0080**] In process (G), a process which is performed before the metal layer **42** is etched to form the conductive circuit and which is a process for easily forming a fine pattern is carried out with which the non-penetrating holes are previously formed by a laser process, followed by etching the overall surface of the metal layer **42** to reduce the thickness to about 1 μm to about 10 μm, preferably about 2 μm to about 8 μm.

[**0081**] As shown in process (H), a mask having a predetermined pattern is applied, and then the metal layer **42** is etched to form the conductive circuit **32***a*. Initially, a photosensitive dry film is applied or liquid-type photosensitive resist coat is applied. Then, exposure and development are performed to conform to the predetermined circuit pattern so that an etching resist is formed. Then, the metal layer in the portions in which the etching resist is not formed is etched so that a conductor pattern is formed. It is preferable that the etching is performed by using solution of at least one type of material selected from sulfuric acid-hydrogen peroxide, persulfate, cupric chloride and ferric chloride.

[**0082**] Note that the uppermost pattern may be formed by etching the metal layer after the laminate pressing process has been completed. When the metal layer is etched after the laminate pressing process has been completed, an advantage can be realized in that heat pressing can be performed with uniform pressure because the surfaces which must be pressed are flat surfaces.

[**0083**] It is preferable that the surface of the conductive circuit **32***a* is subjected to a coarsening process. The reason for this lies in that the adhesiveness with the adhesive layer **34** described with reference to **FIG. 1** can be improved in the foregoing case to prevent separation (delamination). The coarsening process may be, for example, a soft etching process, a blackening (oxidizing)-reducing process, formation of needle-shape alloy plating ("INTERPLATE" which is trade name of Ebara) of copper-nickel-phosphorus or surface coarsening process using etching solution "MECH ETCHBOND" which is trade name of Mech.

[0084] In process (I), bumps **38***a* are formed on the surfaces of the via holes **36***a* opposite to the surface on which the conductive circuit **32***a* has been formed. The bumps **38***a* can be formed by, for example, a method with which conductive paste is screen-printed by using a metal mask having openings formed at predetermined positions, a method with which paste of solder which is metal having a low melting point is printed, a method with which solder plating is performed or a method with which immersion in solution in which solder has been melted is performed.

[0085] The metal having the low melting point may be Pb—Sn type solder, Ag—Sn type solder or indium solder.

[0086] It is preferable that the height of each bump from the insulating base member **40** is 3 μm to 60 μm. If the height is smaller than 3 μm, absorption of dispersion of the heights of the bumps by virtue of deformation of the bumps cannot be realized. If the height is larger than 60 μm, the resistance value is raised excessively. To a worse extent, the bumps are expanded in the lateral direction when the bumps have been deformed, causing short circuit to occur.

[0087] In the foregoing state or before the bumps are formed, inspections of the conductive circuit **32***a* and the via holes **36***a* can be performed. The conventional multilayer printed circuit board permits the inspection of the conductive circuit to be performed only after lamination has been performed, that is, after completion. As compared with this, whether or not the single-sided circuit board **30**A has a defect can be inspected before the laminating operation. Since only single-sided circuit board **30**A free from any defect can be used in a laminating process to be described later, a satisfactory high yield of the multilayer printed circuit board can be obtained.

[0088] The single-sided circuit board of the present invention laminates plural single-sided circuit boards to each other or is laminated to the core substrate **20** shown in **FIG. 2**. The adhesive in this case, for example, shown in the process (J), coats the overall surface of the insulating base member **40** adjacent to the bumps **38***a* with resin. Then, the resin is dried so that an adhesive layer **34** constituted by non-hardened resin is formed.

[0089] The adhesive layer **34** may be formed by coating the overall surface of the single-sided circuit board on which the conductive circuit has been formed, the overall opposite surface or the overall surface of substrate **20** on which the conductive circuit **25***b* has been formed, the substrate **20** being a substrate having a conductive circuit. Therefore, a necessity for forming holes for establishing conduction in the adhesive layer can be eliminated.

[0090] It is preferable that the adhesive layer **34** is made of organic adhesive agent. It is preferable that the organic adhesive agent is a resin selected from epoxy resin, polyimide resin, thermosetting polyphenylene ether (PPE), composite resin of the epoxy resin and the thermosetting resin, composite resin of epoxy resin and silicon resin or BT resin.

[0091] The non-hardened resin which is the organic adhesive agent can be applied by using a curtain coater, a spin coater, a roll coater or a spray coater or by screen printing. Also the formation of the adhesive layer can be performed by laminating an adhesive sheet. It is preferable that the thickness of the adhesive layer is 5 μm to 50 μm. To facilitate handling, it is preferable that the adhesive layer is pre-cured.

[0092] The process of laminating the core substrate **20** described with reference to **FIG. 2** and the single-sided circuit board **30** described with reference to **FIGS. 3 and 4** will continuously be described with reference to **FIG. 5**.

[0093] In process (K), the single-sided circuit board **30**A, the single-sided circuit board **30**B, **30**C and **30**D formed by a process similar to the above-mentioned process and the core substrate **20** are laminated. All of the single-sided circuit boards **30**A, **30**B, **30**C and **30**D and the core substrate **20** must be substrates subjected to inspection for a defective portion. Initially, the single-sided circuit board **30**B is placed on the organic adhesive layer **34** of the single-sided circuit board **30**A, while the core substrate **20** is placed on the organic adhesive layer **34** of the single-sided circuit board **30**B. The foregoing substrates are laminated on the core substrate in such a manner that the single-sided circuit boards **30**C and **30**D are inverted, that is, the organic adhesive layer **34** of the single-sided circuit board **30**C faces the core substrate **20**. Moreover, the organic adhesive layer **34** of the single-sided circuit board **30**D faces the single-sided circuit board **30**C. The lamination is performed while position alignment is being performed by inserting a guide pin (not shown) into a guide hole (not shown) formed around the single-sided circuit board **30** and the core substrate **20**. A portion of circle C of the laminated substrate shown in the drawing is indicated by enlarging the same in (M). The position alignment may be performed by an image process.

[0094] Finally, in process (L), the laminated substrates are heated to 150° C. to 200° C. by using a heating press and applied with pressure of 5 kgf/cm^2 to 100 kgf/cm^2, preferably 20 kgf/cm^2 to 50 kgf/cm^2. Thus, the single-sided circuit boards **30**A, **30**B, **30**C and **30**D and the core substrate **20** are integrated into a multilayer structure by one press molding operation. A portion of circle C of the laminated substrates shown in the drawing is shown in (N). Since the pressure is applied, the bump **38***a* of the single-sided circuit board **30**A squeezes out the non-hardened resin (the insulating resin) existing between the bump **38***a* and the conductive circuit **32***b* adjacent to the single-sided circuit board **30**B. Thus, the bump **38***a* is brought into contact with the conductive circuit **32***b* so that the connection between the bump **38***a* and the conductive circuit **32***b* is established. Similarly, the bumps **38***b*, **38***c* and **38***d* of the single-sided circuit board **30**B, **30**C and **30**D and the conductive circuit are connected to one another. Since also heat is applied simultaneously with exertion of the pressure, the adhesive layer **34** of the single-sided circuit board **30**A is hardened so that strong adhesion is realized with the single-sided circuit board **30**B. It is preferable that the heating press is vacuum heating press. As a result, the multilayer printed circuit board **10** described with reference to **FIG. 1** can be manufactured.

[0095] Another embodiment will now be described with reference to **FIG. 7**.

[0096] In process (B), a protective film **100** which is usually used as a mask serving in a process for printing conductive paste is bonded to a single-sided copper-clad laminate **40** which has been prepared in process (A) shown in **FIG. 7**. In process (C), an operation for laser-processing the single-sided copper-clad laminate **40** is performed so that non-penetrating holes are formed. For the protective film **100**, for example, a polyethylene terephthalate film (PET) having an adhesive layer formed on the surface

thereof may be employed. Deposition of plating onto the metal layer **42** must be prevented by bonding a mask **48** in process (D). As an alternative to this, the metal layers **42** are brought into hermetic contact with each other in process (E) to prevent contact with the electrolytic plating solution. In process (F) a portion of the non-penetrating holes is filled with electrolytic plating **46**. In process (G) conductive paste **460** is enclosed in residual spaces. In the foregoing embodiment, dispersion of the heights of the electrolytic plating can be corrected by using conductive paste **460** so that the heights of the bumps are uniform. As an alternative to the foregoing conductive paste, the metal having the low melting point can be enclosed.

[**0097**] An average charging rate of the electrolytic plating in the non-penetrating holes (heights t of electrolytic plating×100/depth T of the non-penetrating holes: refer to **FIG. 8** (L)) is not lower than 50% nor lower than 100%, preferably 55% to 95%, more preferably 60% to 90%.

[**0098**] The conductive paste **460** enclosed in the opening portions of the protective film **100** is formed into bumps. In process (H) a film **101** for protecting the conductive paste **460** is bonded. Then, the metal layer **42** is etched so that a conductive circuit is formed. Then, in the process (I) the film **101** is removed to expose the bumps formed by the conductive paste **460** so that a single-sided circuit board **30**E of the present invention is obtained.

[**0099**] It is preferable that the bumps made of the conductive paste is in a semi-hardened state. Since the conductive paste is hard if it is in the semi-hardened state, the conductive paste is able to penetrate the organic adhesive layer softened during the heat pressing process.

[**0100**] When the pressing process is performed, the conductive paste is deformed, causing the area of contact to be enlarged. As a result, the conduction resistance can be lowered and dispersion of the heights of the bumps can be corrected. **FIG. 9** shows an enlarged photograph of the structures of the via hole and the bump portion.

[**0101**] Then, the single-sided circuit substrate **30**E obtained by performing steps (A) to (I) are laminated in process (J) so that three layers for each side are placed opposite to each other through the adhesive layers **80**. The lamination is performed while position alignment is being performed by inserting a guide pin (not shown) into a guide hole (not shown) formed in the peripheries of the single-sided circuit board **30** and the core substrate **20**. The position alignment may be performed by performing an image process.

[**0102**] Then, the multilayer printed circuit board **10** structured in process (K) may be manufactured by performing heat pressing.

[**0103**] In the foregoing embodiment, the multilayer printed circuit boards have four laminated single-sided circuit boards **30** and six laminated single-sided circuit boards **30**, respectively. The single-sided circuit board according to the present invention may be applied to a multilayer printed circuit board having three layers or five or more layers. The single-sided circuit boards according to the present invention may be laminated on a single-sided printed circuit board, a double-sided printed circuit board, a double-sided through-hole printed circuit board or a multilayer printed circuit board to manufacture a multilayer printed circuit board.

[**0104**] Although the foregoing embodiment has the structure that the holes for forming the via holes are formed by the laser process, the holes may be formed by a mechanical method, such as drilling, punching or the like.

[**0105**] The multilayer printed circuit board manufactured by the single-sided circuit board according to the present invention may be subjected to a variety of usual processes to which the printed circuit board has been subjected. For example, formation of solder resist on the surface, nickel/gold plating, soldering, hole formation, a cavity forming process and plating of through holes may be performed.

[**0106**] As described above, the multilayer printed circuit board and a manufacturing method therefor according to the present invention are arranged such that the single-sided circuit boards each having a conductive circuit which incorporates a predetermined wiring pattern formed thereon are previously and individually manufactured. Therefore, inspection for detecting whether or not the conductive circuit or the like has a defective portion can be performed before the single-sided circuit boards are laminated. Hence it follows that only single-sided circuit boards free from any defect can be used in the laminating process. That is, the manufacturing method according to the present invention is able to reduce defects in the manufacturing process. As a result, the multilayer printed circuit board having the IVH structure can be manufactured with a high manufacturing yield by the single-sided circuit board according to the present invention.

[**0107**] Also, it is not required by single-sided circuit board according to the present invention to repeat the heating press operation while the prepreg is being laminated as distinct from the conventional technique. That is, the present invention enables heat pressing operation to be completed at a time such that a plurality of the single-sided circuit boards are laminated through the adhesive agents placed on the single-sided circuit boards. Therefore, it is free from a necessity for repeating the laminating process in which the complicated heat press is performed and the patterning process. Hence it follows that the multilayer printed circuit board having the IVH structure can efficiently be manufactured. Since the single-sided circuit boards are integrated with physical force exerted at the time of the pressing operation, the reliability of the connection can be improved.

[**0108**] Furthermore, in the present invention, in order to manufacture the single-sided circuit board, formation of the non-penetrating hole in the organic insulating base member is performed by the laser process. The previous formation of the conducting hole in the organic adhesive layer is not required. The necessity for simultaneously forming holes in the insulating base member and the adhesive layer by the laser process can be eliminated. That is, after the holes have been formed in the insulating base member by the laser process, the adhesive layer can be formed on the single-sided circuit board or the substrate having the conductive circuit. Therefore, the desmear process, which is performed after the holes have been formed can be performed before the adhesive layer is formed. As a result, the desmear process does not erode the organic adhesive layer.

[**0109**] Also in a case where the non-penetrating hole is filled with the electrolytic plating, the adhesive layer can be formed on the single-sided circuit board or the substrate having the conductive circuit after the non-penetrating hole

has been formed in the insulating base member by performing the laser process and the non-penetrating hole has been filled with the electrolytic plating. Therefore, the electrolytic plating solution and the adhesive layer are not made contact with each other. As a result, the erosion of the adhesive layer with the plating solution can be prevented.

[0110] Since the adhesive layer is not hardened until the heat pressing process which is the final process is performed, the adhesive layer easily deteriorates during the desmear process or the plating solution. The present invention has characteristics that the above-mentioned problem can be prevented and a reliable substrate can be easily formed.

[0111] Furthermore, in the single-sided board of the present invention, the via holes are formed by enclosing the electrolytic plating in the non-penetrating holes of the insulating base member. The projecting conductors made of the conductive paste or the metal having a low melting point are formed on the surfaces of the via holes formed on the surface of said insulating base member opposite to the surface on which conductive circuit has been formed. Therefore, since the conductive paste or the metal having a low melting point is deformed during the heat pressing and absorption of dispersion of the heights of the electrolytic plating can be realized, the multilayer printed circuit board which the defective connection can be prevented and is highly reliable in connection is obtained.

[0112] Moreover, a necessity for previously forming a conducting hole in the adhesive layer can be eliminated according to the present invention. Therefore, defective conduction caused from deviation in the positions of the hole in the adhesive layer and the projecting conductors provided for the organic insulating base member can be prevented.

[0113] In the present invention, the projecting conductors comprised the conductive paste or metal having a low melting point are formed on the via holes filled with the electrolytic plating. Therefore, the electrical connection between the upper and lower conductive layers can be easily established by penetrating the relatively thin organic adhesive layer on the multilayer printed wiring board. Therefore, the height and the diameter of each projecting conductor can be reduced. Hence it follows that the pitch between adjacent projecting conductors can be shortened. Therefore, the pitch between adjacent via holes can also be shortened. As a result, addressing to the raising of the density can be permitted.

What is claimed is:

1. A single-sided circuit substrate comprising: an insulating base member on either side of which a conductive circuit is formed, wherein said insulating base member has non-penetrating holes which reach said conductive circuit, via holes are formed by enclosing electrolytic plating in said non-penetrating holes, projecting conductors made of conductive paste or metal having a low melting point are formed on the surfaces of said via holes formed on the surface of said insulating base member opposite to the surface on which said conductive circuit has been formed.

2. A single-sided circuit substrate according to claim 1, wherein said non-penetrating holes are completely filled with electrolytic plating.

3. A single-sided circuit substrate according to claim 1 or **2**, wherein said non-penetrating holes are filled with the electrolytic plating to an average depth of 50% or higher of the depth of said non-penetrating holes and lower than 100% of the same.

4. A single-sided circuit substrate according to any one of claims 1 to 3, wherein said insulating base member is an organic insulating member.

5. A single-sided circuit substrate according to any one of claims 1 to 4, wherein said electrolytic plating is copper electrolytic plating.

6. A single-sided circuit substrate according to any one of claims 1 to 5, wherein said insulating member is a single-sided copper-clad laminate.

7. A method of manufacturing a single-sided circuit substrate at least comprising the steps (1) to (4):

(1) forming non-penetrating holes which reach a metal layer by a laser process in a insulating base member having said metal layer formed on either side thereof;

(2) enclosing electrolytic plating into said non-penetrating holes formed in step (1) to form via holes;

(3) forming a conductive circuit by etching said metal layer; and

(4) forming projecting conductors made of conductive paste or metal having a low melting point on the surfaces of said via holes formed on the surface of said insulating base member opposite to the surface on which said conductive circuit has been formed so that a single-sided circuit substrate is obtained.

8. A method of manufacturing a single-sided circuit substrate at least comprising the steps (1) to (3):

(1) forming non-penetrating holes which reach a metal layer by a laser process in an insulating base member having said metal layer formed on either side thereof;

(2) enclosing electrolytic plating into said non-penetrating holes formed in step (1) to form via holes and forming projecting conductors made of conductive paste or metal having a low melting point on the surfaces of said via holes formed on the surface of said insulating base member opposite to the surface on which said conductive circuit has been formed; and

(3) etching said metal layer to form a conductive circuit so that a single-sided circuit substrate is obtained.

9. A method of manufacturing a single-sided circuit substrate according to claim 7 or **8**, wherein said step (1) is performed such that a film is bonded to said insulating base member having the metal layer formed on either side thereof and non-penetrating holes which penetrate said film and said insulating base member to reach said metal layer are formed by a laser process.

10. A method of manufacturing a single-sided circuit substrate according to any one of claims 7 to 9, wherein said insulating base member is an organic insulating base member.

11. method of manufacturing a single-sided circuit substrate according to any one of claims 7 to 10, wherein said insulating base member is a single-sided copper cladding laminate.

12. A single-sided circuit substrate according to any one of claims 7 to 11, wherein said electrolytic plating is copper electrolytic plating.

13. A method of manufacturing a single-sided circuit substrate according to any one of claims 7 to 12, wherein said projecting conductors are formed by printing conductive paste.

14. A method of manufacturing a single-sided circuit substrate according to any one of claims 7 to 13, wherein said projecting conductor are formed by printing metal paste having a low melting point, plating of metal having a low melting point or immersion of metal having a low melting point into molten solution.

* * * * *