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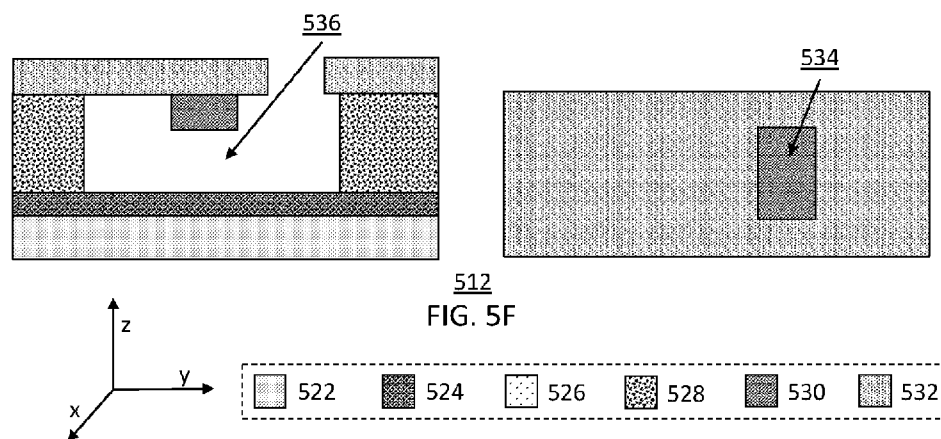
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- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- of inventorship (Rule 4.17(iv))

(54) Title: INVERTED MICROSTRIP TRANSMISSION LINES FOR QUBITS



(57) Abstract: Described herein are new transmission line structures, and methods for fabrication thereof, for use as resonators and non-resonant interconnects in quantum circuits. In one aspect of the present disclosure, a proposed transmission line structure includes a substrate, a ground structure disposed over the substrate, and a signal path (i.e. a strip of a conductive material, preferably a super-conductive material) suspended over the ground structure and supported by a signal path support layer. The proposed structure further includes an opening in the signal path support layer, the opening being indicative of using the fabrication process described herein for forming the proposed structure. Transmission line structures as proposed herein could be used for providing microwave connectivity to, from, or/and between the qubits, or to set the frequencies that address individual qubits.



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INVERTED MICROSTRIP TRANSMISSION LINES FOR QUBITSTechnical Field

[0001] This disclosure relates generally to the field of quantum computing, and more specifically, to transmission lines for use in quantum circuits and to methods of fabricating thereof.

Background

[0002] Quantum computing refers to the field of research related to computation systems that use quantum mechanical phenomena to manipulate data. These quantum mechanical phenomena, such as superposition (in which a quantum variable can simultaneously exist in multiple different states) and entanglement (in which multiple quantum variables have related states irrespective of the distance between them in space or time), do not have analogs in the world of classical computing, and thus cannot be implemented with classical computing devices.

Brief Description of the Drawings

[0003] To provide a more complete understanding of the present disclosure and features and advantages thereof, reference is made to the following description, taken in conjunction with the accompanying figures, wherein like reference numerals represent like parts, in which:

[0004] FIG. 1 provides a schematic illustration of an example quantum circuit, according to some embodiments of the present disclosure.

[0005] FIG. 2 provides a schematic illustration of an example quantum computing device that may include any of the transmission lines described herein, according to some embodiments of the present disclosure.

[0006] FIGs. 3A and 3B provide a schematic illustration of a coplanar waveguide provided over a substrate.

[0007] FIG. 4 provides a schematic illustration of an inverted microstrip transmission line fabricating using a conventional flip-chip approach.

[0008] FIGs. 5A-5F provide a schematic illustration of fabricating inverted microstrip transmission lines with chimneys, according to some embodiments of the present disclosure.

[0009] FIG. 6 provides a flow chart of a method for fabricating inverted microstrip transmission lines with chimneys, according to some embodiments of the present disclosure.

[0010] FIG. 7 provides a schematic illustration of an TEM/SEM image with inverted microstrip transmission lines with a chimney, according to some embodiments of the present disclosure.

Detailed Description

[0011] As previously described herein, quantum computing, or quantum information processing, refers to the field of research related to computation systems that use quantum-mechanical phenomena to manipulate data. One example of quantum-mechanical phenomena is the principle of quantum superposition, which asserts that any two or more quantum states can be added together, i.e. superposed, to produce another valid quantum state, and that any quantum state can be represented as a sum of two or more other distinct states. Quantum entanglement is another example of quantum-mechanical phenomena. Entanglement refers to groups of particles being generated or interacting in such a way that the state of one particle becomes intertwined with that of the others. Furthermore, the quantum state of each particle cannot be described independently. Instead, the quantum state is given for the group of entangled particles as a whole. Yet another example of quantum-mechanical phenomena is sometimes described as a “collapse” because it asserts that when we observe (measure) particles, we unavoidably change their properties in that, once observed, the particles cease to be in a state of superposition or entanglement (i.e. by trying to ascertain anything about the particles, we collapse their state).

[0012] Put simply, superposition postulates that a given particle can be simultaneously in two states, entanglement postulates that two particles can be related in that they are able to instantly coordinate their states irrespective of the distance between them in space and time, and collapse postulates that when one observes a particle, one unavoidably changes the state of the particle and its’ entanglement with other particles. These unique phenomena make manipulation of data in quantum computers significantly different from that of classical computers (i.e. computers that use phenomena of classical physics). Classical computers

encode data into binary values, commonly referred to as bits. At any given time, a bit is always in only one of two states – it is either 0 or 1. Quantum computers use so-called quantum bits, referred to as qubits (both terms “bits” and “qubits” often interchangeably refer to the values that they hold as well as to the actual devices that store the values). Similar to a bit of a classical computer, at any given time, a qubit can be either 0 or 1. However, in contrast to a bit of a classical computer, a qubit can also be 0 and 1 at the same time, which is a result of superposition of quantum states. Entanglement also contributes to the unique nature of qubits in that input data to a quantum processor can be spread out among entangled qubits, allowing manipulation of that data to be spread out as well: providing input data to one qubit results in that data being shared to other qubits with which the first qubit is entangled.

[0013] Compared to well-established and thoroughly researched classical computers, quantum computing is still in its infancy, with the highest number of qubits in a solid-state quantum processor currently being about 10. One of the main challenges resides in protecting qubits from decoherence so that they can stay in their information-holding states long enough to perform the necessary calculations and read out the results. For this reason, materials, structures, and fabrication methods used for building quantum circuits continuously focus on reducing spurious (i.e. unintentional and undesirable) two-level systems (TLS's), thought to be the dominant source of qubit decoherence. In general, as used in quantum mechanics, a two-level (also referred to as “two-state”) system is a system that can exist in any quantum superposition of two independent and physically distinguishable quantum states. Another challenge that is unique to quantum computing is the ability to provide substantially lossless connectivity between qubits at very low powers, e.g. as low as a power of a single photon that may be present in a particular resonator interconnecting two qubits.

[0014] As the foregoing illustrates, ability to manipulate and read out quantum states, making quantum-mechanical phenomena visible and traceable, and ability to deal with and improve on the fragility of quantum states of a qubit present unique challenges not found in classical computers. These challenges explain why so many current efforts of the industry and the academics continue to focus on a search for new and improved physical systems whose functionality could approach that expected of theoretically designed qubits. Physical systems for implementing qubits that have been explored until now include e.g. superconducting qubits, quantum dot qubits, single trapped ion qubits, Silicon (Si) photon polarization qubits, etc.

[0015] Quantum circuits based on various physical systems for implementing qubits use microwave transmission line resonators to control the qubits. In order to provide substantially lossless connectivity to, from, and between the qubits, such resonators are typically made from superconducting materials. One conventional approach to fabricating such resonators is to employ a coplanar waveguide architecture to implement the resonators. In an alternative approach, resonators having an inverted microstrip line architecture fabricated using a flip-chip approach as used in IC manufacturing of classical computers have also been proposed.

[0016] Inventors of the present disclosure realized that, when used in quantum circuits, both of these approaches have drawbacks.

[0017] Embodiments of the present disclosure propose new transmission line structures for use as resonators, as well as for use as non-resonant interconnects, in quantum circuits. Fabrication techniques for forming such structures are also disclosed.

[0018] In one aspect of the present disclosure, a proposed transmission line structure includes a substrate, a ground structure disposed over the substrate, and a signal path (i.e. a strip of a conductive material, preferably a superconductive material) suspended over the ground structure and supported by a signal path support layer. In other words, the signal path is suspended from the signal path support layer and is separated from the ground structure by a gap, forming a transmission line structure similar to an inverted microstrip line. The proposed structure further includes an opening in the signal path support layer, the opening referred to herein as a “chimney” and being indicative of using the fabrication process described herein for forming the proposed structure.

[0019] In general, transmission line structures as proposed herein could be used for providing microwave connectivity to, from, or/and between the qubits, or to set the frequencies that address individual qubits.

[0020] For the purposes of the present disclosure, the terms such as “upper,” “lower,” “over,” “under,” “between,” and “on” as used herein refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first

layer "on" a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening layers.

[0021] The phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges. As used herein, the notation "A/B/C" means (A), (B), and/or (C).

[0022] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. The accompanying drawings are not necessarily drawn to scale.

[0023] As used herein, terms indicating what may be considered an idealized behavior, such as e.g. "superconducting" or "lossless", are intended to cover functionality that may not be exactly ideal but is within acceptable margins for a given application. For example, a certain level of loss, either in terms of non-zero electrical resistance or non-zero amount of spurious TLS's may be acceptable such that the resulting materials and structures may still be referred to by these "idealized" terms. One metric of interest may be the decay rate associated with these losses (e.g. losses either from TLS's or residual resistance), and as long as the decay rate associated with these mechanisms is not worse than needed in order to achieve a fault-tolerant quantum calculation, then the losses are deemed acceptable and the idealized terms (e.g. superconducting or lossless) - appropriate. Specific values associated with an acceptable decay are expected to change over time as fabrication precision will improve and as fault-tolerant schemes may become more tolerant of higher decay rates. An adapted version of this metric, as well as other metrics suitable for a particular application in determining whether certain behavior may be referred to using idealized terms, are within the scope of the present disclosure.

[0024] Furthermore, while the present disclosure includes references to microwave signals, this is done only because current qubits are designed to work with such signals because the energy in the microwave range is higher than thermal excitations at the temperature that qubits are operated at. In addition, techniques for the control and measurement of microwaves are well known. For these reasons, typical frequencies of qubits are in 5-10 gigahertz (GHz) range, in order to be higher than thermal excitations, but low enough for ease of microwave engineering. However, advantageously, because excitation energy of qubits is controlled by the circuit elements, qubits can be designed to have any frequency. Therefore, in general, qubits could be designed to operate with signals in other ranges of electromagnetic spectrum and embodiments of the present disclosure could be modified accordingly. All of these alternative implementations are within the scope of the present disclosure.

[0025] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0026] Furthermore, in the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present disclosure may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present disclosure may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0027] Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present disclosure. However, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation. Operations described may be performed in a different order from the described

embodiment(s). Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0028] FIG. 1 provides a schematic illustration of a quantum circuit 100 that may include any of the transmission lines described herein, according to some embodiments of the present disclosure. As shown in FIG. 1, an exemplary quantum circuit 100 includes a plurality of qubits 102. The qubits 102 may be implemented as any of the suitable qubits, such as e.g. transmons, quantum well qubits, or quantum dot qubits.

[0029] As also shown in FIG. 1, an exemplary quantum circuit 100 typically includes a plurality of resonators 104, e.g. coupling and readout resonators.

[0030] Coupling resonators allow coupling different qubits together in order to realize quantum logic gates. A coupling resonator may be implemented as a microwave transmission line that includes capacitive connections to ground on both sides (i.e. a half wavelength resonator), which results in oscillations (resonance) within the transmission line. Each side of a coupling resonator is coupled, either capacitively or inductively, to a respective (i.e. different) qubit by being in sufficient proximity to the qubit. Because each side of a coupling resonator has coupling with a respective different qubit, the two qubits are coupled together through the coupling resonator. In this manner, state of one qubit depends on the state of the other qubit, and the other way around. Thus, coupling resonators may be employed in order to use a state of one qubit to control a state of another qubit, a necessary functionality for implementing logic gates.

[0031] Readout resonators may be used to read the state(s) of qubits. In some embodiments, a corresponding readout resonator may be provided for each qubit. A readout resonator is similar to a coupling resonator in that it may be implemented as a transmission line that includes a capacitive connection to ground on one side. On the other side, a readout resonator may either have a capacitive connection to ground (for a half wavelength resonator) or may be shorted to the ground (for a quarter wavelength resonator), which also results in oscillations within the transmission line, with the resonant frequency of the oscillations being close to the frequency of the qubit. A readout resonator is coupled to a qubit by being in sufficient proximity to the qubit, again, either through capacitive or inductive coupling. Due to a coupling between a readout resonator and a qubit, changes in the state of the qubit result in

changes of the resonant frequency of the readout resonator. In turn, changes in the resonant frequency of the readout resonator can be read externally via e.g. wirebonding pads.

[0032] At least some of the resonators 104 shown in FIG. 1 may be implemented as resonant transmission lines in the form of inverted microstripline structures with chimneys as described herein.

[0033] Coupling resonators and readout resonators 104 may be considered as interconnects for supporting propagation of microwave signals in a quantum circuit. In addition to such resonant structures, a typical quantum circuit also includes non-resonant microwave transmission lines for providing microwave signals to different quantum circuit elements and components, such as e.g. flux bias lines, microwave lines, or drive lines, collectively indicated in FIG. 1 as non-resonant transmission lines 106. At least some of the non-resonant transmission lines 106 shown in FIG. 1 may be implemented as non-resonant transmission lines in the form of stripline or microstrip line structures as described herein.

[0034] In general, resonators 104 differ from non-resonant microwave transmission lines 106 in that the resonators are configured for capacitive coupling to other circuit elements at one or both ends in order to have resonant oscillations, whereas non-resonant transmission lines such as e.g. flux bias lines and microwave lines may be similar to conventional microwave transmission lines because there is no resonance in these lines.

[0035] The non-resonant transmission lines may also be considered as being included within a broad category of interconnects.

[0036] Further, any other connections for providing microwave or other electrical signals to different quantum circuit elements and components, such as e.g. connections between electrodes of various circuit components, or connections between two ground lines of a particular transmission line for equalizing electrostatic potential on the two ground lines, are also referred to herein as interconnects. Still further, the term “interconnect” may also be used to refer to elements providing electrical interconnections to/from/between quantum circuit elements and components and non-quantum circuit elements, which may also be provided in a quantum circuit, as well as to electrical interconnections between various non-quantum circuit elements provided in a quantum circuit. Examples of non-quantum circuit

elements which may be provided in a quantum circuit may include various analog and/or digital systems, e.g. analog to digital converters, mixers, multiplexers, amplifiers, etc.

[0037] In various embodiments, the interconnects included in a quantum circuit could have different shapes and layouts. In general, the term “line” as used herein in context of signal lines or transmission lines does not imply straight lines, unless specifically stated so. For example, some transmission lines or parts thereof (e.g. conductor strips of transmission lines) may comprise more curves and turns while other transmission lines or parts thereof may comprise less curves and turns, and some transmission lines or parts thereof may comprise substantially straight lines. In some embodiments, various interconnects may intersect one another, in such a manner that they don’t make an electrical connection, which can be done by using e.g. a bridge, bridging one interconnect over the other.

[0038] In some embodiments, materials forming the interconnects include aluminum (Al), niobium (Nb), niobium nitride (NbN), titanium nitride (TiN), and niobium titanium nitride (NbTiN), all of which are particular types of superconductors. However, in various embodiments, other suitable superconductors may be used as well.

[0039] The qubits 102, the resonators 104, and the non-resonant transmission lines 106 of the quantum circuit 100 may be provided on, over, or at least partially embedded in a substrate (not shown in FIG. 1).

[0040] In various embodiments, quantum circuits such as the one shown in FIG. 1 may be used to implement components associated with a quantum integrated circuit (IC). Such components may include those that are mounted on or embedded in a quantum IC, or those connected to a quantum IC. The quantum IC may be either analog or digital and may be used in a number of applications within or associated with quantum systems, such as e.g. quantum processors, quantum amplifiers, quantum sensors, etc., depending on the components associated with the integrated circuit. The integrated circuit may be employed as part of a chipset for executing one or more related functions in a quantum system.

[0041] FIG. 2 provides an illustration of an exemplary quantum computing device that may include any of the transmission lines in the form of inverted microstripline structures with chimneys described herein, e.g. a quantum computer, 200, according to some embodiments of the present disclosure.

[0042] A number of components are illustrated in FIG. 2 as included in the quantum computing device 200, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the quantum computing device 200 may be attached to one or more printed circuit boards (e.g., a motherboard). In some embodiments, various ones of these components may be fabricated onto a single system-on-a-chip (SoC) die. Additionally, in various embodiments, the quantum computing device 200 may not include one or more of the components illustrated in FIG. 2, but the quantum computing device 200 may include interface circuitry for coupling to the one or more components. For example, the quantum computing device 200 may not include a display device 206, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 206 may be coupled. In another set of examples, the quantum computing device 200 may not include an audio input device 218 or an audio output device 208, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 218 or audio output device 208 may be coupled.

[0043] The quantum computing device 200 may include a processing device 202 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 202 may include a quantum processing device 226 (e.g., one or more quantum processing devices), and a non-quantum processing device 228 (e.g., one or more non-quantum processing devices). The quantum processing device 226 may include one or more of the quantum circuits 100 disclosed herein, and may perform data processing by performing operations on the qubits 102 that may be generated in the quantum circuits 100, and monitoring the result of those operations. For example, as discussed above, different qubits may be allowed to interact, the quantum states of different qubits may be set or transformed, and the quantum states of qubits may be read (e.g., by another qubit via a coupling resonator or externally via a readout resonator). The quantum processing device 226 may be a universal quantum processor, or specialized quantum processor configured to run one or more particular quantum algorithms. In some embodiments, the quantum processing device 226 may execute algorithms that are particularly suitable for quantum computers, such as cryptographic algorithms that utilize prime factorization, encryption/decryption, algorithms

to optimize chemical reactions, algorithms to model protein folding, etc. The quantum processing device 226 may also include support circuitry to support the processing capability of the quantum processing device 226, such as input/output channels, multiplexers, signal mixers, quantum amplifiers, and analog-to-digital converters.

[0044] As noted above, the processing device 202 may include a non-quantum processing device 228. In some embodiments, the non-quantum processing device 228 may provide peripheral logic to support the operation of the quantum processing device 226. For example, the non-quantum processing device 228 may control the performance of a read operation, control the performance of a write operation, control the clearing of quantum bits, etc. The non-quantum processing device 228 may also perform conventional computing functions to supplement the computing functions provided by the quantum processing device 226. For example, the non-quantum processing device 228 may interface with one or more of the other components of the quantum computing device 200 (e.g., the communication chip 212 discussed below, the display device 206 discussed below, etc.) in a conventional manner, and may serve as an interface between the quantum processing device 226 and conventional components. The non-quantum processing device 228 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices.

[0045] The quantum computing device 200 may include a memory 204, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the states of qubits in the quantum processing device 226 may be read and stored in the memory 204. In some embodiments, the memory 204 may include memory that shares a die with the non-quantum processing device 228. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random-access memory (STT-MRAM).

[0046] The quantum computing device 200 may include a cooling apparatus 224. The cooling apparatus 224 may maintain the quantum processing device 226 at a predetermined low

temperature during operation to reduce the effects of scattering in the quantum processing device 226. This predetermined low temperature may vary depending on the setting; in some embodiments, the temperature may be 5 degrees Kelvin or less. In some embodiments, the non-quantum processing device 228 (and various other components of the quantum computing device 200) may not be cooled by the cooling apparatus 224, and may instead operate at room temperature. The cooling apparatus 224 may be, for example, a dilution refrigerator, a helium-3 refrigerator, or a liquid helium refrigerator.

[0047] In some embodiments, the quantum computing device 200 may include a communication chip 212 (e.g., one or more communication chips). For example, the communication chip 212 may be configured for managing wireless communications for the transfer of data to and from the quantum computing device 200. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0048] The communication chip 212 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 1402.11 family), IEEE 1402.16 standards (e.g., IEEE 1402.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 1402.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 1402.16 standards. The communication chip 212 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 212 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 212 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives

thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 212 may operate in accordance with other wireless protocols in other embodiments. The quantum computing device 200 may include an antenna 222 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0049] In some embodiments, the communication chip 212 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 212 may include multiple communication chips. For instance, a first communication chip 212 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 212 may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 212 may be dedicated to wireless communications, and a second communication chip 212 may be dedicated to wired communications.

[0050] The quantum computing device 200 may include battery/power circuitry 214. The battery/power circuitry 214 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the quantum computing device 200 to an energy source separate from the quantum computing device 200 (e.g., AC line power).

[0051] The quantum computing device 200 may include a display device 206 (or corresponding interface circuitry, as discussed above). The display device 206 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0052] The quantum computing device 200 may include an audio output device 208 (or corresponding interface circuitry, as discussed above). The audio output device 208 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0053] The quantum computing device 200 may include an audio input device 218 (or corresponding interface circuitry, as discussed above). The audio input device 218 may include any device that generates a signal representative of a sound, such as microphones, microphone

arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0054] The quantum computing device 200 may include a global positioning system (GPS) device 216 (or corresponding interface circuitry, as discussed above). The GPS device 216 may be in communication with a satellite-based system and may receive a location of the quantum computing device 200, as known in the art.

[0055] The quantum computing device 200 may include an other output device 210 (or corresponding interface circuitry, as discussed above). Examples of the other output device 210 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0056] The quantum computing device 200 may include an other input device 220 (or corresponding interface circuitry, as discussed above). Examples of the other input device 220 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0057] The quantum computing device 200, or a subset of its components, may have any appropriate form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device.

[0058] In order to highlight the advantages offered by novel quantum circuit transmission line structures proposed herein, it would be helpful to first explain how conventional quantum circuit resonator structures are implemented.

[0059] As mentioned above, conventionally, quantum circuit resonators have been implemented as coplanar waveguides. An example of a coplanar waveguide is shown in FIGs. 3A and 3B providing, respectively, a perspective and a cross-section illustrations. In FIGs. 3A and 3B, a coplanar waveguide includes two ground planes 304 and 308 and a conductor strip

306 provided in the middle, between the two ground planes. The conductor strip 306 and the ground planes 304 and 308 all lie in the same plane over a dielectric substrate 302. FIG. 3A indicates a height h , which refers to the thickness of the substrate 302, a strip width W of the signal line 306, and slot spaces S between the signal line 306 and each of the ground planes 304 and 308. The height h , strip width W , and slot spaces S are parameters that define characteristics of a coplanar waveguide transmission line, such as e.g. impedance of the transmission line and electromagnetic field distribution.

[0060] FIG. 3B illustrates exemplary electromagnetic field distribution in a coplanar waveguide architecture, where curved arrows illustrate directions of an exemplary electric field. As can be seen in FIG. 3B, in a coplanar waveguide, electromagnetic energy is concentrated immediately below the transmission line, i.e. within the dielectric substrate 302. Some of that energy can leak out above the transmission line (i.e. in air), which is also illustrated in FIG. 3B, but that leakage can be controlled by having a substrate height h , being twice that of the strip width S . Thus, electromagnetic field could be concentrated mainly at an interface between the superconducting material of the coplanar waveguide and the dielectric of the substrate 302, and in the dielectric itself. However, such concentration of the electromagnetic field may be sub-optimal for quantum circuits because superconductor-dielectric interfaces may be one of the causes of spurious TLS's, leading to qubit decoherence.

[0061] As also mentioned above, resonators having an inverted microstrip line architecture fabricated using a flip-chip approach as used in IC manufacturing of classical computers have also been proposed. The flip-chip approach involves forming a ground plane of a microstrip transmission line on one wafer/chip, forming one or more signal lines of the transmission line on another wafer/chip, and then bonding an inverted latter chip with the former chip, i.e. the two chips are bonded with the ground plane and the signal line(s) facing one another. Bonding of two chips is not without issues. One potential problem is that bonding may cause warpage when not performed exactly at bonding points. Another problem is that bonding of two chips leads to variation in distances between the different signal lines and the ground plane, leading to variations in characteristic impedances of transmission lines associated with different signal lines. An example of inverted microstrip transmission lines fabricated using a flip-chip approach is shown in FIG. 4 illustrating a first substrate 402 having a ground plane 406 provided thereon, bonded with a second substrate 412 having multiple signal lines. The multiple signal lines are illustrated in the example of FIG. 4 with four signal lines 416-1, 416-2,

416-3, and 416-4. As shown in FIG. 4, bonding of the substrates 402 and 412 may result in a situation where some or all of the distances h_1 , h_2 , h_3 , and h_4 between each signal line 406 and the ground plane 406 are different. Different distances h_1 - h_4 result in unwanted differences in impedances of the inverted microstrip lines of different signal lines 406-1 through 406-4.

[0062] FIGs. 5A-5F provide a schematic illustration of fabricating inverted microstrip line transmission lines for qubits, according to some embodiments of the present disclosure. A legend provided within a dashed box at the bottom of FIGs. 5A-5F illustrates patterns used to indicate different elements shown in FIGs. 5A-5F, so that the FIGs are not cluttered by many reference numerals. FIGs. 5A-5F will now be described with reference to FIG. 6 providing a flow chart of a method 600 for fabricating suspended Josephson Junctions, according to some embodiments of the present disclosure. In particular, FIGs. 5A-5F illustrate a sequence of structures 502, 504, 506, 508, 510, and 512, each of which is a result of a corresponding one of different subsequent fabrication steps 602, 604, 606, 608, 610, and 612 shown in FIG. 6. Furthermore, each of FIGs. 5A-5F provides two views of the same structure. Namely, the view on the left side of each of FIGs. 5A-5F is a cross-sectional view with a cross-section of the structures taken along a y-z plane, as e.g. shown for the perspective drawing of a transmission line shown in FIG. 3A, while the view on the right side of each of FIGs. 5A-5F is a top-down view of an x-y plane.

[0063] Although the operations discussed below with reference to the method 600 are illustrated in a particular order and depicted once each, these operations may be repeated or performed in a different order (e.g., in parallel), as suitable. Additionally, various operations may be omitted, as suitable. Various operations of the method 600 may be illustrated with reference to one or more of the embodiments discussed above, but the method 600 may be used to manufacture any suitable quantum circuit element comprising one or more inverted microstrip lines with one or more chimneys (including any suitable ones of the embodiments disclosed herein).

[0064] The method 600 may begin with providing a layer of insulating sacrificial material 526 on a ground plane conducting layer 524 provided over a substrate 522 (process 602 of FIG. 6, result of which is illustrated with a structure 502 of FIG. 5A). The substrate 522 may comprise any substrate suitable for housing quantum circuit components, e.g. using some of the

considerations for choosing a substrate as described above. The ground plane conductor 524 may comprise any conducting or superconducting material suitable for serving as an interconnect in a quantum circuit, such as e.g. aluminum (Al), niobium (Nb), niobium nitride (NbN), niobium titanium nitride (NbTiN), titanium nitride (TiN), molybdenum rhenium (MoRe), etc., or any alloy of two or more superconducting/conducting materials.

[0065] The ground plane conductor 524 may be deposited over the substrate using any known techniques for depositing conducting/superconducting materials, possibly in combination with patterning. In various embodiments, techniques for depositing conducting/superconducting layer for forming the ground plane conductor 524 may include e.g. physical vapor deposition (e.g. evaporative deposition, magnetron sputtering, or e-beam deposition), chemical vapor deposition, or electroplating. In various embodiments, any kind of conventional patterning techniques may be used to form ground plane conductor 524 in the desired locations on the substrate 522, such as e.g. techniques employing photoresist or other masks defining the dimensions and location of the future ground plane conductor 524.

[0066] Since the sacrificial layer 526 will need to later be etched to achieve undercutting of the sacrificial material under the signal path line of an inverted microstrip transmission line to provide a gap between at least a portion of the signal path line and the ground plane, e.g. using isotropic etching, etching properties of potential candidate materials are to be considered when selecting a suitable material to be used as the sacrificial layer 526. Besides appropriate etching characteristics, some other considerations in selecting a suitable material may include e.g. possibilities of smooth film formation, low shrinkage and outgassing, and good dielectric properties (such as e.g. low electrical leakage, suitable value of a dielectric constant, and thermal stability). Examples of dielectric materials that may be used as the sacrificial material of the sacrificial layer 526 include, but are not limited to, silicon dioxide (SiO₂), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass.

[0067] In some embodiments, the sacrificial material 526 may be provided as a layer of oxide by oxidizing the top surface of the ground plane conductor 524. In other embodiments, the sacrificial material 526 may include an oxide deposited over the ground plane conductor 524 using e.g. chemical vapor deposition or/and plasma-enhanced chemical vapor deposition, as

typically done in conventional processing. In still other embodiments, the sacrificial material 526 may include a dielectric material formed over the ground plane conductor 524 using coating techniques involving cross-linking of liquid precursors into solid dielectric materials.

[0068] A thickness of the sacrificial layer 526 (i.e. a dimension of the layer 526 in the direction of z-axis as illustrated in FIGs. 5A-5F) would depend on e.g. the desired distance between the signal line path and the ground plane conductor of the future inverted microstrip line. For example, the sacrificial layer 526 may have a thickness between e.g. 10 and 500 nm, typically for qubit applications between 50 and 100 nm.

[0069] The method 600 may then proceed with enclosing an area of the sacrificial layer 526 with an etch-resistant material 528 extending from a surface of the sacrificial layer to the ground plane conductor 524 (process 604 of FIG. 6, result of which is illustrated with a structure 504 of FIG. 5B). Dimensions and a shape of an area enclosed with the etch-resistant material 528 (i.e. the footprint of the enclosed area in the x-y plane as illustrated in FIGs. 5A-5F) would depend on e.g. the desired location and shape of the signal line of the future inverted microstrip line. For example, dimensions of the area enclosed with the etch-resistant material 528 in the x- and y-directions could be, respectively, between 200 and 100000 nm for both the x-axis and y-axis.

[0070] In various embodiments, the etch-resistant material 528 may include any material suitable to resist the isotropic etch of a subsequent etching process (process 612 of FIG. 6). For example, the etch-resistant material 528 may include silicon nitride.

[0071] The process 604 of enclosing an area of the sacrificial layer with the etch-resistant material may include e.g. chemical vapor deposition or/and plasma-enhanced chemical vapor deposition, as typically done in conventional processing.

[0072] Next, one or more signal line/paths are formed at the surface of the sacrificial layer 526 within the area enclosed with the etch-resistant material (process 606 of FIG. 6, result of which is illustrated with a structure 506 of FIG. 5C). FIGs. 5C-5F illustrate an example with only one signal line 530 formed within a structure, but multiple such signal lines may be formed within a single enclosed area of the sacrificial material, in order to form multiple inverted microstrip transmission lines, as e.g. multiple lines shown in FIG. 4.

[0073] In some embodiments, the signal line 530 may be formed using any known dopant implantation techniques. For example, parts of the sacrificial material 526 enclosed with the etch-resistant material 528 where the signal line 530 is to be provided may be doped with phosphorus (P) or arsenic (As) to doping concentrations ranging $1e18$ to $1e21$, including all values and ranges therein, e.g. to about $1e20$. As a result, doped regions such as the region of the signal line 530 could be made superconductive, as suitable for superconducting interconnects, e.g. resonators, employed in quantum circuits.

[0074] In other embodiments, the signal line 530 may be formed by, first, etching parts of the sacrificial material 526 enclosed with the etch-resistant material 528 where the signal line 530 is to be provided, then depositing the superconducting/conducting material using any of the techniques described above, followed by planarizing of the surface to bring the surface of the signal line 530 to the same level as the surface of the sacrificial material 526, as shown in FIG. 5C.

[0075] Any of the known patterning techniques, such as e.g. photoresist patterning techniques, may be used to define the location and the shape of the signal line(s) 530.

[0076] Next, the method 600 may proceed with providing a signal path support layer 532 over the area enclosed with the etch-resistant material (i.e. over the surface of the sacrificial layer 526 and the signal path 530) (process 608 of FIG. 6, result of which is illustrated with a structure 508 of FIG. 5D). In some embodiments, the signal path support layer 532 may be formed of amorphous silicon (a-Si) provided using e.g. plasma-enhanced chemical vapor deposition, as typically done in conventional processing.

[0077] The signal path support layer 532 may then be patterned to form a window in the layer 532 for performing an etch of the sacrificial layer 526 under at least portion of the signal path 530 through the window (process 610 of FIG. 6, result of which is illustrated with a structure 510 of FIG. 5E). Again, any of the known patterning techniques, such as e.g. photoresist patterning techniques, may be used to define a location of the etching window. FIG. 5E illustrates the signal path support layer 532 having a window 534. In other embodiments, multiple such windows may be provided for a single enclosed area of the sacrificial material 526. Such windows may be referred to as “chimneys” to represent the fact that compounds

formed as a result of etching the sacrificial material 526 may be extracted from the enclosed area via these windows.

[0078] Number, dimensions and shape(s) of the chimneys (i.e. the footprint of the etching windows in the x-y plane as illustrated in FIGs. 5A-5F) would depend on e.g. the mechanical strength of support layer 532, and the horizontal etching ability of the etch to remove the sacrificial material 526. In some embodiments, dimensions of the 534 in the x- and y-directions could be, respectively, between 50 and 10000 nm for both the x-axis and y-axis. The range indicated is rather large to highlight the fact that the dimensions (as well as the number and shape(s)) of chimneys can vary a lot, depending on a particular application. In general, a chimney should be large enough so that the etchant can get into the opening and remove the sacrificial material, but not so large that the support material would collapse or bend.

[0079] Next, the sacrificial material 526 is etched through the window 534 to provide a gap between the signal path 530 and the ground plane conductor structure 524 (process 612 of FIG. 6, result of which is illustrated with a structure 612 of FIG. 5F). Preferably, the etching process used is an isotropic etch so that at least a portion of the sacrificial material under the signal path 530 is also etched, even though it is not exposed via the window 534 (i.e. at least a portion of the sacrificial material under the signal path 530 is undercut). Isotropic etching etches in multiple directions (both vertically and horizontally), unlike e.g. dry etching which only etches in a single direction, and, therefore, can be used to achieve undercutting of the sacrificial material 526 under the signal path 530, thereby providing a void or a gap between the signal path 530 and the ground plane conductor 524. Any substance suitable for isotropically etching the sacrificial material 526 may be used. In various embodiments, an etchant may be e.g. corrosive liquid, such as e.g. hydrofluoric acid (HF) or a chemically active ionized gas (i.e. plasma). As a result of the isotropic etching, a gap is formed at least under a portion of, but preferably under the entire, signal path 530 according to one embodiment. FIG. 5F illustrates this with a gap 536 under all of the signal path 530. Note that the left side drawings of FIG. 5F illustrates the gap 536 explicitly, while the view of the right side drawing of this figure implies having the gap 536 because it shows that the window 534 exposes the ground plane conductor 524 (as opposed to e.g. the right side drawing of FIG. 5E showing that the window 534 exposes the sacrificial material 526).

[0080] In some embodiments, the gap 536 may comprise vacuum since fabrication and operation of the quantum systems is typically carried out under vacuum. In this context, it is understood that “vacuum” is an idealized term in that a perfect vacuum (i.e. zero pressure) can never be achieved in practical situations. Therefore, the term “vacuum” is used to cover non-zero pressures as long as they are sufficiently low to be considered nearly vacuum. In other embodiments, the gap 536 could contain air or any other gas or a mixture of gasses.

[0081] As can be seen in FIG. 5F, due to the isotropic etching, both the x- and y- dimensions of the opening 536 would typically be greater than those of the window 534. For example, dimensions of the opening 536 in the x- and y-directions could be, between 50 and 2000 nm larger than the window 534 in the signal path support layer 532.

[0082] FIG. 7 provide a schematic illustration of a cross-section 700 of a structure 700 comprising a plurality, namely three, of signal lines 730-1 through 730-3 suspended over a ground plane conductor 724, according to some embodiments of the present disclosure. As can be seen, FIG. 7 is drawn to reflect example real world process limitations, in that the features are not drawn with precise right angles and straight lines. As shown, FIG. 7 represents a cross-section view similar to that shown on the left side of FIG. 5F but with multiple signal lines shown explicitly. FIG. 7 illustrates a substrate 701, the ground plane conductor 724, the signal lines 730-1 through 730-3, and a signal path support layer 732 with a chimney 734, as could be visible in e.g. a scanning electron microscopy (SEM) image or a transmission electron microscope (TEM) image of a structure. In such an image of a real structure, possible processing defects could also be visible, such as e.g. the rounding of corners and the drooping of the signal lines 730.

[0083] If compared to CPW resonators, proposed transmission line structures reduce uncontrolled interfaces between superconductor (SC) and dielectric, thus reducing the effects of spurious TLS's and improving on the decoherence issues of qubits. If compared to inverted microstrip lines fabricated using flip-chip approach, proposed fabrication techniques allow forming multiple signal lines having smaller variations in the distance to the ground plane conductor.

[0084] Some Examples in accordance with various embodiments of the present disclosure are now described.

[0085] Example 1 provides a transmission line structure including a substrate; a ground structure disposed over the substrate; and a signal path suspended over the ground structure and supported by a signal path support layer (i.e. the signal path is suspended from the signal path support layer and separated from the ground structure by a gap), the signal path support layer including an opening (also referred to herein as a “chimney”).

[0086] Example 2 provides the transmission line structure according to Example 1, where an edge of the opening is less than 10000 nanometers away from the signal path.

[0087] Example 3 provides the transmission line structure according to any one of the preceding Examples, where the largest dimension of the opening is less than 10000 nanometers.

[0088] Example 4 provides the transmission line structure according to any one of the preceding Examples, where a distance from the signal path to the ground structure is between 1 and 10000 nanometers.

[0089] Example 5 provides the transmission line structure according to any one of the preceding Examples, where a surface of the signal path facing the ground structure is substantially parallel to a surface of the ground structure. As used herein, “substantially parallel” refers to deviations of 10 degrees or less from parallel, preferably less than 5 degrees.

[0090] Example 6 provides the transmission line structure according to any one of the preceding Examples, where the signal path is a first signal path, the transmission line structure further including a second signal path suspended over the ground structure (i.e. suspended from the ground structure and separated from the ground structure by a gap) and supported by the signal path support layer.

[0091] Example 7 provides the transmission line structure according to Example 6, where a distance between the first signal path and the ground structure deviates from a distance between the second signal path and the ground structure by less than 5 percent.

[0092] Example 8 provides the transmission line structure according to any one of the preceding Examples, where the signal path includes a first side and a second side, the first side facing the ground structure and the second side being opposite of the first side, and the second side is attached to the signal path support layer.

[0093] Example 9 provides the transmission line structure according to any one of the preceding Examples, where the signal path support layer is an amorphous silicon layer.

[0094] Example 10 provides the transmission line structure according to any one of the preceding Examples, where the signal path and/or the ground structure include one or more of superconductive materials.

[0095] Example 11 provides the transmission line structure according to any one of the preceding Examples, where the signal path and the ground structure form an interconnect of a quantum circuit.

[0096] Example 12 provides the transmission line structure according to any one of the preceding Examples, where the signal path and the ground structure form an inverted microstrip line.

[0097] Example 13 provides a quantum integrated circuit assembly that includes a substrate; one or more qubits disposed over the substrate; and a transmission line coupled to at least one of the one or more qubits. The transmission line includes a ground structure disposed over the substrate and a signal path suspended over the ground structure and supported by a signal path support layer, the signal path support layer including an opening.

[0098] Example 14 provides the quantum integrated circuit assembly according to Example 13, where a surface of the signal path facing the ground structure is substantially parallel to a surface of the ground structure.

[0099] Example 15 provides the quantum integrated circuit assembly according to Examples 13 or 14, where an edge of the opening is less than 10000 nanometers away from the signal path.

[00100] Example 16 provides the quantum integrated circuit assembly according to any one of Examples 13-15, where the largest dimension of the opening is less than 10000 nanometers.

[00101] Example 17 provides the quantum integrated circuit assembly according to any one of Examples 13-16, where the transmission line is a coupling resonator for coupling two or more of the one or more qubits.

[00102] Example 18 provides the quantum integrated circuit assembly according to any one of Examples 13-16, where the transmission line is an interconnect for providing electrical connectivity to the one or more qubits.

[00103] Example 19 provides a quantum computing device, comprising one or more integrated circuit assemblies according to any one of Examples 13-18.

[00104] Example 20 provides the quantum computing device according to Example 19, further comprising a cooling apparatus configured to maintain the one or more qubits at a cryogenic temperature during operation of the one or more qubits.

[00105] Example 21 provides a method for fabricating a transmission line structure, the method including providing a sacrificial layer on a ground structure disposed over a substrate (e.g. box 602); enclosing an area of the sacrificial layer with an etch-resistant material extending from a surface of the sacrificial layer to the ground structure (e.g. box 604); forming a signal path at the surface of the sacrificial layer within the area enclosed with the etch-resistant material (e.g. box 606); providing a signal path support layer over the area enclosed with the etch-resistant material (i.e. over the surface of the sacrificial layer and the signal path) (e.g. box 608); providing a window/opening/chimney in the signal path support layer for performing an etch of the sacrificial layer under at least portion of the signal path through the window (e.g. box 610); and performing the etch of at least a portion of the sacrificial layer through the window in the signal path support layer to provide a gap between the signal path and the ground structure (e.g. box 612).

[00106] Example 22 provides the method according to Example 21, where the sacrificial layer includes a layer of oxide, e.g. silicon oxide.

[00107] Example 23 provides the method according to Examples 21 or 22, where a thickness of the sacrificial layer is between 10 and 300 nm.

[00108] Example 24 provides the method according to any one of Examples 21-23, where the etch includes an isotropic etch.

[00109] Example 25 provides the method according to any one of Examples 21-24, where the etch-resistant material includes a nitride, e.g. a silicon nitride.

[00110] The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize. These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Claims

1. A quantum integrated circuit assembly comprising:

a substrate;

a plurality of qubits disposed over the substrate; and

a transmission line structure for one or more of the plurality of qubits, the transmission line structure comprising

a ground structure disposed over the substrate, and

a signal path structure suspended over the ground structure and supported by a signal path support layer, the signal path support layer comprising an opening.
2. The quantum integrated circuit assembly according to claim 1, wherein an edge of the opening is less than 10000 nanometers away from the signal path structure.
3. The quantum integrated circuit assembly according to claim 1, wherein the largest dimension of the opening is less than 10000 nanometers.
4. The quantum integrated circuit assembly according to claim 1, wherein a distance from the signal path structure to the ground structure is between 1 and 10000 nanometers.
5. The quantum integrated circuit assembly according to any one of claims 1-4, wherein a surface of the signal path structure facing the ground structure is substantially parallel to a surface of the ground structure.
6. The quantum integrated circuit assembly according to any one of claims 1-4, wherein the signal path structure is a first signal path structure, the transmission line structure further comprising a second signal path structure suspended over the ground structure and supported by the signal path support layer.
7. The quantum integrated circuit assembly according to claim 6, wherein a distance between the first signal path structure and the ground structure deviates from a

distance between the second signal path structure and the ground structure by less than 5 percent.

8. The quantum integrated circuit assembly according to any one of claims 1-4, wherein:

the signal path structure comprises a first side and a second side, the first side facing the ground structure and the second side being opposite of the first side, and

the second side is attached to the signal path support layer.

9. The quantum integrated circuit assembly according to any one of claims 1-4, wherein the signal path support layer is an amorphous silicon layer.

10. The quantum integrated circuit assembly according to any one of claims 1-4, wherein the signal path structure and/or the ground structure comprise one or more of superconductive materials.

11. The quantum integrated circuit assembly according to claim 10, wherein the one or more of superconductive materials comprises one or more of aluminum (Al), niobium (Nb), niobium nitride (NbN), titanium nitride (TiN), or niobium titanium nitride (NbTiN).

12. The quantum integrated circuit assembly according to any one of claims 1-4, wherein the transmission line structure forms an inverted microstrip line.

13. The quantum integrated circuit assembly according to any one of claims 1-4, wherein the transmission line structure is coupled to at least one of the plurality of qubits.

14. The quantum integrated circuit assembly according to any one of claims 1-4, wherein the transmission line structure is a coupling resonator for coupling two or more of the plurality of qubits.

15. The quantum integrated circuit assembly according to any one of claims 1-4, wherein the transmission line structure forms an interconnect for providing electrical connectivity to one or more of the plurality of qubits.

16. The quantum integrated circuit assembly according to any one of claims 1-4, wherein the plurality of qubits are superconductive qubits.

17. The quantum integrated circuit assembly according to any one of claims 1-4, wherein the plurality of qubits are quantum dot qubits.

18. The quantum integrated circuit assembly according to any one of claims 1-4, further comprising a cooling apparatus for the plurality of qubits.

19. A method for fabricating a quantum integrated circuit assembly, the method comprising:

providing a plurality of qubits over a substrate;

providing a sacrificial layer on a ground structure disposed over the substrate;

enclosing an area of the sacrificial layer with an etch-resistant material extending from a surface of the sacrificial layer to the ground structure;

forming a signal path structure at the surface of the sacrificial layer within the area enclosed with the etch-resistant material;

providing a signal path support layer over the area enclosed with the etch-resistant material;

providing an opening in the signal path support layer for performing an etch of the sacrificial layer under at least portion of the signal path through the window; and

performing the etch of at least a portion of the sacrificial layer through the opening in the signal path support layer to provide a gap between the signal path structure and the ground structure.

20. The method according to claim 19, wherein the sacrificial layer comprises a layer of oxide.

21. The method according to claim 19, wherein a thickness of the sacrificial layer is between 10 and 300 nm.

22. The method according to any one of claims 19-21, wherein the etch comprises an isotropic etch.

23. The method according to any one of claims 19-21, wherein the etch-resistant material comprises a silicon nitride.

24. The method according to any one of claims 19-21, wherein an edge of the opening is less than 10000 nanometers away from the signal path structure.

25. The method according to any one of claims 19-21, wherein a distance from the signal path structure to the ground structure is between 1 and 10000 nanometers.

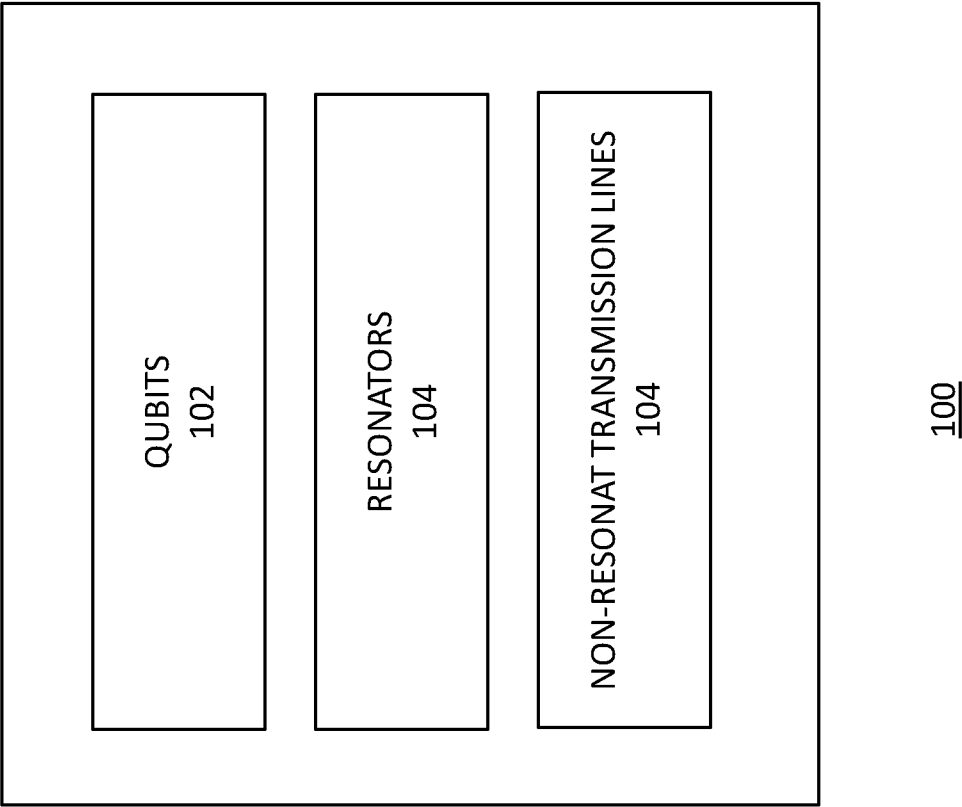


FIG. 1

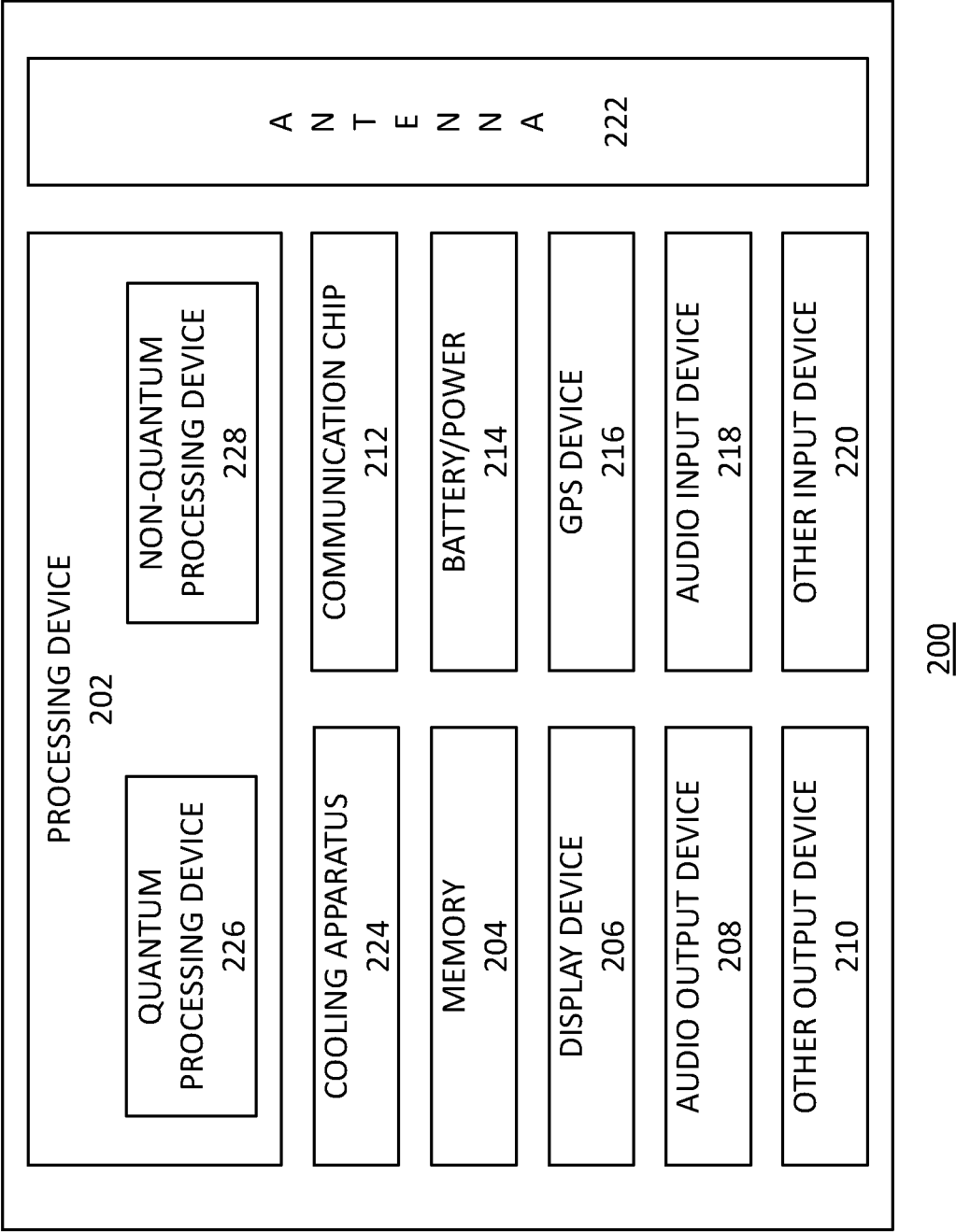


FIG. 2

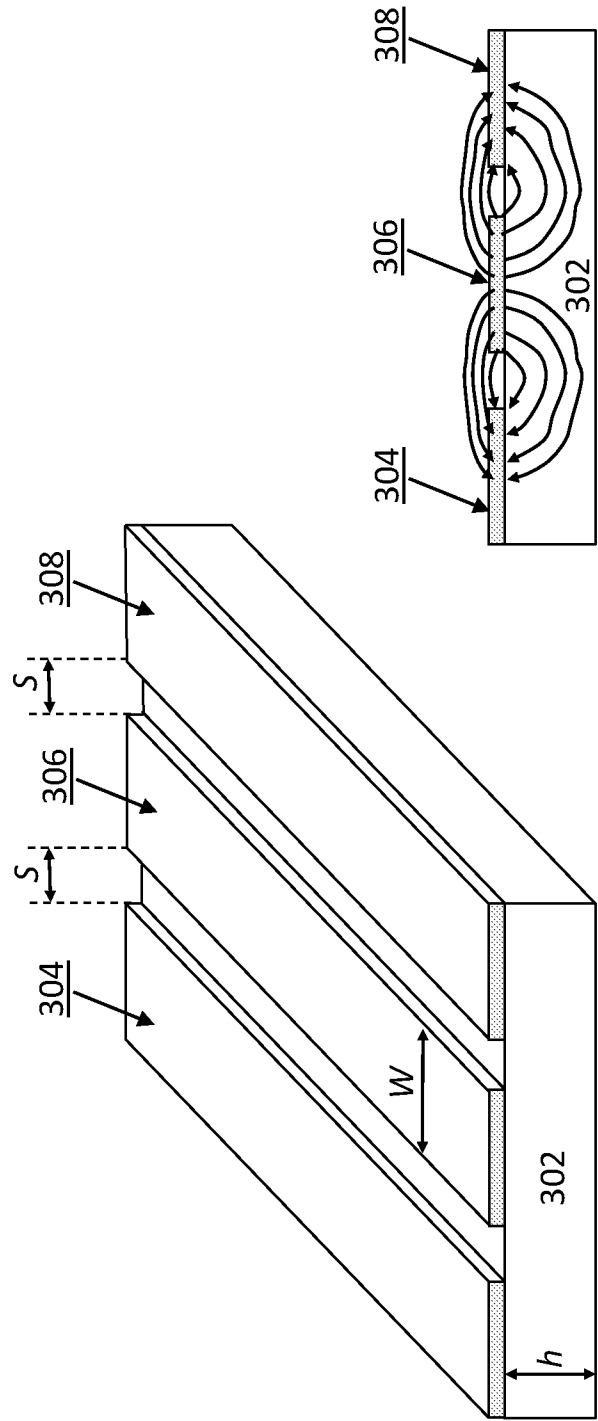


FIG. 3A

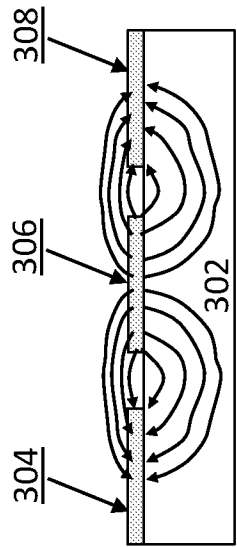


FIG. 3B

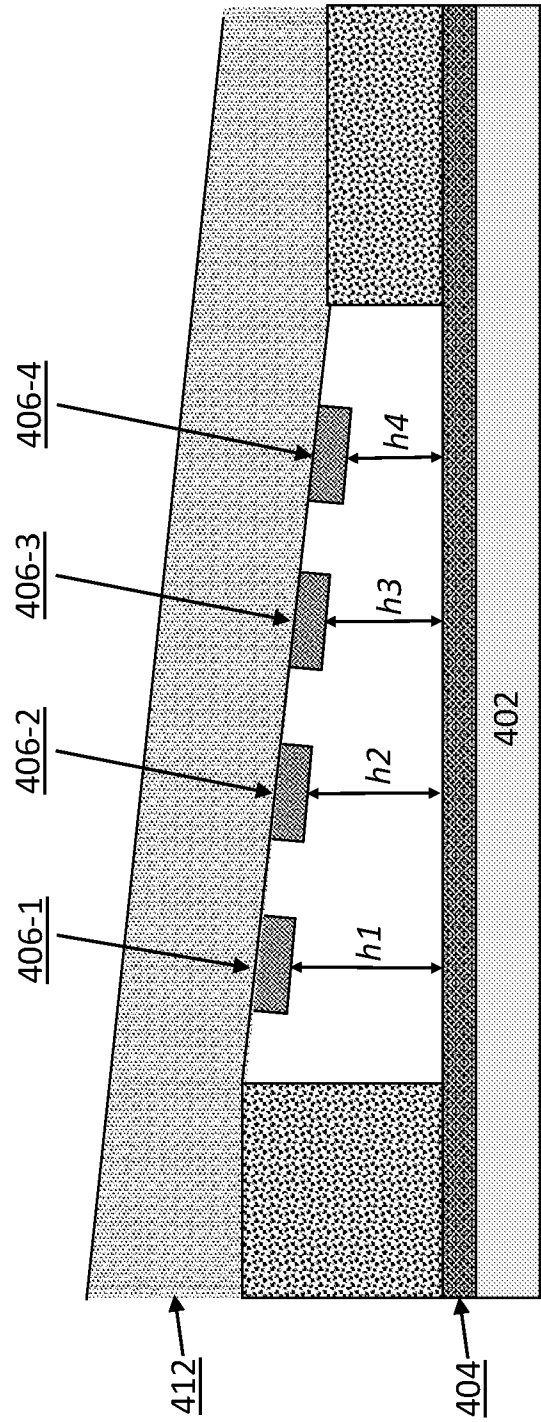
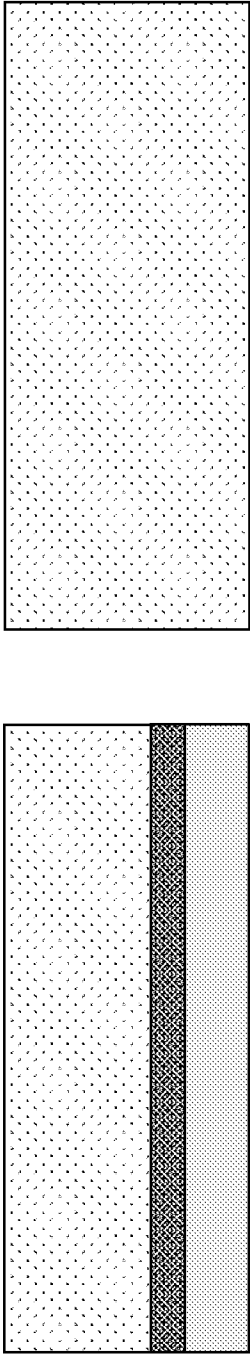
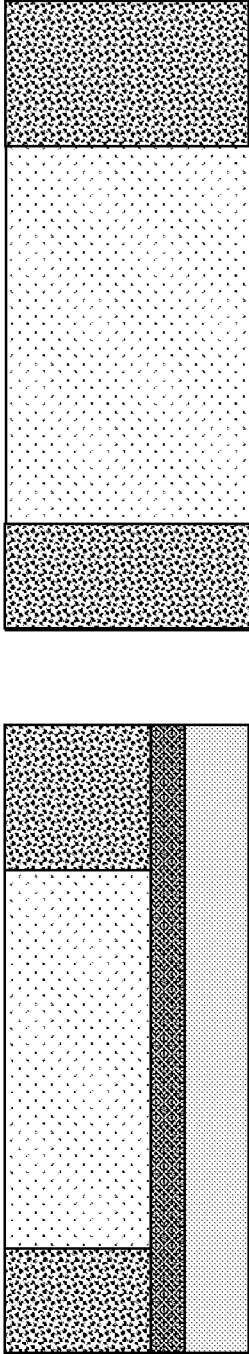


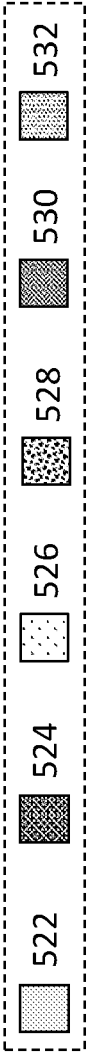
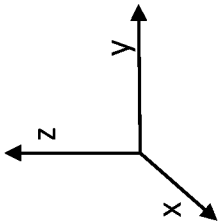
FIG. 4

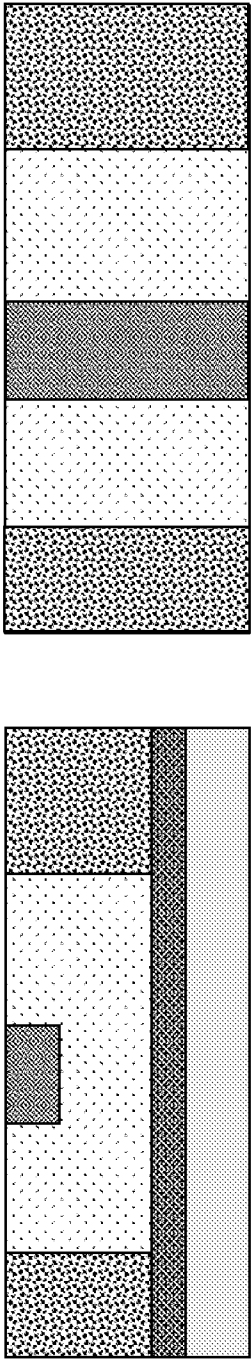


502
FIG. 5A

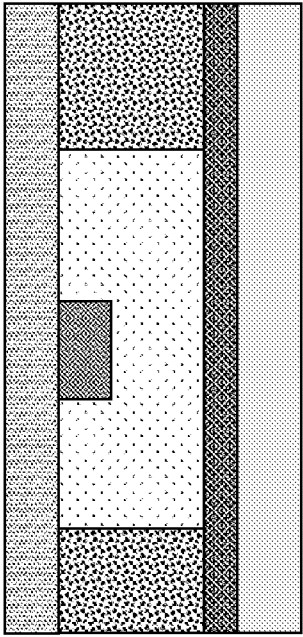


504
FIG. 5B

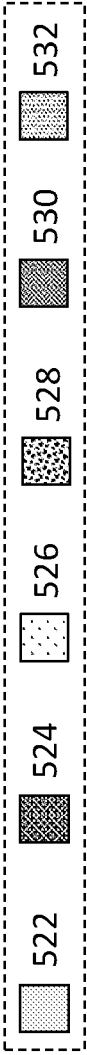
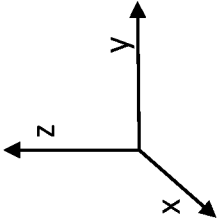




506
FIG. 5C



508
FIG. 5D



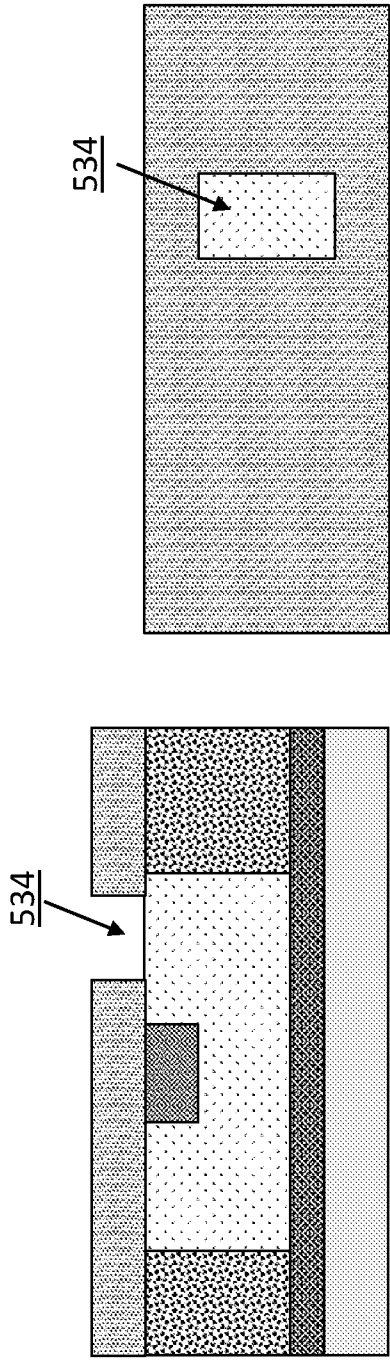


FIG. 5E

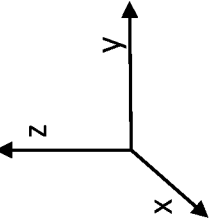
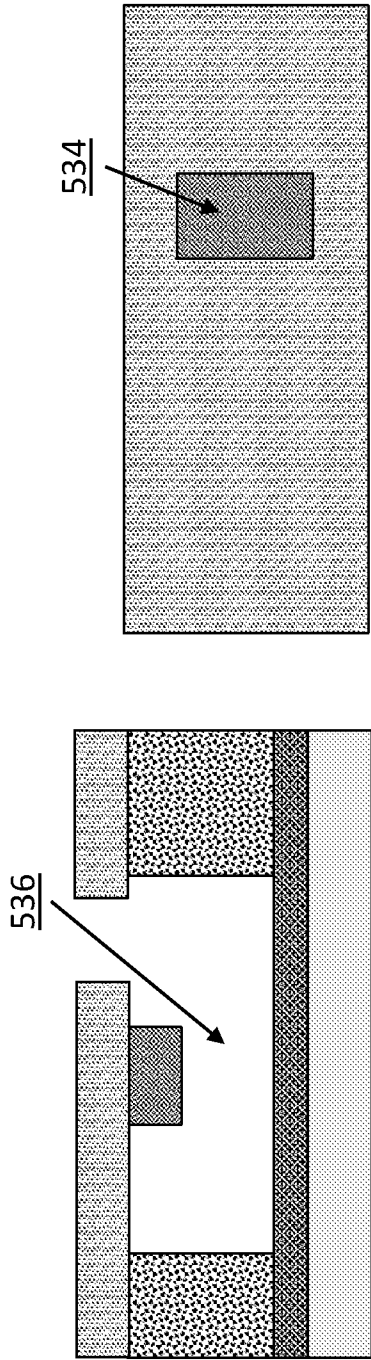
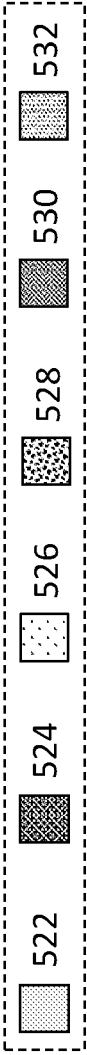


FIG. 5F



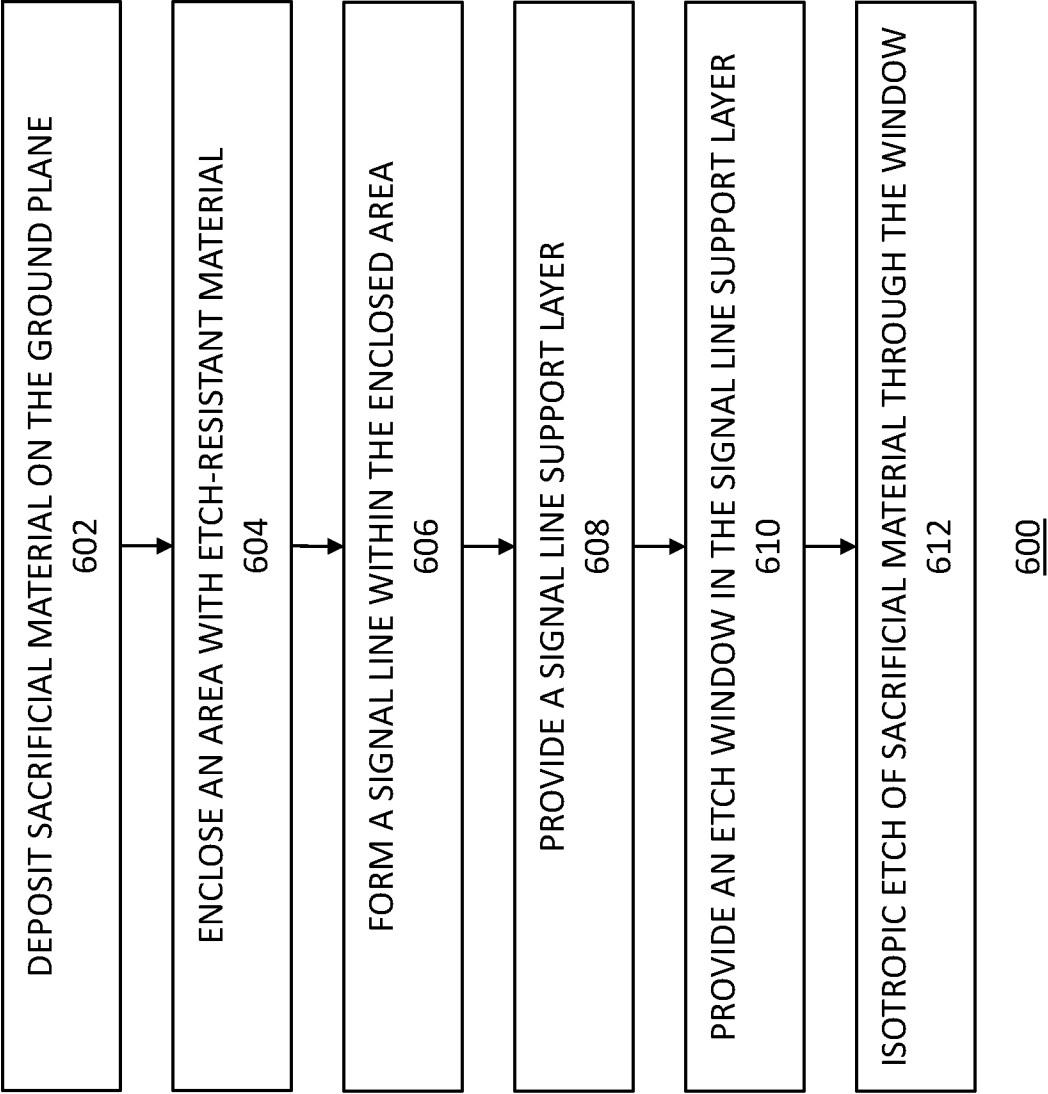


FIG. 6

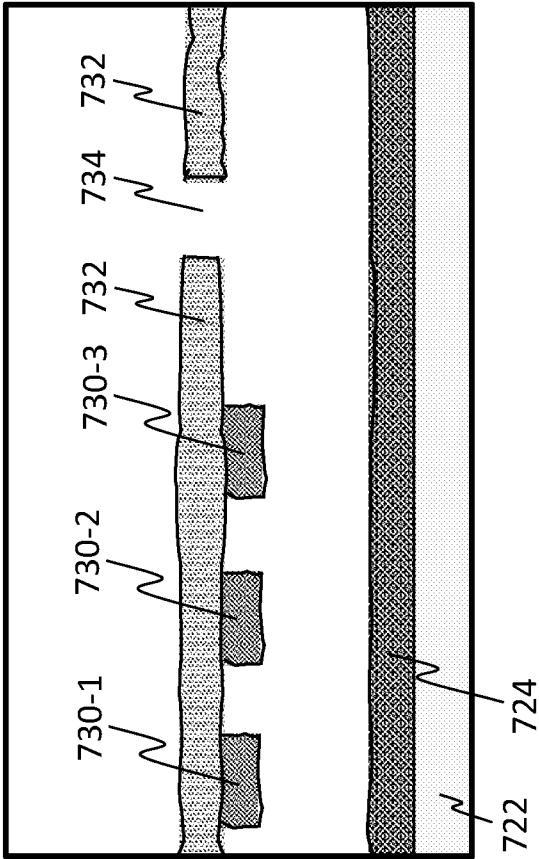


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/048101**A. CLASSIFICATION OF SUBJECT MATTER****H01P 3/00(2006.01)i, H01P 3/08(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01P 3/00; H01P 5/107; H01L 29/08; H01L 23/34; H01L 29/06; H01P 5/08; H01L 29/66; H01P 3/08; H01L 39/04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: quantum integrated circuit assembly, qubit, substrate, signal path structure, signal path support layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 9219298 B2 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 22 December 2015 See column 3, line 31 - column 4, line 25; claim 1; and figures 1-3.	1-25
A	US 5990768 A (KAZUAKI TAKAHASHI et al.) 23 November 1999 See column 5, line 23 - column 7, line 10; claim 1; and figures 1A-4B.	1-25
A	US 2013-0196855 A1 (STEFANO POLETO et al.) 01 August 2013 See paragraphs [0021]-[0025]; claim 1; and figures 1-3.	1-25
A	US 6967543 B2 (DANNY F. AMMAR) 22 November 2005 See column 5, line 40 - column 6, line 38; claim 1; and figures 7-8B.	1-25
A	US 8866291 B2 (ROBERTO W. ALM) 21 October 2014 See column 2, line 54 - column 3, line 12; claim 1; and figure 1.	1-25

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

25 April 2017 (25.04.2017)

Date of mailing of the international search report

25 April 2017 (25.04.2017)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/048101

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