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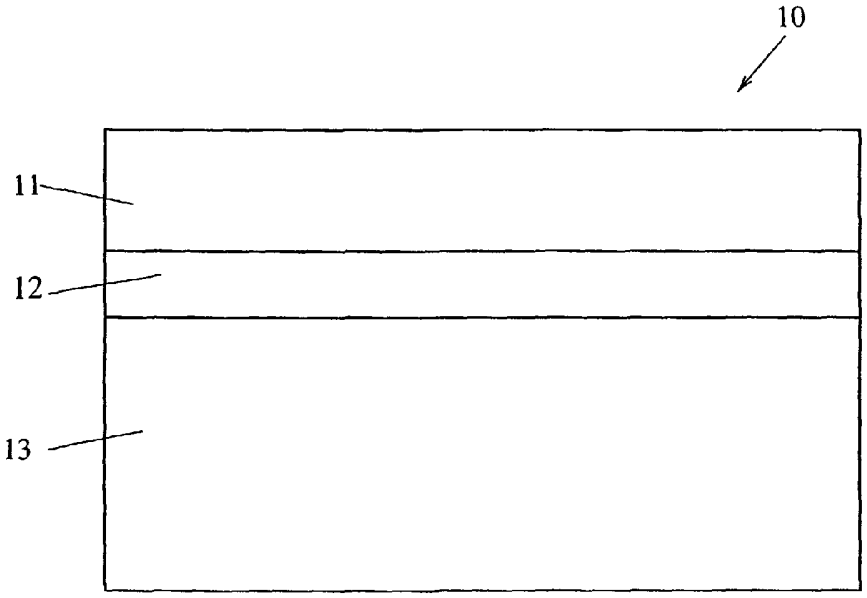

(57) Abstract: A semiconductor structure (10) has a low bandgap semiconductor layer (11), a buried insulator layer (12) below the low bandgap semiconductor layer (11), and a wide bandgap semiconductor substrate (13). The low bandgap semiconductor layer (11) may be for example silicon, SiGe, GaAs or a heterojunction. The wide bandgap semiconductor layer (13) may be for example silicon carbide or diamond. A semiconductor device may be made by bonding a wide bandgap semiconductor wafer (13) via an insulator layer (12) to a low bandgap semiconductor wafer (11) and subsequently forming a semiconductor device in the low bandgap semiconductor wafer (11).

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LATERAL SEMICONDUCTOR STRUCTURE AND METHODS OF MANUFACTURE

The present invention relates to a semiconductor structure and to methods of manufacturing a semiconductor structure.

The present invention has particular application to lateral devices for integrated circuits (ICs) for radio frequency (RF) applications, for power integrated circuits (PICs) and for high voltage integrated circuits (HVICs).

In prior art ICs, there are several technologies which are used for high voltage or power applications and/or high frequency (RF) applications. Among them, the Junction-Isolation (JI) and Silicon-on-Insulator (SOI) technologies are the most common. In Figures 1A and 1B there are shown schematically a typical lateral high-voltage diode (which forms part of a three terminal semiconductor switching device such as a lateral MOSFET) in JI and SOI technologies respectively.

Generally, JI technology offers a higher breakdown ability due to the interaction of two depletion regions formed at junction J1 and junction J2 indicated in Figure 1A and known as the RESURF effect, but suffers from poor isolation (i.e. cross-talk between devices placed on the same chip). SOI technology offers an enhanced degree of isolation due to the presence of the buried oxide which stops the flow of the current through the silicon substrate. In addition, the SOI structure has reduced leakage current and higher temperature operation when compared to that made in JI technology.

The SOI technology suffers from three main drawbacks: reduced breakdown voltage (because the RESURF effect is less effective than in JI technology due to the absence of junction J2, as can be seen by comparison of Figures 1A and 1B); overheating; and lower switching frequency for unipolar devices. The reduced breakdown voltage limits the applicability of the SOI technology to high voltage ICs and imposes a severe limit on the minimum buried oxide thickness. Typically, a thickness of 0.75 to 1 micron for the buried oxide is needed per 100 V blocking voltage. However, the greater the thickness of the buried oxide, the higher the thermal barrier from the active structure to the heat sink, leading to severe self-heating. Finally, the switching frequency of unipolar devices (i.e. devices which operate using one carrier, commonly electrons), such as MOSFETs, MESFETs or LDMOSFETs, is lower than that of equivalent structures made in Junction-Isolation technology due to the absence of the substrate depletion region formed across the J2 junction which serves to decrease the parasitic substrate capacitance during high voltage switching. The absence of the depletion layer in the silicon substrate in the SOI structure (regardless of the doping of the substrate) is due to the field plate shield formed by the inversion/accumulation layer which appears under the buried oxide when a high voltage is applied to the high voltage terminal.

According to a first aspect of the present invention, there is provided a semiconductor structure, the semiconductor structure comprising a low bandgap semiconductor layer, a buried insulator layer below the low

bandgap semiconductor layer, and a wide bandgap semiconductor substrate.

The preferred embodiment of the present invention overcomes the principal drawbacks of the standard Silicon-on-Insulator (SOI) technology, that is severe self-heating, reduced breakdown ability and increased parasitic capacitive coupling to the substrate terminal, yet maintains the advantages of standard SOI technology such as excellent electrical isolation, reduced leakage, radiation hardness and high temperature operation. A device having a structure according to preferred embodiment of the present invention is particularly well suited for use in high voltage and/or high frequency applications.

The low bandgap semiconductor layer preferably comprises silicon. As alternatives, the low bandgap semiconductor layer may comprise SiGe, GaAs or a heterojunction formed of several layers with different bandgaps. As a low bandgap material can be considered any material for which the energy gap between the conduction band and the valence band is less than about 2eV, and more preferably in the range about 0.8 to about 2eV.

The wide bandgap semiconductor layer preferably comprises silicon carbide. As an alternative, the wide bandgap semiconductor layer may comprise diamond. As a wide bandgap material can be considered any material for which the difference between the conduction band and valence band is larger than about 2eV and more preferably in the range about 2eV to about 6eV.

The insulator layer preferably comprises silicon dioxide. The insulator layer may additionally or alternatively comprise silicon nitride. Alternatively or additionally, the insulator layer may comprise aluminium nitride.

The low bandgap semiconductor layer may contain at least one semiconductor device.

The low bandgap semiconductor layer may contain at least one integrated circuit.

The low bandgap semiconductor layer may contain at least one power device.

The low bandgap semiconductor layer may contain at least one high frequency device.

During operation of at least one semiconductor device provided in the low bandgap semiconductor, a depletion region having substantially no mobile carriers is preferably formed in the wide bandgap semiconductor layer below the insulator layer. During the voltage blocking mode of at least one semiconductor device provided in the low bandgap semiconductor, a depletion region having substantially no mobile carriers is preferably formed in the wide bandgap semiconductor layer below the semiconductor device and under the insulator layer.

In a particular cross-section of the structure the depletion region preferably supports at least 25% of the voltage supported by the insulator layer. In this arrangement, the insulator layer can be relatively thinner

than in a comparable prior art device, thereby reducing the effect of the thermal barrier formed by the insulator layer.

The wide bandgap semiconductor layer preferably is or includes at least one sub-layer which is of different conductivity type to the low bandgap semiconductor layer.

The wide bandgap semiconductor layer may be doped such as to obtain maximum breakdown of at least one semiconductor device provided in the low bandgap semiconductor layer.

The wide bandgap semiconductor layer may be doped such as to maximise the operating or switching frequency of at least one semiconductor device provided in the low bandgap semiconductor layer.

The wide bandgap semiconductor layer preferably has a higher thermal conductivity than the low bandgap semiconductor layer.

In the most preferred embodiment, the low bandgap semiconductor is made of silicon, the insulator layer is made of silicon dioxide and the wide bandgap semiconductor layer which acts as the substrate for the entire structure is made of silicon carbide. The silicon carbide may be in the form of 4H-SiC or 6H-SiC or other known polytypes. This structure may be termed SOSiC (silicon/oxide/silicon carbide).

According to a second aspect of the present invention, there is provided a method of manufacturing a semiconductor device on a semiconductor structure, the semiconductor structure comprising a low bandgap semiconductor layer, a buried insulator layer below the low bandgap semiconductor layer, and a wide bandgap semiconductor substrate, the method comprising the steps of: bonding a wide bandgap semiconductor substrate wafer via an insulator layer to a low bandgap semiconductor wafer; and, subsequently forming a semiconductor device in the low bandgap semiconductor wafer.

The method may comprise the step of, after the bonding step and before the forming step, thinning down the low bandgap semiconductor layer to a desired thickness.

The bonding step may be carried out at high temperature.

The insulator layer may be provided on a surface of the wide bandgap semiconductor wafer and the wide bandgap semiconductor wafer may be bonded via that insulator layer to an insulator layer provided on the low bandgap semiconductor wafer.

Alternatively, the insulator layer may be provided on a surface of the wide bandgap semiconductor wafer, the wide bandgap semiconductor wafer being bonded via that insulator layer to the low bandgap semiconductor wafer.

As another alternative, the insulator layer may be provided on a surface of the low bandgap semiconductor wafer, the low bandgap semiconductor wafer being bonded via

that insulator layer to the wide bandgap semiconductor wafer.

According to a third aspect of the present invention, there is provided a method of manufacturing a semiconductor device on a semiconductor structure, the semiconductor structure comprising a low bandgap semiconductor layer, a buried insulator layer below the low bandgap semiconductor layer, and a wide bandgap semiconductor substrate, the method comprising the steps of:

forming a semiconductor device in a low bandgap semiconductor layer;

thinning down part of the low band semiconductor layer below the semiconductor device; and,

subsequently attaching the low bandgap semiconductor layer to an insulator layer provided on a wide bandgap semiconductor substrate.

The attaching step may be achieved by for example low-temperature bonding, pressure contact and/or other mechanical techniques.

Embodiments of the present invention will now be described by way of example with reference to the accompanying drawings, in which:

Figures 1A and 1B show schematically a typical lateral high-voltage diode in JI and SOI technologies respectively;

Figure 2 shows schematically an example of a structure according to an embodiment of the present invention;

Figures 3A and 3B show schematically a conventional SOI diode and an example of a diode according to an embodiment of the present invention;

Figure 4 shows the variation of the breakdown voltage with the substrate doping of the diodes shown in Figures 3A and 3B;

Figures 5A and 5B show the potential lines in the substrates of the diodes shown in Figures 3A and 3B respectively;

Figure 6 shows the optimised breakdown voltage for the diodes shown in Figures 3A and 3B;

Figure 7 shows the electric field distribution in a cross-section along A-A of the diode of Figure 3A (which is shown again in Figure 7);

Figure 8 shows schematically another example of a structure according to an embodiment of the present invention;

Figures 9A, 9B and 9C show schematically variations of the embodiments shown in Figures 2 and 8 in which the substrate is comprised of multiple layers with different conductivities;

Figures 10A and 10B show schematically examples of methods of making a structure according to an embodiment of the present invention;

Figure 11 shows schematically an example of a high voltage LDMOSFET having a structure according to an embodiment of the present invention;

Figure 12 shows schematically an example of a RF long drain MOSFET having a structure according to an embodiment of the present invention;

Figure 13 shows schematically an example of a power integrated circuit cell having a structure according to an embodiment of the present invention; and,

Figure 14 shows schematically an example of a device according to an embodiment of the present invention.

Referring to Figure 2, there is shown schematically an example of a structure 10 according to an embodiment of the present invention. The structure 10 has an upper low bandgap semiconductor layer 11, a buried insulator layer 12 and a wide bandgap semiconductor layer 13 in the form of a "sandwich".

The low bandgap semiconductor layer 11, which is preferably silicon, serves for active device operation and constitutes the active layer of the device 10. This layer 11 is preferably compatible with planar IC technology and in particular CMOS or Bi-CMOS technologies. Devices such as MOSFETs, LDMOSFETs, LIGBTs, MESFETs or bipolar devices can be built in the upper low bandgap semiconductor layer 11.

The insulator layer 12, which is preferably silicon oxide, serves two purposes: (i) electrical isolation between adjacent devices or blocks of devices and (ii)

action as a buffer material between the low bandgap semiconductor layer 11 and the wide bandgap semiconductor layer 13. This insulator layer 12 overcomes the effect of the lattice mismatch between the two semiconductor layers 11,13 and facilitates the fabrication of the sandwich structure via oxide/silicon or oxide-silicon-carbide bonding.

The wide bandgap semiconductor layer 13, which is preferably made of SiC (e.g. 4H SiC or 6H SiC or other polytypes), serves to increase the breakdown voltage and switching frequency and reduces self-heating. The increase in the breakdown voltage on the one hand, and reduction in the substrate capacitance which provides higher switching frequency on the other hand, rely on the formation of a wide depletion region in the SiC substrate 13 under the buried insulating layer 12. This is entirely different from conventional SOI technology using standard silicon substrates.

The reason for the depletion region is due to the wide bandgap of SiC substrate 13. The explanation of this phenomenon is as follows.

Consider the situation of the diodes 10',10 shown in Figures 3A and 3B where region 14 is the anode, region 15 the drift layer n- and region 16 the cathode. Figure 3A shows a conventional SOI diode 10' whereas Figure 3B shows an example of a diode 10 according to the present invention in which the standard silicon substrate 13' is replaced by SiC substrate 13. When a reverse bias high voltage is applied to the high voltage terminal placed on top of the cathode 16, a large fraction of it is seen across the

buried layer 12 (the bottom of the semiconductor substrate 13,13' being grounded via a substrate terminal). A layer of negative charge is induced under the buried oxide due to the well-known Metal Oxide Semiconductor (MOS) capacitor effect. This negative charge is in the form of an inversion layer made of electrons at the surface 17 of the semiconductor substrate 13,13' and/or a layer of fixed charge made of fixed acceptor ions within a depletion region 18. The distribution of charge in the inversion layer 17 or in the depletion region 18 depends on the conditions of the surface inversion expressed by a threshold voltage, as known in the theory of the MOS capacitor.

If the substrate 13' is made of silicon, which is a low bandgap semiconductor, the threshold voltage is relatively low provided that the doping of the substrate 13' is low. In this case, the negative charge created by the application of a high voltage on the high voltage terminal is mainly distributed in the inversion layer 17 and therefore the depth of the depletion region 18 in the substrate is insignificant (and indeed the depletion region is not shown in Figure 3A). This is the situation of the standard prior art structure shown in Figure 3A. On the other hand, if the doping of the substrate 13' is too high, no inversion layer is formed but the depth of the depletion region 18 is very small anyway because of the high doping. Therefore, regardless of the doping of the substrate 13', there is no significant depletion region 18 formed under the buried oxide 12 in the conventional SOI structure. Thus, it can be concluded that in prior art SOI, the silicon substrate 13' does not support a substantial voltage across it and therefore the doping of the silicon

substrate 13' does not influence the breakdown voltage of the structure.

Unlike in silicon, in silicon carbide, because the threshold voltage is higher due to its wide bandgap, a large part of the negative charge induced in the substrate 13 caused by the positive voltage applied to the high voltage terminal is now found in a depletion region 18 of significant depth in the wide bandgap semiconductor substrate 13. This is shown in Figure 3B. The depth of the depletion region 18 is in the micron range (e.g. about 10 microns) and depends on the voltage applied, the doping of the SiC substrate 13 and the thickness of the buried oxide 12. The doping of the SiC substrate 13 can be optimised such that the diode shown in Figure 3B supports an optimum breakdown which is in any event significantly higher than that of a prior art SOI diode 10' shown in Figure 3A.

Figure 4 shows the variation of the breakdown voltage with the substrate doping of the conventional SOI diode 10' shown in Figure 3A featuring a silicon substrate versus the diode structure 10 shown in Figure 3B in which the silicon substrate 13' is replaced by a silicon carbide substrate 13 (the other parts being identical). It can be seen that there is an optimum doping for a maximum breakdown voltage in the present device 10 and the breakdown voltage is significantly higher than that of a standard (prior art) SOI device 10'. As explained earlier, the breakdown of the conventional SOI device 10' does not vary with the doping of the substrate 13'.

Figures 5A and 5B respectively show the equipotential lines distribution in the conventional (prior art) SOI diode 10' shown in Figure 3A and the diode 10 shown in Figure 3B. Referring now to Figure 5B in comparison with Figure 5A, it can be clearly seen that the potential lines penetrate deep into the SiC substrate 13 in the diode 10 within the depletion region 18 formed therein. Thus, a significant drop of the voltage is supported by the depletion region 18 in the SiC substrate 13. This leads to a reduced field pressure on the oxide 12, minimising the risk for vertical breakdown in the top silicon layer 11 at the silicon/oxide interface 11/12, and also facilitates a more uniform distribution of the potential lines at the surface of the silicon layer 11 and hence results in a significant increase in the breakdown voltage. The optimised breakdown voltages for these two examples (conventional SOI and silicon/oxide/SiC (SOSIC)) are shown in Figure 6.

To optimise the voltage supported across the SiC substrate 13, the electric field distribution in a cross-section on A-A indicated in Figure 7 can be considered. To maximise the voltage supported by the SiC substrate 13 within the depletion region 18, and thus reduce the voltage supported by the oxide layer 12 and the depletion region within the silicon layer 11, the hashed area in Figure 7 should be maximised. This area represents half of the product of the electric field peak at the SiC interface with the oxide layer and the depth of the depletion region. The electric field peak at the interface depends on the permittivity ratios between the insulating layer 12 and the SiC substrate 13 and the inversion layer charge present at the interface. The depletion region depth depends on the

doping of the SiC substrate and the voltage applied on the high voltage terminal. Maximising this hashed area results in a maximum voltage supported across the SiC substrate 13. This firstly releases the pressure on the oxide 12 and top silicon layer 11 and also reduces the electric field peaks at the cathode and anode ends of the drift region 15 within the top silicon layer 11.

As shown in Figure 8, the SiC substrate 13 may include at its surface a thin layer 13a which is more highly doped than the bulk 13b of the substrate 13. This prevents the formation of an inversion layer 17 at the surface of the substrate but allows the formation of a wide depletion layer 18 in the more lowly doped portion 13b of the substrate 13.

Figures 9A, 9B and 9C show schematically variations of the embodiments shown in Figures 2 and 8 in which the SiC substrate 13 is comprised of multiple layers with different conductivities. In these examples, the different conductivities are achieved by varying the doping in layers within the SiC substrate 13 as indicated. As shown, given that the silicon layer is normally n type, there is always a p type layer of SiC below the insulator layer 12.

In the examples described above, the depletion layer 18 formed in the SiC substrate 13 serves to reduce the coupling capacitance to the substrate terminal. Thus, the depletion capacitance now appears in series with the insulating layer 12 capacitance, minimising the overall capacitance between the active structure and the substrate terminal. The depletion capacitance decreases with the increase in the depth of the depletion region, and hence

the overall capacitance decreases with the applied voltage on the high voltage terminal. The decrease in this capacitance results in faster switching, lower transient losses and higher cut-off frequencies. This technique is especially valuable for power, RF or power RF applications.

If the structure is part of an integrated circuit, it is also desirable to reduce cross-talk between adjacent devices at high frequencies. This requires the reduction of parasitic active or passive components between devices. The depletion region 18 in the SiC substrate 13 serves to reduce the parasitic coupling capacitance between neighbouring devices, thus helping to achieve that aim.

The device structure 10 described above has a lower thermal resistance than a conventional SOI device, thus reducing the self-heating effect. This is because the thermal conductivity of silicon carbide is three times higher than that of silicon. Hence, the device 10 can dissipate more effectively the heat to the bottom of the structure 10 (which may have an external heat sink attached to it). In other words, the SiC substrate 13 acts as an efficient internal heat sink to remove a large amount of heat, thus preventing high temperatures developing in the active structure (in the top silicon layer 11). This is very important in high power applications or in integrated circuits requiring large currents or large voltages.

Thus, the SiC substrate 13 of the preferred embodiment not only serves to increase the breakdown capability and reduce the parasitic coupling capacitances but also acts as an active heat sink which reduces the undesirable effect of self-heating in the structure. The reduced self-heating

leads to better electrical performance, less probability of latch-up and parasitic hot-spots, and, very importantly, increased reliability.

Examples of methods of making a silicon/oxide/SiC sandwich structure 10 will now be described.

In one example shown schematically in Figures 10A and 10B, the silicon/oxide/SiC structure 10 is made prior to making the devices within the silicon layer 11 by bonding at high temperatures, say in excess of 800°C, an oxidised SiC wafer to a silicon wafer with an oxide grown or deposited on the top. After oxide-to-oxide bonding (Figure 10A), a thermal anneal is performed followed by thinning down the silicon wafer to the required thickness (Figure 10B), for example by chemical etching. Alternatively, the SiC wafer is not oxidised and is bonded directly to the silicon/oxide wafer. As another alternative, the silicon wafer is not oxidised and is bonded to an oxidised SiC wafer.

In another example, the bonding is carried out at low temperature, say below 500°C, after the devices are fabricated. The devices may be fabricated using standard SOI technology followed by etching entirely away the silicon substrate below the semiconductor devices (using for example single sided etching techniques such as chemical or electrochemical etching or dry etching). This may be done before or after the individual chips within the wafers are cut. The low bandgap thin wafer or thin chips are attached through low temperature bonding to an insulating layer provided on a SiC piece of semiconductor

(which can be of the same size as or different size to the silicon/oxide chip/wafer).

Alternatively, other techniques can be used (after the devices are built in the silicon layer) to attach a SiC substrate to the silicon/oxide chip. Thus, pressure contact or mechanical vibrations can be used to make a contact between the SiC substrate and the top silicon layer.

The buried insulating layer 12 can be made of silicon dioxide or, to reduce the stress of the structure, it can be made of a combination of silicon dioxide and silicon nitride. Alternatively, a layer of aluminium nitride can be used with or without oxide layers placed adjacent thereto. The composition of the insulating layer(s) may also be chosen to match the expansion coefficients of silicon and/or the SiC substrate.

An example of a high voltage LDMOSFET 50 having a structure according to an embodiment of the present invention is shown schematically in Figure 11. The device comprises a SiC substrate 13, an insulating layer 12 and a top silicon layer 11 in which the active part of the device 50 is formed. The LDMOSFET 50 features a drift layer 15 formed within the top silicon layer 13, a source region 14 and a drain region 16. The drift region 15 is separated from the source region 14 through a p well region 20. An insulating gate 21 comprising a thin oxide layer and a polysilicon layer is placed on top of the p well 20 and links the source region 14 to the drift region 15. At the surface of the p well 20 in the on-state, an inversion layer is formed which allows electrons to be transported

from the source region 14 to the drift region 15 and further to the drain region 16. A LOCOS layer 22 is commonly provided on top of the drift layer 15 and the polysilicon layer extends by a certain length above the LOCOS layer 22 to create a field plate effect. During the forward-blocking mode in the off-state, the device 50 is required to support a high voltage across the drain-source terminals. The p well 20/n- drift layer 15 junction is reverse biased and thus a depletion layer is formed in the silicon layer 11. In a well designed LDMOSFET 50, to support a high breakdown voltage, the doping and the thickness of the silicon layer 11 are chosen such that the depletion layer reaches the drain region and the electric field peaks at the source end and drain end of the depletion regions are equal. A depletion region 18 also extends in the SiC substrate 13 more deeply in a cross section under the drain and less deeply towards the source as shown in Figure 11. This is because the voltage seen across the buried oxide 12 decreases gradually from the drain terminal to the source terminal which in this case is grounded. The depletion region 18 thus formed in the SiC substrate 13 helps to reduce the electric field at the surface and at the silicon/oxide interface and thus leads to an increased breakdown voltage. This depletion region 18 is also formed during the transient regime of the device 50 and thus yields lower parasitic capacitances leading to increased switching speed and reduced transient losses. During the on-state and high power transient loads, the device 50 may experience self-heating. The SiC substrate 13 is however very effective in reducing the heat by ensuring a very low thermal resistance from the top of the structure 10 to the bottom of the structure 10 where an external heat sink (not shown) may be connected. This

leads to decreased temperatures in the top silicon layer 11 when the device 50 is operational.

For a 600 V device 50, the following parameters may be used. The top silicon layer 11 may have a thickness in the range of about 0.3 micron to about 20 micron. The gate oxide is typically about 20 nm to about 50 nm thick. The p well peak doping concentration is about 10^{17} cm^{-3} and the drift layer doping is in the range of about 10^{15} to about 5 x 10^{16} cm^{-3}. The source and drain are highly doped with peak concentrations exceeding about 10^{19} cm^{-3}. The depth of the source and drain diffusions may range from about 0.2 micron to about 1 micron. The buried layer 12 has a thickness of about 2 to about 2.5 micron and the SiC substrate 13 has a doping concentration of about 10^{15} cm^{-3}. The thickness of the field oxide can be in the range of about 0.6 micron to about 3 microns.

Another example of a device according to an embodiment of the present invention is a RF long drain MOSFET 60, shown schematically in Figure 12, which can be operated at GHz frequencies. The device is similar to an LDMOSFET but has a long drain layer 23 typically built in a p Silicon region 24. For a rated voltage of 80 V, the long drain 23 can have a length of about 3 to about 8 microns and its doping may be about 10^{16} cm^{-3}. Its depth can be of sub-micrometer orders. The channel is formed at the surface of the p region 24. Typically, the length of the channel is under about 1 micron and the gate oxide has a thickness of less than about 40 nm. The SiC substrate 13 helps to remove the parasitic capacitance and increase the breakdown voltage (and thus reduce the dimensions) of the device 60. In addition, as explained above, the device 60 is protected

against over-heating due to the excellent thermal conductivity of the SiC substrate 13. The buried oxide thickness is typically about 0.4 microns to about 1.5 microns. The SiC substrate doping concentration is in the range of about 10^{14} to about 10^{15} cm^{-3}. The size of one cell of the device 60 is typically about 10 to about 20 microns.

An example of a power integrated circuit cell according to an embodiment of the present invention is shown schematically in Figure 13. An LIGBT cell is integrated with low power CMOS cells placed on an oxide/SiC substrate.

Another example of an embodiment of the present invention is shown schematically in Figure 14. A silicon layer 11 is provided on top of an oxide 12 which is on top of a SiC substrate 13. Power devices 30 or CMOS circuits 30 can be placed in the silicon layer 11. In this example, the SiC substrate 13 also serves as the main active layer for a power device 31 that is placed vertically, adjacent to the power devices 30 or CMOS circuits 30 which are placed in the silicon layer 11, and separated from them via an isolation layer 40. This structure allows the use of the SiC layer 13 both as a substrate for the devices 30 built in the silicon layer 11 and also as the main active layer for devices 31 built in SiC.

Although SiC technology is in general a very difficult and expensive technology to use, the material is typically used in the present case only to form the substrate of the structure: the devices themselves are not built in SiC (except for the variant shown by way of example in Figure 14). Thus, it is largely immaterial if the carrier

mobility is low in the SiC or if to a certain extent the material has some defects. Thus, the preferred structure can be regarded as being of silicon type, compatible with silicon planar IC technology, and having an internal heat-sink made of SiC with an active support of the voltage (by having a depletion region) and reduced parasitic coupling capacitances.

The upper low band semiconductor layer can be made of other materials such as SiGe or GaAs or a heterojunction comprising several layers with different bandgaps but all being of low bandgap type. The wide bandgap material is preferably SiC but diamond or other wide bandgap materials can also be used. The wide bandgap material may be doped appropriately to obtain the maximum breakdown voltage of the or at least one semiconductor device in the low bandgap layer and/or to maximise the operating or switching frequency of the or at least one semiconductor device provided in the low bandgap semiconductor layer.

As a low bandgap semiconductor material can be considered any material having an energy bandgap less than about 2eV and typically in the range of about 0.8 eV to 2 eV. As a wide band semiconductor material can be considered any material having an energy bandgap greater than about 2eV and typically in the range of about 2eV to 6eV.

The structure can be used to fabricate power devices such as LDMOSFETs, LIGBTs, 3D and multiple RESURF devices with improved breakdown ability when compared to prior SOI techniques, but can also be used in the low-power domain

for devices such as MOSFETs, MESFETs, HBTs, and BJTs to reduce self-heating and/or enhance the switching frequency.

Embodiments of the present invention have been described with particular reference to the examples illustrated. However, it will be appreciated that variations and modifications may be made to the examples described within the scope of the present invention.

CLAIMS

1. A semiconductor structure, the semiconductor structure comprising a low bandgap semiconductor layer, a buried insulator layer below the low bandgap semiconductor layer, and a wide bandgap semiconductor substrate.

2. A semiconductor structure according to claim 1, wherein the low bandgap semiconductor layer comprises silicon.

3. A semiconductor structure according to claim 1, wherein the low bandgap semiconductor layer comprises SiGe.

4. A semiconductor structure according to claim 1, wherein the low bandgap semiconductor layer comprises GaAs.

5. A semiconductor structure according to claim 1, wherein the low bandgap semiconductor layer comprises a heterojunction

6. A semiconductor structure according to any of claims 1 to 5, wherein the wide bandgap semiconductor layer comprises silicon carbide.

7. A semiconductor structure according to any of claims 1 to 5, wherein the wide bandgap semiconductor layer comprises diamond.

8. A semiconductor structure according to any of claims 1 to 7, wherein the insulator layer comprises silicon dioxide.

9. A semiconductor structure according to any of claims 1 to 8, wherein the insulator layer comprises silicon nitride.

10. A semiconductor structure according to any of claims 1 to 9, wherein the insulator layer comprises aluminium nitride.

11. A semiconductor structure according to any of claims 1 to 10, wherein the low bandgap semiconductor layer contains at least one semiconductor device.

12. A semiconductor structure according to any of claims 1 to 11, wherein the low bandgap semiconductor layer contains at least one integrated circuit.

13. A semiconductor structure according to any of claims 1 to 12, wherein the low bandgap semiconductor layer contains at least one power device.

14. A semiconductor structure according to any of claims 1 to 13, wherein the low bandgap semiconductor layer contains at least one high frequency device.

15. A semiconductor structure according to any of claims 1 to 14, wherein, during operation of at least one semiconductor device provided in the low bandgap semiconductor, a depletion region having substantially no mobile carriers is formed in the wide bandgap semiconductor layer below the insulator layer.

16. A semiconductor structure according to claim 15, wherein, during the voltage blocking mode of at least one semiconductor device provided in the low bandgap semiconductor, a depletion region having substantially no mobile carriers is formed in the wide bandgap semiconductor layer below the semiconductor device and under the insulator layer.

17. A semiconductor structure according to claim 15 or claim 16, wherein in a particular cross-section of the structure the depletion region supports at least 25% of the voltage supported by the insulator layer.

18. A semiconductor structure according to any of claims 1 to 17, wherein the wide bandgap semiconductor layer is or includes at least one sub-layer which is of different conductivity type to the low bandgap semiconductor layer.

19. A semiconductor structure according to any of claims 1 to 18, wherein the wide bandgap semiconductor layer is doped such as to obtain maximum breakdown of at least one semiconductor device provided in the low bandgap semiconductor layer.

20. A semiconductor structure according to any of claims 1 to 19, wherein the wide bandgap semiconductor layer is doped such as to maximise the operating or switching frequency of at least one semiconductor device provided in the low bandgap semiconductor layer.

21. A semiconductor structure according to any of claims 1 to 20, wherein the wide bandgap semiconductor layer has a

higher thermal conductivity than the low bandgap semiconductor layer.

22. A method of manufacturing a semiconductor device on a semiconductor structure, the semiconductor structure comprising a low bandgap semiconductor layer, a buried insulator layer below the low bandgap semiconductor layer, and a wide bandgap semiconductor substrate, the method comprising the steps of:

bonding a wide bandgap semiconductor wafer via an insulator layer to a low bandgap semiconductor wafer; and,

subsequently forming a semiconductor device in the low bandgap semiconductor wafer.

23. A method according to claim 22, comprising the step of, after the bonding step and before the forming step, thinning down the low bandgap semiconductor layer to a desired thickness.

24. A method according to claim 22 or claim 23, wherein the bonding step is carried out at high temperature.

25. A method according to any of claims 22 to 24, wherein the insulator layer is provided on a surface of the wide bandgap semiconductor wafer and the wide bandgap semiconductor wafer is bonded via that insulator layer to an insulator layer provided on the low bandgap semiconductor wafer.

26. A method according to any of claims 22 to 24, wherein the insulator layer is provided on a surface of the wide bandgap semiconductor wafer, the wide bandgap semiconductor

wafer being bonded via that insulator layer to the low bandgap semiconductor wafer.

27. A method according to any of claims 22 to 24, wherein the insulator layer is provided on a surface of the low bandgap semiconductor wafer, the low bandgap semiconductor wafer being bonded via that insulator layer to the wide bandgap semiconductor wafer.

28. A method of manufacturing a semiconductor device on a semiconductor structure, the semiconductor structure comprising a low bandgap semiconductor layer, a buried insulator layer below the low bandgap semiconductor layer, and a wide bandgap semiconductor substrate, the method comprising the steps of:

forming a semiconductor device in a low bandgap semiconductor layer;

thinning down part of the low bandgap semiconductor layer below the semiconductor device; and,

subsequently attaching the low bandgap semiconductor layer to an insulator layer provided on a wide bandgap semiconductor layer.

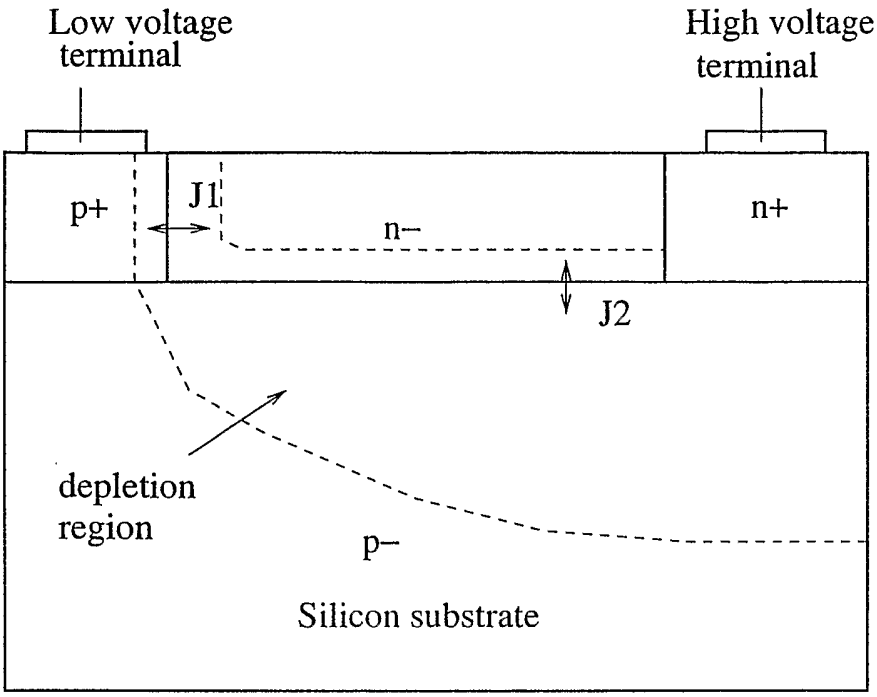

FIGURE 1A

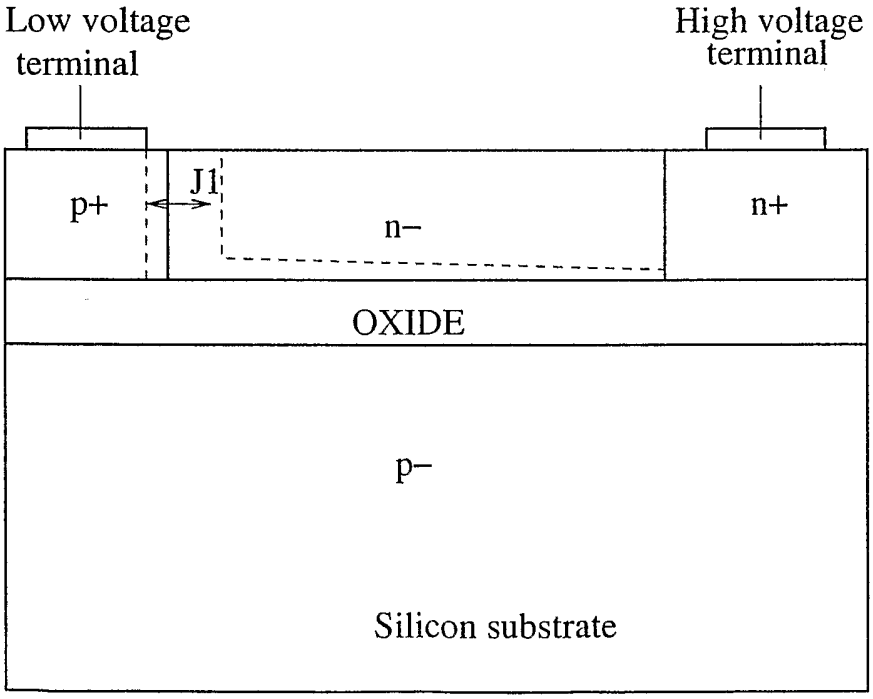

FIGURE 1B

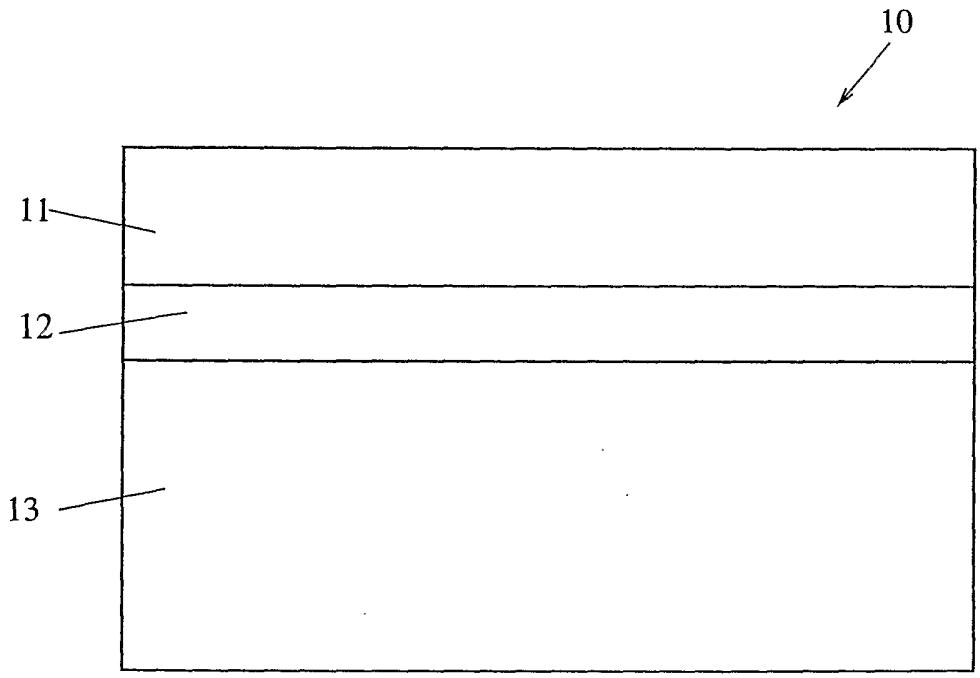

FIGURE 2

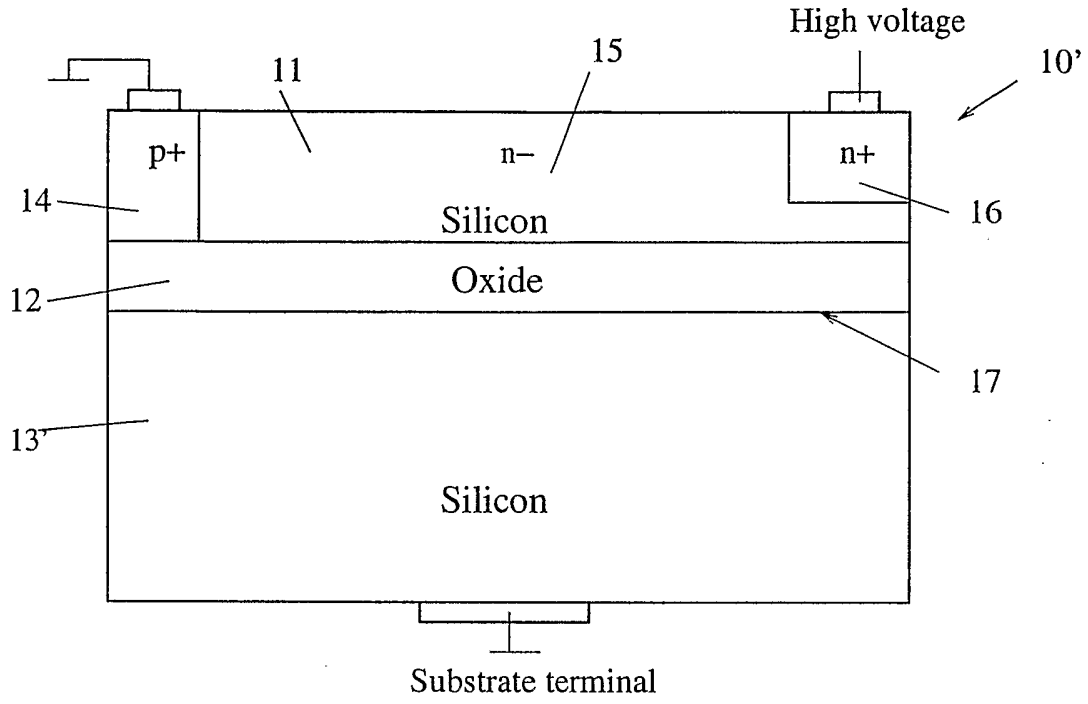

FIGURE 3A

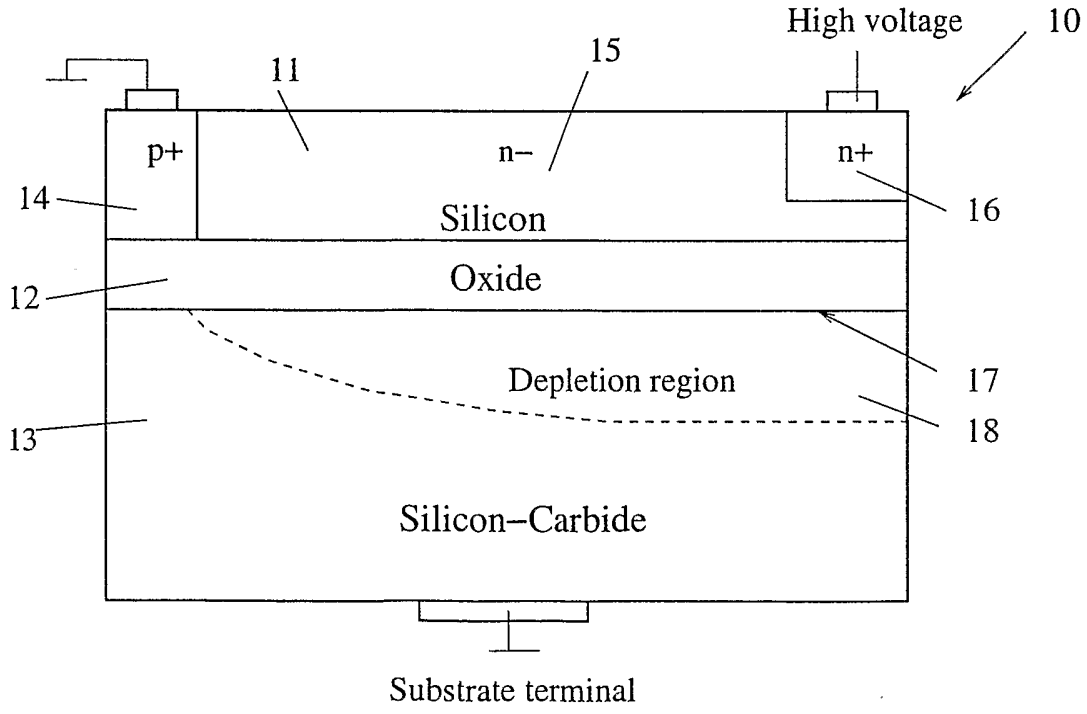

FIGURE 3B

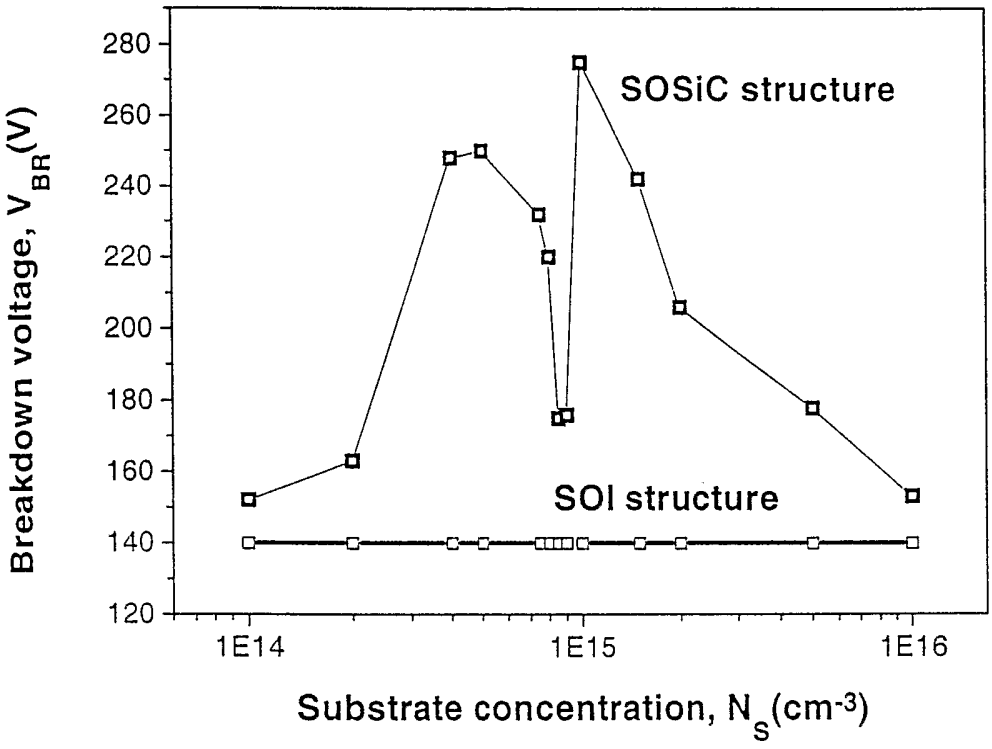
Breakdown voltage, V_{BR}(V)
280
260
240
220
200
180
160
140
120
SOSiC structure
SOI structure
1E14
1E15
1E16
Substrate concentration, N_s(cm^{-3})

Figure 4

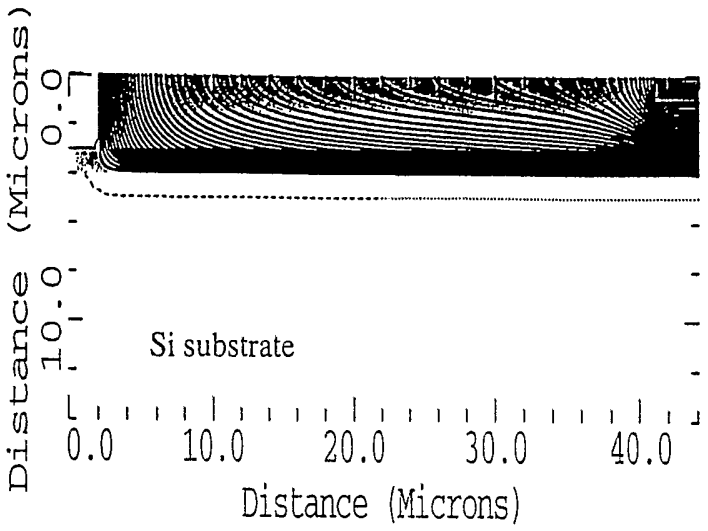

Figure 5A

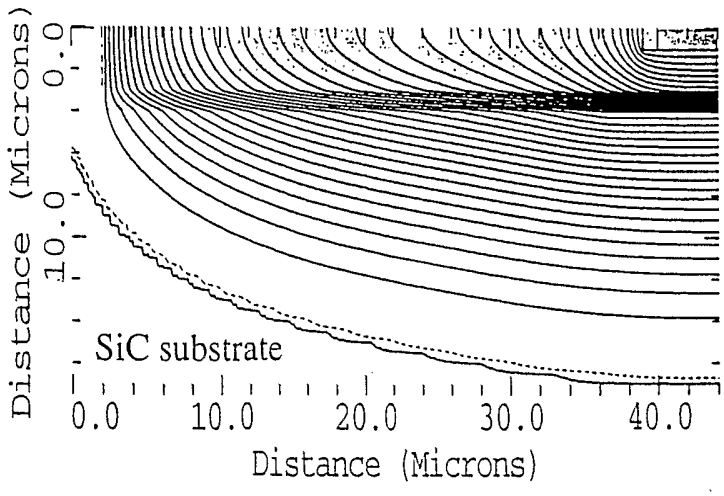

Figure 5B

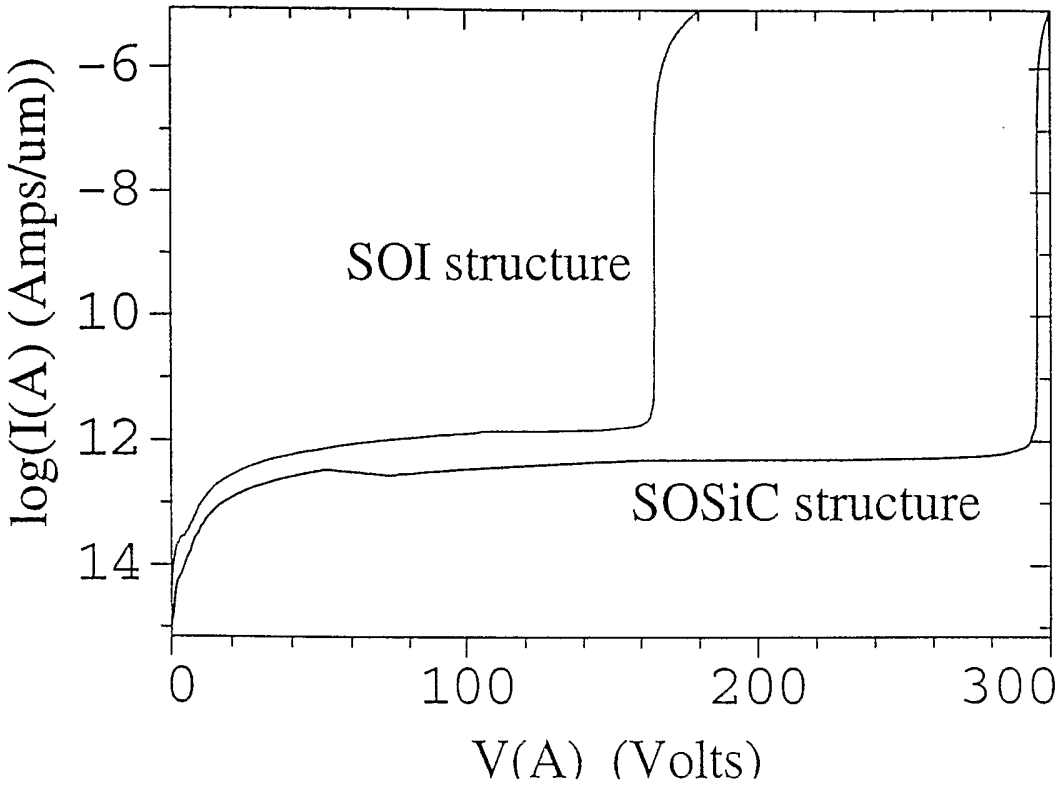
log(I(A) (Amps/um))
-6
-8
10
12
14
SOI structure
SOSiC structure
0
100
200
300
V(A) (Volts)

Figure 6

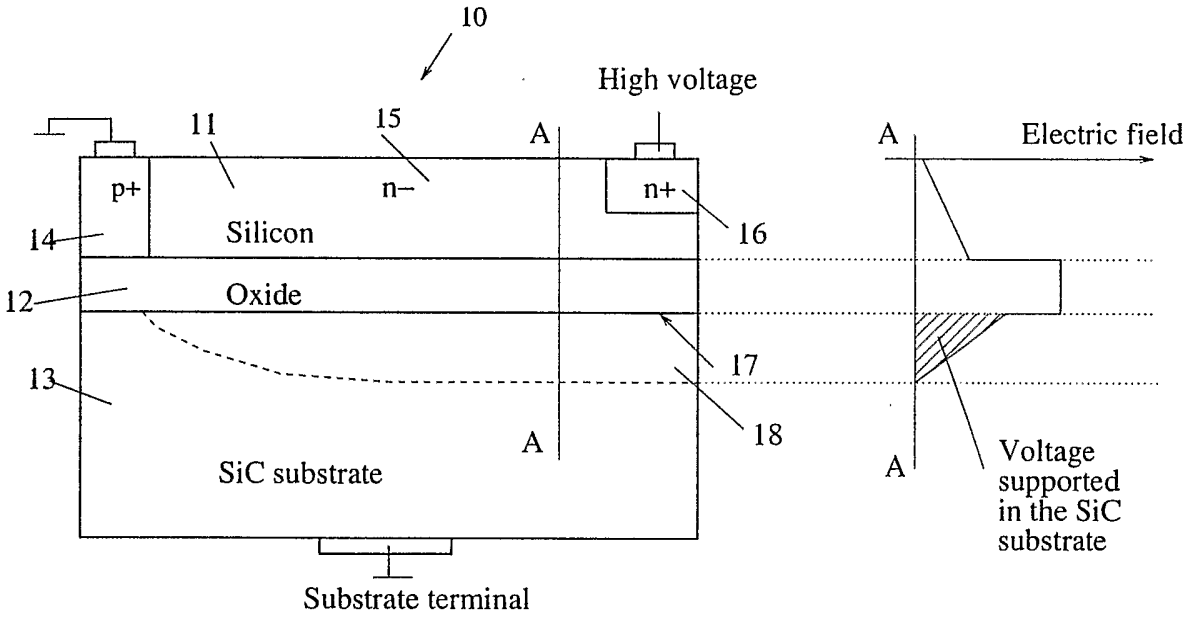
10
High voltage
11
15
A
A
Electric field
p+
n–
n+
14
Silicon
16
12
Oxide
17
13
18
A
A
SiC substrate
Voltage supported in the SiC substrate
Substrate terminal

Figure 7

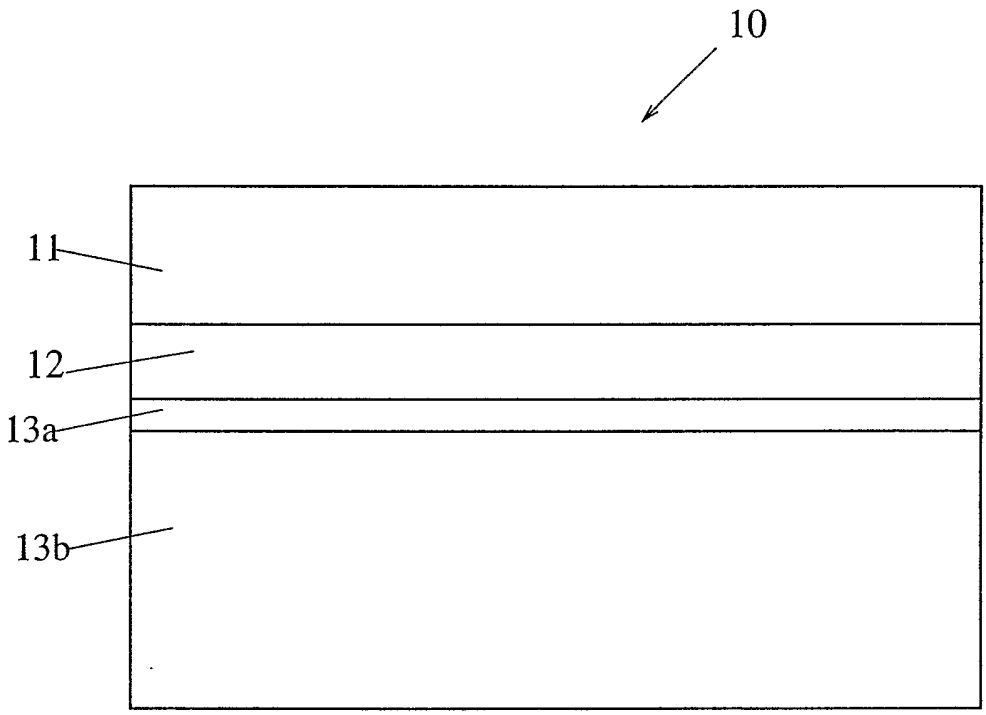

FIGURE 8

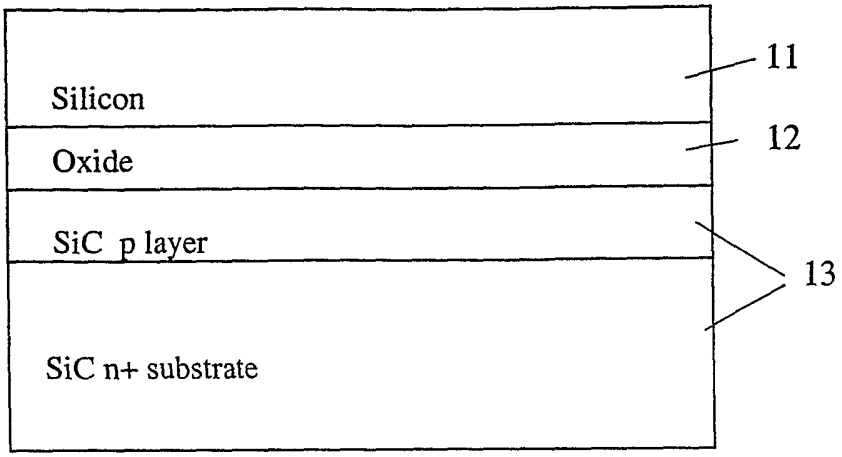

FIGURE 9A

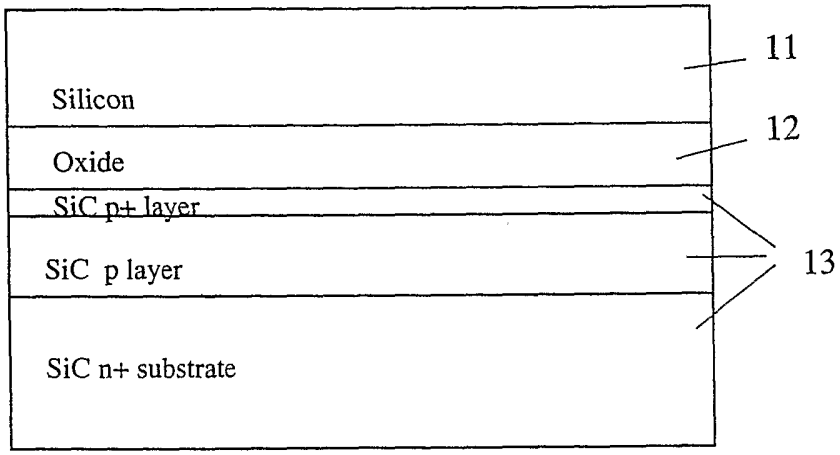

FIGURE 9B

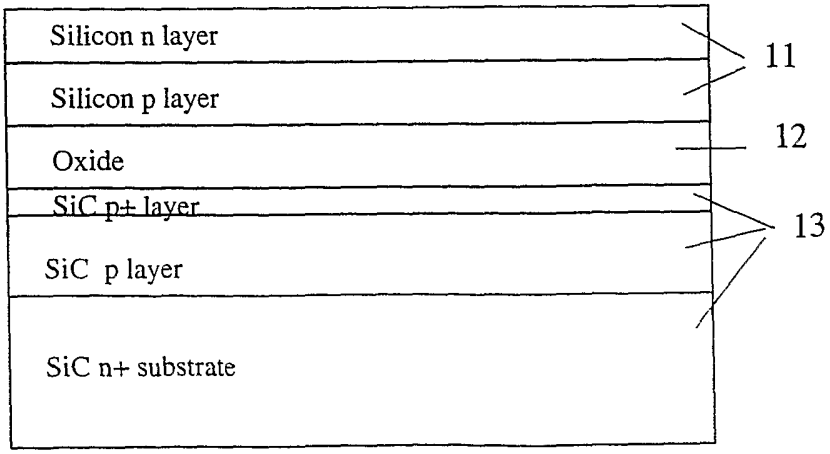

FIGURE 9C

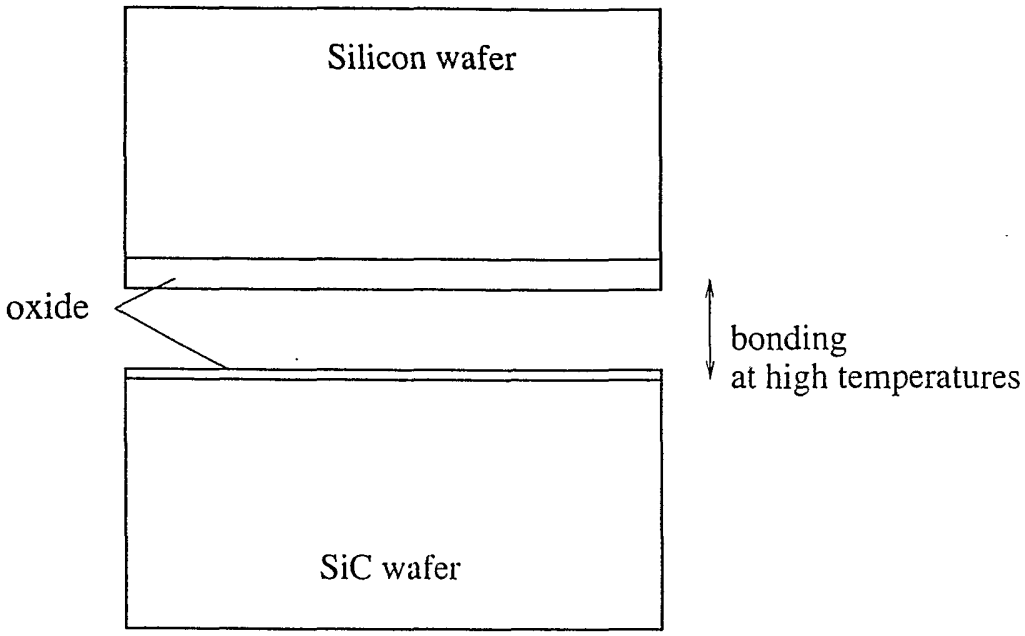

FIGURE 10A

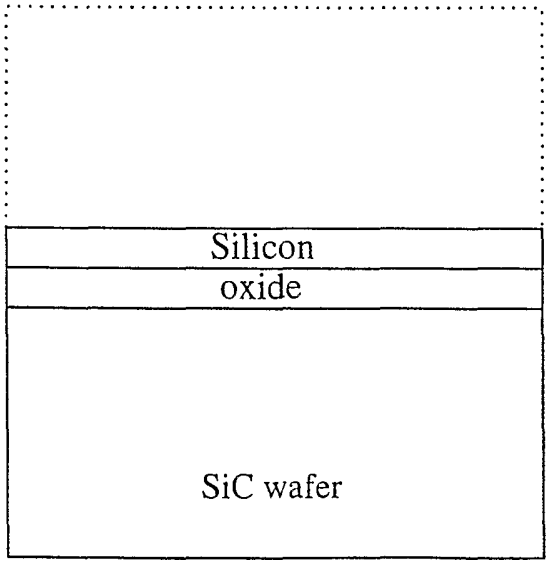

FIGURE 10B

thining down (etching)
of the Silicon to the desired
thickness

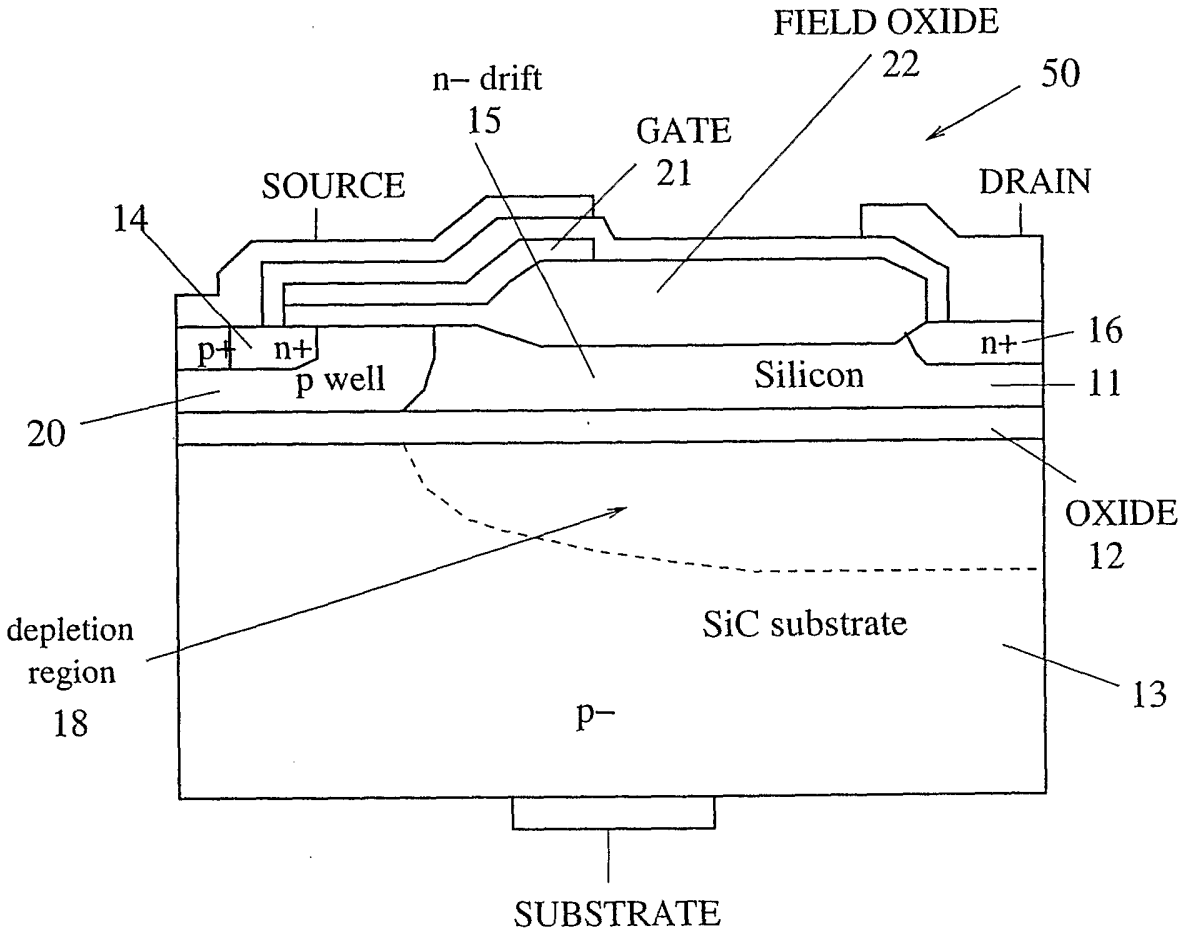
FIELD OXIDE
22
50
n– drift
15
GATE
21
SOURCE
DRAIN
14
p+
n+
p well
Silicon
n+
16
11
20
OXIDE
12
depletion
region
18
SiC substrate
13
p–
SUBSTRATE

FIGURE 11

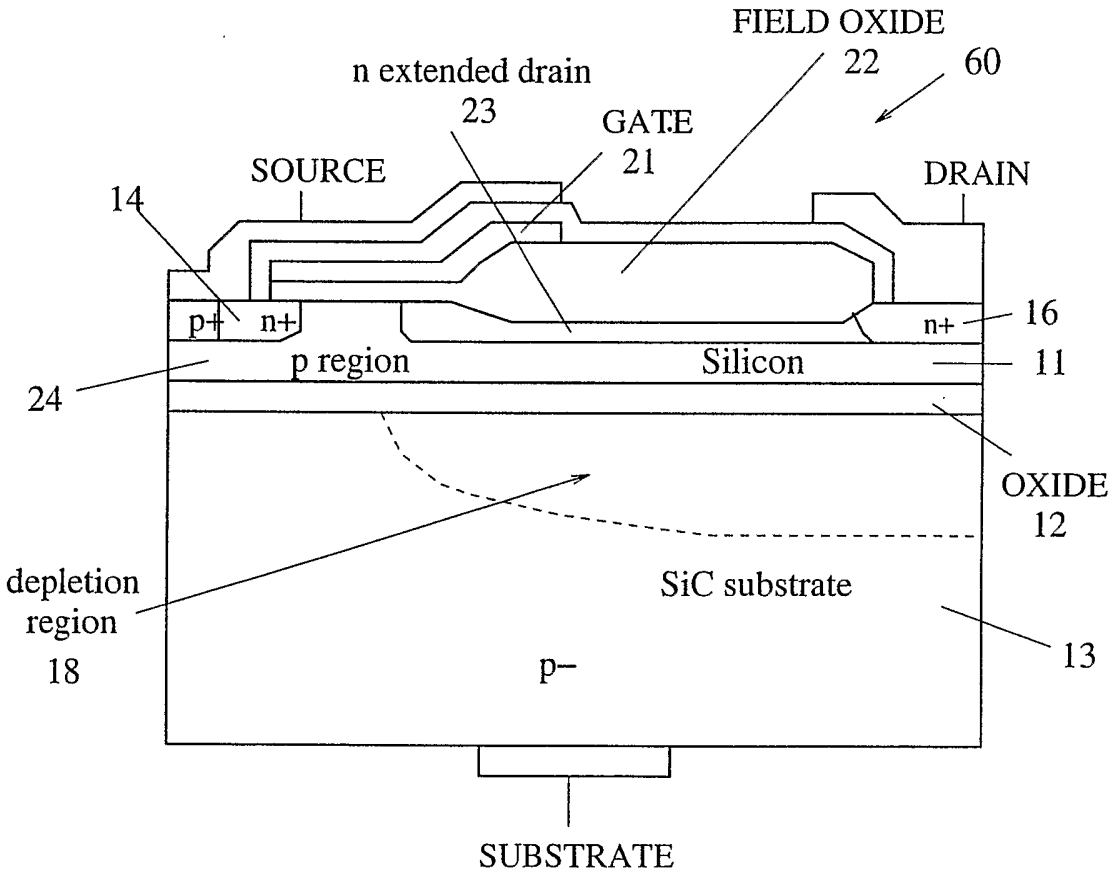
FIELD OXIDE
22
60
n extended drain
23
GATE
21
SOURCE
DRAIN
14
p+
n+
n+
16
p region
Silicon
11
24
OXIDE
12
depletion
region
18
SiC substrate
13
p–
SUBSTRATE

FIGURE 12

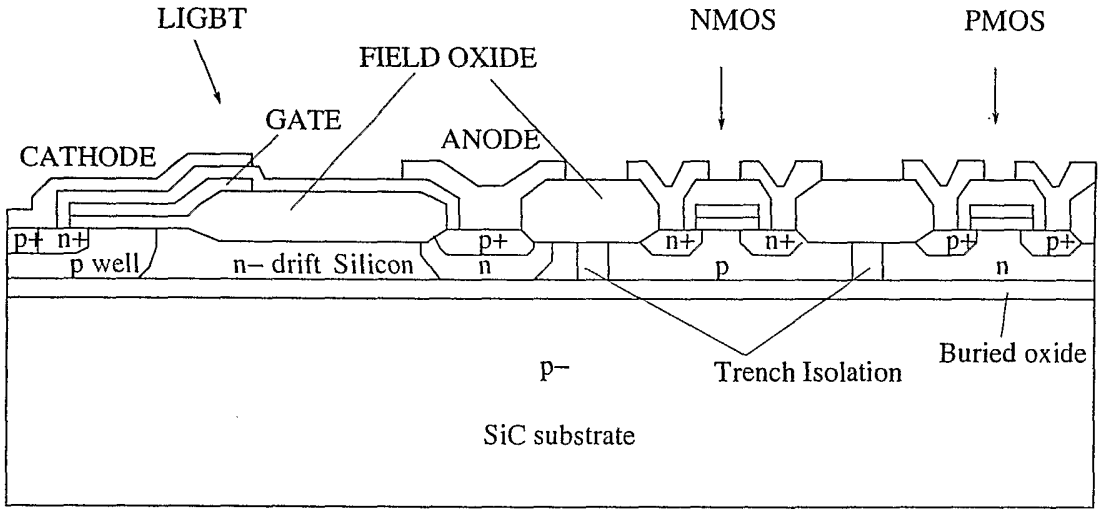
LIGBT
NMOS
PMOS
FIELD OXIDE
GATE
ANODE
CATHODE
p+ n+
p well
n– drift Silicon
p+
n
n+
n+
p
p+
p+
n
Buried oxide
p–
Trench Isolation
SiC substrate

FIGURE 13

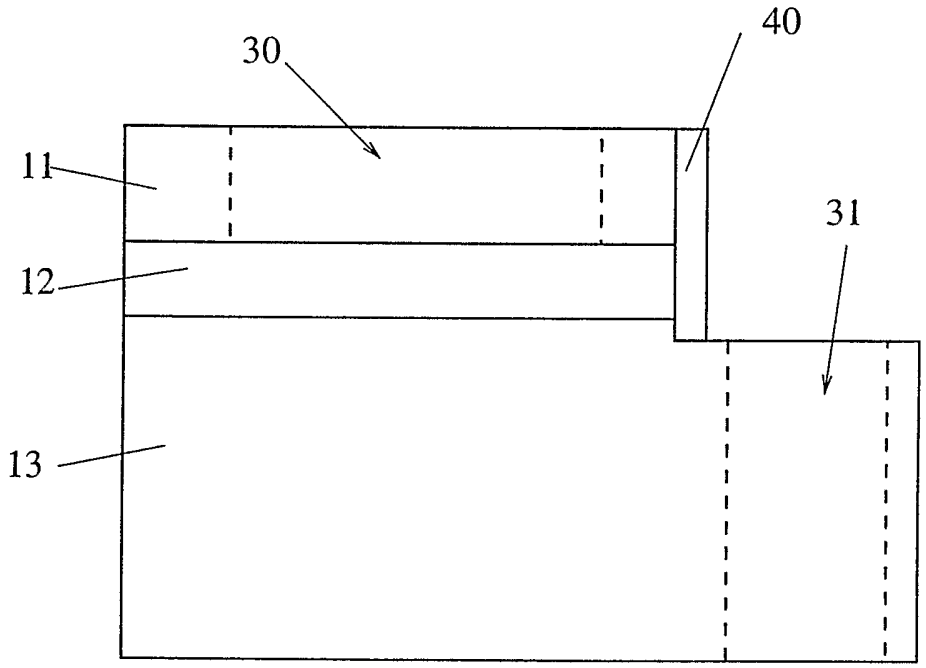

FIGURE 14