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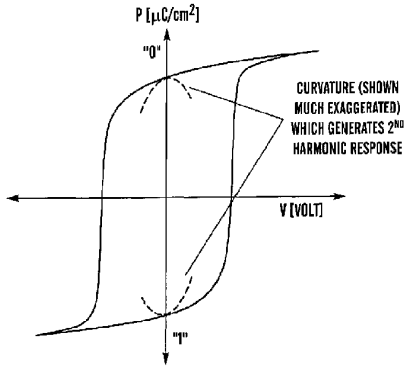
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(54) Title: A METHOD FOR NON-DESTRUCTIVE READOUT AND APPARATUS FOR USE WITH THE METHOD



(57) Abstract: In a method for determining a logic state of a memory cell in a data storage device, wherein the cell stores data in the form of an electrical polarization state in a capacitor containing a polarizable material, a time-dependent small-signal voltage is applied over the capacitor, and at least one component of a generated small-signal current response is recorded. This component shall have either a linear or non-linear relationship to the small-signal voltage, such that logic state can be determined by temporal correlation between the small-signal voltage and a recorded component. According to a first embodiment, an apparatus for performing a phase comparison in the above method comprises a phase-sensitive detector and discriminator, connected with a memory cell for receiving a response signal therefrom and with a signal generator for receiving the read signal input to the memory cell, applying the read signal as a reference in the phase sensitive detector and discriminator for determining a logic state of the memory cell.

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A method for non-destructive readout and apparatus for use with the method

The present invention concerns a method for determining a logic state of a memory cell in a data storage device, wherein said cell stores data in the form of an electrical polarization state in a capacitor containing a polarizable material, wherein said polarizable material is capable of maintaining a non-vanishing electrical polarization in the absence of an externally impressed voltage across said capacitor, and of generating a current response to an applied voltage, said current response comprising linear and non-linear components. The present invention also concerns respectively a first apparatus and a second apparatus for performing a phase comparison in the method according to the invention.

Particularly the present invention concerns a non-destructive readout of memory cells, wherein the polarizable material exhibits hysteresis, notably an electret or a ferroelectric material, as known in the art.

During recent years, data storage has been demonstrated in electrically polarizable media consisting of thin films of ceramic or polymeric ferroelectrics. A major advantage of such materials is that they retain their polarization without the permanent supply of electrical energy, i.e. the data storage is non-volatile.

Two main classes of memory devices have been demonstrated where the logic state of an individual memory cell is represented by the polarization direction of the ferroelectric thin film in that cell. In both cases data are written into the memory cells by polarizing the film in the desired direction through the application of an appropriately directed electrical field exceeding the coercive field of the ferroelectric. However, device architectures are fundamentally different:

In the first class of devices, each memory cell incorporates at least one transistor. The overall memory architecture is of the active matrix type, the major advantage compared with traditional SRAM and DRAM devices being the non-volatile nature of the ferroelectrically stored logic state.

One broad sub-class of such ferroelectric-based memory devices, commonly termed FeRAM or FRAM (a Symetrix Corp. copyrighted term), is extensively described in the scientific and patent literature and is presently being

commercialized by a number of companies worldwide. In its simplest form (1T-1C architecture), each FeRAM memory cell has a single transistor and capacitor as illustrated in fig. 1, where the capacitor contains a ferroelectric which can be polarized in one or the other direction, representing a logic "0" or "1", respectively. A given memory cell is written, i.e. prepared with the ferroelectric capacitor polarized in the desired direction, by applying appropriate voltages to the wordline, bitline and driveline serving that cell. Reading is performed by floating the bitline and applying a positive voltage to the driveline while asserting the wordline. Depending on the direction of polarization in the capacitor, i.e. whether the cell stores a logic "0" or a "1", the charge transferred to the bitline in this process shall be either significant or small, and the logic state of the cell is determined by recording the magnitude of this charge. Since this read operation is destructive, the data must be written back afterwards to avoid permanent loss of stored information. A large number of patents have been issued on variants of the basic FeRAM concept, see, e.g. US patents Nos. 4,873,664 (Ramtron International Corp.), 5,539,279 (Hitachi, Ltd.), 5,530,668 (Ramtron International Corp.), 5,541,872 (Micron Technology), 5,550,770 (Hitachi, Ltd.), 5,572,459 (Ramtron International Corp.), 5,600,587 (NEC Corp.), 5,883,828 (Symetrix Corp.). The patents address both circuit architectures and materials, reflecting difficult problems that have hindered practical implementation of ferroelectric memories since their conceptual introduction decades ago. Thus, the destructive read aspect of these memories has comported fatigue in the ferroelectric materials used, limiting the operational lifetime and thus basic usability for large classes of applications. Following intensive efforts, certain materials (e.g. PZT and SBT) have been refined and modified so as to sustain the large number of switching cycles (10^{10} to 10^{14}) of relevance in the most demanding applications, as well as exhibiting adequate resistance to imprint, etc. However, these optimized materials require annealing at high temperatures, are vulnerable to hydrogen exposure, etc, and generally pose costly and complex problems in connection with integration into high volume production based on established silicon device manufacturing. Further, their requirement for thermal treatment makes them unsuitable for future integration in polymer-based electronic devices. Some of the patents reflect efforts to circumvent drift and manufacturing tolerance problems by making use of more complex architectures. This may include memory cells containing two ferroelectric capacitors and two transistors (2C-

2T designs) to allow for referencing cells and circuits and more complex pulsing protocols. It may be noted that at present all ferroelectric memories in production use the 2C-2T architecture, since materials are still lacking that have adequate stability under exposure to time, temperature and voltage cycling (cf.: D. Hadnagy: "Making ferroelectric memories", The Industrial Physicist, pp.26-28 (December 1999)).

In another subclass of devices employing one or more transistors in each memory cell, the source-drain resistance of a transistor in the cell is directly or indirectly controlled by the polarization state in a ferroelectric capacitor in that cell. The basic idea is not new and has been described in the literature (cf., e.g. Noriyoshi Yamauchi, "A metal-Insulator-Semiconductor (MIS) device using a ferroelectric polymer thin film in the gate insulator", Jap.J.Appl.Phys. 25, 590-594 (1986); Jun Yu et al., "Formation and characteristics of $Pb(Zr,Ti)O_3$ buffer layer", Appl.Phys.Lett. 70, 490-492 (1997); Si-Bei Xiong and Shigeki Sakai "Memory properties of $SrBi_2Ta_2O_9$ thin films prepared on SiO_2/Si substrates", Appl.Phys.Lett. 70, 1613-1615 (1999)). In US Pat.No. 5,592,409 (Rohm Co., Ltd.), Nishimura et al. describe a non-volatile memory based on a ferroelectric film which is polarized in one or the other direction, representing a logic "0" or "1". The polarized ferroelectric provides bias on the gate of a transistor, thereby controlling the current flow through the transistor. An obvious advantage of this mode of operation is that the logic state of the memory cell can be read non-destructively, i.e. without incurring polarization reversal in the ferroelectric capacitor. A related concept disclosed in US Pat. No. 5,070,385 (J.T. Evans and J.A. Bullington), is based on a semiconductor material in close contact with the ferroelectric. Here, the semiconducting material exhibits an electrical resistance which depends on the state of polarization in the ferroelectric. Unfortunately, there remain severe unsolved materials- and processing issues in connection with all of the above-mentioned concepts (cf., e.g. D. Hadnagy, "Making ferroelectric memories", The Industrial Physicist, pp. 26-28 (December 1999)), and their successful commercialization in the foreseeable future is at present doubtful.

In both subclasses referred above, the need for one or more transistors in each cell represents a major disadvantage in terms of complexity and reduced areal data storage density.

In the second class of devices, which is of particular relevance here, memory cells are laid out in a passive matrix architecture where two sets of mutually orthogonal electrodes form arrays of capacitor-like structures at the crossing points between the electrodes. Each memory cell may be created very simply as illustrated in fig. 2, by employing ribbon-like electrodes that define an overlap region where they cross, the overlap region constituting a sandwich of polarizable material between parallel electrode planes. Alternative capacitor structures are possible, however, where the electrical fields that interact with the polarizable material have major components directed parallel to the substrate rather than perpendicular to it. Such "lateral" architectures shall not be discussed further here, however, since the particular choice of cell architecture is immaterial to the subject matter of the present invention. According to prior art, the data in individual memory cells are read by applying an electrical field to the material in each cell in question, of sufficient magnitude to overcome the hysteresis effect and align the electrical polarization in the cell in the direction of the applied field. If the material already were polarized in that direction prior to application of the field, no polarization reversal takes place and only a small transient current flows through the cell. If, however, the material had been polarized in the opposite direction, polarization reversal takes place, causing a much larger transient current to flow through the cell. Thus, the logic state, i.e. the direction of the electrical polarization in the individual memory cell, is determined by application of a voltage of magnitude sufficient to exceed the coercive field in the ferroelectric, and detection of the resulting current.

Compared to active matrix based devices, the passive matrix based ones can be made with much higher memory cell density, and the memory matrix itself is much less complex. However, the readout process according to prior art is destructive, involving loss of the data content in the cell that is read. Thus, data that are read must be written back into the memory device if further storage of those data is desired. A more serious consequence of the polarization switching is fatigue, i.e. a gradual loss of switchable polarization which typically is accompanied by a need for higher applied voltage to the cell to effect the polarization reversal. Fatigue limits the number of read cycles that can be sustained by a given memory cell and thus the range of applications. In addition, it leads to slower response and higher voltage requirements for the memory device. The attendant gradual variation in the operation parameters for individual memory cells in a given device cannot be

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predicted a priori and leads to a need for "worst case" design and operation which is sub-optimal.

Efforts have been made to develop techniques that allow non-destructive readout from ferroelectric-based memories while maintaining simple elementary memory cell architecture. Thus, C.J. Brennan describes ferroelectric capacitor cells and associated elementary circuit modules for data storage in US Patent Nos. 5,343,421; 5,309,390; 5,262,983; 5,245,568; 5,151,877 and 5,140,548. By probing the small-signal capacitance values while simultaneously subjecting the ferroelectric to moderate bias fields, i.e. bias fields that do not lead to the peak voltage across the cell during read-out exceeding the coercive field in the ferroelectric, the direction of the spontaneous polarization in the capacitor and thus the logic state of the memory cell is determined. However, there are certain very specific premises for applying the methods and apparatus as described by Brennan, invoking phenomena based on space charge accumulation at the electrodes which is explicitly dependent on the materials used in the electrodes and the adjoining ferroelectric. Readout of data involves probing of the space charge, which must be performed on time scales that are compatible with such charge accumulation. Furthermore, Brennan's patents contain no teachings on how the small-signal and biasing voltages shall be timed and correlated in relation to each other, which is of paramount importance for implementation in practical devices. The above mentioned US Pat. 5 140 548 describes a device which does not require bias from an external source, deriving an internal bias from a contact potential difference between the electrodes sandwiching the ferroelectric core. While elegant in principle, this solution suffers from serious drawbacks when faced with the task of implementations in practical devices. Thus, the predictability and control that can be achieved by external biasing is sacrificed, being replaced by a fixed bias which is explicitly dependent on materials purity and processing conditions as well as operating temperature. The unipolar and continuous nature of the internally generated bias promotes imprint in the ferroelectric, a well-known and highly undesirable phenomenon in ferroelectric memory devices. Finally, a fixed bias is of little or no value when implementing correlation strategies as taught in the present document.

Japanese patent publications Nos. JP-A-06275062 and JP-A-05129622 (Masayoshi Omura) disclose non-destructive readout of a passive

matrix-addressable ferroelectric memory device. The polarization state of individual memory cell is determined by recording the phase of the second harmonic current response of a memory cell excited by a small signal periodic voltage. Moreover JP-A-06275062 teaches the application of a bias voltage for positioning the working point on the hysteresis curve close to the point of maximum curvature for one of the logic states, thus enhancing the second harmonic amplitude.

US patent No. 5,666,305 (Mihara & al.) discloses non-destructive readout in a passive matrix-addressable ferroelectric memory by applying perturbing voltage pulses at a level well below the coercive voltage.

US patent No. 3,132,326 (J.W.Crownover) discloses non-destructive readout of a ferroelectric memory cell in a similar manner by using voltage pulses smaller than the coercive voltage to probe a memory cell current response.

US patent No. 5,262,982 (Brassington & al.) discloses the use of positive unipolar pulse with simultaneous detection of a current repose to probe the average slope of the hysteresis curve to the right of the polarization axis followed by a negative unipolar pulse probing the hysteresis curve in a similar manner and then providing a difference between the result obtained both pulses.

These latter five patent publications having in common that they all base a non-destructive readout by generally applying a read or probing signal at a voltage level appreciably smaller than the coercive voltage and then performing the detection of a logic state on some parameter of a current response. In one case a second harmonic response is used for the detection. Generally of these prior art methods are encumbered by inherent weaknesses with regard to providing a reliable determination of a memory cell logic state, the more so as the use of a single read signal will not allow the application of more sophisticated correlation techniques which shall be a requirement when a non-destructive readout is to be performed in the small signal domain.

Finally, with regard to obtaining a more reliable non-destructive readout in a passive matrix-addressable ferroelectric memory, US patent No. 5,530,667 (Omura & al.) proposes a memory device with a ferroelectric memory material providing hysteresis curve with non-linear portions in two steep

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rising/ascending regions. Non-destructive readout is carried out by using a probing signal without exceeding the coercive voltage and applying this probing signal in regions of the hysteresis curve that will ensure a detectable capacitance differential between two recorded logic states.

Generally and particularly with regard to making passive matrix-addressable ferroelectric memory devices that are commercially viable, there is a pressing need for devices and methods whereby data can be read non-destructively from memory cells in the form of capacitors with electrical polarizable material exhibiting hysteresis and wherein the memory cells are not dependent on containing active circuits elements as transistors. Taking into account the fact that non-destructive readout in a passive matrix-addressable ferroelectric memory must take place with read voltages appreciably lower than the coercive voltage and usually in a small signal regime, there is also a need for more reliable non-destructive readout methods than those hitherto suggested by prior art as cited above.

The discussion of the background to the invention is included herein to explain the context of the invention. It is not to be taken as an admission or a suggestion that any of the material referred to was published, known or part of the common general knowledge as at the priority date of any of the claims.

It is desirable that the present invention to provide a conceptual basis for non-destructive read-out of data from data storage devices containing cells with electrically polarizable media, in particular ferroelectrics.

By extension of the above, it is desirable to permit read-out of data without incurring the fatigue and wear that accompany the traditional read-out by polarization switching and which limits the usable life span of memory devices based on ferroelectrics. Further it is desirable to obviate the need for restoring the data content of cells that have been read, which is required in destructive readout techniques, and thus to simplify the readout protocol and reduce the hardware complexity.

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It is also desirable to enhance the reliability in the readout process by providing more than one discrimination criterion for determination of logic state in a given memory cell.

Finally, it is also desirable to describe generic procedures and hardware to implement such non-destructive read-out of data.

According to a first aspect of the present invention, there is a method for determining a logic state of a memory cell in a data storage device, wherein said cell stores data in the form of an electrical polarization state in a capacitor containing a polarizable material, wherein said polarizable material is capable of maintaining a non-vanishing electrical polarization in the absence of an externally impressed voltage across said capacitor, and of generating a current response to an applied voltage, said current response including linear and non-linear components, and wherein said method includes the following steps:

applying a first time-dependent small-signal voltage over said capacitor, said small-signal voltage having an amplitude and/or duration less than that required for causing a significant permanent change in the polarization state of said capacitor,

applying a second time-dependent voltage over said capacitor, said second time-dependent voltage being added to said first time-dependent voltage, the sum of the first and second time-dependent voltages having an amplitude and/or duration less than that required for causing a significant permanent change in the polarization state of said capacitor,

recording at least one characteristic of a generated small-signal current response over said capacitor, said at least one characteristic having either a linear or non-linear relationship to said first and/or second applied time-dependent voltages,

performing a correlation analysis based on correlation reference signals derived from both said first and said second time-dependent voltages applied over said capacitor,

determining the logic state by establishing a numerical value for the result of said correlation analysis, and

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assigning the determined logic state a logic value according to a predetermined protocol.

In the method according to an embodiment of the invention, it is considered advantageous performing the correlation analysis in two stages, the first stage of said correlation analysis comprising recording a temporal correlation between said small-signal voltage and said at least one recorded characteristic of a generated small-signal current response over said capacitor to establish the magnitude(s) of at least one parameter which characterizes said at least one recorded characteristic of a generated small-signal current response over said capacitor, and the second stage of said correlation analysis comprising recording the correlation between said at least one parameter on the one hand and the magnitude, sign and/or phase of said second time-dependent voltage on the other hand.

In the method according to another embodiment of the invention, it is also considered advantageous performing the correlation analysis in a single stage where said at least one characteristic of a generated small-signal current response over said capacitor is correlated with a reference signal derived from both first and second applied time-dependent voltages.

In the method according to yet another embodiment of the invention it is considered advantageous that the second time-dependent voltage applied over said capacitor is a quasi- static voltage of either polarity, and then it is preferred that it is switched between a set of positive and negative values.

In the method according to still another embodiment of the invention, it is considered advantageous that the second time-dependent voltage over said capacitor is a low-frequency or a slowly varying voltage, and then it is preferred that it is a sinusoidally varying voltage.

In a first preferred embodiment of the method according to the invention said first time-dependent small signal voltage is selected as being periodic with a dominant Fourier component at frequency ω, the phase of the 2^{nd} harmonic component of said current response recorded, and said first part of said correlation analysis is performed with a reference phase derived from said first time-dependent small-

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signal voltage impressed on said capacitor. In that connection it is considered preferable selecting said first time-dependent small-signal voltage as being sinusoidal.

In a second preferred embodiment of the method according to the present invention said time-dependent voltages are selected as two periodically varying signals with dominant Fourier components at frequencies ω_1 and ω_2, respectively, the phases of the components of said current response are recorded at the sum and difference frequencies $\omega_1+\omega_2$ and $\omega_1-\omega_2$, and said phases compared with a reference phase derived from said time-dependent voltages impressed on said capacitor. In that connection it is considered preferable selecting said periodically varying voltage components as sinusoidal. It is also then preferable recoding the phases of two or more of the non-linear current response components, at $2\omega_1$ and/or $2\omega_2$ and/or $\omega_1+\omega_2$ and/or $\omega_1 . \omega_2$, and comparing said phases with a reference phase derived from said time dependent voltages impressed on said capacitor, or comparing said phases with the reference phase derived from a reference cell of a known logic state that is subjected to the same impressed voltages.

In a third preferred embodiment of the method according to the invention recording said at least one characteristic of a generated small-signal response over said capacitor comprises recording the ratio between the magnitude of said small-signal current response to said first time-dependent small-signal voltage on the one hand and the magnitude of said first time-dependent small-signal voltage on the other hand, said ratio corresponding to the slope of the hysteresis curve, at two or more values of said second time-dependent voltage. In that connection it is considered preferable selecting said second time-dependent voltage as a low-periodic or slowly varying offset voltage which is varied between a set of predetermined positive and/or negative values, and then particularly selecting said second time-dependent voltage varying periodically between a positive and a negative value. In that connection it is alternatively also considered preferable selecting said second time-dependent voltage as a smoothly varying voltage sweeping a voltage range between two positive values or two negative values or a positive and a negative value, and then sweeping said second time-dependent

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voltage periodically at a frequency lower than said time dependent voltage. The second time-dependent voltage can then advantageously be selected as varying sinusoidally with time.

In the method according to the present invention it is preferred that said predetermined protocol assigns said logic state either of two logic values dependent on the established numerical value.

Another aspect of the present invention provides apparatus for performing a phase comparison in the method according to the present invention, the apparatus including a signal generator for supplying two or more read signals with given phases to a memory cell connectable therewith, the memory cell in response to said read signals outputting a response signal having two or more non-linear current components; a phase sensitive detector connectable with the memory cell and adapted for performing a phase sensitive detection of at least two phases in the response signal output from the memory cell; a reference source connected with said signal generator and adapted for generating phase references from the sum and differences of the phases of the input read signals to the phase sensitive detector connected therewith for detecting and correlating said response components, and performing a phase comparison between the phase references and at least one detected and correlated response component; and a discriminator/logic circuit being connected with the phase sensitive detector for receiving the output thereof and adapted for determining a logic state of the memory cell.

In that connection it is considered advantageous that an $\omega+\pi$ phase shifter is connected with the reference source for receiving the output thereof and delivering the $\omega+\pi$ phase shifted output to the phase sensitive detector and optionally also to the discriminator and logic circuit.

Finally, an aspect of the present invention provides apparatus according to the present invention, which includes a signal generator for supplying a first periodic read signal superimposed on a second periodic read signal with lower frequency

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than the first read signal to a memory cell connectable therewith, said memory cell outputting a response signal at twice the frequency of the first read signal; and a phase-sensitive detector and discriminator connectable with said memory cell for receiving the response signal therefrom as well as phase reference signals respectively in the form of the first and second read signals from the signal generator, and correlating the phase of the response signal with the phase of either phase reference signal or both, said phase sensitive detector and discriminator determining a logic state of the memory cell by the magnitude and/or the phase of the phase-correlated response signal.

The foregoing and other objects, features and advantages of the invention will become more readily apparent from the following detailed description of preferred embodiments of the inventions, when read in conjunction with the appended drawing figures, of which

fig. 1 shows an example of a prior art 1C-1T ferroelectric memory cell structure incorporating one transistor and one ferroelectric capacitor in each cell, as mentioned above,

fig. 2 shows a passive matrix addressing structure with memory cells formed at the intersection of crossing electrodes in an orthogonal grid pattern, as mentioned above,

fig. 3a shows a generic hysteresis curve for a memory substance of the ferroelectric type, with certain salient features highlighted,

fig. 3b shows a generic high-frequency small-signal polarization response as a function of polarization history and applied bias voltage,

figs. 4a-4d show examples of read-out by local slope detection, i.e. the polarization vs. voltage response for a memory cell that is excited by a voltage signal as shown, as applied in the present invention,

fig. 5a shows the principle of read-out by second harmonic detection as applied in the present invention,

fig. 5b shows a block diagram of a prior art apparatus used for readout by second harmonic detection,

fig. 6 shows block diagram of an apparatus according to the invention and used for readout by parametric mixing,

fig. 7a shows the principle of readout by enhancement of 2nd harmonic response by periodically shifted offset voltages according to the present invention,

fig. 7b shows a block diagram of a variant of the apparatus in fig. 5b and used for readout by enhancement of the second harmonic response according to the present invention,

fig. 8a shows the principle of readout by periodic modulation of 2nd harmonic response by a sinusoidal, lower frequency offset voltage according to the present invention, and

fig. 8b a shows block diagram of a variant of the apparatus in fig. 5b and used for readout by periodic modulation of the second harmonic response according to the present invention.

As described above, prior art techniques for reading of logic state stored as a polarization direction in a ferroelectric capacitor in a memory cell shall typically involve either one of the following, viz. employing a microcircuit in each memory cell, where the sense of polarization in the memory capacitor (i.e. its logic state) determines the bias at the gate of a transistor and thus the current flow to a sense amplifier reading that cell, or imposing a voltage across the ferroelectric capacitor, and of sufficient magnitude to cause polarization reversal in the capacitor. Depending on whether the sense of polarization in the capacitor is parallel or opposite to the imposed field, polarization will remain unchanged or flip to the opposite direction. While the former provides non-destructive read-out, there are severe problems relating to materials and processing, cf. the prior art discussion above. The latter set of readout techniques are destructive, involving polarization switching with inherent fatigue problems, etc., and loss of data content.

As shall now be described with reference to generic electrical polarization response characteristics of materials exhibiting polarization remanence, in particular ferroelectrics, there exist alternative read-out methods that are non-

destructive, simple to implement and compatible with active matrix as well as passive matrix addressing schemes. However, the physical phenomena that are involved are numerous and complex, and therefore it is necessary to tailor the read-out scheme to the materials, architectures and time scales of interest in each given situation.

According to the present invention, the logic state, i.e. the direction of the electrical polarization, in a given cell in the memory device is determined by recording the non-linear electric impedance response of said cell to a time-varying voltage with a voltage excursion much less than that which is required to effect polarization reversal in said cell. As will be shown, this non-linear response may exhibit a bias voltage-dependent small-signal impedance where the magnitude of this impedance can be correlated with the bias voltage to reveal the logic state of the cell. Alternatively, the non-linearity engenders a response of different spectral frequency content than that of the exciting voltage, e.g. it may contain higher harmonics and/or sum-and difference frequency components relative to the frequency content of the exciting voltage, where the phase and/or magnitude of said non-linear response components shall be different, depending on the logic state of the cell.

In the present context, it is important to distinguish between the polarization response through interaction with the dipoles that are responsible for the remanent polarization, on the one hand, and on the other hand the response from the quasi-bound mobile charges that accumulate in response to the polarization set up by these dipoles and by the impressed field from the electrodes. This shall have an impact upon the frequencies and readout pulse protocols that can be used in each case, as well as upon possible restrictions that apply with respect to the selection of electrode materials.

With reference to the former case, the generic hysteresis loop shown in fig. 3a illustrates the response of a pre-polarized medium to an impressed external voltage on the electrodes in the capacitor-like structure. The impressed voltage in this case follows a cyclic variation between two extreme values at positive and negative polarities as shown. The relationship is complex, where the local polarization vs. voltage response at a given point on the curve is dependent on previous polarization/voltage history as well as being non-linear on macroscopic as well as microscopic scales. Depending

on whether the material has been prepared in a logic "0" and "1" state, respectively, there exist logic state-dependent differences in the local polarization vs. voltage response which can be exploited to provide non-destructive means for reading the logic state. These differences manifest themselves in a small-signal polarization response which depends on the position on the curve, and where the small-signal polarization response may contain both linear and non-linear response components relative to an imposed small-signal exciting voltage. Accordingly, the small-signal complex impedance sensed across a memory cell in the form of a capacitor containing material with characteristics as shown in fig. 3a may be analyzed in correlation with the imposed voltages on the capacitor to reveal the logic state of the memory cell. It must be observed that the frequencies of the applied bias and small-signal probing voltages must be selected sufficiently low to allow the dipole-originated polarization to follow. Depending on the material in question, temperature, etc, the maximum allowable frequency may range widely (hundreds of Hz to GHz), with displacive inorganic ferroelectric ceramics responding very fast and alignment-based polymeric ferroelectric polymers responding more slowly.

Turning now to the latter case, where the polarization response is due to quasi-bound or mobile charges that accumulate under the influence of internal fields in the material, a survey of the scientific literature shows that the basic phenomena of polarization-dependent asymmetry, bias dependence and non-linear response appears to be a general attribute of all ferroelectric materials in capacitor-like structures of the type relevant here. Although in many cases the magnitude of the polarization response is greatly diminished, this applies even at frequencies far exceeding those where the ferroelectric polarization can follow, in which case it is not pertinent to explain these phenomena in terms of the hysteresis curve of fig. 3a.

In the present invention, the logic state, i.e. the direction and/or magnitude of the remanent polarization, is determined by exploiting the nonlinearities inherent in the polarization response of the material under an impressed electric field. Two basic approaches shall now be described.

In the first, the material is subjected to a small-signal probing voltage superimposed on a bias voltage, and the polarization response at the same frequency as that of the probing voltage is determined as a function of the

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bias voltage. A generic small-signal polarization response curve is shown in fig. 3b. With the response being recorded at the same frequency as the driving voltage, this response is simply the bias-dependent capacitance which is related to the polarization state of the material. It is important to realize that while exhibiting the same qualitative behaviour, there is a fundamental difference between the physical mechanisms leading to such curves by interaction with accumulated quasi-bound or mobile charges on the one hand, and on the other hand curves obtained by small-signal probing of the slope of the hysteresis curve. Due to the similarities in certain of the read-out schemes to be described below, the descriptions of preferred embodiments as based on principles as illustrated in figs. 4a-d shall be cast in terms of the local small-signal response on different parts of the hysteresis curve, which provides an easily understood intuitive grasp of the basic principles involved. It is to be understood, however, that the technical description of the read-out apparatus and voltage protocols shall also apply for the cases where quasi-bound and/or mobile charges are being probed. The latter case shall not only encompass frequency regions where full or partial reversal of the remanent polarization can take place as evinced by hysteresis curves, but also high-frequency regions where domain switching cannot follow. In this connection one may note that the readout schemes taught by C. Brennan in his above cited patents are explicitly based on interaction with accumulated space charges, according to a specific model where the probed space charges are proximate each electrode with a neutral region between, the relative size of the neutral and space charge regions defining the perceived capacitance. This places Brennan's schemes outside the realm of that part of the present discussion that is based on the hysteresis curves, as well as ignoring numerous other physical phenomena leading to small-signal response characteristics of the type shown qualitatively in fig. 3b.

In the second, the material acts as a polarization-state dependent parametric mixing device, yielding an output response which contains new frequency components in addition to those present in the small-signal excitation voltage. Thus, driving the polarization at a given frequency engenders a polarization response and thus a detectable current which in addition to the fundamental frequency also contains higher harmonics. If the driving voltage contains several frequency components, the response may contain sum-and difference frequency components also, with specific phase relationships that can be uniquely linked to the remanent polarization state of the medium.

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Again, the descriptions in the examples given below are given with reference to the hysteresis curves, which provides a simple, intuitive approach to understanding the underlying principles. As discussed above, however, the same basic read-out principles and apparatus shall be applicable in high-frequency regimes where the polarization switching manifested in hysteresis curves cannot follow, being linked to quasi-bound or mobile space charges.

Certain preferred embodiments are described below by way of examples 3, 4 and 5. They represent generic classes of possible implementations sharing the common feature of small-signal excitation of the memory cell to excite via non-linearity and polarization history generated asymmetry a logic state-dependent polarization response. In order to simplify the discussion, it shall be assumed that the polarization response to a time varying voltage of small amplitude shall trace back and forth along a portion of the curve in fig. 3a. This assumption ignores the effects of partial switching and fatigue which lead to a gradual reduction in polarization magnitude, as well as causing the small-signal polarization response to exhibit hysteresis in itself.

Before preferred embodiments are described, two examples giving a general background for and elucidating the underlying principles of the present invention shall be discussed in some detail in the following.

Example 1: Differentials in small-signal polarization response

The slope, i.e. the small-signal linear polarization response representing the first derivative dP/dV of the hysteresis curve, is voltage- and history-dependent. In the generic curve shown in fig. 3a the slope is identical for the two logic states at "0" and "1" and a slope measurement at these points shall not reveal the logic state. By imposing a certain voltage bias V and probing the slope behaviour in the vicinity of the points "1" and "0", the logic state can be determined. Now defining :

Slope near "0" and at bias voltage V = $\text{Slope}_{\text{"0"}}$ (V)

Slope near "1" and at bias voltage V= $\text{Slope}_{\text{"1"}}$ (V),

one obtains from fig. 3:

$$\text{Slope}_{\text{"0"}}(+\Delta V) < \text{Slope}_{\text{"1"}}(+\Delta V)$$

$$\text{Slope}_{\text{"0"}}(-\Delta V) > \text{Slope}_{\text{"1"}}(-\Delta V).$$

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Thus, the logic state of the cell in question can be read out by applying a bias voltage of known magnitude and polarity and recording the slope in at least two points on the curve. This can be achieved in different ways:

a) By recording the magnitude of the slope at two or more discrete bias voltage values as illustrated in fig. 4a, and comparing the differential between the slopes with a threshold value.

b) By monitoring the magnitude of the small-signal polarization response while imposing a probing voltage consisting of a slow periodic sweeping voltage on which is superimposed a small periodic voltage swing at a higher frequency, as illustrated in fig. 4b.

c) By recording the differential polarization between selected discrete points on the hysteresis curve. An example is illustrated in fig. 4c.

For a "0" logic state, one has

$$|P(+\Delta V) - P(0)| < |P(0) - P(-\Delta V)|$$

while for a "1" logic state,

$$|P(+\Delta V) - P(0)| > |P(0) - P(-\Delta V)|.$$

d) By recording the asymmetry of the polarization excursions (peak-to-peak, RMS, or the like) in response to imposed sweeping voltages of positive and negative polarity. An example showing two separate sweeps is shown in Fig. 4d, but the asymmetry can be detected in a number of ways apparent to a person skilled in the electronic art.

Example 2: Harmonic detection of response to sinusoidal input voltage

The following simple treatment may be helpful in gaining an intuitive insight into the basic idea.

Referring to fig. 3a, it is desired to establish whether the memory material in a given memory cell is in the logic state "0" or "1". The two logic states are characterized by different curvatures at the points where the hysteresis curve intercepts the V = 0 axis. Expanding to 2nd order, one may write:

(1) $P(\text{"0"}) = P_0 + \alpha V - \beta V^2$

(2) $P(\text{"1"}) = -P_0 + \alpha V + \beta V^2$

Assume now that the cell is excited by a sinusoidally varying voltage of amplitude much less than that which is required to switch the polarity of the cell, as illustrated in fig. 5a, one has

(3) $V(t) = V_0 \cos(\omega t)$

The polarization response becomes

(4) $P(\text{“0”}) = P_0 + \alpha V_0 \cos(\omega t) - \beta V_0^2 \cos^2(\omega t)$
$= (P_0 - \frac{1}{2} \beta V_0^2) + \alpha V_0 \cos(\omega t) + \frac{1}{2} \beta V_0^2 \cos(2\omega t + \pi)$

and

(5) $P(\text{“1”}) = -P_0 + \alpha V_0 \cos(\omega t) + \beta V_0^2 \cos^2(\omega t)$
$= -(P_0 - \frac{1}{2} \beta V_0^2) + \alpha V_0 \cos(\omega t) + \frac{1}{2} \beta V_0^2 \cos(2\omega t)$

Thus, the polarization response of the memory cell at the 2nd harmonic frequency depends on whether the cell is in a “0” or a “1” state, i.e. the 2nd harmonic responses in the two states are in anti-phase to each other (mutually out of phase by 180 degrees). By suitable detection, e.g. coherent averaging (lock-in detection), this difference can manifest itself in a qualitative manner, for instance as a positive or negative polarity in a detection signal.

A prior art apparatus for performing a detection of the polarization response at the second hamonic is shown as a schematic block diagram in fig. 5b. A signal source inputs a sinusoidally varying voltage at the frequency ω to a memory cell which outputs a response signal with harmonics to a phase-sensitive detector as shown. The phase-sensitive detector can in variant embodiments be regarded as a combined phase-sensitive detector and discriminator. Simultaneously the signal source also generates an input phase reference to a reference source which outputs a reference signal at twice the frequency ω of the read signal to the phase-sensitive detector. The output voltage from the phase-sensitive detector shall be dependent on the logic state of the memory cell, and the actual logic state can be based on simply a qualitative parameter, e.g. the polarity of the detection signal as stated.

As can be readily ascertained and as is apparent to persons skilled in the art of signal analysis, higher order non-linearities in the polarization response of the memory cell shall more generally result in higher than second harmonics appearing in the detected signal. By the same basic principles as outlined above and depending on the specific response characteristics of the memory

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cell in question, such signal components may also be extracted from the overall signal and reveal the direction of polarization and thus the logic state of the cell. Thus, the above example based on 2nd harmonic detection shall not be implied or construed to preclude detection of higher than 2nd harmonics as the operative principle for determination of the logic state of the cell in question.

As mentioned above a number of preferred embodiments now shall be discussed in an exemplary manner, which shall not in any sense be regarded as limiting for the actual scope of the invention.

Example 3: Sum and difference frequency detection of response to two superimposed sinuoidal input voltages

Similarly to the treatment in the previous section, a simple analysis can be performed for the case where the excitation of the memory cell can be written as the sum of two sinusoidally varying voltages at two distinct frequencies ω_1 and ω_2. In this case, one has

(6) $V(t) = V_1 \cos(\omega_1 t) + V_2 \cos(\omega_2 t)$,

and the polarization responses become

(7) $P(\text{“0”}) = [P_0 - \frac{1}{2}\beta(V_1^2 + V_2^2)] + \alpha[V_1 \cos(\omega_1 t) + V_2 \cos(\omega_2 t)] + \frac{1}{2}\beta[V_1^2 \cos(2\omega_1 t + \pi) + V_2^2 \cos(2\omega_2 t + \pi) + 2V_1V_2(\cos((\omega_1+\omega_2)t+\pi) + \cos((\omega_1-\omega_2)t+\pi)]$,

and

(8) $P(\text{“1”}) = -[P_0 - \frac{1}{2}\beta(V_1^2 + V_2^2)] + \alpha[V_1 \cos(\omega_1 t) + V_2 \cos(\omega_2 t)] + \frac{1}{2}\beta[V_1^2 \cos(2\omega_1 t) + V_2^2 \cos(2\omega_2 t) + 2V_1V_2(\cos(\omega_1+\omega_2)t + \cos(\omega_1-\omega_2)t)]$,

which can be seen to collapse to the expressions (4) and (5) by inserting $V_1 = V_2 = V_0/2$ and $\omega_1 = \omega_2 = \omega$.

In addition to the linear time dependent responses at ω_1 and ω_2 and the 2nd harmonic responses at $2\omega_1$ and $2\omega_2$ there are now response components at the sum and difference frequencies $(\omega_1 + \omega_2)$ and $(\omega_1 - \omega_2)$, as shown in fig. 6. The latter are in anti-phase to each other, in analogy with the case discussed in the previous paragraph, depending on whether the cell is in a logic “0” or “1” state. This provides an alternative non-destructive route to data read-out,

where it is possible to select the values of ω_1 and ω_2 in such a manner that the detection frequency at $(\omega_1 + \omega_2)$ or $(\omega_1 - \omega_2)$ is positioned in a convenient region, e.g. where noise spectral density is low and/or where the frequency is optimal for the sensing and processing circuitry. It is also possible to discriminate against harmonics of the excitation voltages that are injected into the detection circuitry by mechanisms unrelated to the polarization response of interest here (e.g. non-linearities in the driving or detection circuitry).

An apparatus according to the invention for performing a sum and difference frequency detection of the response to sinusoidal input voltages at respectively frequencies ω_1 and ω_2 is shown in block diagram form in fig. 6. Herein a signal source generating read signals as frequency ω_1 and ω_2 respectively input these signals to a memory cell and the response from of the memory cell is input to a phase-sensitive detector which performs the detection at respectively the sum frequency $\omega_1 + \omega_2$ or the difference frequency $\omega_1 - \omega_2$. A reference source is connected with a signal source for receiving the appropriate phase relationships and outputs reference sum and difference frequencies to the phase-sensitive detector, the output of which is connected to a discriminator/logic circuit for performing the necessary phase comparison in order to determine the actual logic state of the memory cell. Optionally a $\omega+\pi$ phase shifter is connected between the reference source and the phase-sensitive detector for delivering the reference shifted by π to the phase-sensitive detector and optionally to the discriminator/logic circuit.

Since the logic state of the cell manifests itself in the phase responses at several different frequencies simultaneously (i.e. $2\omega_1$, $2\omega_2$, $\omega_1 + \omega_2$ and $\omega_1 . \omega_2$), the phase detection results can be correlated at two or more frequencies to enhance the confidence and/or speed in each readout operation.

Example 4: Non-linear response detection where input voltages have a slow-periodic or low-frequency offset

A nearly universal attribute of non-linear responses in matter is the strong dependence on the amplitude of the excitation. As was mentioned in the above, it must in the present case be selected an excitation which is sufficiently strong to permit rapid and reliable detection of the non-linear

response, while at the same time being so weak that the polarization in the memory material is not reduced or reversed.

Another strategy for increasing the detection signals is to move the operating point to a region on the hysteresis curve where the latter exhibits a strong non-linear relationship between the polarization response and the applied voltage. This can be illustrated by referring to figs. 3a and 7a.

Assume, e.g. that the cell is in a "1" logic state, and that a small sinusoidally varying field at frequency ω is applied to probe the 2nd harmonic response. Now, however, there is a slow-periodic or low-frequency offset voltage which may be selected to position the working point on the hysteresis curve, viz.

(9) $V(t) = V_{OFFSET} + V_0 \cos(\omega t)$

Assuming for simplicity that the 2nd harmonic is directly proportional to the upwards or downwards curvature of the hysteresis curve at the working point, one can see by inspection of fig. 3a that for a cell in the "1" logic state, the 2nd harmonic signal shall increase in strength as V_{OFFSET} increases from zero and approaches V_C (in practice, the maximum voltage permissible in a passive matrix addressed memory shall be $V_C/3$, to avoid disturbing the other memory cells in the matrix), and for a cell in the "0" logic state, the 2nd harmonic signal is in anti-phase to the "1" signal and remains small as V_{OFFSET} increases from zero and upwards.

Conversely, if V_{OFFSET} is negative, the result is the mirror image of that above: As the offset voltage is given increasing negative values, the 2nd harmonic signal remains small if the cell is in the "1" logic state, and increases if the cell is in the "0" logic state.

Thus, in addition to a possible enhancement of the 2nd harmonic signal strength, the application of an offset voltage introduces additional phenomena which can be exploited to reveal the logic state of the cell, as shown in fig. 7a. In a "1" state the 2nd harmonic signal amplitude increases in response to an offset voltage of positive polarity, while remaining small at negative polarity offset voltages. In a "0" state the signal increases in response to an offset voltage of negative polarity and remains small at positive polarity offset voltages. Amongst several excitation voltage protocols which can be used for data read-out based on this asymmetry, one

preferred embodiment involves a sequence of measurements with different slow-periodic or low-frequency offset voltages, exemplified by the simple case where two 2nd harmonic amplitude and phase measurements are made, one at + V_{OFFSET} and one at - V_{OFFSET}. If the cell is in a "1" state, this shall reveal itself as a large 2nd harmonic signal with in-phase correlation with a reference signal when the offset is + V_{OFFSET}, and a smaller 2nd harmonic signal with the same phase at - V_{OFFSET} offset. If the cell is in a "0" state, the 2nd harmonic signal shall be small and in anti-phase to the reference signal when the offset is + V_{OFFSET}, and large but still in anti-phase when the offset is - V_{OFFSET}.

For performing a non-linear response detection according to the invention with input voltages with either a slow-periodic or low-frequency offset signal a variant embodiment of the apparatus shown in fig. 5b may be used. This variant embodiment conforms to the schematic block diagram of fig. 7b. A signal generator outputs the periodic, e.g. a sinusoidal, read signal superimposed on biasing voltage in the form of a slow-periodic offset voltage or alternatively a low-frequency offset voltage. The memory cell outputs a response signal with a frequency component at 2ω which is input to a combined phase-sensitive detector and discriminator for determining the logic state of the memory cell. The combined phase-sensitive detector and discriminator is also connected with the signal generator for receiving a reference signal in the form of e.g. sinusoidal varying voltage at frequency ω superimposed on the offset voltage as shown.

Example 5: Frequency detection of response when using an offset voltage and sinuoidal voltage with widely different frequencies and voltage values

Another preferred embodiment exploiting the asymmetric offset dependence of the 2nd harmonic response involves the application of a continuously varying offset voltage, e.g. a sinusoidal offset voltage that oscillates at a frequency Ω which is much less than the frequency ω of the voltage that excites the 2nd harmonic, as shown in fig. 8. Then

$$(10) \quad V(t) = V_{OFFSET} \cos(\Omega t) + V_0 \cos(\omega t)$$

This is a special case of the two-frequency excitation described above, but now $\Omega << \omega$, and $V_{OFFSET} >> V_0$. Since the non-linear response coefficient β in (1) and (2) depends on the offset voltage, an implicit time dependence is obtained as

(11) $\beta \approx \beta(V_{OFFSET} \cos(\Omega t))$,

and the 2nd harmonic response is modulated at the frequency Ω, to first order. The dependence of β upon the offset voltage depends on the material in question, and the temporal behaviour of the polarization response at 2ω may be quite complex. However, a hysteresis curve of the general shape shown in Fig. 1 shall yield a 2nd harmonic response which is amplitude modulated with a maximum at a time t_p when the offset voltage reaches its peak value in the positive polarity direction, for a "1" logic state. For a "0" state, the maximum 2nd harmonic response occurs at peak negative polarity in the offset voltage, i.e. at time $t_p + \pi/\Omega$. Again, the 2nd harmonic signal phases are in antiphase in the two instances. From these manifestations, a person skilled in the electronic art shall be able to design electronic circuitry which can detect whether the cell in question is in a "1" or "0" logic state.

For detection of the response when using an offset voltage and a sinusoidal voltage as disclosed in the above example, a variant embodiment of the apparatus in fig. 7b can be used. This variant embodiment is shown in block diagram form in fig. 8b and comprises a signal generator outputting the sinusoidally varying voltage of frequency ω superimposed on a slowly varying sinusoidal offset voltage at a low frequency Ω as shown, to the memory cell which outputs a response signal component at the frequency 2ω to the phase-sensitive detector and discriminator for determining the logic state of the memory cell. The signal generator also outputs a phase reference at respectively 2ω for recording the antiphase of the second harmonic signal phases as well as the offset signal of frequency Ω for recording the magnitude in the response signal.

*

Since this concept for data read-out does not cause polarization reversal in the memory medium, it carries with it substantial advantages, as set out and high-lighted below.

- Being non-destructive, no refresh writing cycle needs to be implemented, conferring speed and simplicity to the memory device.
- In all presently known memory substances of relevance, fatigue is linked to the number of polarization reversals that the material has

been subjected to. Obviating the need for polarization switching during read-out of data implies a dramatic increase in lifetime for virtually all types of memory devices, since read operations are typically performed more often than write operations.

- In the case of sum frequency or harmonic detection, discrimination between a "0" and a "1" bit can be cast in terms of qualitative criteria such as determining the polarity of a voltage rather than analogue threshold detection of voltages on a grey scale. This may simplify the post-detection circuitry that makes decisions regarding logic state.
- Finally, the use of two biasing or offset voltages at appropriately selected frequencies, amplitudes and durations shall allow the use of detection schemes based on correlation methods, which dramatically enhances the determination of a memory cell logic state in a non-destructive readout involving small-signal responses only.

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CLAIMS

1. A method for determining a logic state of a memory cell in a data storage device, wherein said cell stores data in the form of an electrical polarization state in a capacitor containing a polarizable material, wherein said polarizable material is capable of maintaining a non-vanishing electrical polarization in the absence of an externally impressed voltage across said capacitor, and of generating a current response to an applied voltage, said current response including linear and non-linear components, and wherein said method includes the following steps:

applying a first time-dependent small-signal voltage over said capacitor, said small-signal voltage having an amplitude and/or duration less than that required for causing a significant permanent change in the polarization state of said capacitor,

applying a second time-dependent voltage over said capacitor, said second time-dependent voltage being added to said first time-dependent voltage, the sum of the first and second time-dependent voltages having an amplitude and/or duration less than that required for causing a significant permanent change in the polarization state of said capacitor,

recording at least one characteristic of a generated small-signal current response over said capacitor, said at least one characteristic having either a linear or non-linear relationship to said first and/or second applied time-dependent voltages,

performing a correlation analysis based on correlation reference signals derived from both said first and said second time-dependent voltages applied over said capacitor,

determining the logic state by establishing a numerical value for the result of said correlation analysis, and

assigning the determined logic state a logic value according to a predetermined protocol.

2. A method according to claim 1, wherein said correlation analysis is performed in two stages, the first stage of said correlation analysis including recording a temporal correlation between said small-signal voltage and said at least one recorded characteristic of a generated small-signal current response over said capacitor to establish the magnitude(s) of at least one parameter which

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characterizes said at least one recorded characteristic of a generated small-signal current response over said capacitor, and

the second stage of said correlation analysis including recording the correlation between said at least one parameter on the one hand and the magnitude, sign and/or phase of said second time-dependent voltage on the other hand.

3. A method according to claim 1, wherein said correlation analysis is performed in a single stage, where said at least one characteristic of a generated small-signal current response over said capacitor is correlated with a reference signal derived from both said first and second applied time-dependent voltages.

4. A method according to claim 1, wherein said second time-dependent voltage applied over said capacitor is a quasi-static voltage of either polarity.

5. A method according to claim 4, wherein said second time-dependent voltage applied over said capacitor is switched between a set of positive and/or negative values.

6. A method according to claim 1, wherein said second time-dependent voltage applied over said capacitor is a low frequency or slowly varying voltage.

7. A method according to claim 6, wherein said second time-dependent voltage applied over said capacitor is a sinusoidally varying voltage.

8. A method according to claim 1, wherein said first time-dependent small-signal voltage is selected as being periodic with a dominant Fourier component at frequency ω, the phase of the 2^{nd} harmonic component of said current response is recorded, and said first stage of said correlation analysis is performed with a reference phase derived from said first time-dependent small-signal voltage impressed on said capacitor.

9. A method according to claim 8, wherein said first time-dependent small-signal voltage is selected as being sinusoidal.

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10. A method according to claim 1, wherein said time-dependent voltages are selected as two periodically varying signals with dominant Fourier components at frequencies ω_1 and ω_2, respectively, the phases of the components of said current response are recorded at the sum and difference frequencies $\omega_1+ \omega_2$ and $\omega_1- \omega_2$, and said phases are compared with a reference phase derived from said time-dependent voltages impressed on said capacitor.

11. A method according to claim 10, wherein said periodically varying voltage components are selected as sinusoidal.

12. A method according to claim 10, wherein the phases of two or more of the non-linear current response components are recorded at $2\omega_1$ and/or $2\omega_2$ and/or $\omega_1+ \omega_2$ and/or $\omega_1 . \omega_2$, and said phases are compared, with a reference phase derived from said time dependent voltages impressed on said capacitor.

13. A method according to claim 10, wherein the phases of two or more of the non-linear current response components are recorded, at $2\omega_1$ and/or $2\omega_2$ and/or $\omega_1+ \omega_2$ and/or $\omega_1 - \omega_2$, and said phases are compared with a reference phase derived from a reference cell of known logic state that is subjected to the same impressed voltages.

14. A method according to claim 1, wherein recording said at least one characteristic of a generated small-signal response over said capacitor includes recording the ratio between the magnitude of said small-signal current response to said first time-dependent small-signal voltage on the one hand and the magnitude of said first time-dependent small-signal voltage on the other hand, said ratio corresponding to the slope of the hysteresis curve, at two or more values of said second time-dependent voltage.

15. A method according to claim 14, wherein said second time-dependent voltage is selected as a low-periodic or slowly varying offset voltage which is varied between a set of predetermined positive and/or negative values.

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16. A method according to claim 15, wherein said second time-dependent voltage is selected, varying periodically between a positive and a negative value.

17. A method according to claim 14, wherein said second time-dependent voltage is selected as a smoothly varying voltage sweeping a voltage range between two positive values or two negative values or a positive and a negative value.

18. A method according to claim 17, further including the step of sweeping said second time-dependent voltage periodically at a frequency lower than said first time dependent voltage.

19. A method according to claim 17, wherein said second time-dependent voltage is selected as varying sinusoidally with time.

20. A method according to claim 1, wherein said predetermined protocol assigns said logic state either of two logic values dependent on the established numerical value.

21. Apparatus for performing a phase comparison in the method according to claim 1, the apparatus including:
a signal generator for supplying two or more read signals with given phases to a memory cell connectable therewith, the memory cell in response to said read signals outputting a response signal having two or more non-linear current components; a phase sensitive detector connectable with the memory cell and adapted for performing a phase sensitive detection of at least two phases in the response signal output from the memory cell; a reference source connected with said signal generator and adapted for generating phase references from the sum and differences of the phases of the input read signals to the phase sensitive detector connected therewith for detecting and correlating said response components, and performing a phase comparison between the phase references and at least one detected and correlated response component; and a discriminator/logic circuit

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being connected with the phase sensitive detector for receiving the output thereof and adapted for determining a logic state of the memory cell.

22. Apparatus according to claim 21, further including an $\omega+\pi$ phase shifter being connected with the reference source for receiving the output thereof and delivering the $\omega+\pi$ phase shifted output to the phase sensitive detector and optionally also to the discriminator and logic circuit.

23. Apparatus for performing a phase comparison in the method according to claim 1, the apparatus including:
a signal generator for supplying a first periodic read signal superimposed on a second periodic read signal with lower frequency than the first read signal to a memory cell connectable therewith, said memory cell outputting a response signal at twice the frequency of the first read signal; and a phase-sensitive detector and discriminator connectable with said memory cell for receiving the response signal therefrom as well as phase reference signals respectively in the form of the first and second read signals from the signal generator, and correlating the phase of the response signal with the phase of either phase reference signal or both, said phase sensitive detector and discriminator determining a logic state of the memory cell by the magnitude and/or the phase of the phase-correlated response signal.

24. A method for determining a logic state of a memory cell substantially as hereinbefore described with reference to any one of the embodiments illustrated in Figures 4a to 4d, 5a, or 6 to 8b.

25. Apparatus for performing a phase comparison substantially as hereinbefore described with reference to any one of the embodiments illustrated in Figures 4a to 4d, 5a, or 6 to 8b.

DATED : 25 January, 2005
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Attorneys For:
THIN FILM ELECTRONICS ASA

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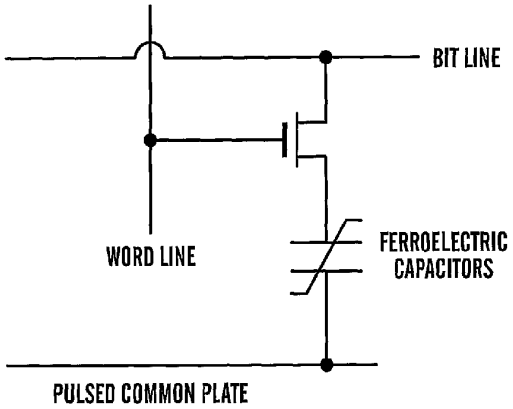


Fig. 1 (Prior Art)

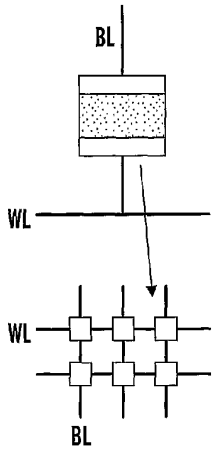


Fig.2

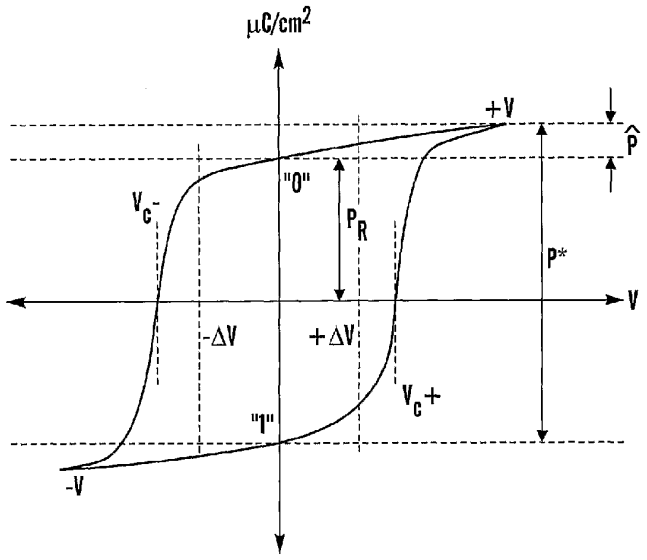

μC/cm2
+V
P̂
"0"
Vc-
PR
P*
V
-ΔV
+ΔV
Vc+
"1"
-V

Fig.3a

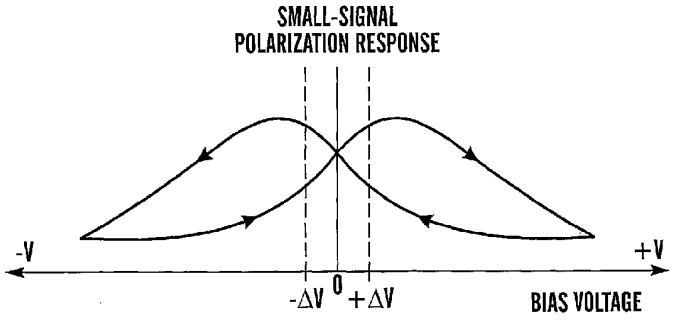
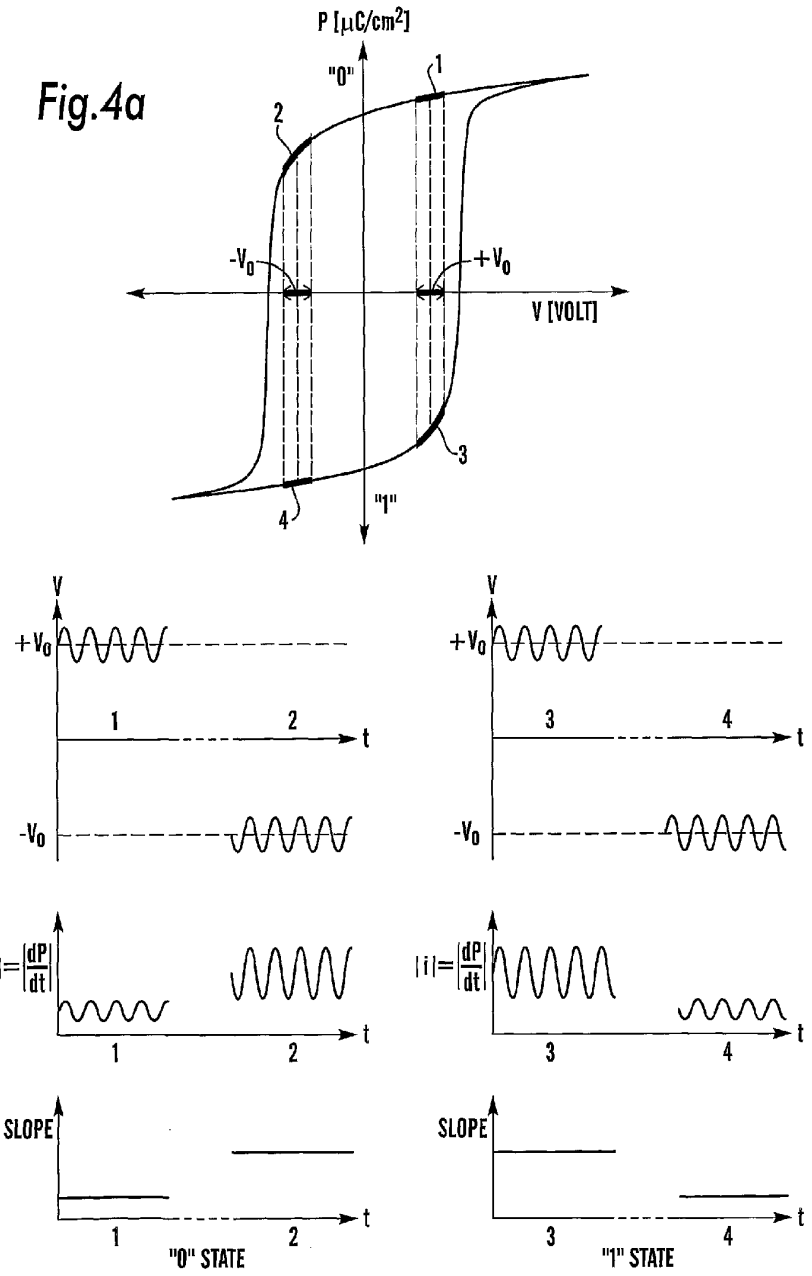

SMALL-SIGNAL
POLARIZATION RESPONSE
-V
+V
-ΔV
0
+ΔV
BIAS VOLTAGE

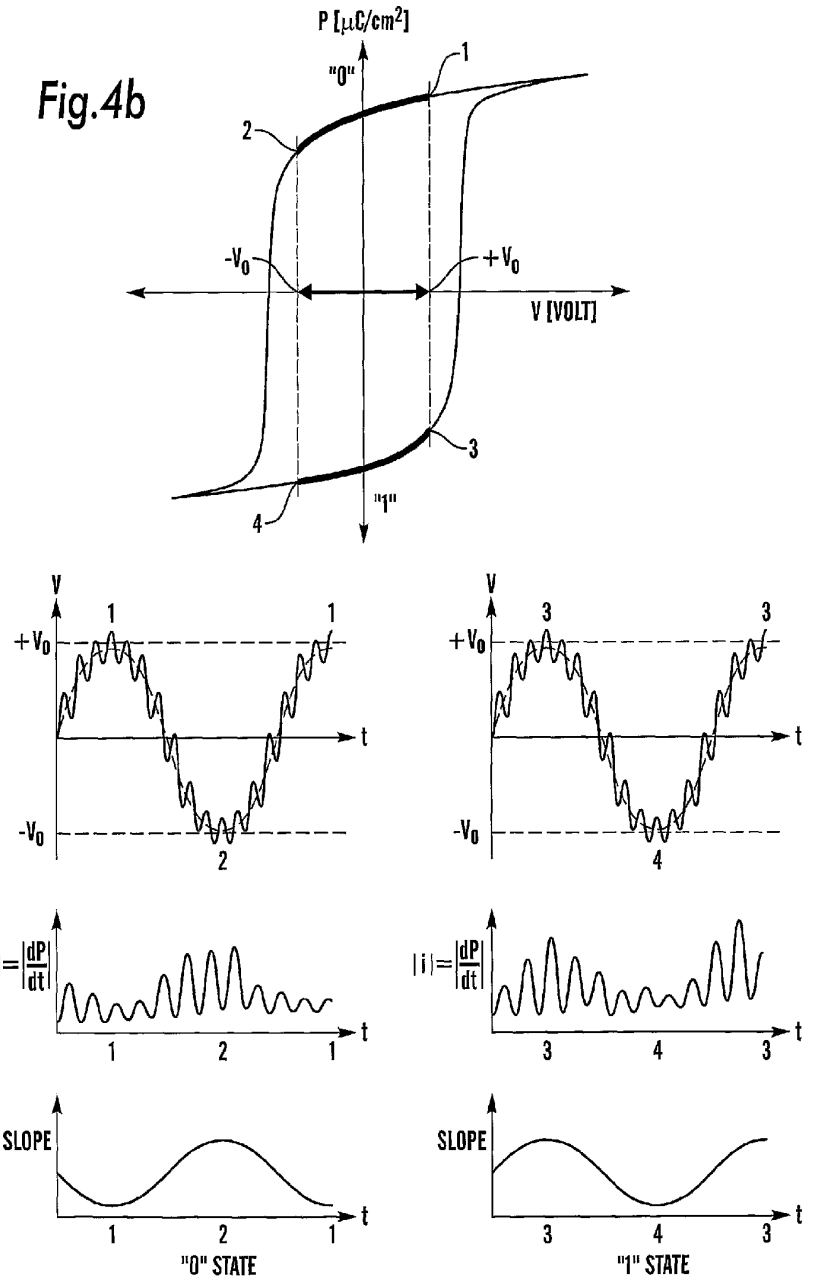
Fig.3b

Fig.4a



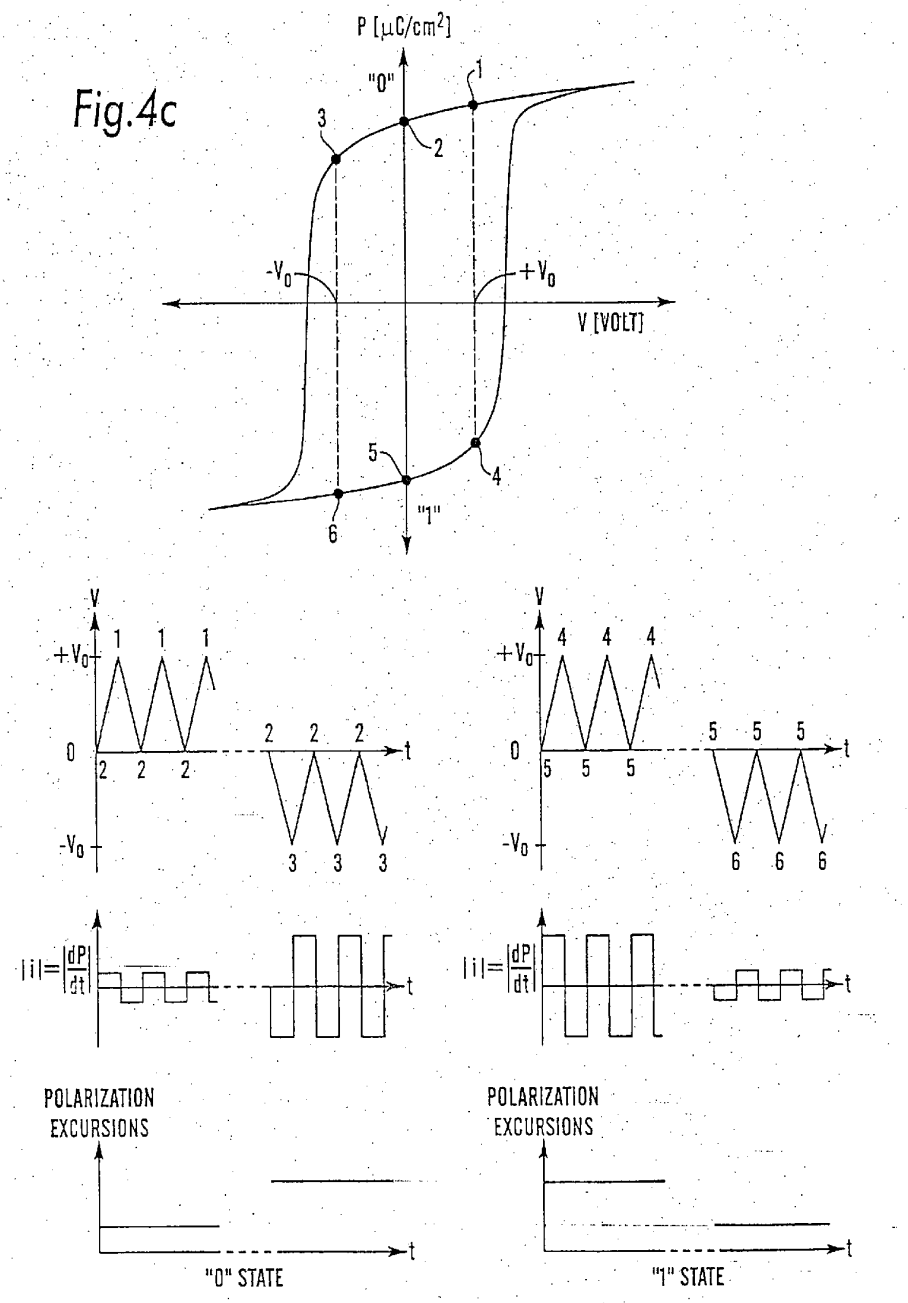
4/10

Fig.4b



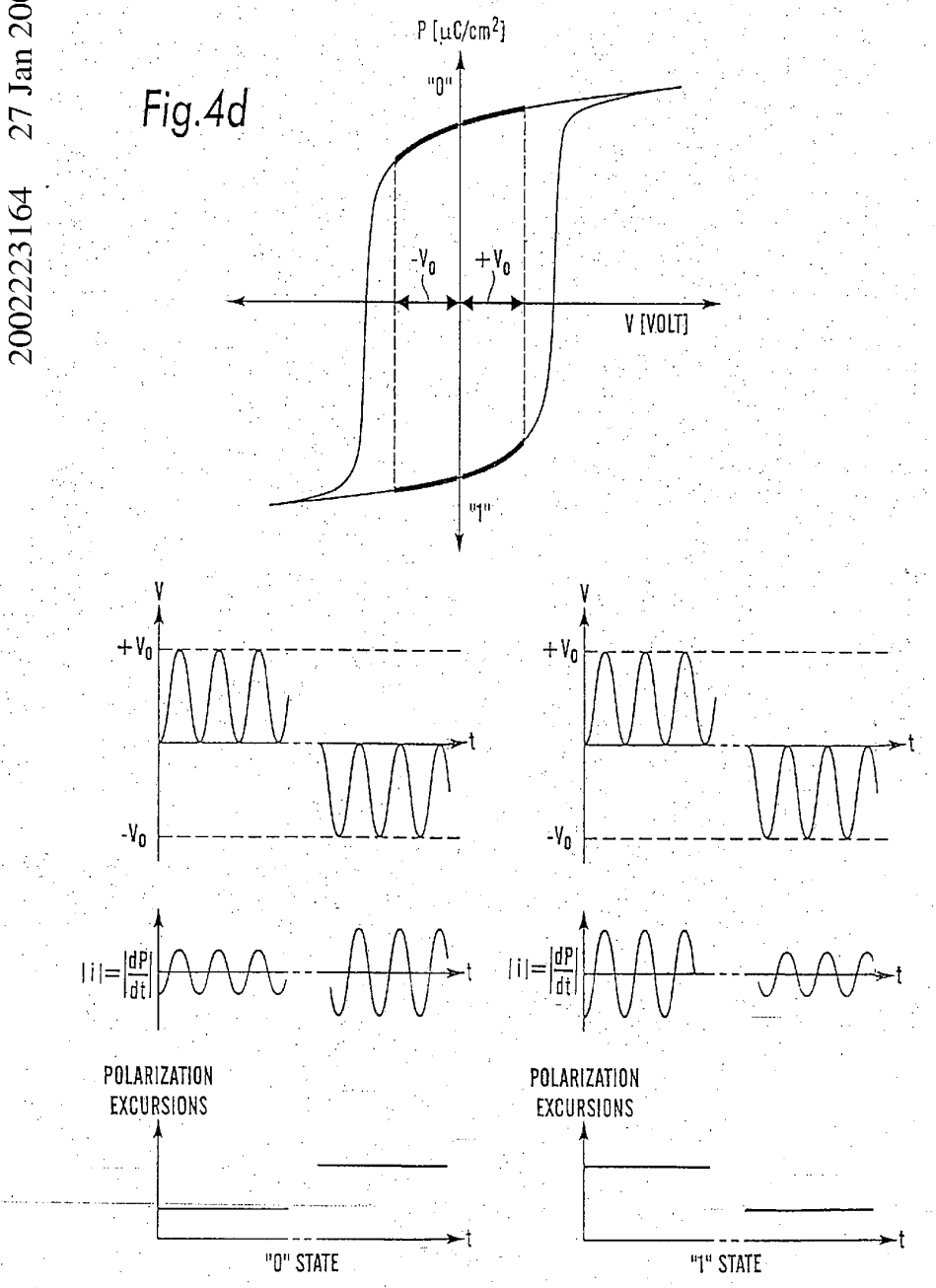
SUBSTITUTE SHEET (RULE 26)

Fig.4c


P [μC/cm²]
"0"
"1"
-V0
+V0
V [VOLT]
V
t
POLARIZATION EXCURSIONS
"0" STATE
"1" STATE

2002223164 27 Jan 2005

Fig.4d



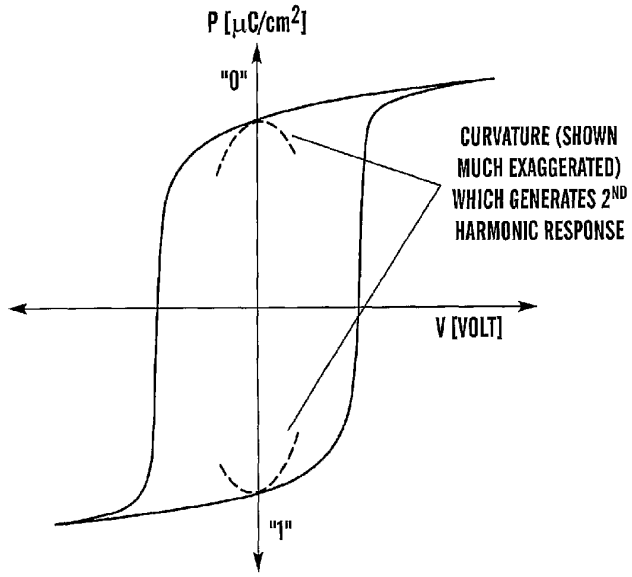

P [μC/cm2]
"0"
CURVATURE (SHOWN MUCH EXAGGERATED) WHICH GENERATES 2ND HARMONIC RESPONSE
V [VOLT]
"1"

Fig.5a

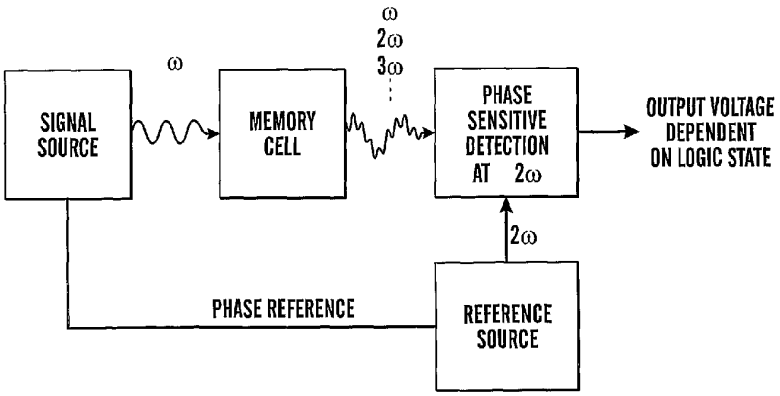

ω
2ω
3ω
ω
SIGNAL SOURCE
MEMORY CELL
PHASE SENSITIVE DETECTION AT 2ω
OUTPUT VOLTAGE DEPENDENT ON LOGIC STATE
2ω
PHASE REFERENCE
REFERENCE SOURCE

Fig.5b

8/10

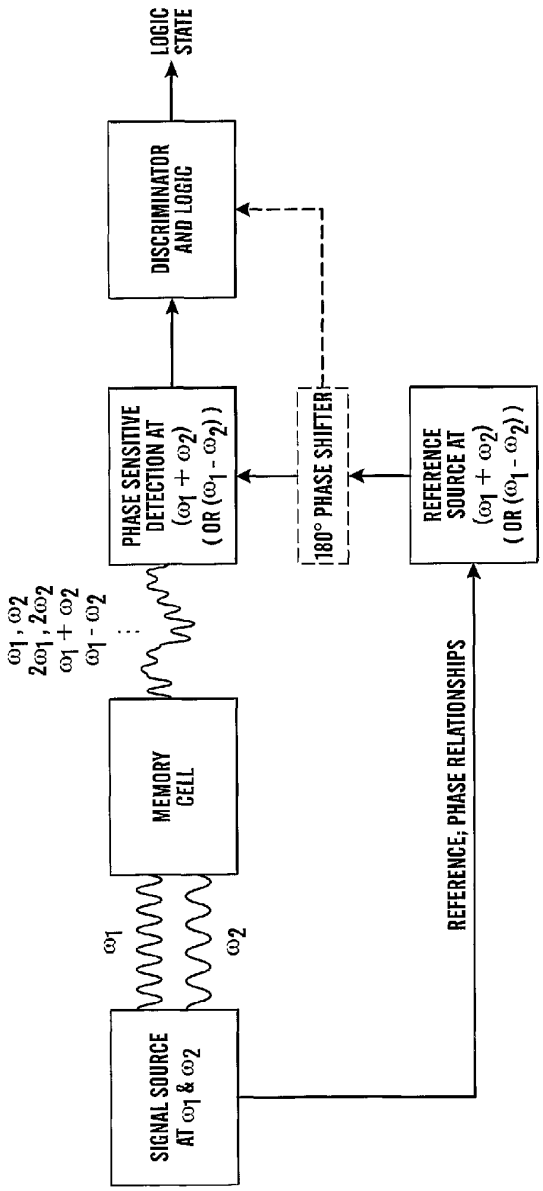


Fig.6

SUBSTITUTE SHEET (RULE 26)

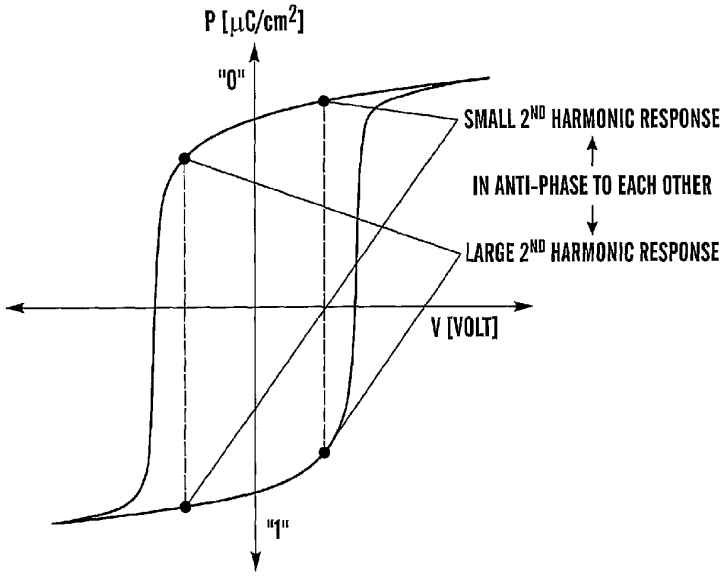

P [μC/cm²]
"0"
SMALL 2ND HARMONIC RESPONSE
IN ANTI-PHASE TO EACH OTHER
LARGE 2ND HARMONIC RESPONSE
V [VOLT]
"1"

Fig.7a

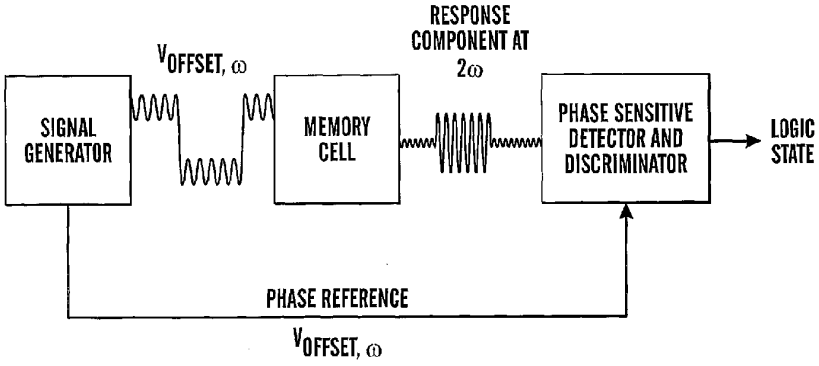

RESPONSE COMPONENT AT 2ω
VOFFSET, ω
SIGNAL GENERATOR
MEMORY CELL
PHASE SENSITIVE DETECTOR AND DISCRIMINATOR
LOGIC STATE
PHASE REFERENCE
VOFFSET, ω

Fig.7b

10/10

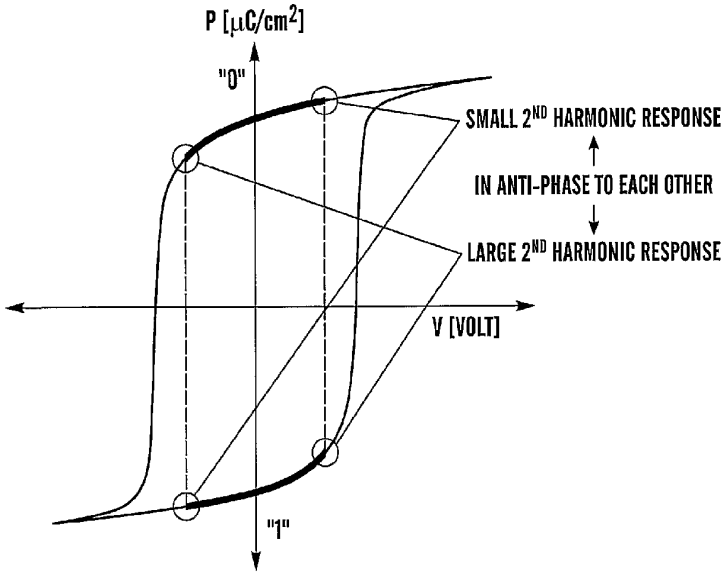


Fig.8a

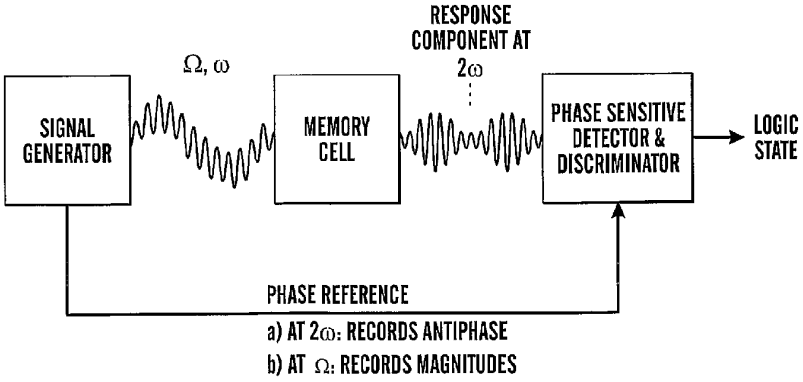


Fig.8b