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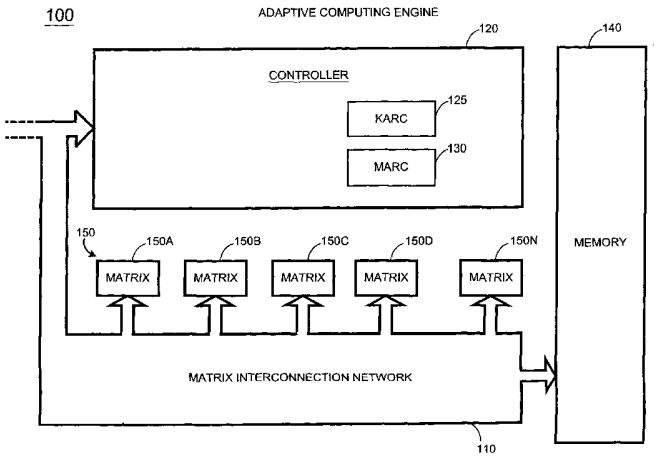
(54) Title: METHOD AND SYSTEM FOR DIGITAL SIGNAL PROCESSING IN AN ADAPTIVE COMPUTING ENGINE



(57) Abstract: Aspects of a method and system for digital signal processing within an adaptive computing engine are described. These aspects include a mini-matrix, the mini-matrix comprising a set of composite blocks, each composite block capable of executing a predetermined set of instructions. A sequencer is included for controlling the set of composite blocks and directing instructions among the set of composite blocks based on a data-flow graph. Further, a data network is included and transmits data to and from the set of composite blocks and to the sequencer, while a status network routes status word data resulting from instruction execution in the set of composite blocks. With the present invention, an effective combination of hardware resources is provided in a manner that provides multi/bit digital signal processing capabilities for an embedded system environment, particularly in an implementation of an adaptive computing engine. These and other advantages will become readily apparent from the following detailed description and accompanying drawings.

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F15/78 G06F15/80

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	KNEIP J ET AL: "AN ALGORITHM ADAPTED AUTONOMOUS CONTROLLING CONCEPT FOR A PARALLEL SINGLE-CHIP DIGITAL SIGNAL PROCESSOR" JOURNAL OF VLSI SIGNAL PROCESSING SYSTEMS FOR SIGNAL, IMAGE, AND VIDEO TECHNOLOGY, KLUWER ACADEMIC PUBLISHERS, DORDRECHT, NL, vol. 16, no. 1, 1 May 1997 (1997-05-01), pages 31-40, XP000655946 ISSN: 0922-5773 figure 4 page 36, left-hand column page 37-38, paragraph 4.3 --- -/--	1-24

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Bosch Vivancos, P

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	CHEN D C ET AL: "A RECONFIGURABLE MULTIPROCESSOR IC FOR RAPID PROTOTYPING OF REAL-TIME DATA PATHS" IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE, IEEE INC. NEW YORK, US, vol. 35, 1 February 1992 (1992-02-01), pages 74-75,249, XP000315770 ISSN: 0193-6530 the whole document	1-24
A	US 4 393 468 A (NEW BERNARD J) 12 July 1983 (1983-07-12) figure 2 figure 3 column 8, line 46 - line 51	1-24

INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4393468 A	12-07-1983	DE 3279776 D1	27-07-1989
		EP 0075593 A1	06-04-1983
		JP 2030538 B	06-07-1990
		JP 58500424 T	17-03-1983
		WO 8203481 A1	14-10-1982