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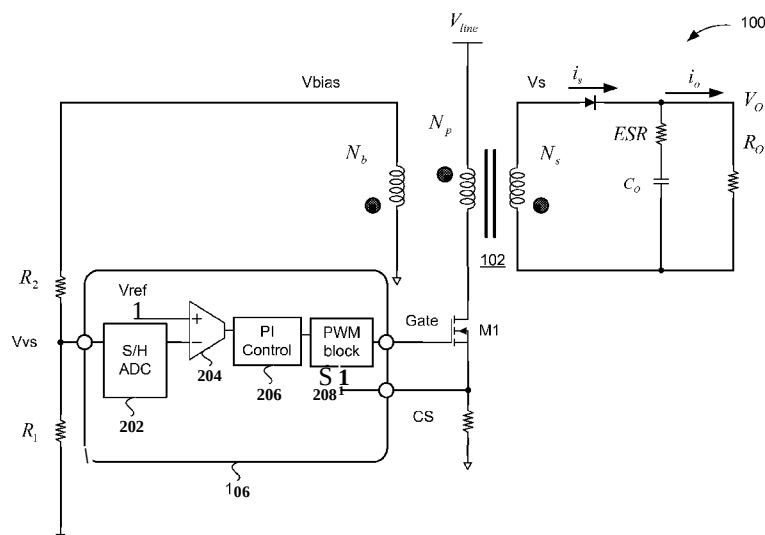


Fig. 2

(57) Abstract: In one embodiment, an apparatus includes a sampling component. The sampling component receives a first voltage signal on a primary side of a transformer and monitors the first voltage signal to determine a voltage sampling time. The determined voltage sampling time is when the first voltage signal is used to estimate a second voltage level on a secondary side of the transformer. The first component further samples the first voltage signal at the voltage sampling time to determine a first voltage level. A second component outputs a control signal to control a switch to regulate the second voltage level based on the first voltage level.

Primary Side Voltage Control in Flyback Converter

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present disclosure claims priority to U.S. Provisional App. No. 61/360,369 for "Single Stage Flyback Primary Side Voltage Control" filed June 30, 2010, which is
5 incorporated herein by reference in its entirety for all purposes.

BACKGROUND

[0002] Particular embodiments generally relate to voltage estimation.

[0003] Unless otherwise indicated herein, the approaches described in this section are not prior art to the claims in this application and are not admitted to be prior art by inclusion in
10 this section.

[0004] The use of electronic devices is popular in stationary and mobile environments. One kind of visual display is typically used in both environments. For example, the same kind of visual display is used in electronic devices from large sign/advertising boards to cellular phones or portable game players. Energy consumption is a concern in the design of
15 the electronic devices. For example, in the marketplace, an electronic device that uses less energy may take significant precedence over other devices.

[0005] Light-emitting diodes (LEDs) are being used in displays because of the LEDs' energy efficiency, reliability, low maintenance, and environmental friendliness. LEDs have been used in various devices, such as signal devices (e.g. traffic lights, exit signs, and
20 signboards) as well as in some illumination devices, such as flashlights. Additionally, LEDs may be used in light sources for general illumination in homes to commercial applications. LEDs have many advantages, such as long life, energy savings, better quality light output, safety, size, and durability.

[0006] A single-stage flyback solution is used because of the flyback solution's simplicity
25 and cost reduction. The flyback solution requires that an output voltage be detected on the secondary side of a transformer of the flyback solution. This increases the amount of components in the implementation, such as output components, secondary constant current control circuits, and an optocoupler are needed on the secondary side. These components are used to detect the output voltage on the secondary side and then send the output voltage back
30 to the primary side. The detected output voltage is used by the primary side to adjust an on and off time of a switch in the flyback solution to regulate the output voltage.

SUMMARY

[0007] In one embodiment, an apparatus includes a sampling component. The sampling component receives a first voltage signal on a primary side of a transformer and monitors the first voltage signal to determine a voltage sampling time. The determined voltage sampling time is when the first voltage signal is used to estimate a second voltage level on a secondary side of the transformer. The first component further samples the first voltage signal at the voltage sampling time to determine a first voltage level. A second component outputs a control signal to control a switch to regulate the second voltage level based on the first voltage level.

[0008] In one embodiment, the sampling time is at a point when it is determined a current in the secondary side is zero.

[0009] In one embodiment, the first voltage level is used to estimate the second voltage level of a second voltage signal on the secondary side of the transformer at a time when the second voltage level equals an output voltage on the secondary side.

[0010] In one embodiment, the first component is configured to: detect a first time when the first voltage signal reaches a first level; detect a second time when the first voltage signal reaches a second level; and use the first time and the second time to determine the sampling time.

[0011] In one embodiment, a system includes a primary winding on the primary side of the transformer and a secondary winding on the secondary side of the transformer and a bias winding on the primary side of the transformer, wherein the first voltage signal is received from the bias winding.

[0012] In one embodiment, a method receives a first voltage signal on a primary side of a transformer and monitors the first voltage signal to determine a voltage sampling time. The determined voltage sampling time is when the first voltage signal is used to estimate a second voltage level on a secondary side of the transformer. The method also samples the first voltage signal at the voltage sampling time to determine a first voltage level and outputs a control signal to control a switch to regulate the second voltage level based on the first voltage level.

[0013] In one embodiment, determining the voltage sampling time includes: detecting a first time when the first voltage signal reaches a first level; detecting a second time when the first

voltage signal reaches a second level; and using the first time and the second time to determine the sampling time.

[0014] The following detailed description and accompanying drawings provide a more detailed understanding of the nature and advantages of the present invention.

5 BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Fig. 1 depicts an example circuit for estimating an output voltage according to one embodiment.

[0016] Fig. 2 depicts a more detailed example of the circuit according to one embodiment.

[0017] Fig. 3 depicts a graph showing the relationship between the primary current and the
10 secondary current according to one embodiment.

[0018] Fig. 4 depicts a graph showing a sampling time according to one embodiment.

[0019] Fig. 5 shows a graph showing waveforms used to detect the sampling time according to one embodiment.

[0020] Fig. 6 depicts a simplified flowchart of a method for determining the sampling time
15 according to one embodiment.

DETAILED DESCRIPTION

[0021] Described herein are techniques for a voltage estimation system. In the following description, for purposes of explanation, numerous examples and specific details are set forth in order to provide a thorough understanding of embodiments of the present invention.

20 Particular embodiments as defined by the claims may include some or all of the features in these examples alone or in combination with other features described below, and may further include modifications and equivalents of the features and concepts described herein.

[0022] Fig. 1 depicts an example circuit 100 for an output voltage according to one embodiment. Circuit 100 includes a transformer 102, a switch (SW) 104, an input voltage V_{in} , a diode (D), a capacitor (C_0), a load (R_o), and an input resistor (R_i). In one embodiment, circuit 100 may be a single-stage flyback solution; however, other circuits may be used. A primary current (I_p) is a current through a primary side of transformer 102. A secondary current (I_s) is a current through the secondary side of transformer 102.
25

[0023] When switch 104 is on, the primary side of transformer 102 is directly connected to input voltage V_{in} . The primary current equals a current I_{mosfet} through switch 104 when switch 104 is on. When switch 104 is on, this results in an increase of magnetic flux in a primary winding of transformer 102. The voltage across a secondary winding of transformer 102 is negative such that diode D is reverse-biased (e.g., blocked). At this time period, capacitor C_0 supplies energy to load R_o . In one embodiment, load R_o may be a LED/LED string that is being driven by circuit 100, but other loads may be used. When switch 104 is off, the energy stored in the primary winding of transformer 102 is transferred to the secondary winding. The energy is then transferred to capacitor C_0 and load R_o through diode D, which is forward biased.

[0024] Particular embodiments use a bias voltage measured on the primary side of transformer 102 and use the measured bias voltage to regulate an output voltage on the secondary side of transformer 102. The bias voltage is sampled at a time in which it is determined that the bias voltage is substantially proportional to the output voltage by the transformer winding turn ratio. The measured bias voltage is then used to adjust a control signal that is used to control switch 104. For example, the measured bias voltage is compared to a reference and the comparison is used to adjust a duty cycle of the control signal to a transistor. In one example, a control signal circuit 106 is used to measure the bias voltage, perform the comparison, and output the control signal that turns switch 104 on and off. The on and off time may be varied regulate the output voltage. In one embodiment, this may control the power provided to the LED/LED string. Using the bias voltage to estimate the output voltage reduces the complexity of circuitry on the secondary side.

[0025] Fig. 2 depicts a more detailed example of circuit 100 according to one embodiment. Transformer 102 includes a primary winding N_p and a secondary winding N_s . A turn-ratio of transformer 102 is $N = N_p/N_s$. A bias winding N_b is also provided to allow a bias voltage V_{bias} to be measured on a primary side of transformer 102. The bias voltage may also be measured on the primary winding. Bias voltage V_{bias} is the voltage at the bias winding and secondary voltage V_s is the voltage at the secondary winding. In one embodiment, the number of turns for the bias winding is equal to the number of turns for the secondary winding. In other embodiments, the number of turns for the bias winding may be different from the number of turns of a secondary winding, and the turn-ratio between the bias winding

and the secondary winding may be used to estimate the output voltage. For example, the following equation may be used to determine the relationship between V_{bias} and V_s :

$$N_b/N_s = V_{bias}/V_s$$

V_{bias} : The voltage on N_b

5 V_s : The voltage on N_s

[0026] The output voltage V_0 is defined by the equation $V_0 = V_s - (V_f + I_s \cdot ESR)$. V_f is the drop across diode **D** and ESR is the equivalent series resistance of capacitor C_0 . When the secondary current is not zero, the output voltage may not be exactly proportional to the bias voltage V_{bias} . When the secondary current is zero, the output voltage equals the secondary
10 voltage. The diode drop is zero and also there is no voltage across the ESR of capacitor C_0 .

[0027] In one embodiment, the bias voltage that is sampled, voltage V_{vs} , is through a resistor divider. As will be described below, the sampled voltage V_{vs} is sampled at a time in which the output voltage equals the secondary voltage. The sampled voltage is then used to regulate the output voltage. For discussion purposes, the bias voltage V_{bias} and voltage V_{vs}
15 may be used interchangeably. It will be understood that the bias voltage V_{bias} may be sampled through various resistor dividers as long as the resistance ratio is known. The relationship of the output voltage to the sampled voltage is defined by:

$$V_{vs} = (R_1 + R_2) / (R_1 \cdot V_{bias})$$

$$V_0 = V_{vs} \cdot \frac{R_1 + R_2}{R_2} \cdot \frac{N_s}{N_{bias}}$$

20 [0028] The time to sample the bias voltage may be based on the current on the secondary side. Fig. 3 depicts a graph 300 showing the relationship between the primary current and the secondary current according to one embodiment. The control signal (PWM) shows the turn on time and turn off time of switch 104. In one example, switch 104 may be implemented using MOSFET M1 that is turned on and off to close switch 104 and open switch 104.

25 [0029] An on time T_{ON} is the switch on time. A constant on time T_{ON} is applied for a half line cycle. The off time T_{OFF} is defined by the duration of turning switch 104 off to allow the secondary current I_s to reach zero. A peak current $I_{peak,P}$ of the primary side and the peak current of the secondary side, $I_{peak,P}$, may be related based on a turn ratio N of transformer 102.

[0030] The bias voltage should be sampled when the secondary current goes to zero. Secondary current goes to zero when the energy in the secondary winding is fully discharged into capacitor C_0 and load R_o . The current slope is determined by the inductance value of transformer 102. The peak current on the primary side may be equal to

$$I_{\text{peak, p}} = V_{\text{line}} * T_{\text{on}} / L_m,$$

where:

V_{line} is the input line voltage and $V_{\text{line}} = V_{\text{rms}} * \sqrt{2} \sin(\theta)$

T_{on} : MOSFET On-time

L_m : Magnetizing Inductance

10

The secondary current may be related to the primary current by the turn-ratio $N = N_p / N_s$. The following equations provide the secondary current:

$$N = N_p / N_s$$

$$I_s = N * I_p$$

$$15 \quad I_s = N * V_o * T_{\text{off}} / L_m$$

[0031] When the secondary current goes to zero, the bias voltage should be sampled. Fig. 4 depicts a graph 400 showing a sampling time according to one embodiment. At 402, the on-time and off-time of switch 104 is shown. For example, the on-time is when a MOSFET M1 is on and the off-time is when MOSFET M1 is off. A cycle may be defined by the on-time and off-time of MOSFET M1 and is shown as a time T_s . MOSFET M1 may turn on and turn off multiple times in a half line cycle of an input to the primary side of transformer 102.

[0032] At 404, primary current I_p is shown and, at 406, secondary current I_s is shown. The primary current and secondary current are the same as shown in Fig. 3. For example, the primary current increases during the on-time of MOSFET M1 and the secondary current decreases during the off-time of MOSFET M1. A sampling time at 408 is desired when a secondary current discharges and reaches zero. This time is shown as a time t_{dis} . The slope

of the secondary current may be defined as $-\frac{N^2 \cdot V_o}{L_p}$. L_p is the magnetizing inductance of

the primary winding and N is the turn ratio.

[0033] It is desirable to sample the voltage V_{bias} at this point because V_{bias} may be substantially the same value as the output voltage V_o . For example, when MOSFET M1

turns off, energy is delivered to a secondary side through diode D. When diode D turns on and delivers energy to the secondary side, the waveform V_{bias} is flattened and is sometimes called "the knee". This portion is shown at 410. Before the secondary current is zero, the diode drop across diode D is reflected into the secondary voltage. If the bias voltage is detected when the diode drop is reflected into the secondary voltage, then the bias voltage may not be accurate. After fully discharging the secondary current into capacitor C_0 and load R_o , the voltage V_{bias} starts ringing based on the magnetizing inductance of the primary winding and a parasitic output capacitance of MOSFET M1. This may be referred to as the "magnetizing resonance frequency". When the voltage V_{bias} is sampled at the sampling point before the ringing starts, the secondary current is zero and the voltage of the diode drop is not reflected into voltage V_{bias} . For example, in this case, $V_s = V_0$. Thus, the bias voltage can be used as an accurate estimate of the output voltage.

[0034] V_{bias} may be sampled during any edge transition of an ADC_Sample waveform at 412. One of these transitions is selected as the sampling time. As will be discussed in more detail below, an analog-to-digital converter (ADC) samples voltage V_{bias} on the edge of the ADC_Sample waveform. If voltage V_{bias} is sampled at a time before the point shown at 408, an accurate reading for the output voltage may not be received. Thus, it is desirable to determine the sampling time be as close to point 408 as possible.

[0035] Referring back to Fig. 2, the process of using the sampled voltage at the sampling time will be described in more detail. The bias voltage is sampled at a point V_{vs} . The voltage V_{vs} that is input into control signal circuit 106 is defined by a resistor divider including the resistors R1 and R2. Voltage V_{vs} may be represented by the equation $V_{vs} = (R1 + R2)/(R1 * V_{bias})$.

[0036] Voltage V_{vs} is input into an ADC 202, which may be a sample and hold (S/H) ADC that samples voltage V_{vs} . Possible sampling points are based on sampling clock ADC_Sample. The sampling time is detected using logic in ADC 202 (described below) and the sampled value at the sampling time is selected and output to an amplifier 204. A reference V_{ref} is also input into amplifier 204. The reference V_{ref} may be an internal reference generated in the chip. The reference is used to determine how to regulate the output voltage. Depending on the values of voltage V_{vs} and the reference V_{ref} , amplifier 204 outputs an error value. A proportional integral (PI) control 206 calculates a duty cycle for a pulse width modulator (PWM) signal based on the error value. The duty cycle is input

into a pulse width modulator (PWM) block 208, which generates the PWM signal to input into a gate of MOSFET M1. The turn-off and turn-on time of MOSFET M1 may be adjusted to regulate the output voltage. For example, the duty cycle of a PWM signal input into the gate of MOSFET M1 may be adjusted to alter the turn-on time of MOSFET M1.

5 **[0037]** Altering the turn-on time has the effect of regulating the output voltage. For example, if voltage V_{vs} is lower than the reference V_{ref} , the error signal is negative. The duty cycle of the PWM signal may be increased to increase the turn-on time of MOSFET M1, which stores more energy in the primary winding of transformer 102. When transistor M1 is turned off, the energy transferred to the secondary side may increase. This increases the
10 secondary current, which increases the output voltage. The opposite is true when the turn-on time of transistor M1 is reduced. This process may be used to regulate the output voltage.

[0038] Different logic may be used to determine the sampling time. The logic may be found inside of ADC 202 and/or be external to ADC 202. In one embodiment, two comparators may be used to determine the sampling time, but other implementations may be
15 used. Fig. 5 shows a graph 500 showing waveforms used to detect the sampling time according to one embodiment. At 502, the waveform for voltage V_{vs} is shown. Voltage sampling point at 408 is shown before the ringing occurs.

[0039] At 504, a graph of an output for a first comparator is shown. The first comparator compares the voltage V_{vs} to a first reference value that is equal to one-half of the reference
20 voltage V_{ref} . The level of reference voltage V_{ref} and reference voltage $1/2V_{ref}$ is shown on the Y-axis of graph 502. The $1/2V_{ref}$ value may be $V_{ref} * \cosine(60^\circ) = 1/2V_{ref}$. This equation may be used because the resonance frequency is a cosine waveform.

[0040] At 506, a graph for the output for a second comparator is shown. The second comparator compares the voltage V_{vs} with ground (0V). The output of the first comparator
25 and the second comparator generate timing signals that are used to determine the voltage sampling time. The timing signals are determined based on a present cycle (i.e., a turn-on and turn-off time of MOSFET M1), and used to determine the voltage sampling time for the next cycle (the next turn-on and turn-off time for MOSFET M1). For example, the sampling time as a function of the time from the turn on time of MOSFET M1 is determined in a
30 present cycle. This time may be used from the turn on time of MOSFET M1 in a next cycle.

[0041] The first comparator measures a time T1 in which the resonance frequency goes below reference voltage $1/2V_{ref}$. In this case, the signal output by the first comparator goes low. The second comparator measures a time T2 when the resonance frequency goes below zero or passes the voltage 0V. In this case, the signal output by the second comparator goes high.

[0042] To determine the voltage sampling time, the following equations may be used:

$$\Delta T = T_2 - T_1.$$

$$\text{Voltage sampling time} = T_1 - 2 * \Delta T [V_{ref} * \cosine(60^\circ) = 1/2 V_{ref}]$$

[0043] Time ΔT is the difference between time T2 and time T1. The on-time prediction is the time in which it is predicted where the valley switching point is reached and MOSFET M1 turns on again. In this case, the valley switching point is known as the constant peak current provides the same turn-on and turn-off timing. The voltage sampling time for the next cycle can then be determined as $T_1 - 2 * \Delta T$. In this case, as of the symmetric shape of the resonance frequency, taking the difference between the half-way point and the 0V level and subtracting that from the time T1 yields the sampling point in which the secondary current goes to zero and the bias voltage starts ringing in the next cycle. The resonance frequency is symmetrically equivalent for a half line cycle. Thus, determining times T1 and T2 allows the prediction of the voltage sampling time for the next cycle of turning MOSFET M1 on and off in the half line cycle.

[0044] The sampling time may vary and may be calculated every cycle such that an accurate sampling time is used. In one embodiment, a variable input voltage is input to circuit 100. The variable input voltage affects the external capacitance Coss value of MOSFET M1. When the input voltage diminishes, the magnetizing inductance resonance frequency is also changed. Both of these factors may affect when the appropriate sampling time should be (due to a change in the slope of the secondary current). To guard against changes in the sampling time, the timing signals may be determined every cycle by the first comparator and second comparator to ensure the voltage sampling time is accurately determined within a threshold. By determining the sampling time every cycle, gradual changes to the sampling time are reflected due to variations in the input voltage. Slight changes between two consecutive cycles may occur, but these changes may be slight and be within an error tolerance. Although every cycle is used to detect the next sampling time, other methods may be used, such as once a half line cycle.

[0045] Fig. 6 depicts a simplified flowchart 600 of a method for determining the sampling time according to one embodiment. At 602, a first voltage signal is received on the primary side of transformer 102. For example, the bias voltage associated with a bias winding is determined.

5 [0046] At 604, the first voltage signal is monitored to determine a voltage sampling time. For example, the voltage levels for the first voltage signal may be monitored for a previous cycle in which MOSFET M1 was turned on and turned off. This monitoring is used to determine a voltage sampling time to sample the first voltage signal.

[0047] At 606, the first voltage signal is sampled at the voltage sampling time to determine
10 a first voltage level. The first voltage level is used to estimate the second voltage level of a second voltage signal on the secondary side of transformer 102. At 608, the sampled first voltage signal is compared to a reference voltage to determine an error.

[0048] At 610, the error is used to adjust the turn-on and turn-off time of MOSFET M1.
15 For example, a duty cycle of a PWM signal is adjusted to adjust the ON time of MOSFET M1.

[0049] Accordingly, particular embodiments use a voltage V_{bias} that is determined on the primary side to estimate the output voltage on the secondary side. This eliminates the need for secondary side components to detect the output voltage and send the output voltage back to the primary side for use in voltage regulation.

20 [0050] As used in the description herein and throughout the claims that follow, "a", "an", and "the" includes plural references unless the context clearly dictates otherwise. Also, as used in the description herein and throughout the claims that follow, the meaning of "in" includes "in" and "on" unless the context clearly dictates otherwise.

[0051] The above description illustrates various embodiments of the present invention
25 along with examples of how aspects of the present invention may be implemented. The above examples and embodiments should not be deemed to be the only embodiments, and are presented to illustrate the flexibility and advantages of the present invention as defined by the following claims. Based on the above disclosure and the following claims, other arrangements, embodiments, implementations and equivalents may be employed without
30 departing from the scope of the invention as defined by the claims.

WHAT IS CLAIMED IS:

1 1. An apparatus comprising:
2 a sampling component configured to:
3 receive a first voltage signal on a primary side of a transformer;
4 monitor the first voltage signal to determine a voltage sampling time,
5 wherein the determined voltage sampling time is when the first voltage signal is used
6 to estimate a second voltage level on a secondary side of the transformer; and
7 sample the first voltage signal at the voltage sampling time to
8 determine a first voltage level;
9 a second component configured to output a control signal to control a switch
10 to regulate the second voltage level based on the first voltage level.

1 2. The apparatus of claim 1, wherein the sampling time is at a point when
2 it is determined a current in the secondary side is zero.

1 3. The apparatus of claim 1, further comprising a third component
2 configured to:
3 compare the first voltage level to a reference voltage; and
4 output an error signal.

1 4. The apparatus of claim 3, further comprising a fourth component
2 configured to use the error signal to adjust an on time of the switch.

1 5. The apparatus of claim 4, wherein:
2 the control signal comprises a pulse width modulation (PWM) signal, and
3 a fourth component is configured to adjust a duty cycle of the pulse width
4 modulation (PWM) signal to adjust the on time of the switch.

1 6. The apparatus of claim 1, wherein the first voltage level is used to
2 estimate the second voltage level of a second voltage signal on the secondary side of the
3 transformer at a time when the second voltage level equals an output voltage on the
4 secondary side.

1 7. The apparatus of claim 1, wherein the first component is configured to:
2 detect a first time when the first voltage signal reaches a first level;

3 detect a second time when the first voltage signal reaches a second level; and
4 use the first time and the second time to determine the sampling time.

1 8. A system comprising the apparatus of claim 1, the system further
2 comprising:
3 a primary winding on the primary side of the transformer and a secondary
4 winding on the secondary side of the transformer; and
5 a bias winding on the primary side of the transformer, wherein the first voltage
6 signal is received from the bias winding.

1 9. The system of claim 8, wherein the bias winding has a same number of
2 turns as the secondary winding.

1 10. A method comprising:
2 receiving a first voltage signal on a primary side of a transformer;
3 monitoring the first voltage signal to determine a voltage sampling time,
4 wherein the determined voltage sampling time is when the first voltage signal is used to
5 estimate a second voltage level on a secondary side of the transformer;
6 sampling the first voltage signal at the voltage sampling time to determine a
7 first voltage level; and
8 outputting a control signal to control a switch to regulate the second voltage
9 level based on the first voltage level.

1 11. The method of claim 10, wherein the sampling time is at a point when
2 it is determined a current in the secondary side is zero.

1 12. The method of claim 10, wherein:
2 the sampling time is determined using monitored voltage levels during a first
3 cycle, and
4 the sampling is performed at the sampling time in a second cycle.

1 13. The method of claim 12, wherein:
2 the first cycle comprises a turn on time of the switch and a turn off time of a
3 switch, and
4 the second cycle comprises a next turn on time of the switch and a next turn
5 off time of the switch.

1 14. The method of claim 10, wherein determining the voltage sampling
2 time comprises:

3 detecting a first time when the first voltage signal reaches a first level;

4 detecting a second time when the first voltage signal reaches a second level;

5 and

6 using the first time and the second time to determine the sampling time.

1 15. The method of claim 10, wherein the first voltage level is used to
2 estimate the second voltage level of a second voltage signal on the secondary side of the
3 transformer at a time when the second voltage level equals an output voltage on the
4 secondary side.

1 16. The method of claim 10, further comprising:

2 comparing the first voltage level to a reference voltage; and

3 outputting an error signal.

1 17. The method of claim 16, further comprising using the error signal to
2 adjust an on time of the switch.

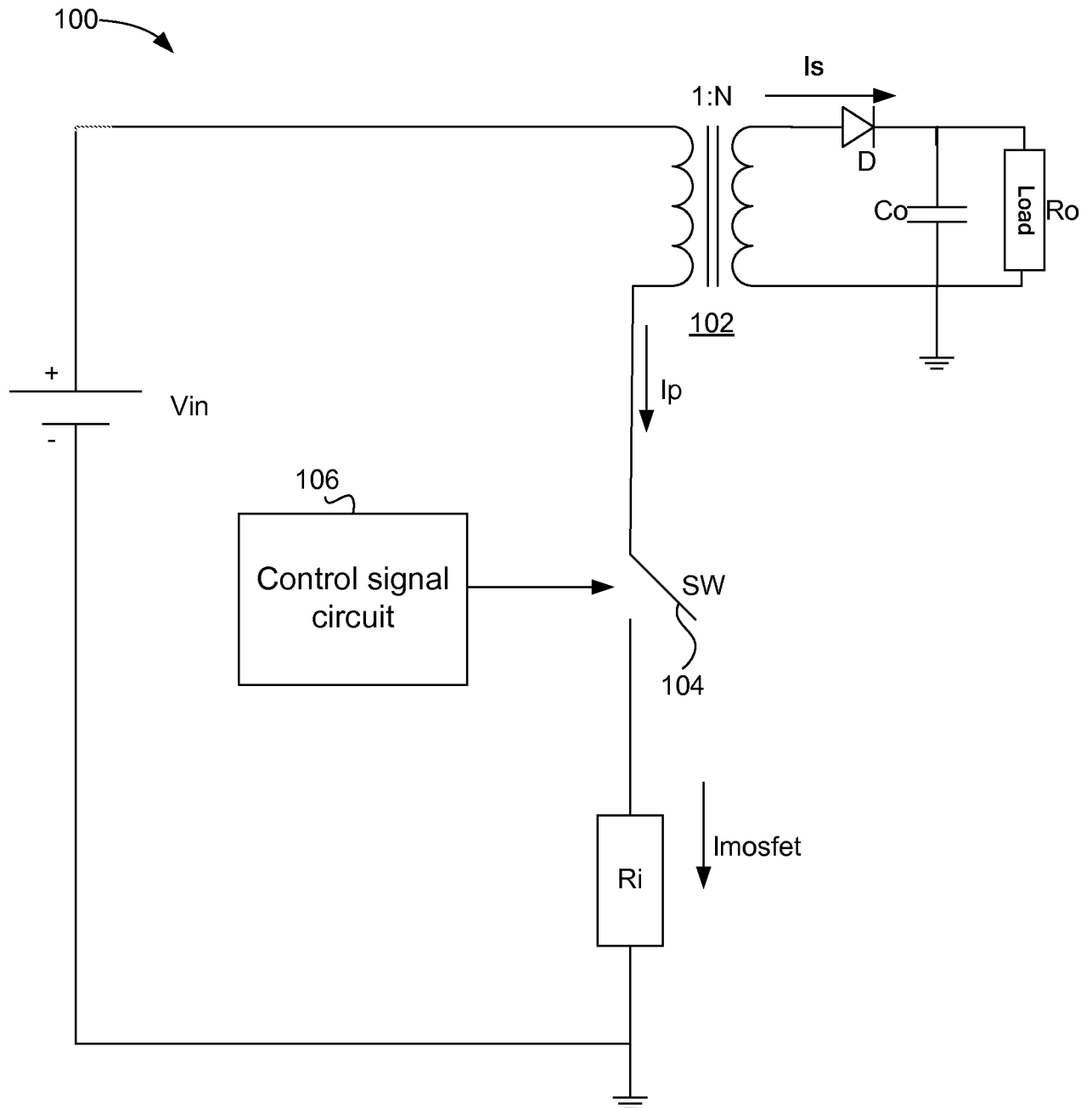
1 18. The method of claim 17, wherein the control signal comprises a pulse
2 width modulation (PWM) signal, the method further comprising:

3 adjusting a duty cycle of the pulse width modulation (PWM) signal to adjust
4 the on time of the switch.

1 19. The method of claim 10, wherein the first voltage signal is received
2 from a bias winding on the primary side of the transformer.

1 20. The method of claim 19, wherein the bias winding has a number of
2 turns equal to a number of turns of a secondary winding on the secondary side.

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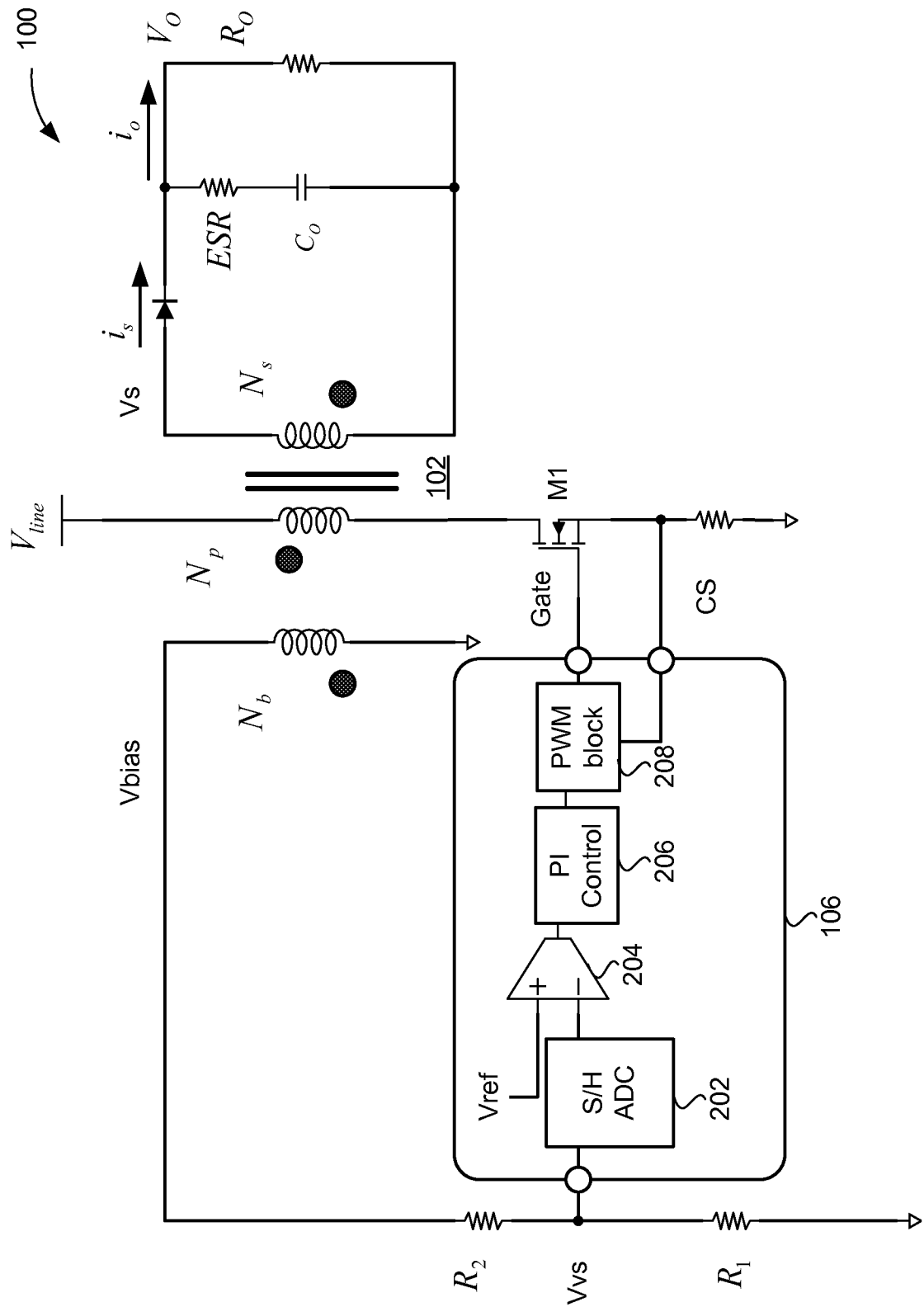


Fig. 2

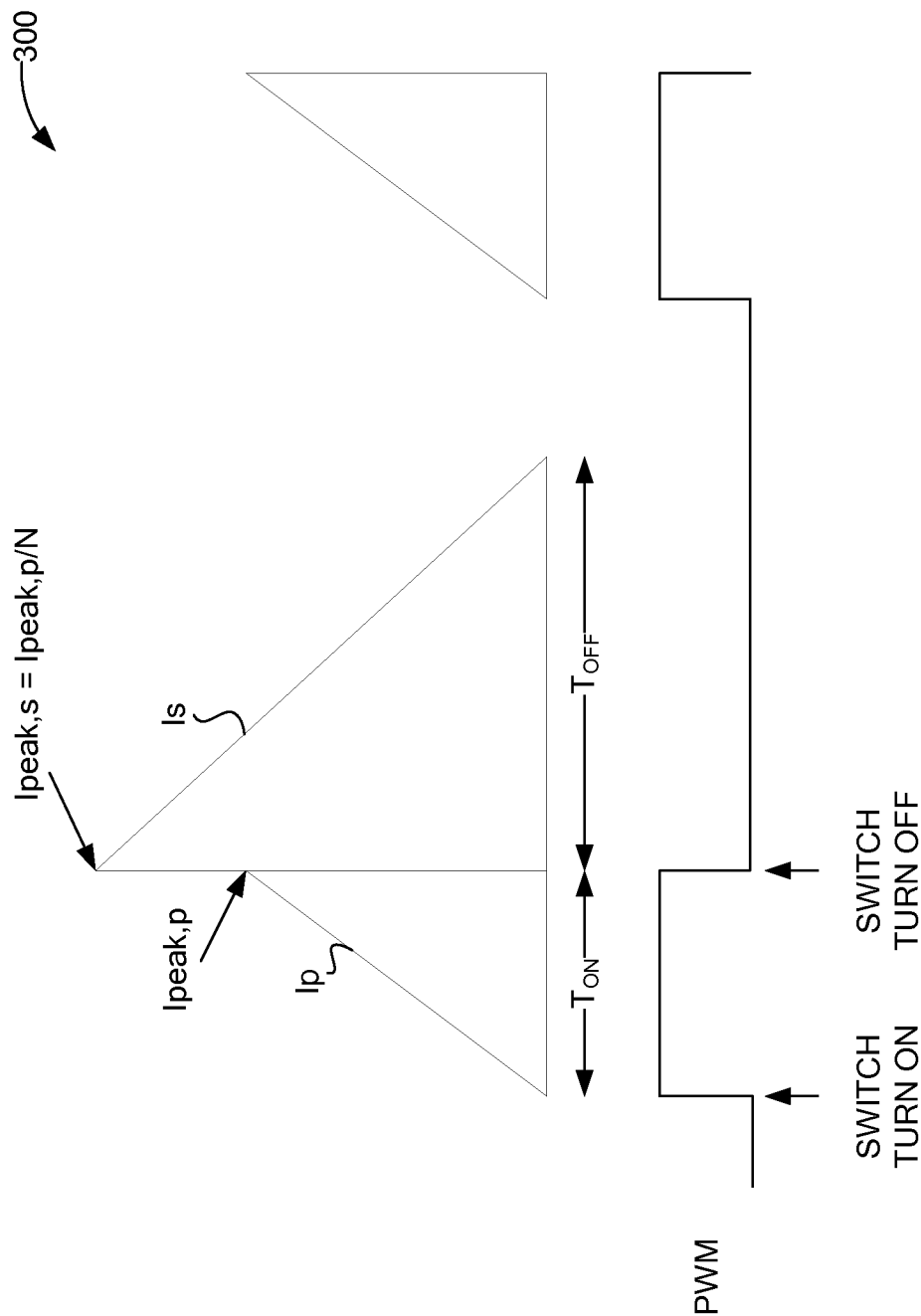


Fig. 3

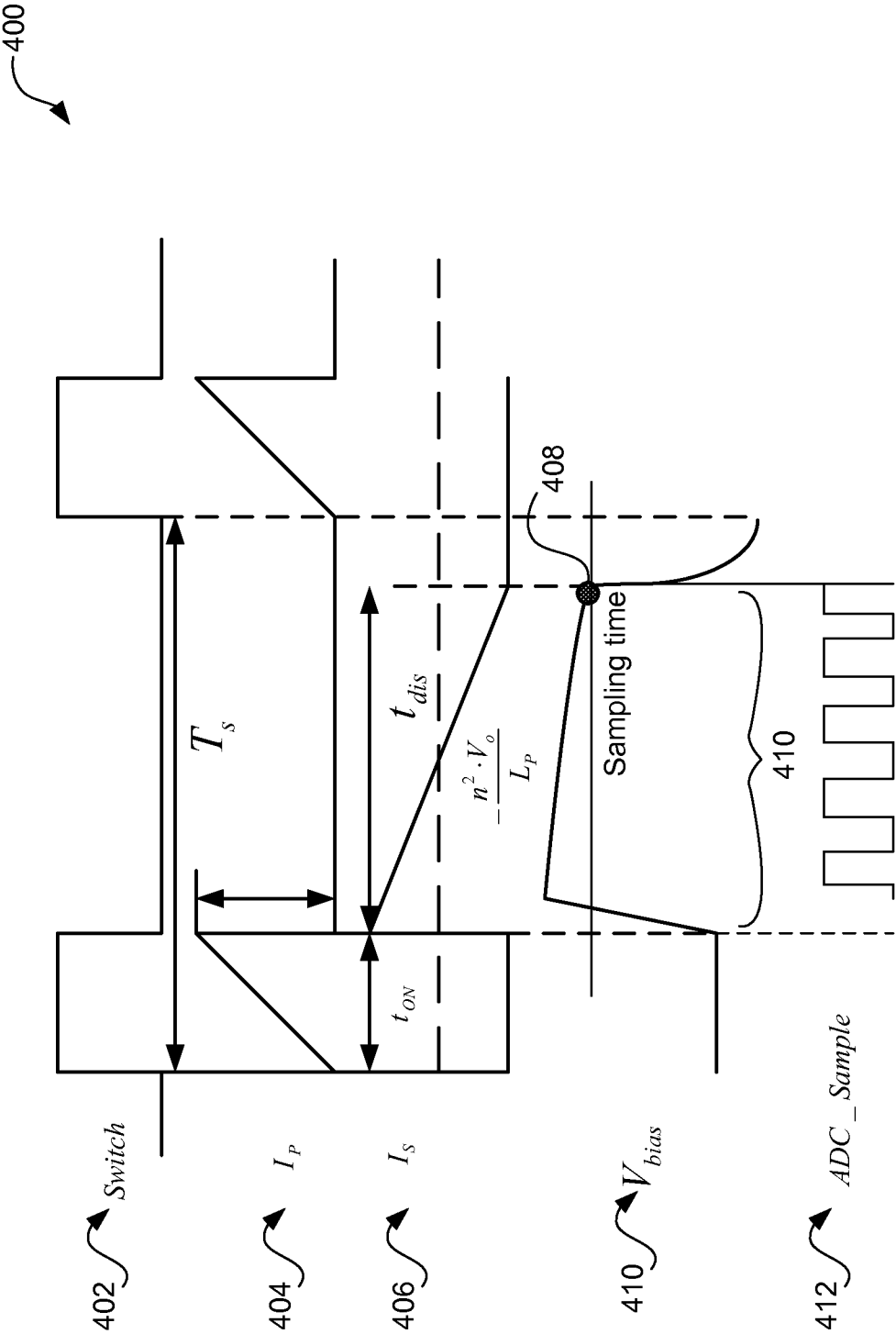


Fig. 4

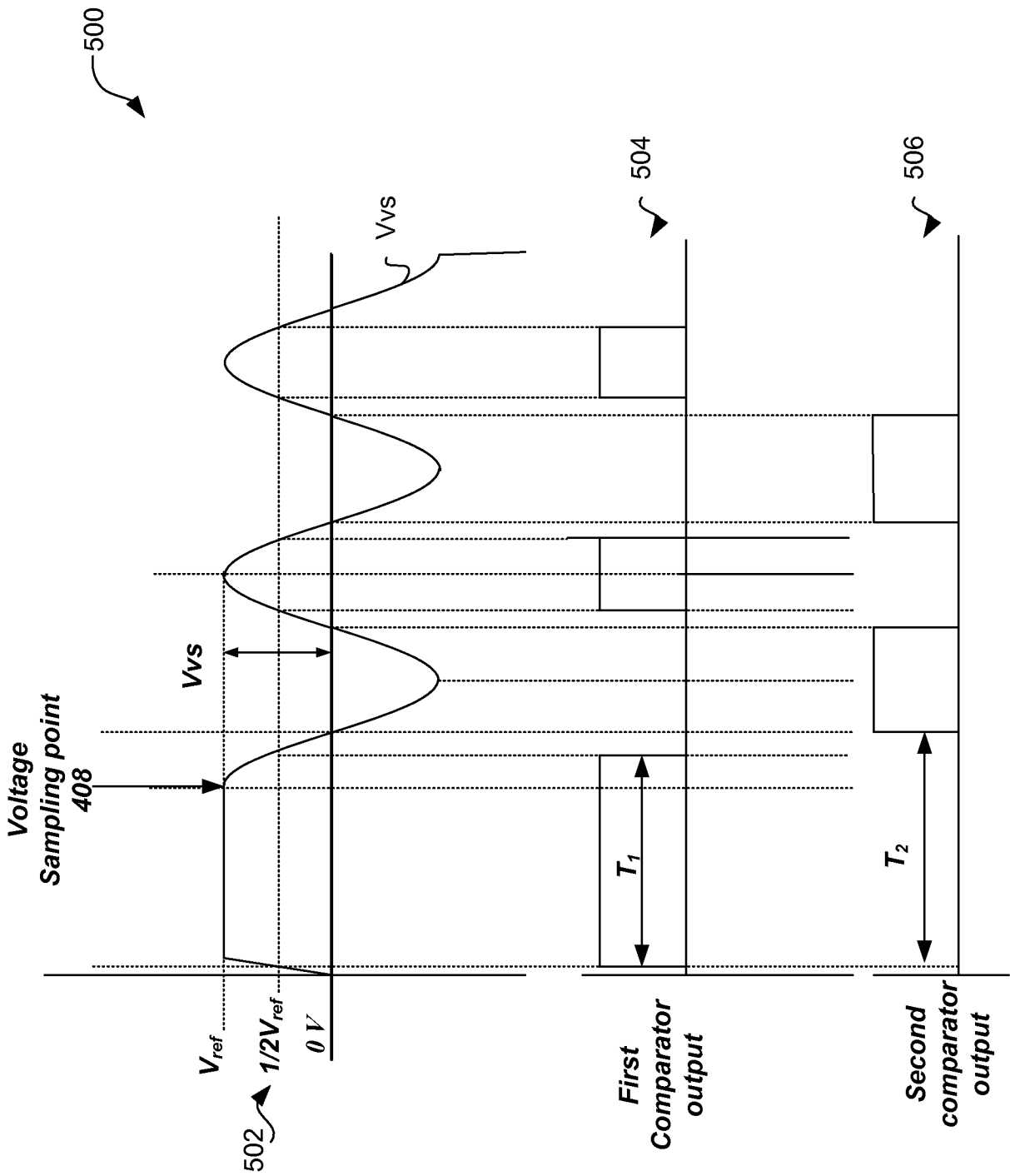


Fig. 5

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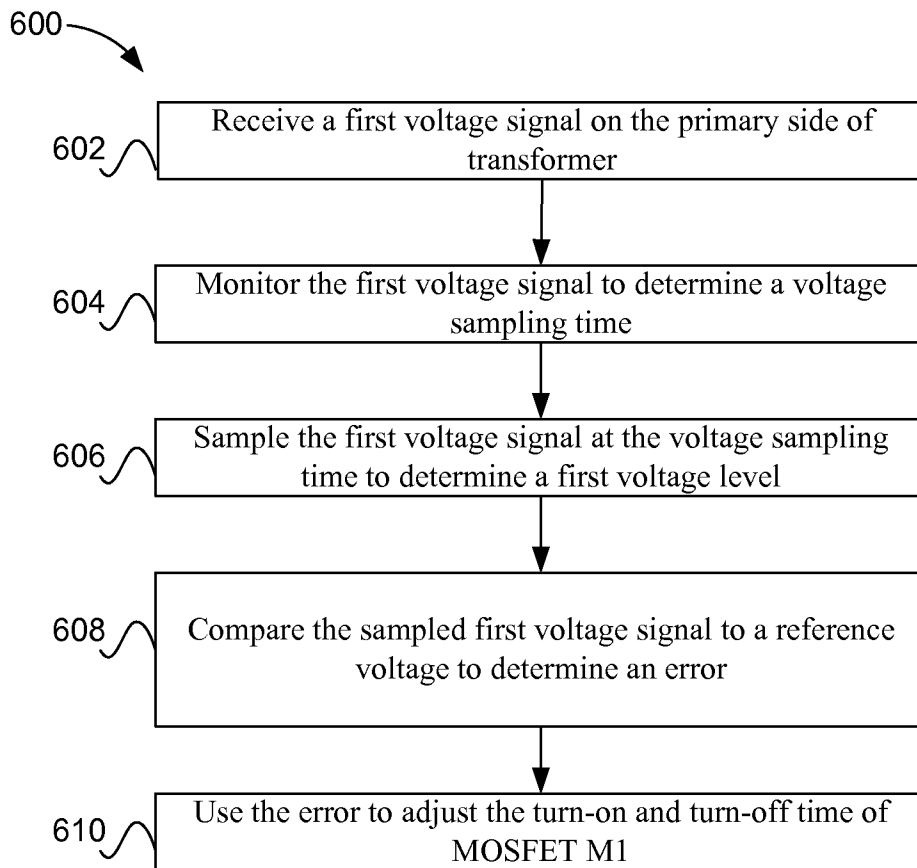


Fig. 6

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 11/40220

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H02M 3/335 (201 1.01)**USPC - 363/19**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 363/19Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 363/13,16,19,20,21.01,21 .03,21.07,21.09,21.12,21.18,21.18,21.21,41,97,131 (keyword limited - see terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PubWEST (PGPB, USPT, USOC, EPAB, JPAB); GOOGLE; Google Scholar

Search Terms: transformer, voltage, regulation, sampling, adjusting, error, timing, pulse width, PWM, duty cycle, primary, secondary, switching, winding, bias, turns, estimate, flyback, monitor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	* Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2005/0024898 A1 (Yang et al.) 03 February 2005 (03.02.2005), entire document, especially; abstract, para. [0017]-[0020], [0036], [0059], [0067], [0072]	1 - 20
Y	US 2010/0157630 A1 (Polivka et al.) 24 June 2010 (24.06.2010), entire document, especially; abstract, para. [0032]-[0034]	1 - 20
A	US 2005/0270000 A1 (Chang et al.) 08 December 2005 (08.12.2005), entire document	1 - 20

☐ Further documents are listed in the continuation of Box C.
 ☐

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"I" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

16 September 2011 (16.09.2011)

Date of mailing of the international search report

03 OCT 2011

Name and mailing address of the ISA/US

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