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METHOD FOR FABRICATING SELF-ASSEMBLING MICROSTRUCTURES

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(57) Claim

1. A method of assembling a microstructure on a substrate, said substrate comprising a top surface with at least one recessed region thereon, comprising the steps of:

providing a plurality of shaped blocks, said shaped block comprising an integrated circuit device thereon;

transferring said shaped blocks into a fluid to form a slurry; and

dispensing said slurry over said substrate at a rate where at least one of said shaped blocks is disposed into a recessed region.

19. A method of fabricating shaped blocks comprising an integrated circuit device, comprising:

providing a substrate including a release layer overlying the substrate, and a block layer overlying the release layer;

patterning said block layer to form a plurality of shaped blocks;

preferential etching said release layer to release said plurality of shaped blocks.

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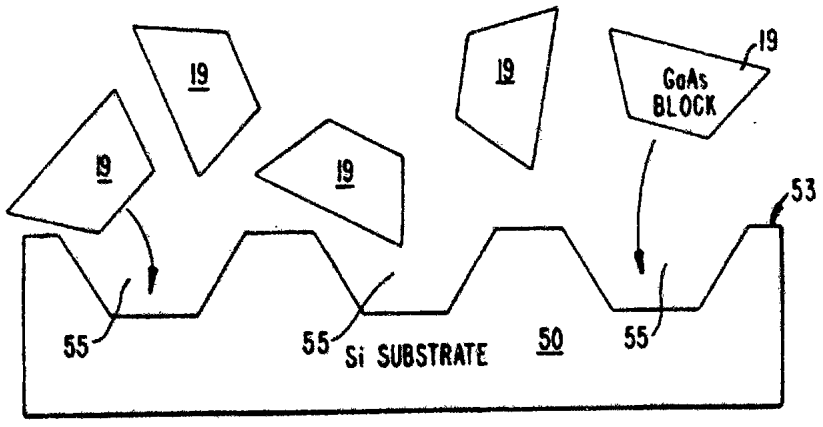

(57) Abstract

A method for assembling microstructures onto a substrate through fluid transport. The microstructures being shaped blocks (19) self-align into recessed regions (55) located on a substrate (50) such that the microstructure becomes integral with the substrate. The improved method includes a step of transferring the shaped blocks into a fluid to create a slurry. Such slurry is then poured evenly over the top surface (53) of a substrate having recessed regions thereon. The microstructure via the shape and fluid tumbles onto the surface of the substrate, self-aligns, and engages into a recessed region.

METHOD FOR FABRICATING SELF-ASSEMBLING MICROSTRUCTURES

GOVERNMENT RIGHTS NOTICE

This invention was made with government support under Grant (Contract) Nos. AFOSR-91-0327 and F49620-92-J-054-1 awarded by the Department of Defense. The Government has certain rights to this invention.

BACKGROUND OF THE INVENTION

The present invention relates to the field of electronic integrated circuits. The invention is illustrated in an example with regard to the manufacture of gallium arsenide microstructures onto a silicon substrate, but it will be recognized that the invention will have a wider range of applicability. Merely by way of example, the invention may be applied in the manufacture of devices containing silicon based electronic devices integrated with a gallium arsenide based microstructures (or devices) such as light emitting diodes (LED), lasers, tunneling transistors, Gunn oscillators, integrated circuits, solar collectors, and others.

Industry currently needs a cost effective, efficient, and practical method for assembling a higher cost microstructure onto a lower cost commercially available substrate. In particular, a material such as gallium arsenide possesses substantially better characteristics for some specific electronic and opto-electronic applications rather than materials such as silicon. However, in the fabrication of gallium arsenide devices, substantial regions of a gallium arsenide wafer are typically unused and wasted. Such unused regions generally create an inefficient use of precious die area. In addition, processing gallium arsenide typically requires special techniques, chemicals, and equipment, and is therefore costly.

Other applications such as very large scale integrated (VLSI) circuits may be better fabricated in silicon rather than gallium arsenide. In still further applications, it may be desirable to produce integrated circuits having characteristics of both types of materials. Accordingly, industry needs to develop an effective method of fabricating a gallium arsenide device integrated with a silicon based integrated circuit. The resulting structure of such method includes advantages of both gallium arsenide and silicon based devices.

Methods such as flip chip bonding, lift off methods, and others, generally require large areas of a substrate and are incompatible with a micron sized state-of-art microstructure. Such methods often create difficulty in positioning a particle onto a substrate. Accordingly, industry needs to develop an effective

method of fabricating higher cost materials such as a gallium arsenide microstructure onto a lower cost substrate such as silicon.

Industry utilizes or has proposed several methods for fabricating individual electronic components (or generally microstructures) and assembling such structures onto a substrate. One approach is to grow gallium arsenide devices directly onto a silicon substrate. This approach becomes limiting because the lattice structure of gallium arsenide mismatches that of silicon. In addition, growing gallium arsenide onto silicon is inherently difficult and therefore costly. Accordingly, gallium arsenide can not efficiently be grown on a silicon substrate.

Another approach is described by Yando in U.S. Patent No. 3,439,416. Yando describes components or structures placed, trapped, or vibrated on an array of magnets. Such magnets include magnetized layers alternating with non-magnetized layers to form a laminated structure. Components are matched onto the array of magnets forming an assembly thereof. However, severe limitations exist on the shape, size, and distribution of the components. Component width must match the spacing of the magnetic layers and the distribution of components are constrained by the parallel geometry of lamination. In addition, self-alignment of components requires the presence of the laminated structure. Furthermore, the structures disclosed by Yando typically possess millimeter sized dimensions and are therefore generally incompatible with micron sized integrated circuit structures. Accordingly, the method and structure disclosed by Yando is thereby too large and complicated to be effective for assembling a state-of-art microstructure or component onto a substrate.

Another approach involves mating physical features between a packaged surface mount device and substrate as described in U.S. Patent No. 5,034,802, Liebes, Jr. et al. The assembly process described requires a human or robotics arm to physically pick, align, and attach a centimeter sized packaged surface mount device onto a substrate. Such process is limiting because of the need for the human or robotics arm. The human or robotics arm assembles each packaged device onto the substrate one-by-one and not simultaneously, thereby limiting the efficiency and effectiveness of the operation. Moreover, the method uses centimeter sized devices (or packed surface mount integrated circuits), and would have little applicability with micron sized integrated circuits in die form.

Another approach, such as the one described in U.S. Patent No. 4,542,397, Biegelsen et al. involves a method of placing parallelogram shaped structures onto a substrate by mechanical vibration. Alternatively, the method may also employ pulsating air through apertures in the support surface (or substrate). A limitation to the method includes an apparatus capable of vibrating

the structures, or an apparatus for pulsating air through the apertures. Moreover, the method described relies upon centimeter-sized dies and would have little applicability with state-of-art micron sized structures.

A further approach such as that described in U.S. Patent No. 4,194,668 by Akyurek discloses an apparatus for aligning and soldering electrode pedestals onto solderable ohmic anode contacts. The anode contacts are portions of individual semiconductor chips located on a wafer. Assembling the structures requires techniques of sprinkling pedestals onto a mask and then electromagnetic shaking such pedestals for alignment. The method becomes limiting because of the need for a shaking apparatus for the electromagnetic shaking step. In addition, the method also requires a feed surface gently sloping to the mask for transferring electronic pedestals onto the mask. Moreover, the method is solely in context to electrode pedestals and silicon wafers, thereby limiting the use of such method to these structures.

Still another approach requires assembling integrated circuits onto a substrate through electrostatic forces as described in Application Serial No. 07/902,986 filed June 23, 1992 by Cohn. The electrostatic forces vibrate particles such that the particles are arranged at a state of minimum potential energy. A limitation with such method includes providing an apparatus capable of vibrating particles with electrostatic forces. Moreover, the method of Cohn creates damage to a portion of the integrated circuits by mechanically vibrating them against each other and is also generally ineffective. Accordingly the method typically becomes incompatible with a state-of-art microstructure.

From the above it is seen that a method of assembling a microstructure onto a substrate that is compact, low cost, efficient, reliable, and requires little maintenance is desired.

~~SUMMARY OF THE INVENTION~~

~~The present invention pertains to a method and resulting~~ structure for assembling a microstructure onto a substrate. In particular, the method includes transferring shaped blocks or generally structures via a fluid onto a top surface of a substrate having recessed regions or generally binding sites or receptors. Upon transferring, the blocks self-align through their shape into the recessed regions, and integrate thereon. The resulting structure may include a variety of useful electronic integrated circuits containing silicon based electronic devices integrated with a gallium arsenide based microstructures such as a light emitting diodes (LED), lasers, tunneling transistors, Gunn oscillators, integrated circuits, solar ~~collectors, and others~~.

According to one aspect of the present invention there is provided a method of assembling a microstructure on a substrate, said substrate comprising a top surface with at least one recessed region thereon, comprising the steps of:

providing a plurality of shaped blocks, said shaped block comprising an integrated circuit device thereon;

transferring said shaped blocks into a fluid to form a slurry; and

dispensing said slurry over said substrate at a rate where at least one of said shaped blocks is disposed into a recessed region.

According to another aspect of the present invention there is provided a method of fabricating shaped blocks comprising an integrated circuit device, comprising the steps of:

providing a substrate having a top surface and a backside;

growing a sacrificial layer made from a material selected from the group consisting of aluminum arsenide, indium phosphate and silicon dioxide overlying said top surface;

forming a block layer overlying said top surface; and

masking and etching said block layer up to said sacrificial layer forming a plurality of shaped blocks on and in contact with said sacrificial layer.

According to yet another aspect of the present invention there is provided a method of fabricating shaped blocks comprising an integrated circuit device, comprising the steps of:

providing a substrate having a top surface and a backside;

growing a sacrificial layer overlying said top surface;

forming a block layer overlying said top surface; and

masking and etching said block layer up to said sacrificial layer forming a plurality of shaped blocks on and in contact with said sacrificial layer;

depositing a filler layer onto a top surface of said shaped blocks and exposed portions of said sacrificial layer;

attaching a top surface of an intermediate substrate onto said top surface of said shaped blocks;

removing said substrate from said shaped blocks;

processing portions of said shaped blocks, said processing step forming integrated circuit devices on said blocks; and

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removing said filler layer and said shaped blocks from said intermediate substrate.

A further understanding of the nature and advantages of the invention will become apparent by reference to the remaining portions of the specification and drawings describing preferred embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a gallium arsenide wafer having a molecular beam epitaxy (MBE) grown gallium arsenide layer for the improved method of fabrication;

Fig. 2 is an illustration of trapezoidal shaped gallium arsenide blocks etched from an MBE grown gallium arsenide layer;

Fig. 3 is an illustration for a lift-off step of gallium arsenide blocks;

Fig. 4 is an illustration of a portion of an alternative lift-off step using a intermediate substrate;

Fig. 5 is an illustration of another portion of the alternative lift-off step of Fig. 4;

Fig. 6 is an illustration of each gallium arsenide block self-aligning onto a silicon substrate;

Fig. 7 is an embodiment of a microstructure assembled onto the silicon substrate according to the improved method depicted by Figs. 1-3 and 6;

Fig. 8 is an alternative embodiment of a microstructure assembled onto a substrate;

Fig. 9 is an embodiment of a microstructure assembled onto a substrate forming a gallium arsenide diode;

Fig. 10 is an alternative embodiment of a microstructure assembled onto a substrate forming a gallium arsenide diode;

Fig. 11 is further alternative embodiment of a microstructure assembled onto a substrate forming a gallium arsenide diode·

Fig. 12 is an illustration of examples of shaped blocks;

Fig. 13 is a photograph of an assembled microstructure according to the experiment;

Fig. 14 is a photograph of an operational photo diode according to the experiment;

Fig. 15 is a photograph of a metallised ring layer overlying a gallium arsenide block;

Fig. 16 is a current-voltage representation for a gallium arsenide diode according to the experiment; and

Fig. 17 is a current-voltage representation for a gallium arsenide/aluminum arsenide resonant-tunneling diode according to the experiment.

DESCRIPTION OF SPECIFIC EMBODIMENTS

With reference to Figs. 1-17, the present invention provides an improved method of fabricating a microstructure onto a substrate, and an improved resulting structure. Figs. 1-17 are, for example, in context to fabricating and assembling a shaped gallium arsenide block onto a silicon substrate for illustrative purposes only.

In the assembly of a gallium arsenide block onto a silicon wafer, trapezoidal shaped blocks self-align into inverted trapezoidal shaped recessed regions located on the top surface of the silicon wafer. Steps for such method include forming the gallium arsenide blocks, transferring the blocks into a solution forming a slurry, and spreading the slurry evenly over the top surface of a silicon substrate having recessed regions. During the spreading steps, the blocks self-align and settle into the recessed regions while being transported with the fluid across the top surface. The details of fabricating the silicon substrate having recessed regions will be discussed in detail below after a brief discussion of forming the gallium arsenide blocks.

In a specific embodiment, the method provides as an example a step of forming trapezoidal shaped blocks from a gallium arsenide wafer. Such step includes providing a gallium arsenide wafer 10 as illustrated in Fig. 1. The method also provides forming sacrificial layer 13 by chemical vapor deposition, sputtering, or the like overlying top surface 15 of gallium arsenide wafer 10. Such sacrificial layer 13 includes, for example, aluminum arsenide. Other sacrificial layers may include indium phosphate, silicon dioxide, photoresist, among other materials capable of being selectively etched. Of course, the sacrificial layer used depends upon the particular application. For an aluminum arsenide sacrificial layer, thickness for such layer is between about 0.1 μm and about 5.0 μm, and preferably at about 1 μm. Before forming sacrificial layer 13, a step of etching top surface 15 by methods such as wet etching, plasma etching, or reactive ion etching clears off any native oxide. Alternatively, a step of desorption in the presence of arsenic removes the native oxide layer. A subsequent step of preferential etching (to be discussed in detail later) removes sacrificial layer 13 to facilitate the lift-off of each gallium arsenide block (also called a mesa shaped or trapezoidal shaped or truncated pyramid shaped structure) formed overlying sacrificial layer 13.

In Fig. 1, gallium arsenide layer 17 forms overlying sacrificial layer 13. Such gallium arsenide layer may be fabricated by methods including molecular beam epitaxy, chemical vapor deposition, and others. The thickness (T) of the gallium arsenide layer is at least about 10 nm and greater, and preferably at about 10 μm and greater, depending upon the particular application.

To produce the desired dimensions for the block, the improved method provides the steps of masking and etching gallium arsenide layer 17. Fig. 2 illustrates gallium arsenide substrate 10 after such masking and etching steps and includes gallium arsenide blocks 19 and a photoresist layer 21 overlying gallium arsenide layer 17 (not shown). Generally, unexposed portions of gallium arsenide layer 17 are etched up to sacrificial layer 13 as illustrated in Fig. 2. Such etching step provides a plurality of shaped gallium arsenide blocks 19. For the present example, the shaped blocks include a trapezoidal profile or truncated pyramid shape. Such trapezoidal profile may be fabricated by methods of wet etching, plasma etching, ion milling, reactive ion etching, among others, depending on the application.

Generally, a wet etch produces a sloping profile along the sides or edges of each gallium arsenide block. For mask edges parallel to the [1$\bar{1}$0] direction, a wet etch produces an outward sloping profile as illustrated in Fig 2. Alternatively, mask edges parallel to the [110] direction, produces an inward sloping (or reverse mesa) profile. The outward sloping profile provides a desired shape which integrates into a silicon substrate having recessed regions shaped in a complementary manner.

Ion milling produces gallium arsenide blocks with outward sloping profiles, depending upon the beam angle. Beam angle is adjusted between about 0° to about 30° from a normal to top surface 15 on gallium arsenide substrate 10. To create the outward sloping (or truncated pyramid shape) profile for each block, the entire structure is typically rotated during such etching step.

Reactive ion etching (RIE) also produces gallium arsenide blocks having a shaped profile. Generally, such etching method creates blocks having undercut sides or a reverse mesa profile. Depending upon variables such as the etchant, pressure, equipment, and others, such etching method may create blocks having substantially consistent shapes and/or profiles.

After etching the MBE grown layer, trapezoidal shaped blocks are removed through a lift-off technique from gallium arsenide substrate 10 by preferential etching sacrificial layer 13 as illustrated in Fig. 3. Such lift-off technique occurs by, for example, a preferential wet etch of the aluminum arsenide sacrificial layer. In the gallium arsenide example, such wet etching step is

typically performed by a chemical such as a hydrofluoric acid solution or the like. The etchant used substantially etches the sacrificial layer but does not aggressively attack gallium arsenide blocks and/or substrates.

After separating the gallium arsenide blocks from substrate 10, methods of diluting and decanting the wet etchant solution remove the blocks from the solution. In the gallium arsenide example, the wet etchant is diluted and decanted using purified water, methanol, ethanol, or the like. Optionally, a rinsing step occurs after the diluting and decanting step. The rinsing step relies on solutions such as acetone, methanol, ethanol, or any other inert solution having low corrosive properties. Such solution also provides a medium (or fluid) for creating a mixture having blocks suspended therein or generally a slurry.

Instead of the lift-off technique illustrated in Fig. 3, an alternative lift-off method creates intermediate structure 250 of Fig. 4 from the gallium arsenide structure of Fig. 2. Such alternative lift-off method also promotes lift-off of the shaped blocks in applications where the devices are formed onto the backside of the blocks. As shown, the method includes spreading a filler or wax layer 253 preferably high temperature wax overlying the top surface of exposed portions of sacrificial layer 13 and gaps 255 between each block 19. One such wax includes a product by the name of TECH WAX made by TRANSENE Co., Inc. The method then includes inverting the gallium arsenide structure of Fig. 2 and attaching top surface 21 onto intermediate substrate 257. Such intermediate substrate is, for example, a silicon wafer or the like. However, prior to the attaching step, intermediate substrate surface 261 undergoes steps of etching off any native oxide preferably with a wet etchant such as hydrofluoric acid, and treating the cleaned surface with an adhesion promotor such as hexamethyldisilazane also called HMDS. In removing gallium arsenide substrate 10, backside 263 is lapped about 50 μm remains on substrate 10. The remaining thickness of substrate 10 is then etched up to aluminum arsenide layer 13. An etchant such as ammonium hydroxide and hydrogen peroxide (6:200 $NH_3OH:H_2O_2$) preferentially etches the gallium arsenide substrate up to aluminum arsenide layer 13. Accordingly, the aluminum arsenide layer acts as an etch stop protecting gallium arsenide blocks 19. Removing aluminum arsenide layer 13 requires a step of wet etching using an etchant such as hydrofluoric acid. Such etchant typically removes aluminum arsenide layer 13 after a short dip in such solution. After the aluminum arsenide layer is completely removed, steps including masking, sputtering, and etching form metallized ring contacts 265 as illustrated in Fig. 5. Such metallized ring contacts were made by patterns formed from photoresist layer 267. The

metallization for such contacts include materials such as gold, aluminum, among others. Alternatively, other processing steps such as etching, masking, implantation, diffusion, and the like may be performed on the blocks to create other profiles as well as active devices thereon. A solution such as trichloroethane (TCA) dissolves the filler or wax disposed between each block 19 and photoresist layer 21, and lifts off the gallium arsenide blocks 19 from intermediate substrate 257. To decrease corrosion, the gallium arsenide blocks are transferred to an inert solution such as acetone, methanol, ethanol, or any other solution having low corrosive characteristics. Such inert solution and blocks are often called a mixture or generally a slurry.

The slurry comprises an inert solution (of fluid) and shaped blocks. Enough solution exists in the slurry to allow the blocks to slide across the top surface of the substrate. Preferably, the amount of solution in the mixture is at least the same order as the amount of blocks. Of course, the amount of solution necessary depends upon characteristics such as block size, block material, substrate size, substrate material, and solution. After preparation, the slurry is transferred or spread over top surface 53 of silicon substrate 50 as illustrated in Fig. 6. The details of the transferring technique are discussed below after a brief discussion in fabricating silicon substrate 50.

As shown in Fig. 6, silicon substrate 50 comprises etched recessed regions 55. A variety of techniques including wet etching, plasma etching, reactive ion etching, ion milling, among others provide recessed regions 50, or generally trenches, receptors, or binding sites. Such techniques etch recessed regions 50 with a geometric profile which is complementary to block 19. In the silicon substrate, for example, each recessed region includes a trapezoidal profile or inverted truncated pyramid shape. The trapezoidal profile allows block 19 to self-align and fit closely into recessed region 50 via the improved transferring technique.

The transferring technique includes a step of evenly spreading or pouring the slurry over top surface 53. The transferring technique may be accomplished by pouring a vessel of slurry evenly over top surface 53. Alternatively, the slurry may also be transferred from a pipet, flask, beaker, or any other type of vessel and/or apparatus capable of evenly transferring the slurry over top surface 53. Generally, the slurry is poured over top surface 50 at a rate which allows substantial coverage of the top surface, but prevents blocks already disposed into the recessed regions from floating or popping out. Slurry flow is typically laminar but can be non-laminar, depending upon the particular application. In the gallium arsenide block example, the fluid flux

over top surface 53 occurs at a velocity between about 0.01 mm/sec. and about 100 mm/sec. Preferably, fluid flux occurs at about 1 mm/sec. At such flux rates, the blocks flow evenly with the fluid, tumble onto top surface 53, self-align, and settle into recessed regions 55. Optionally, to prevent the blocks already disposed in the recessed regions from floating out, the transferring step may take place in a centrifuge or the like. A centrifuge, for example, places a force on the blocks already disposed in the recessed regions and thereby prevents such blocks from floating out with solution.

In a specific embodiment, the resulting structure 20 of the method described by Figs. 1-3 and 6 is illustrated in Fig. 7. The assembled microstructure includes silicon substrate 10, gallium arsenide blocks 19, and recessed regions 55. The trapezoidal shape of the blocks and recessed regions allows a block to self-align and fit closely into a recessed region during the transferring step. An angle (A) formed between one side of the block and the corresponding side of the recessed region is between about substantially 0° to about 20°. Preferably, such angle is less than about 5° but greater than substantially 0°. Such angle facilitates the self-alignment process of each block. The improved method allows for the fabrication of multiple blocks or microstructures onto a substrate by various shaped blocks and recessed region geometries and the fluid transferring step.

In a modification to the preceding specific embodiment, the blocks 19 are attached into recessed regions 55 through eutectic layer 75 as represented in structure 70 of Fig. 8. Prior to the lift-off step, a metallized layer such as gold, silver, solder, or the like is formed onto surface 73. Alternatively, the layer attaching the block with each recessed region may be a synthetic adhesive or the like instead of a eutectic layer. Process steps comprising masking, etching, and sputtering typically form such metallized layer. Subsequent to the transferring step, heating structure 70 forms eutectic layer 75 between metallization layer 73 and silicon substrate 10. The eutectic layer provides both mechanical and electrical contact between substrate 10 and block 19. The method of attaching the blocks onto the substrate provides an efficient, cost effective, and easy technique.

In an alternative specific embodiment, the portions of the improved method of Figs. 1, 2, 4, 5, and 6 provides the resulting gallium arsenide light emitting diodes (LED) 200 as illustrated in Fig. 9. As shown, the gallium arsenide LED includes silicon substrate 203 and gallium arsenide block 205. Each gallium arsenide block includes at least metallized ring contacts 207, p-type gallium arsenide layer 209, n-type gallium arsenide layer 211, and eutectic layer 213. To illuminate the device, voltage is applied to

metallized ring contact 207 or metallization layer. Photons (hv) are illuminated from a center region within each metallized ring contact 207 of gallium arsenide block 205 as shown.

In a further alternative specific embodiment, the improved structure forms gallium arsenide light emitting diodes (LED) 90 as depicted in Fig. 10. Like the previous embodiment, the gallium arsenide LED includes silicon substrate 93 and gallium arsenide block 95. Each gallium arsenide block also includes at least metallized surface 97, p-type gallium arsenide layer 101, n-type gallium arsenide layer 103, and eutectic layer 105, similar to the preceding embodiment. To illuminate the device, voltage is applied to metallization layer 97 by, for example, a probe. Photons (hv) are illuminated from an edge region instead of a center region of gallium arsenide block 95 as shown.

Still in another specific embodiment, the improved structure forms gallium arsenide structure 120 having tapered aperture opening 123 as illustrated in Fig. 11 (not to scale). A process step such as wet etching, ion milling, reactive ion etching, and others forms the tapered aperture opening 123. The gallium arsenide structure may be an LED, laser, or the like. Similar to the previous embodiment, gallium arsenide structure 120 includes substrate 125 and gallium arsenide block 127. Structure 120 also includes a top metallization layer 131 such as aluminum overlying gallium arsenide block 127 and an insulating layer 133. A ring contact layer 135 provides mechanical and electrical contact between substrate 125 and gallium arsenide block 127. Mechanical support and electrical contact for the gallium arsenide block comes from ledge 137. Also shown is a light emitting (or lasing) aperture 139 having a dimension between about 5 μm and about 40 μm. To turn-on the device, voltage is applied to metallization layer 131. Photons (hv) illuminate from gallium arsenide block 127, through light emitting aperture 139, and through tapered aperture opening 123 as shown. Fiber optic cable 141 receives the photons. Such fiber optic cable includes a tapered receiver end with a diameter between about 50 μm and about 200 μm.

The improved method and resulting structure are in context to a trapezoidal shaped block made of gallium arsenide merely for illustrative purposes only. Alternatively, the improved method and structure can be in context to almost any block having shaped features. Shaped features allow such blocks to move over the surface of the substrate via fluid transport, align with a corresponding recessed region, and insert into such recessed region. Fig. 12 illustrates further examples of the shaped blocks. As shown, the blocks may, for example, include a rectangular shape 300, octagonal shape 303, or circular shape 305. The rectangular shaped block

includes up to four orientations for insertion into a substrate having a corresponding recessed region. Alternatively, the octagonal shaped block includes up to eight orientations and the circular shaped block includes continuous orientations as long as the narrow end inserts first into the recessed region. Such blocks may also comprise a material such as silicon, gallium arsenide, aluminum gallium arsenide, diamond, germanium, other group III-V and II-VI compounds, multilayered structures, among others. Such multilayered structures may include metals, insulators such as silicon dioxide, silicon nitride and the like, and combinations thereof. Generally, the block can be made of almost any type of material capable of forming shaped features. Typically, such blocks are fabricated by methods including ion milling, reactive ion etching, and the like. In facilitating alignment of each block onto a recessed region, an angle between a side of the block and the corresponding side of the recessed region for a disposed block is between about substantially 0° to about 20°. Preferably, such angle is less than about 5° but greater than substantially 0°.

The shaped block assembles with a substrate such as a silicon wafer, plastic sheet, gallium arsenide wafer, glass substrate, ceramic substrate, or the like. The substrate includes almost any type of material capable of forming shaped recessed regions or generally binding sites or receptors thereon which complement the shaped blocks.

Examples

To prove the principle and demonstrate the operation of the method and structure, a gallium arsenide block in the form of a diode was assembled onto a silicon substrate and operated.

In a gallium arsenide example, a slurry including gallium arsenide blocks were transferred such that the blocks self-aligned into recessed regions located on a top surface of a silicon substrate. The steps for such method included forming the gallium arsenide blocks, transferring the blocks into a solution forming a slurry, and transporting the slurry evenly over a top surface of a silicon substrate having recessed regions. The shaped blocks generally tumble onto the top surface of the substrate, self-align and engage with a recessed region having a complementary shape.

In creating the silicon substrate, a solution of ethylenediamine pyrocatechol pyrazine (EDP) or potassium hydroxide (KOH) produced recessed regions having a trapezoidal profile or inverted truncated pyramid shape. Each solution created trapezoidal shaped profiles having an outward slope of about 55° from an angle normal to the top surface of the substrate. Trapezoidal profiles occurred due to the selectivity (1:100) between the {111} plane and

the {100} or {110} plane. Specifically, the {111} plane etched slower than the {100} or {110} plane by a ratio of 1:100.

In the present example, an EDP solution etched recessed regions into a silicon substrate. EDP includes ethylenediamine (about 500 ml.), pyrocatechol (about 160 gms.), water (about 160 gms.), pyrazine (about 1 gm.). The EDP bath was also at a temperature of about 115 °C. Prior to the etching step, a thermal oxide (SiO_2) layer having a thickness of about 200 nm was first formed on a top surface of such substrate. Masking and etching such oxide layer formed rectangular shaped regions. Such regions were then etched vertically about 10 μm forming square openings on the top surface about 23 μm in length. Sides protrude down symmetrically from each opening to a square base having a length of about 9μm.

In fabricating trapezoidal shaped blocks, an epi-ready two inch n-type gallium arsenide wafer provided a substrate for the formation of the self-aligning blocks. Native oxide on the top surface of such block was first cleared off by a desorption process. The desorption process included exposing the wafer to a temperature of about 700 °C and elements including arsenic. After the desorption step, a sacrificial layer comprising 1 μm of doped or undoped aluminum arsenide was grown on and in contact with the top surface. A thickness of about 10.7 μm of silicon doped gallium arsenide was then grown through an MBE process overlying the aluminum arsenide layer. Silicon dopants were at a concentration of about 10^{18} atoms/cm^3. The top surface of the MBE grown layer was then patterned with photoresist.

Patterning the top surface of the MBE grown layer included spreading a photoresist layer having a thickness of about 1.6 μm over the top surface of the MBE grown gallium arsenide layer. The photoresist used is a product made by Shipley under the name of AZ1400-31. Patterning steps also included at least exposing, developing, and baking the photoresist. Such baking step occurred at a temperature of about 120 °C for about 1 hour to hard-bake the photoresist layer. The patterning steps formed a plurality of rectangles each having a dimension of about 35 μm by 24 μm (exposed portions of the photoresist) on the top surface.

After patterning, unexposed regions were etched forming trapezoidal shaped blocks attached to the aluminum arsenide sacrificial layer. Proper fit between the block and the recessed region requires each block to have substantially the same shape. Accordingly, various concentrations and techniques of wet etching were tested in this particular example.

Generally, wet etching the unexposed regions produced results which depended upon the orientation of the mask edges. If the mask edges were parallel to the $[1\bar{1}0]$ direction, wet etching the

unexposed regions created outward sloping profiles from the top surface of each block. Alternatively, wet etching unexposed regions where mask edges were parallel to the [110] direction created inward sloping (or reverse mesa) profiles.

Wet etching produced such different profiles (mesa and reverse mesa) because gallium arsenide includes two distinct sets of {111} planes. In a {111} A or {111} gallium plane, each gallium atom on the surface has three arsenide atoms bonded below. For a {111} B or {111} arsenic plane, each arsenide atom on the surface includes three gallium atoms bonded below. Each arsenide atom in the {111} B layer includes a pair of dangling electrons and is therefore exposed. Such dangling electrons are not present in the structure of the {111} A plane. Accordingly, {111} B planes tend to etch faster than {111} A planes, thereby forming blocks having a reverse mesa shape which is generally incompatible with the recessed regions etched on the silicon substrate.

Mask edges parallel to the [110] plane produced more undercutting than the cases where mask edges were parallel to the $[1\bar{1}0]$ plane. In the present example, mask edges parallel to the [110] direction produced about 1.1 μm of horizontal etching per micron of vertical etching near the tops of the blocks. Regions near the base of the blocks produced etches of about 0.4 μm of horizontal etching per micron of vertical etching. Alternatively, mask edges parallel to the $[1\bar{1}0]$ plane produced etches of about 0.8 μm of horizontal etching per micron of vertical etching for regions near the top of the blocks, and 0.1 μm of horizontal etching per micron of vertical etch near the bottom of the blocks. The formation of a square region at the base required a longer mask in the [110] direction.

In addition to mask alignment, etchant concentration also affected the shape of each gallium arsenide block. A solution of phosphoric acid, hydrogen peroxide, and water (H_2PO_3:H_2O_2:H_2O) provided a promising etchant for the MBE grown gallium arsenide layer in the present example. Such etchant created three distinct profiles, depending upon the amount of hydrogen peroxide and water added to phosphoric acid. Dilute concentrations of phosphoric acid (1:1:40 H_2PO_3:H_2O_2:H_2O) created a trapezoidal or mesa shaped profile having a 30° angle between the top surface of the block and a corresponding side. Etchant solutions which were less concentrated produced shallower trapezoidal or mesa shaped profiles at angles from about 10° to 20°. Such shallower profiles were probably a result of etching reactions being transport limited in the {111} B planes.

Higher concentrations of phosphoric acid (1:1:20 H_2PO_3:H_2O_2:H_2O and above) created inward sloping (or reverse mesa) profiles limited by the reaction of the {111} B planes. Preferably,

a phosphoric acid concentration (1:1:30 $H_2PO_4:H_2O_2:H_2O$) between the dilute and concentrated solutions provides better profiles for assembly with recessed regions etched on the silicon substrate. Such etchant produced blocks having angles of 55° parallel to the [110] plane and 49° parallel to the $[1\bar{1}0]$ plane, and typically etched the MBE grown layer at a rate of about 0.133 μm/minute (or about 133 nm/min). In producing the results described, etchant solution was typically replenished when depleted.

Increasing the ratio of phosphoric acid to hydrogen peroxide by 3:1 produced similar profiles to the experiments described, but generally caused rough surfaces on the sides. Such rough surfaces were desirable for the present application.

In a modification to this example, a similar wet etchant (1:1:30 $H_2PO_3:H_2O_2:H_2O$) facilitated the formation of aluminum gallium arsenide blocks from an aluminum gallium arsenide MBE grown layer. Such etchant provided an inward sloping profile parallel to the [110] direction for an aluminum gallium arsenide (x=0.1, $Al_xGa_{1-x}As$) grown MBE layer. Vertical etch rates were about the same as the gallium arsenide MBE grown layer. However, the presence of aluminum arsenide increased etching of the {111} B plane into the reaction-rate limited regime. Such etchant produced an inward sloping profile because etching x=0.1, $Al_xGa_{1-x}As$ was more reactive in the {111} B plane than gallium arsenide.

In addition to wet etching, ion milling was also used to create the gallium arsenide trapezoidal shaped blocks. Ion milling the MBE grown gallium arsenide layer provided outward sloping profiles ranging at angles of about 68° to 90° between the top surface and a corresponding side. To produce such angles, the ion beam angles ranged from about 0° to 25° in reference to a normal from the top surface of the MBE grown layer. Steeper beam angles (closer to 90°) generally created vertical or substantially vertical profiles. Ion milling also required the substrate to be rotated about a center axis during such processing step. Other processing variables included an argon gas etchant, pressure of about 50 millitorr, ion energy of about 1000 v, and an ion milling rate of 1 μm every seven minutes. As the photoresist mask eroded laterally about 5 μm every 70 minutes during milling, sidewalls having angles at about 68° were produced. Selectivity between the gallium arsenide and photoresist was about 3:1. Ion milling produced substantially consistent gallium arsenide blocks and was therefore more effective than wet etching in this particular example.

A final bath having a concentration of 1:1:30 $H_2PO_3:H_2O_2:H_2O$ was used to clear off remaining oxides of either gallium arsenide and aluminum arsenide. Such oxides were typically formed when aluminum arsenide was exposed to etching baths or ion

milling. Hydrofluoric acid may then be used to clear off the oxide layers (typically rough looking and brown in appearance). Generally, such oxide layers reduce the effectiveness of hydrofluoric acid (HF) etching on the sacrificial aluminum arsenide layer.

After clearing off any oxide layers, a HF solution preferentially etched the sacrificial layer of aluminum arsenide to lift-off the gallium arsenide blocks. In particular, a HF solution having a concentration of about 5:1 H_2O:HF was used to etch the sacrificial layer and lift off the blocks. Any blocks still remaining on the substrate possibly through surface tension can be mechanically removed from the substrate into a solution. Removed blocks include a base dimension of about 22 μm by 23 μm, compared to a designed dimension of 24 μm by 24 μm.

After removing the blocks from the substrate, a teflon pipet was used to remove a substantial portion of the HF solution from the gallium arsenide blocks. Any remaining HF was rinsed off with water. Such rinsing step created a mixture including blocks and water. An inert solution such as acetone then replaced the water to decrease any oxide formation on the blocks. Once in the inert solution, the blocks may cluster together and either float to the surface or settle to the bottom of the solution. Such clusters, often visible to the naked eye, decreased the effectiveness of a subsequent transferring step, and were therefore separated by mechanically agitating the solution with ultrasonic vibration.

The inert solution including gallium arsenide blocks were then transferred (or poured) evenly over the top surface of the silicon substrate. In particular, a pipet was used to transfer such solution over the top surface of the substrate. The solution is transferred at a rate creating substantially a laminar flow. Such laminar flow allowed the blocks to tumble and/or slide onto the top surface of the substrate and then self-align into the recessed regions via the trapezoidal profile. Generally, the transfer rate should provide an even flow of solution including blocks over the substrate surface but should not free or remove any blocks already disposed into the recessed regions.

Blocks fabricated by ion milling produced higher yields than wet etched blocks. Ion milled blocks having substantially consistent profiles self aligned and inserted into more than 90% of the recessed regions located on the substrate surface before the solution substantially evaporated. As the solution evaporates, surface tension often pulled a portion of the blocks out of the recessed regions. About 30% to 70% of the recessed regions remained filled after evaporation. The decrease in yield can be addressed by using liquids having lower surface tension during evaporation or by super critical drying methods which substantially eliminates surface

tension. Alternatively, blocks may be bonded into the recessed regions prior to evaporation of the solution, thereby fixing the yield. Wet etched blocks having less consistent block profiles inserted correctly into about 1% to 5% of available recessed regions. Accordingly, ion milled blocks provided higher yields relative to the blocks fabricated by wet etching.

Photographs shown in Fig. 13 illustrate gallium arsenide blocks disposed into recessed regions of the silicon substrate 150 according to the present example. A top portion 153 of each recessed region is square and measures about 23 μm at length. As shown, the photograph includes recessed regions 155, silicon substrate 157, and trapezoidal shaped block 159.

To further illustrate the operation of the present example, an illuminated diode 170 is shown in the photograph of Fig. 14. The photograph includes silicon substrate 173 and illuminated gallium arsenide LED 175. The gallium arsenide LED emitted infrared radiation while under electrical bias. Each gallium arsenide LED which was grown on an MBE layer included an N+ gallium arsenide cap layer (about 100 nm thickness), an N+ $Al_{0.1}Ga_{0.9}As$ transport layer (about 1 μm thickness), a P- active region (about 1 μm thickness), and a P+ buffer layer (about 1 μm thickness). The gallium arsenide LED also required a ring metallized contact 400 for applying voltage and an opening 403 for light output at a top portion of each block as illustrated in Fig. 15. A current-voltage (I-V) curve 500 illustrated in Fig. 16 exhibits typical p-n junction characteristics for the gallium arsenide structure of Fig. 14.

Gallium arsenide/aluminum arsenide resonant-tunneling diodes (RTD's) were also integrated onto silicon. RTD's grown on an MBE layer include gallium arsenide wells (depth at about 5.0 nm) between two aluminum arsenide barriers (depth at about 2.5 nm). Current-voltage characteristics 600 for the RTD's integrated with silicon exhibited proper differential negative resistance (NDR) at V_{PEAK} = 2.0 v. as illustrated in Fig. 17. At such voltage, peak-to-valley ratio was about 2.5. Oscillations (rf) observed after biasing the RTD's in the NDR region were limited to about 100 MHz. External capacitances and inductances of the biasing circuit caused such limitations in frequency.

The description above is in terms of assembling a gallium arsenide block onto a silicon substrate for illustrative purposes only. As shown, the invention may be applied to forming gallium arsenide diodes onto silicon substrates. Another commercial application includes gallium arsenide lasers assembled with silicon integrated circuits. The silicon chips can communicate with other chips with integrated optical detectors on extremely high bit-rate optical channels. Other applications may also include integration of

microwave gallium arsenide devices onto silicon integrated circuits for the purpose of microwave electronics. Still a further application includes microstructures integral with a plastic sheet forming active liquid crystal displays (ALCD) and the like. In such application, the plastic sheet may be fabricated by a technique including stamping, injection molding, among others. The concept of the invention can be used with almost any type of microstructure which assembles onto a larger substrate.

Also described in general terms is the unique profiles for creating self-assembling devices. Such unique profiles, for example, are terms of a single block structure having a corresponding recessed region structure on a substrate for illustrative purposes only. The block structure may also include a variety of shapes such as a cylindrical shape, rectangular shape, square shape, hexagonal shape, pyramid shape, T-shape, kidney shape, and others. The block structure includes widths, lengths, and heights to promote self-assembly for a desired orientation. In addition, more than one type of structure may be present in the mixture (solution and blocks) as long as each structure includes a specific binding site on the substrate.

Although the foregoing invention has been described in some detail by way of illustration and example, for purposes of clarity of understanding, it will be obvious that certain changes and modifications may be practiced within the scope of the appended claims.

The above description is illustrative and not restrictive. Many variations of the invention will become apparent to those of skill in the art upon review of this disclosure. Merely by way of example the invention may used to assemble gallium arsenide devices onto a silicon substrate as well as other applications. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A method of assembling a microstructure on a substrate, said substrate comprising a top surface with at least one recessed region thereon, comprising the steps of:

providing a plurality of shaped blocks, said shaped block comprising an integrated circuit device thereon;

transferring said shaped blocks into a fluid to form a slurry; and

dispensing said slurry over said substrate at a rate where at least one of said shaped blocks is disposed into a recessed region.

2. The method of claim 1 wherein said substrate is selected from a group consisting of a silicon wafer, plastic sheet, gallium arsenide wafer, glass substrate, and ceramic substrate.

3. The method of claim 1 wherein said rate is substantially a laminar flow and allows each of said shaped blocks to self-align into said recessed region.

4. The method of claim 1 wherein said shaped blocks include a trapezoidal profile.

5. The method of claim 4 wherein each of said recessed regions in said substrate is shaped substantially trapezoidal to complement each of said shaped blocks.

6. The method of claim 4 wherein said trapezoidal shaped blocks include a length of about 10μm and greater.

7. The method of claim 1 wherein said fluid is an inert fluid selected from a group consisting of water, acetone, and alcohol.

8. The method of claim 1 wherein said slurry includes enough fluid to allow said shaped blocks to slide across said substrate.

9. The method of claim 4 wherein said trapezoidal blocks are fabricated by a method comprising the steps of :

providing a second substrate having a top surface;

growing a sacrificial layer overlying said top surface;

forming a block layer overlying said top surface;

masking and etching said block layer up to said sacrificial layer forming a plurality of trapezoidal shaped blocks on and in contact with said sacrificial layer;

preferential etching said sacrificial layer lifting off each of said trapezoidal shaped blocks; and

transferring said trapezoidal shaped blocks into a solution to form said slurry.

10. The method of claim 9 further comprising a step of rinsing said blocks subsequent to said preferential etching step.

11. The method of claim 9 wherein said preferential etching step is a step of wet etching.

12. The method of claim 9 wherein said wet etching step includes a hydrogen fluoride etchant.

13. The method of claim 9 wherein said second substrate is selected from the group consisting of gallium arsenide, gallium aluminium arsenide, silicon, and diamond.

14. The method of claim 4 wherein said trapezoidal shaped block further comprising a truncated pyramid shape including a top surface with four sides protruding therefrom to a base.

15. The method of claim 14 wherein said base has a length between about 10 μm and about 50μm, and a width between 10 μm and about 50μmm, and each of said four sides has a height between about 5μm and about 15μm.

16. A method of fabricating shaped blocks comprising an integrated circuit device, comprising the steps of:

providing a substrate having a top surface and a backside;

growing a sacrificial layer made from a material selected from the group consisting of aluminum arsenide, indium phosphate and silicon dioxide overlying said top surface;

forming a block layer overlying said top surface; and

masking and etching said block layer up to said sacrificial layer forming a plurality of shaped blocks on and in contact with said sacrificial layer.

17. The method of claim 16 further comprising a step of preferential etching said sacrificial layer lifting off each of said shaped blocks.

18. A method of fabricating shaped blocks comprising an integrated circuit device, comprising the steps of :

providing a substrate having a top surface and a backside;

growing a sacrificial layer overlying said top surface;

forming a block layer overlying said top surface; and

masking and etching said block layer up to said sacrificial layer forming a plurality of shaped blocks on and in contact with said sacrificial layer;

depositing a filler layer onto a top surface of said shaped blocks and exposed portions of said sacrificial layer;

attaching a top surface of an intermediate substrate onto said top surface of said shaped blocks;

removing said substrate from said shaped blocks;

processing portions of said shaped blocks, said processing step forming integrated circuit devices on said blocks; and

removing said filler layer and said shaped blocks from said intermediate substrate.

19. A method of fabricating shaped blocks comprising an integrated circuit device, comprising:

providing a substrate including a release layer overlying the substrate, and a block layer overlying the release layer;

patterning said block layer to form a plurality of shaped blocks;

preferential etching said release layer to release said plurality of shaped blocks.

20. The method of claim 19 wherein said release layer is made from a material selected from the group consisting of aluminum arsenide, indium phosphate, and silicon dioxide.

21. The method of claim 19 wherein said patterning step includes reactive ion etching.

22. The method of claim 19 wherein said patterning step includes potassium hydroxide etching.

23. The method of claim 19 wherein said preferential etching step comprises hydrofluoric acid etching.

24. The method of claim 19 wherein each of said plurality of shaped blocks includes a sloped sidewall.

25. The method of claim 24 wherein said sloped sidewall is negative.

26. The method of claim 24 wherein said sloped sidewall is positive.

27. A method of assembling a microstructure substantially as hereinbefore described with reference to the accompanying drawings.

Dated this 29th day of August, 1996

THE REGENTS OF THE UNIVERSITY OF CALIFORNIA

By Their Patent Attorneys

DAVIES COLLISON CAVE

13046|95

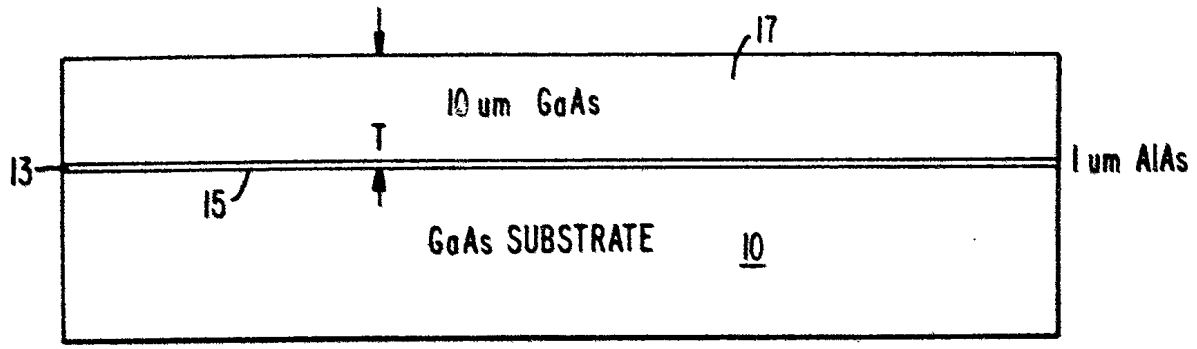


FIG. 1.

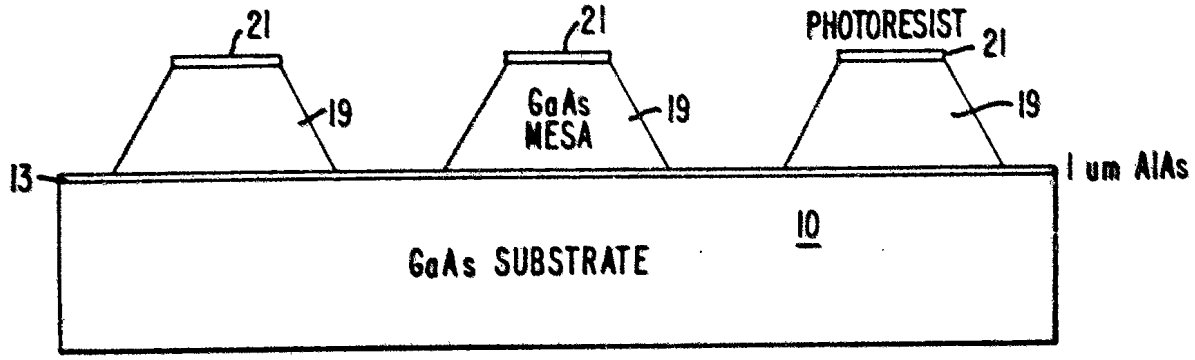


FIG. 2.

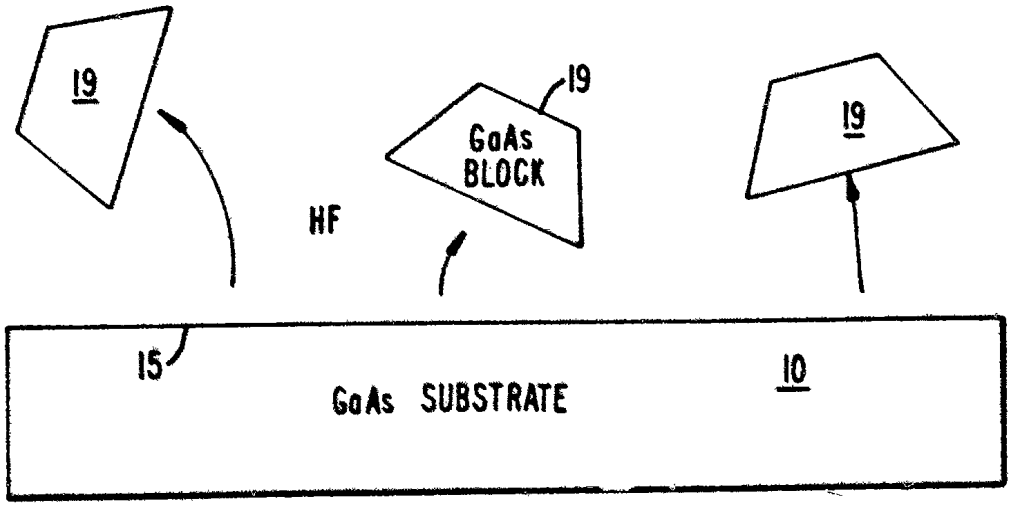


FIG. 3.

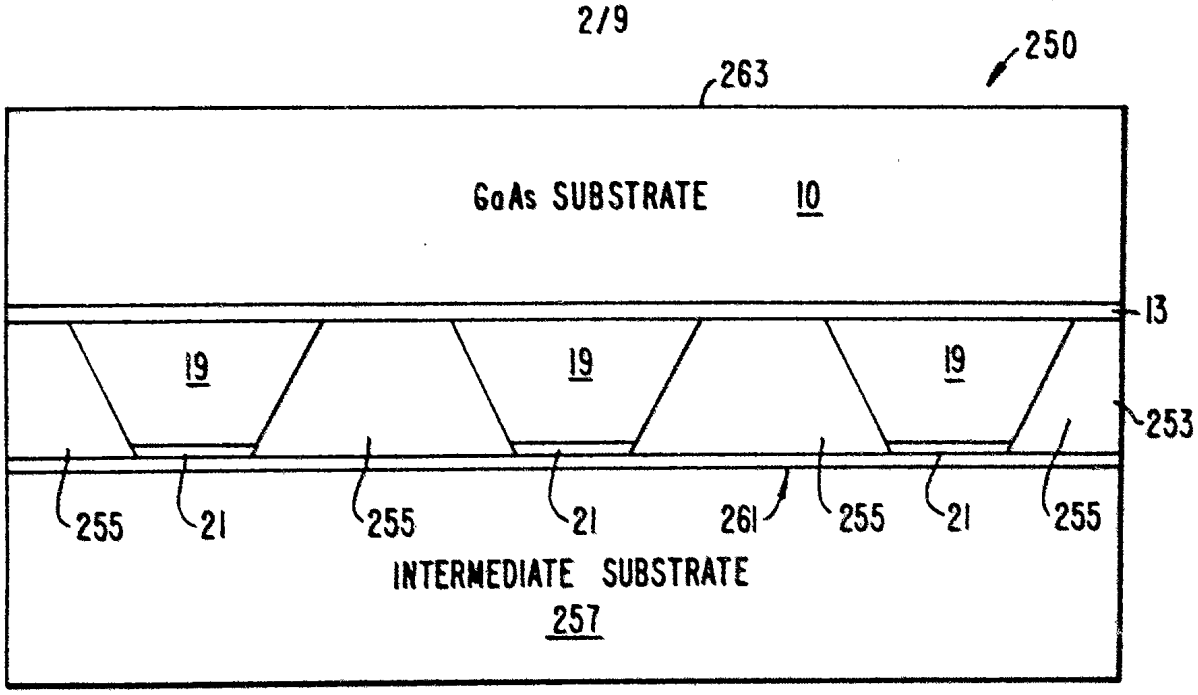
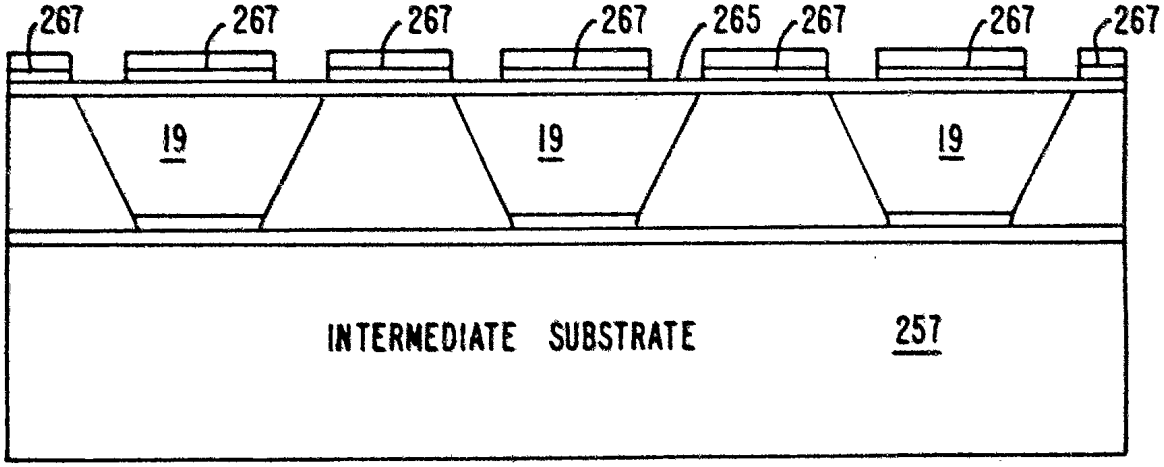


FIG. 4.



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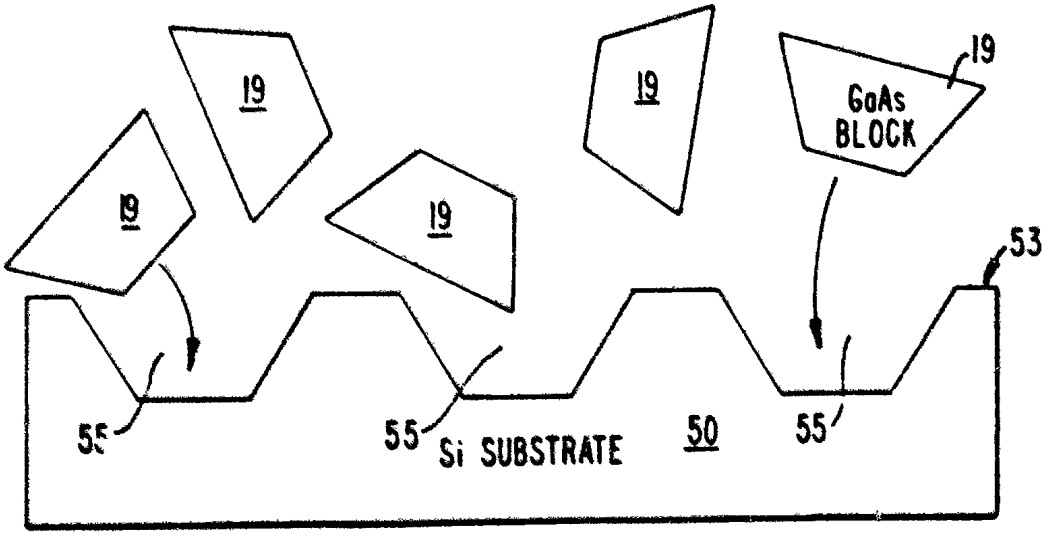

FIG. 6.

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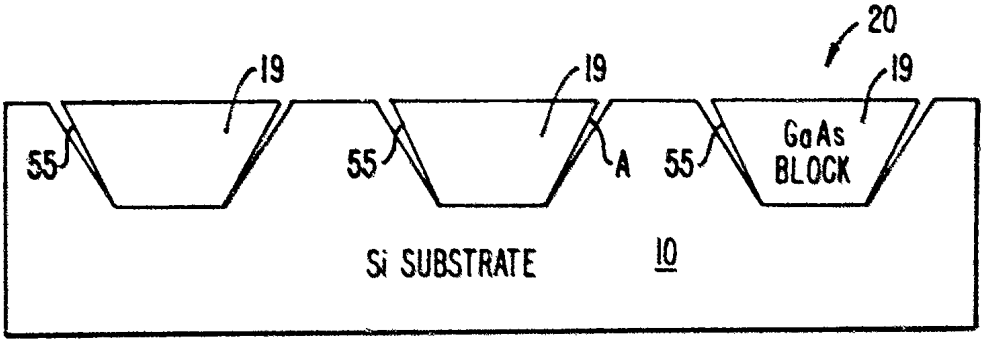


FIG. 7.

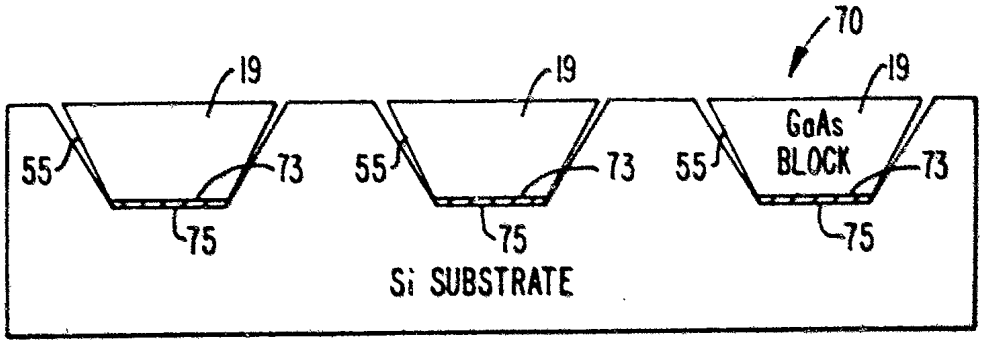


FIG. 8.

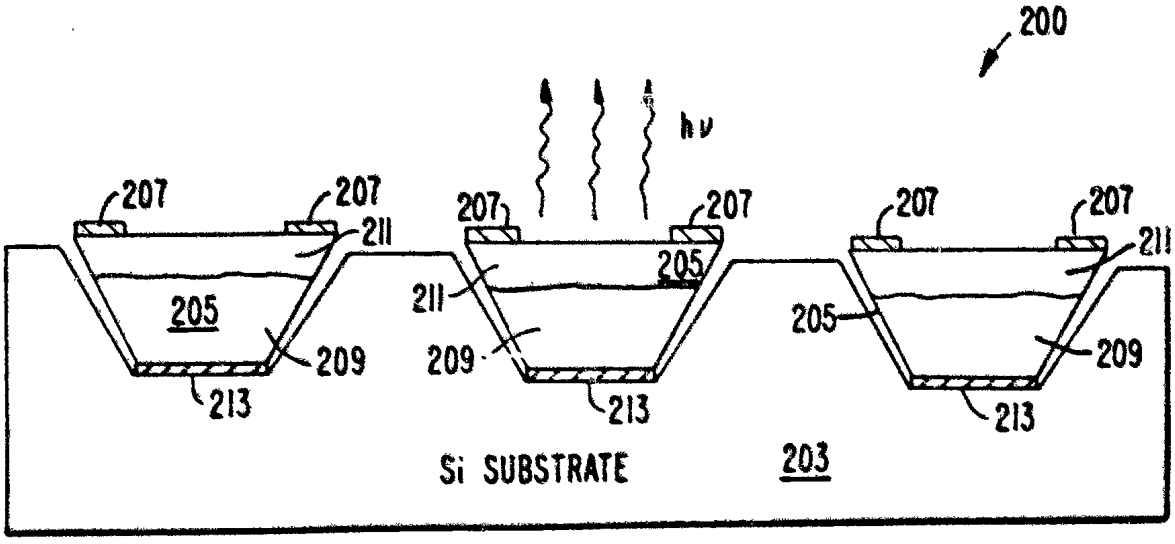
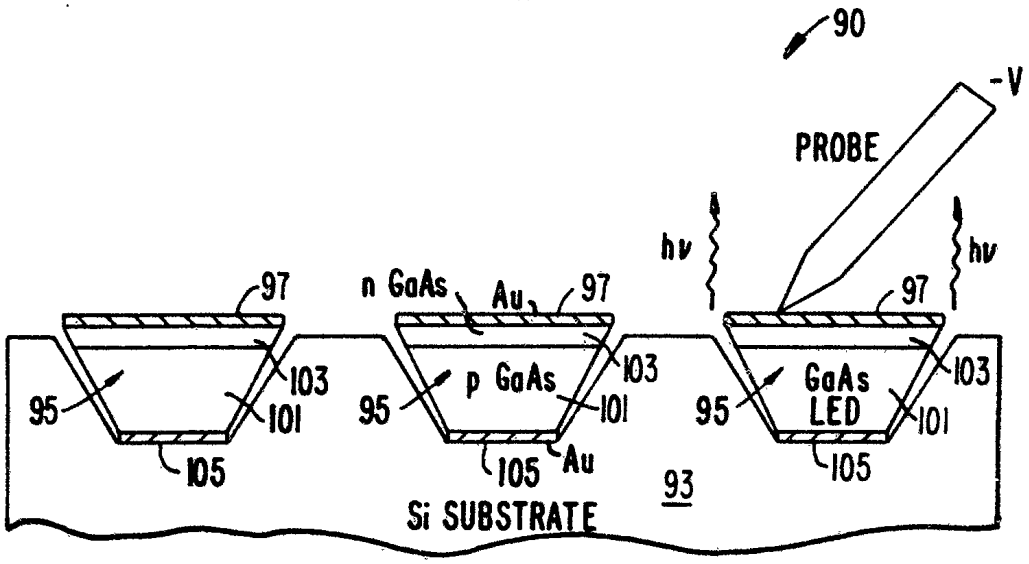


FIG. 9.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hv
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Au
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97
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LED
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95
101
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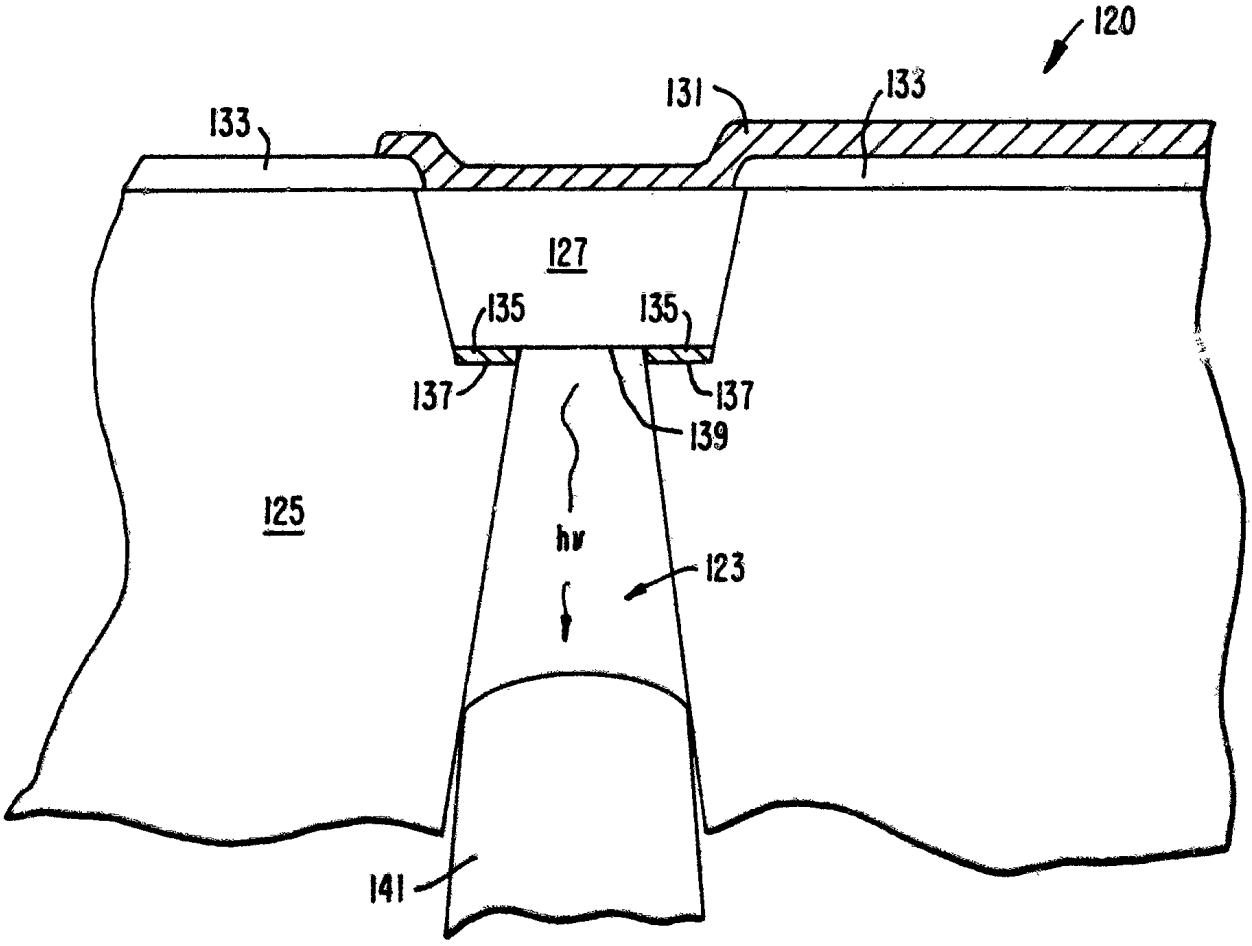
105
Au
105
93
Si SUBSTRATE

FIG. 10.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139
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hv
123
141

FIG. 11.

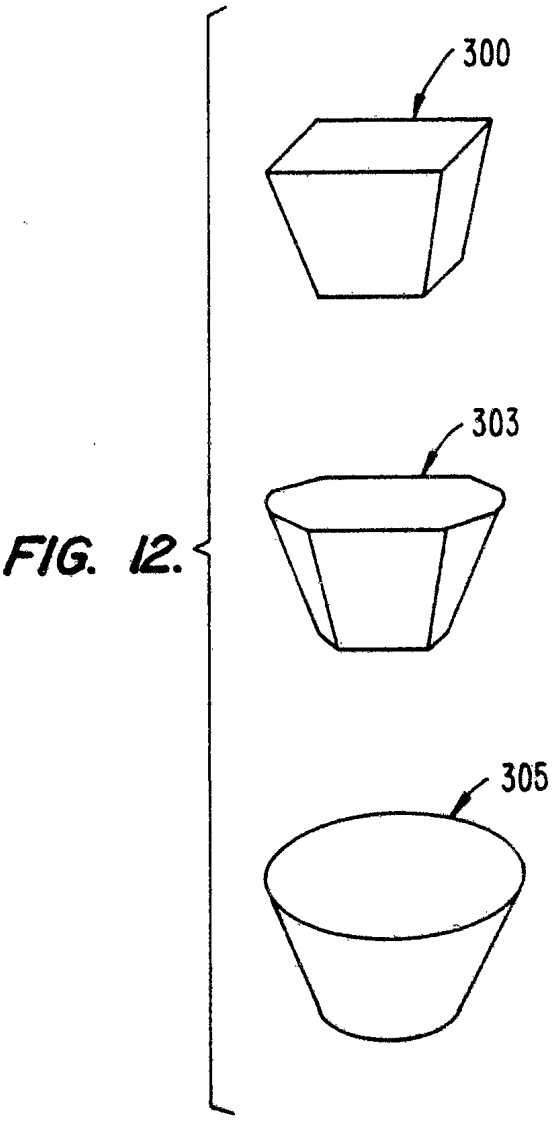


FIG. 12.

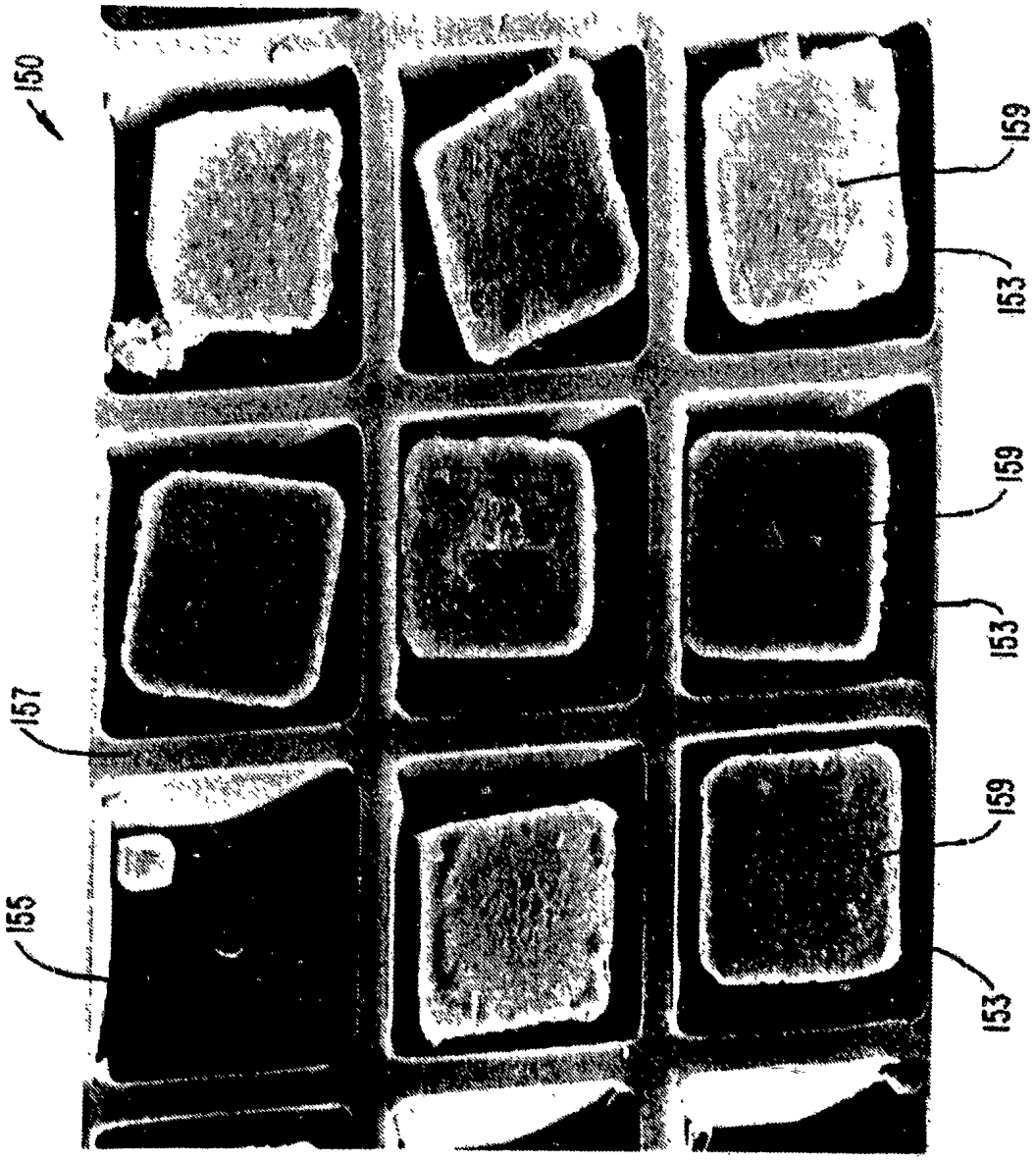


FIG. 13.

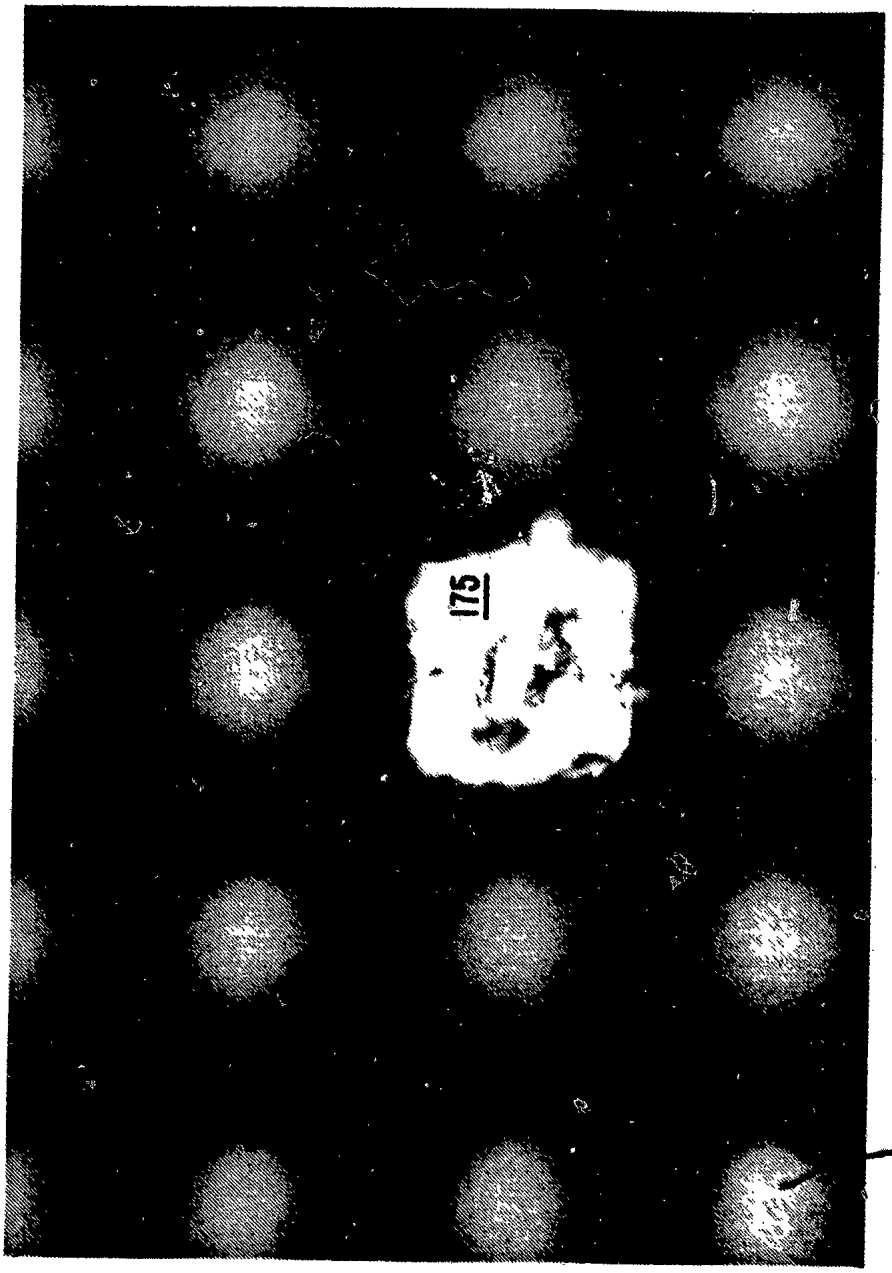


FIG. 14.

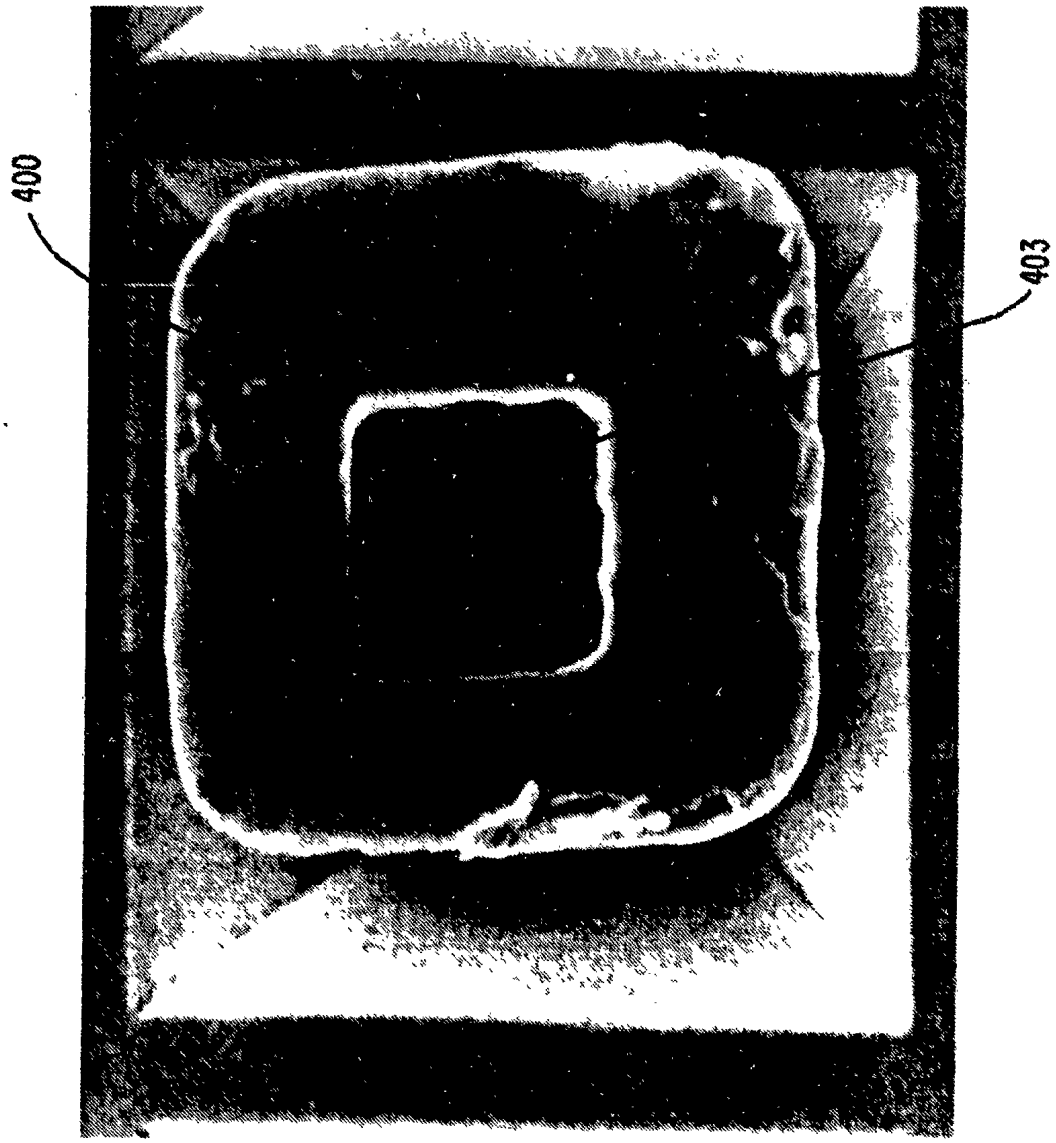
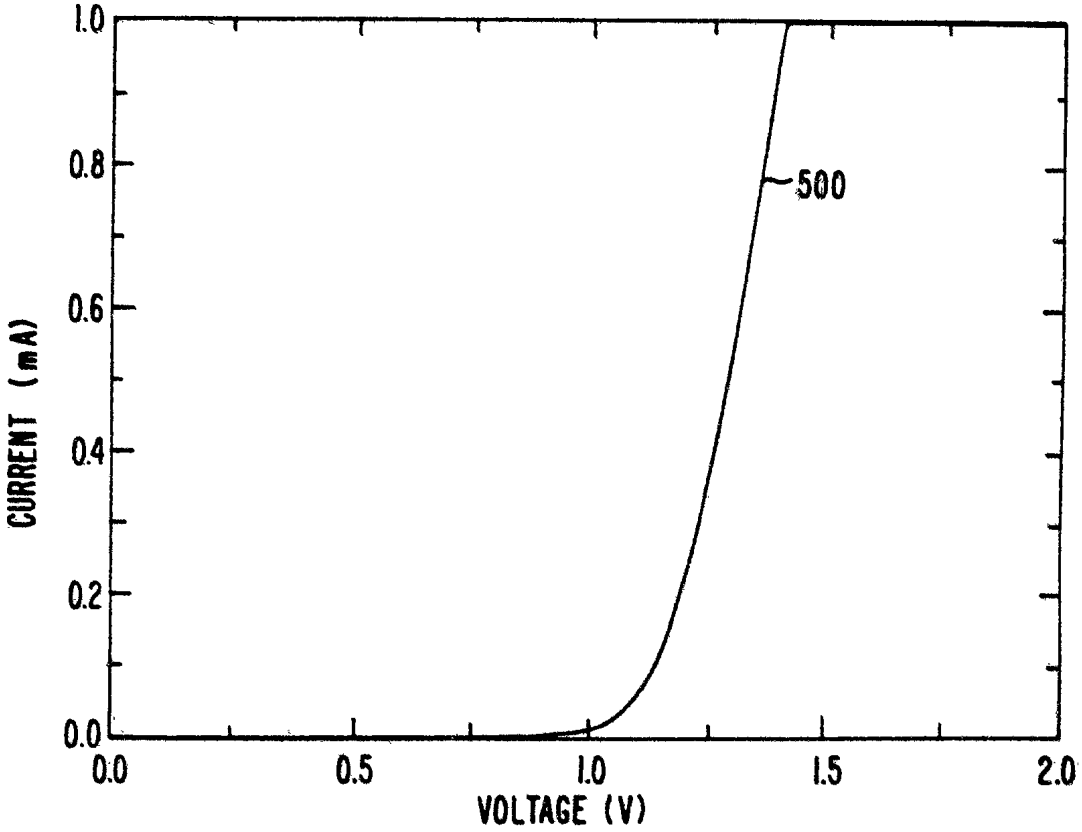


FIG. 15.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0.4
0.2
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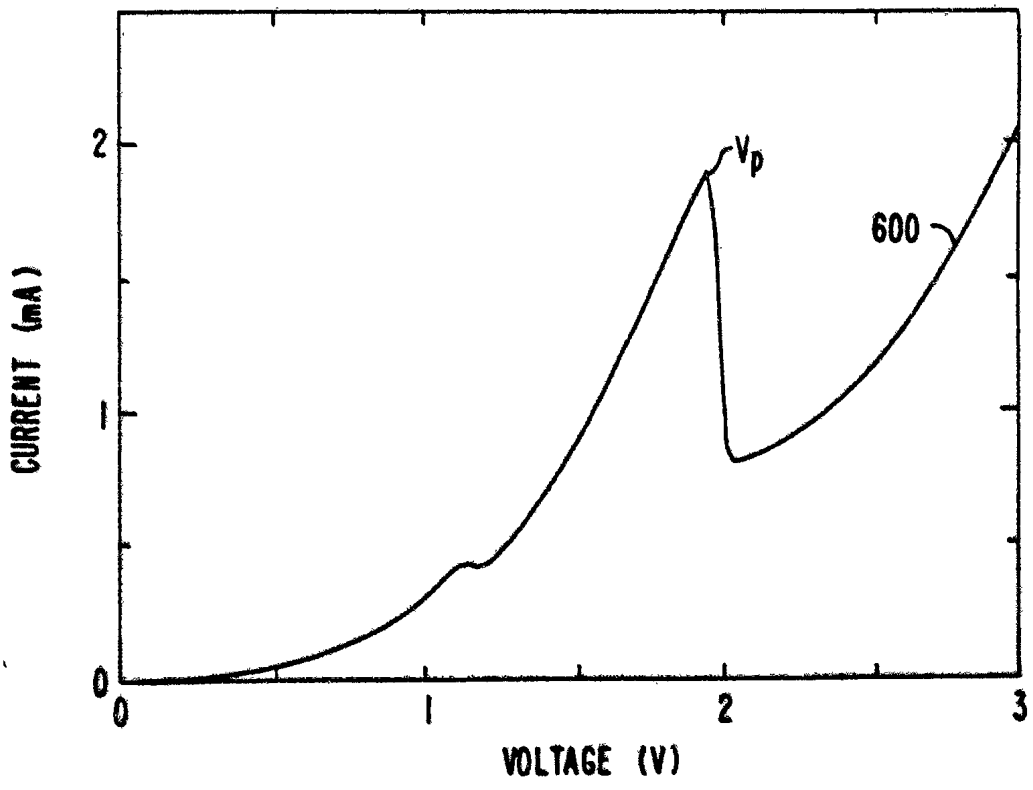
1.0
1.5
2.0
VOLTAGE (V)

FIG. 16.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0
CURRENT (mA)
V_p
600
0
1
2
3
VOLTAGE (V)

FIG. 17.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/14152

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : H01L 21/302, 306
US CL : 156/647, 657, 659.1; 257/084, 521; 437/078, 226
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 156/631, 643, 647 648, 649, 652, 657, 659.1; 662; 257/084, 520, 521; 437/078, 086, 203, 209, 226

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A 4,990,462 (Sliwa) 05 February 1991. See ABSTRACT and Figs. 4a-4b.	1-22
A	US,A, 3,725,160 (Bean ET AL.) 03 APRIL 1973. See Figs. 4 and 6.	16-19

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 24 FEBRUARY 1995	Date of mailing of the international search report 13 MAR 1995
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer WILLIAM A. POWELL Telephone No. (703) 308-1975

Form PCT/ISA/210 (second sheet)(July 1992)*