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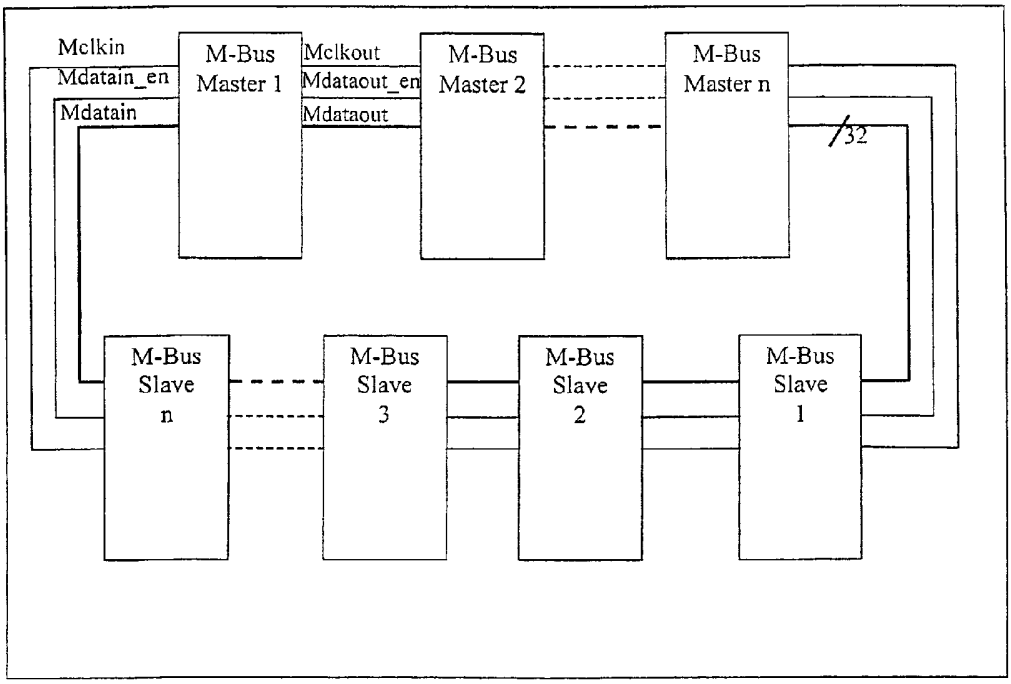
[Continued on next page]

(54) Title: BUS ARCHITECTURE AND COMMUNICATION PROTOCOL



(57) Abstract: A bus architecture wherein a plurality of devices are connected in a continuous loop. The devices included at least one master device (M-Bus Master 1, 2, n) and at least one slave device (M-Bus Slave 1, 2, n), the plurality of devices being directly connected to the continuous loop. Data is propagated through the devices from a source device to a destination device, terminates at the destination device, and can be sent out over a plurality of signal lines (Mdatain and Mdataout).

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— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

BUS ARCHITECTURE AND COMMUNICATION PROTOCOL

Field of the Invention

This invention relates to a bus architecture and communication protocol and refers particularly, though not exclusively, to a bus architecture and communication protocol for an expandable, high speed, off-chip communication interface.

Definition

Throughout this specification a reference to a continuous loop includes a closed loop.

Background to the Invention

Recent developments in chip technology have seen speeds of greater than 1GHz becoming common. However, for machine performance to be able to match chip performance, bus performance must also be improved.

At present, multi-drop bus topology is used for off-chip communication. It has been developed to its present extent by using many techniques such as for example, increasing frequency, widening the interface, splitting, and pipelining transactions. Using such techniques to further develop bus performance will create a number of problems such as, for example, limitation on the maximum frequency useable due to amongst others, signal skew and loading; expandability; the increasing number of pins on the semi-conductor device; reduction in the number of interfaces; and production cost.

Examples of bus technologies are PCI, ISA and AMBA, all of which are based on multi-drop bus architecture. InfiniBand architecture is optimised for links between a plurality of servers within an enterprise cluster to form a SAN.

The RapidIO™ architecture is an electronic data communications standard for interconnecting chips on a circuit board. This relatively new high-performance, packet-switched, interconnect technology was designed for embedded systems, primarily for the networking and communications markets. Industry leaders in networking, communications, semiconductors, and embedded systems founded the RapidIO Trade Association to develop and support this new open standard. RapidIO

architecture offers the bandwidth, software independence, fault tolerance, and low latency required in the networking market. The RapidIO specification defines a high-performance interconnect architecture designed for passing data and control information between microprocessors, DSPs, communications and network processors, system memory, and peripheral devices within a system. It uses a point-to-point bus architecture.

US Patent 6266730 by Rambus Inc. entitled "High frequency bus system" relates to the Rambus system, which is a complete memory subsystem that uses a dedicated bus called a channel and includes:

- a controller (memory interface);
- channel (three-byte wide data and command/address bus; two bytes for data; and one byte for command and addresses);
- connectors;
- Rambus DRAMs (RDRAMS);
- RIMM modules (in-line memory modules for RDRAM chips);
- continuity modules (used in empty connectors); and
- optional repeater chips.

The specification discloses a bus that has a memory module with a substrate and a plurality of devices mounted on it. A bus is coupled to each of the devices that are mounted on the substrate and connect between a first edge of the memory module, and a second edge of the memory module. All signals are of equal electric length to ensure uniform arrival times, and the motherboard consists of plurality of memory modules. The bus is coupled between each of the plurality of memory modules. An overall memory system has a motherboard, a memory controller, and a number of memory modules. The memory controller has a first edge that is connected to the first edge of first memory module; and a second edge that is connected to the first edge of a second memory module. The signals are terminated at and by an end resistor.

US patents 6,201,995 and 5,907,486 describe a multi-tier, master-slave control network having a number of nodes connected in a continuous loop. This is for macro-scale installations as the example given is a train. Each segment of the loop has a

cable connector being a feed-through, or cross over connector. They are not for, nor could they work in, micro or nano scale systems.

A problem with present bus interfaces is that when handling high speed processing data, multiple integrated circuits signal lines are used. If one IC sends streaming data at the same time as another IC sends streaming data on the same line, the effective data transmission rate may drop considerably.

It is therefore the principal object of the present invention to provide a bus architecture and communication protocol having one or more of the following features:

a) minimum control input/output signals; and/or
b) no arbitration switch; and/or
c) simplified hardware implementation; and/or
d) multiple processing support; and/or
e) use of at least one master device and at least one slave device; and/or
f) expandable in relation to the number of master devices and/or the number of slave devices; and/or
g) all devices (master and slave) to be in a looped signal chain; and/or
h) no bus arbitration; and/or
i) communication between master and slave devices to be synchronous and/or asynchronous; and/or
j) master devices to have response buffers; and/or
k) responses from slave devices can be buffered; and/or
l) it suitable for implementation in micro and nano scale systems; and/or
m) be suitable for controlling microstructures (MEMS); and/or
n) may not require tristate signals.

Summary of the Invention

With the above and other objects in mind, the present invention provides a bus architecture wherein a plurality of devices is connected in a continuous loop. Data is propagated through the devices from a source device to a destination device. Preferably, the data terminates at the destination device. More preferably, each of the plurality of devices is directly connected to the continuous loop, and the data may be

sent over a plurality of signal lines. The devices may include at least one master device and at least one slave device.

In another form, the present invention provides a bus architecture including a plurality of master devices and a plurality of slave devices, all master devices and slave devices being connected to each other. The connection is by use of a continuous loop in which all devices are connected, preferably directly connected.

Again, data may be propagated through the devices from a source device to a destination device, and terminating at the destination device. Preferably, the data is sent over a plurality of signal lines.

For both forms, there may be a first number of master devices, and a second number of slave devices, the first number and the second number being the same or, alternatively, different.

In a further form, the present invention provides a bus architecture including a plurality of master devices and a plurality of slave devices connected in a continuous loop, the continuous loop including a plurality of signal lines, each master device being able to communicate with any or all of the slave devices.

The plurality of devices may be directly connected to the continuous loop, and data may be propagated through the devices from a source device to a destination device and terminates at the destination device.

Preferably, for all forms, the devices include at least one master device and at least one slave device. There may be a first number of master devices, and a second number of slave devices, the first number and the second number being the same or, alternatively, different.

Each master device may be able to act as a slave device, and all permutations and combinations of master and slave devices are possible. Each master device may communicate with any number of slave devices and/or master devices.

In a final form the present invention provides a bus communication protocol, the bus having an architecture including a first number of master devices and a second number of slave devices all connected in a continuous loop, wherein a master access word is sent by a master device, and a slave access word is sent by a slave device only in response to a request from the master device. The request may generate responses from a plurality of slave devices.

The master access word is preferably sent as a frame of at least one word depending on read or write access. For a read access there is one or more words and for a write access the frame is two or more consecutive words. They may be the same (symmetric) or different (asymmetric).

Each master access word includes access information, requestor identification, destination identification, an offset address of the destination, signifier for read or write access, and a page address of the destination. For write access a payload is included as a further word. A response frame includes at least one word having a response identification, the requestor identification, the offset address of the response, and a response payload.

The access information may be one or more access bits.

In all forms, the bus is a single data bus, a plural number of data buses being not required.

A master device may command a slave device to enter a mode to provide a periodic read-out, the slave device remaining in the mode until turned off by the master device. A plurality of the first number of master devices may be able to command the slave device to provide a plurality of periodic read-outs. The slave device may be able to respond to other commands from other master devices when in the mode. Preferably, the master devices and the slave devices each have an identity space.

Upon receipt the destination ID may be decoded and, if the decoded destination identification is not zero, the destination identification is decremented and the data sent on. If the decoded destination is zero, it will decode the received data. If the data

terminates at that device, it will write the data into the corresponding register. If the read is read with wait state, data will be put into the bus and the host will wait for the data in the wait state.

Description of the Drawings

In order that the invention may be better understood and readily put into practical effect, there will now be described by way of non-limitative example only a preferred embodiment of the present invention, the description being with reference to the accompanying illustrative drawings in which:

Figure 1 is an illustration of the bus architecture of the present invention;

Figure 2 is an illustration of the configuration of a bus controller of the present invention; and

Figure 3 is a preferred timing diagram of the present invention.

Description of the Preferred Embodiment

The embodiment is a bus architecture and communication protocol for an expandable high-speed off-chip communication interface. The bus features master/slave devices, and a communication protocol, that requires a minimal set of control/input/output signal pins. It may support multiple master devices and slave devices and, preferably, no tri-state signal is required. The architecture and protocol are suited for systems at the micro and nano scales, but are not limited to such systems. By controlling multiple channels/slaves using minimum I/O the present invention is suitable for controlling microstructures (MEMS), as the microstructure (MEMS) may require many channel/s signals.

By using the present invention in one form, it may be possible to achieve speeds for the bus clock of up to 120 MHz, and bus width may be as wide as 32 bits. However, higher speeds may be achieved, and other bus widths may be used.

The bus master and slave devices are connected in a continuous loop as in Figure 1. Bus data is propagated through the devices from source to destination and will terminate at the destination device. Preferably, all devices are directly connected to the continuous loop.

Table 1 below lists the description of each signal, width and direction.

TABLE 1

Signal Name	Description	Width	Direction
Mclkout	Data output clock	1	Output
Mdataout_en	Data Valid on Output Bus	1	Output
Mdataout	Data Output Bus	32	Output
Mclkin	Data input clock	1	Input
Mdatain_en	Data Valid on Input Bus	1	Input
Mdatain	Data Input Bus	32	Input

There may be any number of master devices and any number of slave devices. The number of master devices may be linked to the number of slave devices, and vice versa.

Each master device may also act as a slave device, and each master device can work with one or more slave devices. In this way one or more devices can communicate with one or more slave devices. All permutation and combinations of master and slave devices are possible.

As is clear from Figure 1, signal lines in multiples of 8 can be used (32 as illustrated) so that streaming data from one device can be sent over a different signal line to streaming data from another device, thus maintaining an effective, high-speed data transmission rate. With a 32-bit data bus according to the present invention, it is possible to have up to 64 master devices and up to 256 slave devices connected in a continuous loop.

There are two types of access words sent on the bus: a master access word and a slave access word. A master access word is sent only by a master device and the slave access word by a slave device in response to a master device request. Not all master device accesses necessarily generate a single response as multiple responses may also be generated.

A master device can command a slave device to provide a periodic read-out of a particular offset. Once a slave device enters this mode, the slave device will "originate" periodic responses to the master device until this mode is turned off by the master device. The slave device can have one or more such update commands to which it shall periodically transmit response messages. While the slave device is in this state, it is able to respond to other regular commands from other master devices.

A master access word is sent as a frame of one 32-bit word or two consecutive 32-bit words on Mdataout depending on a read or write access. The following describes the data bits representation:

Bit	31	30	29-24	23-16	15-8	7-0
Desc.	Acc	r/w	REQID	DESID	PAGE	OFFSET
	word(0)					

Bit	63-32	31-16
Desc.	Reserved	PAYLOAD(DATA)
	word(1)	

Where:

Acc – Access bit. Must be set to '1'.

rw – Signifies a read or write access. If the access is a read access, no PAYLOAD field is required and the frame will consists of only one 32-bit word(0). '1' – write, '0'-read.

REQID – Requestor Identification. The 6-bits signifies the master device accessing the bus.

DESID – Destination Identification. The 8-bits signifies the destination device being accessed.

PAGE – 8-bit page address of the destination device.

OFFSET – 8-bit offset address of the destination device.

PAYLOAD – 16 bits data for the destination register. If the access is a read access, no PAYLOAD field is required and the frame will consists of only one 32-bit word(0).

The response frame consists of two 16-bit words in the following format. The REQID is copied from the REQID byte of the master access word:

Bit	31	30	29-24	23-16	15-0
Desc.	Res	Unused	REQID	OFFSET	PAYLOAD(DATA)
	word(0)				

Where:

Res – Response bit. Must always be cleared to '0'.

REQID – Requestor Identification. The 6-bits signifies the MEX-BUS Master the slave is responding to.

OFFSET – Offset Address of the response data.

PAYLOAD – 16-bits data.

There are three registers for control and initialization of the bus. The host interface (AHB Slave) to the MEX-BUS controller is addressed as 32-bit word locations. These registers are to be set after the reset sequence and may be modified during operation. Table 2 summarizes the various addresses, register name, description, width and access.

Address (Hex)	Register Name	Description	Width	Access
0x000	REQID	Requestor ID	6-bit	Word* R/W
0x004	DESID	Destination ID of the device being accessed	8-bit	Word* R/W
0x008	PAGE	Page address which makes the upper 8-bits of the 16-bit address	8-bit	Word* R/W
0x800-0xAFF	ASYNCBASE	512 bytes of asynchronous slave access offset locations	16-bit	Hword* R/W
0xB00-0xDFF	SYNCBASE	512 bytes of synchronous slave access offset locations	16-bit	Hword* R

*Word access means that the access to the location has to be 32-bit access. Hword access means that the access to the location has to be 16-bit access.

Table 2

*Word mean

There are two sets of 256 16-bit (512bytes) offset access locations for the host access to the bus slave devices that are mapped into 512 byte locations on the host. It is only during the access to the even location that will initiate an access on the bus. The 16-bit data is in big-endian format. Accessing either set of locations effectively accesses similar physical location on the destination device.

The first set of 512 byte access locations (0x100-0x1FF) will halt the processor and add waitstate cycles until the read data cycle completes. Writes will not cause waitstate unless the previous output data cycle has not been completed.

The second set of 512 byte access locations (0x200-0x2FF) will not halt the processor. A read access effectively reads from the internal register and not from the actual physical device.

The host may communicate with only one slave at a time so that the host can assume that any data response it receives is from the slave to which it is communicating.

Bus Controller

The bus master device controller has a transmit holding register which holds the 8-bit offset address, and the 16-bit data. These two values (address and data) are obtained from the host processor bus and enabled by the address decoder output.

Data in the Mdatain Holding register, if does not terminate at this device, will always have a high priority for transmission out through bus dataout. This ensures there will be no loss of datain.

The bus decoder will decode the destination ID. If the decoded destination ID is not zero, it decrements the ID and sends the data on. If the decoded destination is zero, it will decode the received data. If the data terminates at that device, it will write the data into the corresponding register. If the read is read with waitstate, data will be put into the bus and the host will wait for the data in the wait state.

A master device decodes the datain assuming a slave access word. Thus, if the REQID matches with its own REQID, the lower byte is assumed to be the offset address into the DPRAM.

The bus slave controller is preferably similar to the master controller described above. A difference will be the bus decoder and control. A slave device will only decode the datain as a master access word (looks for MSB of word (0) to be '0') according to the bus protocol. If it is not, then the word will immediately be forwarded to the next bus device.

Figure 3 shows the relationship between the clock pulses and the dataout.

As can be seen, the dataout is clocked out on the rising edge of the clock pulse, and is only valid when the Mdataout_en signal is high. Similarly on Mdatain, data is clocked out on the rising edge of Mclkin. Data on the Mdatain bus is valid only when the Mdatain_en signal is high.

From this it can be seen that the present invention does not use a bus administrator, thus simplifying the construction, and operation. It allows for minimal control input/output signals. By adopting a master/slave system, each master device can interact with any one or more of the slave devices thus providing an architecture that has greater flexibility, and the possibility of greater use of resources.

Whilst there has been described in the foregoing description a preferred embodiment of the present invention, it will be understood by those skilled in the technology that many variations or modifications in details of design or implementation may be made without departing from the present invention.

The present invention extends to all features disclosed both individually, and in all possible permutations and combinations.

Claims

1) A bus architecture wherein a plurality of devices is connected in a continuous loop, and data is propagated through the devices from a source device to a destination device.

2) A bus architecture as claimed in claim 1, wherein the devices include at least one master device and at least one slave device.

3) A bus architecture as claimed in claim 2, wherein there a first number of master devices, and a second number of slave devices.

4) A bus architecture as claimed in claim 3, wherein the first number and the second number are linked.

5) A bus architecture as claimed in claim 3, wherein the first number and the second number are different.

6) A bus architecture as claimed in claim 1, wherein the plurality of devices is directly connected to the continuous loop.

7) A bus architecture as claimed in claim 1, wherein the propagated data terminates at the destination device.

8) A bus architecture as claimed in claim 6, wherein the propogated data terminates at the destination device.

9) A bus architecture as claimed in claim 1, wherein the data can be sent over a plurality of signal lines.

10) A bus architecture as claimed in claim 8, wherein the data can be sent of a plurality of signal lines.

11) A bus architecture as claimed in claim 2, wherein each master device is capable of acting as a slave device.

12) A bus architecture including a plurality of master devices and a plurality of slave devices, all master devices and slave devices being connected to each other in a continuous loop.

13) A bus architecture as claimed in claim 12, wherein all devices are directly connected to the continuous loop.

14) A bus architecture as claimed in claim 13, wherein the devices include at least one master device and at least one slave device.

15) A bus architecture as claimed in claim 14, wherein there are a first number of master devices, and a second number of slave devices.

16) A bus architecture as claimed in claim 15, wherein the first number and the second number are linked.

17) A bus architecture as claimed in claim 15, wherein the first number and the second number are different.

18) A bus architecture as claimed in claim 12, wherein data is propagated through the devices from a source device to a destination device, and terminates at the destination device.

19) A bus architecture as claimed in claim 18, wherein the data can be sent over a plurality of signal lines.

20) A bus architecture as claimed in claim 12, wherein the bus is a single bus.

21) A bus architecture including a plurality of master devices and a plurality of slave devices connected in a continuous loop, the continuous loop including a plurality of signal lines, each master device being able to communicate with any or all of the slave devices.

22) A bus architecture as claimed in claim 21, wherein each of the master devices can communicate with more than one slave device at any one time.

23) A bus architecture as claimed in claim 21, wherein there are a first number of master devices, and a second number of slave devices.

24) A bus architecture as claimed in claim 23, wherein the first number and the second number are linked.

25) A bus architecture as claimed in claim 23, wherein the first number and the second number are different.

26) A bus architecture as claimed in claim 21, wherein the plurality of devices is directly connected to the continuous loop.

27) A bus architecture as claimed in claims 21, wherein data is propagated through the devices from a source device to a destination device, and terminates at the destination device.

28) A bus architecture as claimed in claim 21, wherein each master device is capable of acting as a slave device.

29) A bus communication protocol, the bus having an architecture including a first number of master devices and a second number of slave devices all connected in a continuous loop, wherein a master access word is sent by a master device, and a slave access word is sent by a slave device only in response to a request from the master device.

30) A bus communication protocol as claimed in claim 29, wherein the request generates responses from a plurality of slave devices.

31) A bus communication protocol as claimed in claim 29, wherein the master access word is sent as a frame of at least one word depending on whether read or write access is intended.

32) A bus communication protocol as claimed in claim 31, wherein for a read access there is at least one word, and for a write access the frame is at least two consecutive words.

33) A bus communication protocol as claimed claim 29, wherein each word is propagated through the master and slave devices from a source device to a destination device, and terminates at the destination device.

34) A bus communication protocol as claimed in claim 32, wherein each master access word includes access information, requestor identification, destination identification, an offset address of the destination, a signifier for read or write access, and a page address of the destination.

35) A bus communication protocol as claimed in claim 34, wherein for a write access a payload is included as a further word.

36) A bus communication protocol as claimed in claim 34, wherein a response frame includes at least one word having a response identification, the requestor identification, the offset address of the response, and a response payload.

37) A bus communication protocol as claimed in claim 34, wherein the access information is at least one access bit.

38) A bus communication protocol as claimed in claim 29, wherein a master device commands a slave device to enter a mode to provide a periodic read-out, the slave device remaining in the mode until turned off by the master device.

39) A bus communication protocol as claimed in claim 38, wherein a plurality of the first number of master devices can command the slave device to provide a plurality of periodic read-outs.

40) A bus communication protocol as claimed in claim 38, wherein the slave device can respond to other commands from other master devices when in the mode.

41) A bus communication protocol as claimed in claim 29, wherein the master devices and the slave devices each have an identity space.

42) A bus communication protocol as claimed in claim 34, wherein upon receipt the destination ID is decoded and, if the decoded destination identification is not zero, the destination identification is decremented and the data sent on.

43) A bus communication protocol as claimed in claim 34, wherein upon receipt the destination identification is decoded and, if the decoded destination is zero, it will decode the received data.

44) A bus communication protocol as claimed in claim 43, wherein if the data terminates at that device, it will write the data into the corresponding register.

45) A bus communication protocol as claimed in claim 43, wherein if the read is read with wait state, data will be put into the bus and the host will wait for the data in the wait state.

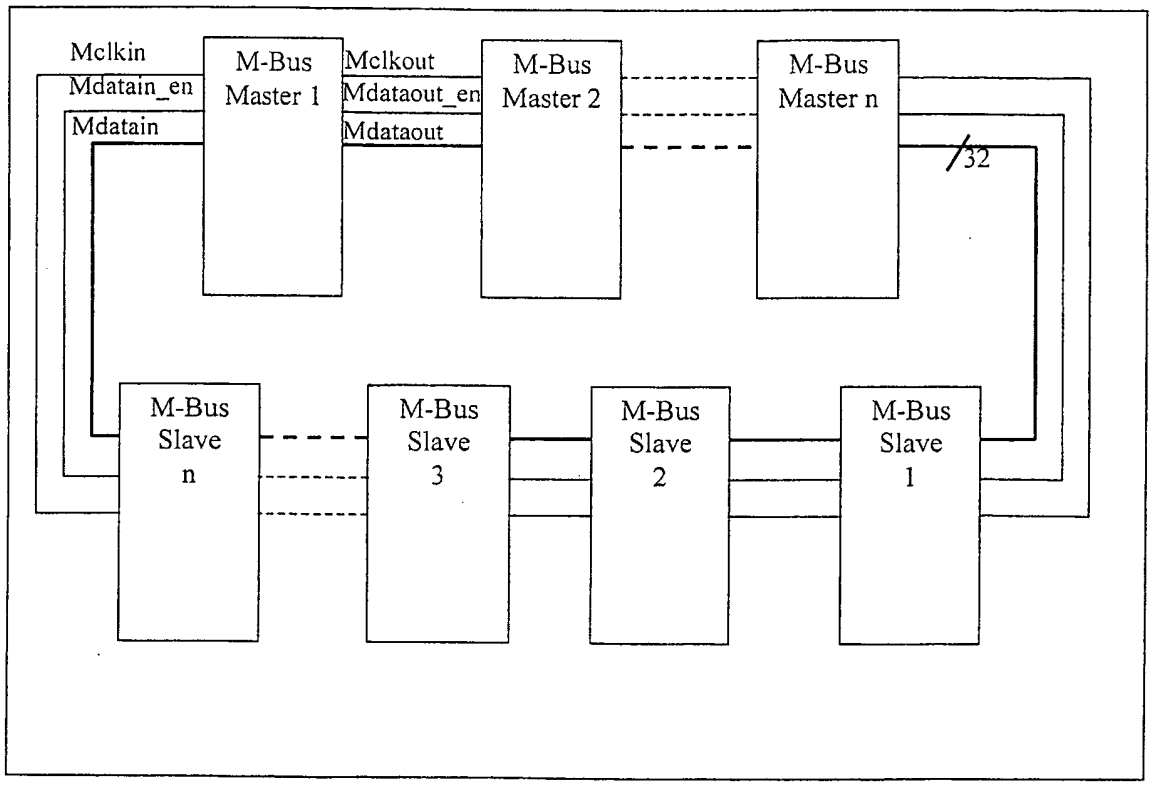
Mclkin
Mdatain_en
Mdatain
M-Bus Master 1
Mclkout
Mdataout_en
Mdataout
M-Bus Master 2
M-Bus Master n
32
M-Bus Slave n
M-Bus Slave 3
M-Bus Slave 2
M-Bus Slave 1

Figure 1

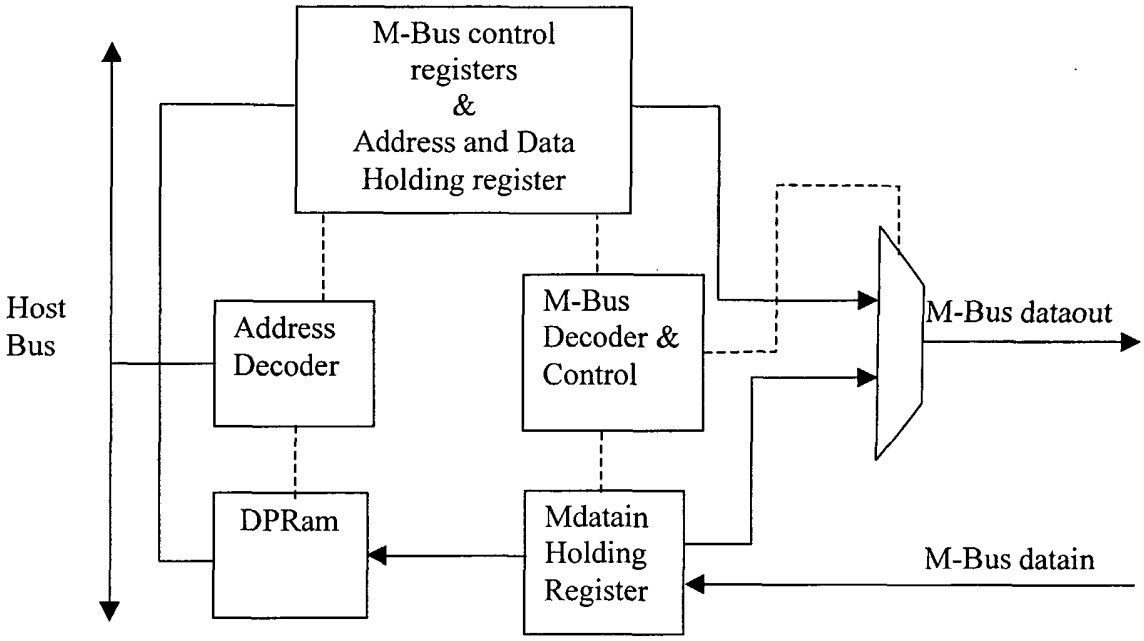
M-Bus control registers & Address and Data Holding register
Host Bus
Address Decoder
M-Bus Decoder & Control
M-Bus dataout
DPRam
Mdatain Holding Register
M-Bus datain

Figure 2

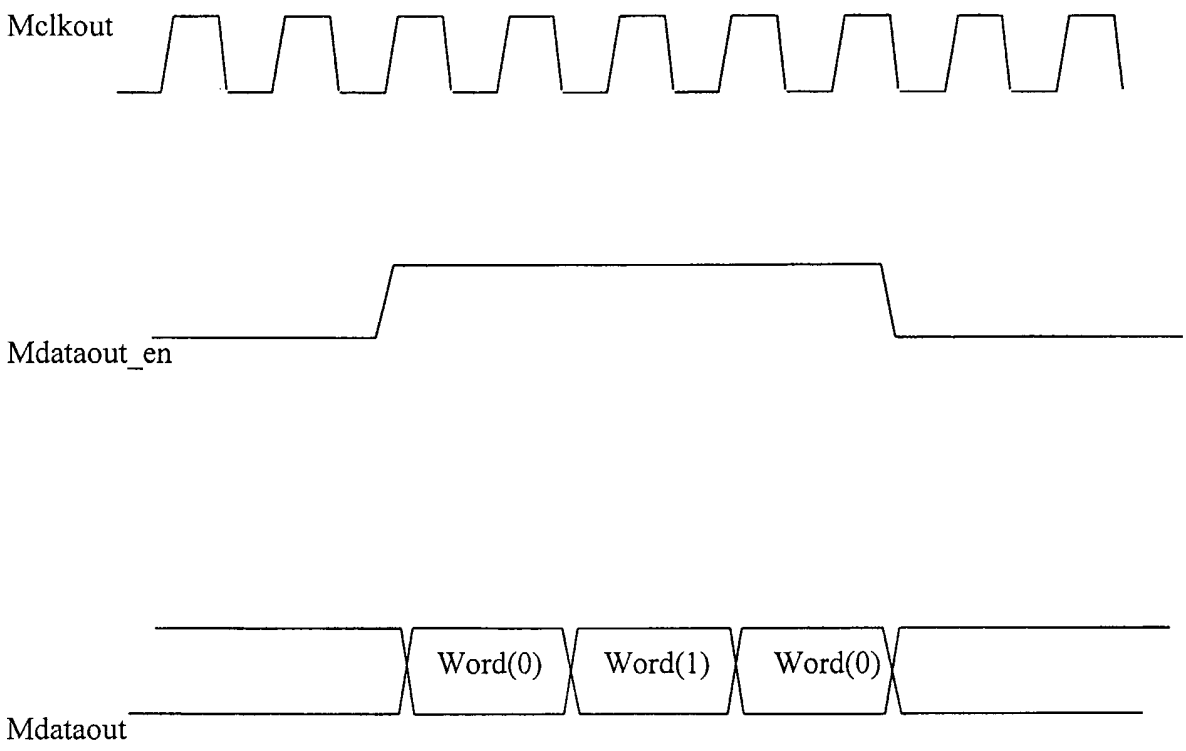

Figure 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/01327

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :G06F 13/14, 13/42; H04L 12/28
US CL :710/305, 105; 370/400
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 370/401-406; 709/251

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

STN

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,091,705 A (REGULA) 18 July 2000, abstract, Figure 1a, col. 2, line 42 - col. 4, line 65.	1-30, 33, 41-43NO
A	US 6,134,647 A (ACTON et al) 17 October 2000, abstract.	1-45
A	US 6,134,617 A (WEBER) 17 October 2000, abstract.	1-45
A	US 5,483,535 A (McMILLEN et al) 09 January 1996, abstract.	1-45
A	US 5,388,223 A (GUTHRIE et al) 07 February 1995, abstract.	1-45
A	US 5,206,857 A (FARLEIGH) 27 April 1993, abstract.	1-45

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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International application No.
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4,937,811 A (HARRIS) 26 June 1990, abstract.	1-45
A	US 4,677,614 A (CIRCO) 30 June 1987, abstract.	1-45
A	US 4,615,029 A (HU et al) 30 September 1986, abstract.	1-45