(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 June 2017 (29.06.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/111775 A1

(51) International Patent Classification:
H01L 23/12 (2006.01) *H01L 25/07* (2006.01)

(21) International Application Number:
PCT/US2015/000206

(22) International Filing Date:
23 December 2015 (23.12.2015)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95054 (US).

(72) Inventors: **MEHANDRU, Rishabh**; 4606 SW 42nd Place, Portland, OR 97221 (US). **NELSON, Don, W.**; 16985 SW Blackberry Lane, Beaverton, OR 97007 (US). **JUN, Kimin**; 1879 NW 193rd Avenue, Unit 203, Hillsboro, OR 97006 (US). **MORROW, Patrick**; 6158 NW Landing Drive, Portland, OR 97229 (US).

(74) Agent: **RAYMOND, Jonathan, R.**; Finch & Maloney PLLC, c/o CPA Global, P.O. Box 52020, Minneapolis, MN 55402 (US).

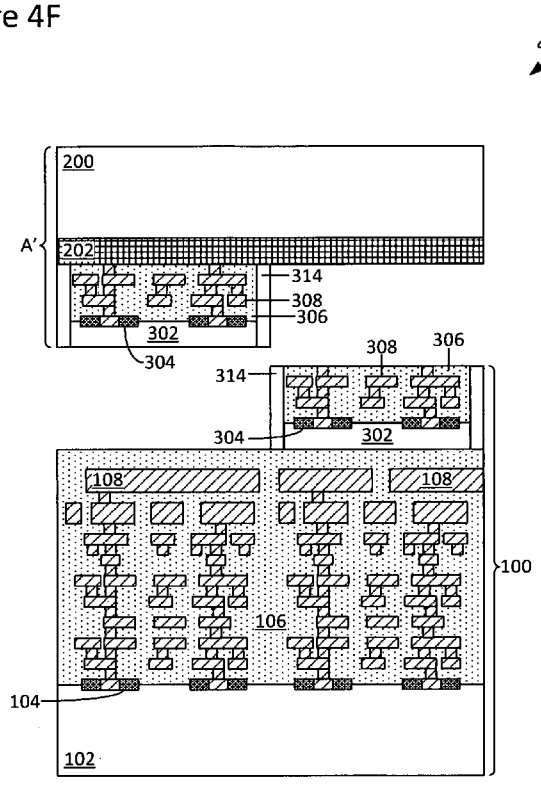
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,

[Continued on next page]

(54) Title: BACK-END REPEATER ELEMENT INTEGRATION TECHNIQUES

Figure 4F



(57) Abstract: Techniques are disclosed for integrating a back-end repeater device with an integrated circuit (IC) chip or die. In accordance with some embodiments, a separately formed repeater device may undergo a flip-and-bond process through which the repeater device may be coupled, for example, directly with an upper back-end-of-line (BEOL) interconnect layer (or layers) of a host IC, local (or otherwise proximate) to a frontside power source or backside power source, as the case may be. In still other embodiments, a host IC may undergo a backside reveal process through which backside interconnects are revealed, and the repeater device may be coupled directly therewith, local (or otherwise proximate) to a given power source. Thus, the separately formed repeater layer can receive its power from a proximate power source, thereby avoiding routing of power supply signals through intervening interconnects from an underlying or otherwise distal device layer.

WO 2017/111775 A1

SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

BACK-END REPEATER ELEMENT INTEGRATION TECHNIQUES

BACKGROUND

Repeaters and line drivers are signal amplifying devices that are commonly used to drive or otherwise propagate signals along lengthy conductors to ensure that the magnitude of the signal acquired at the receiving end is sufficiently strong. In the context of semiconductor interconnects, signal drivers are located all the way down at the semiconductor surface below a given interconnect and are expected to drive the electrical signals the entire length of the above interconnect.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A illustrates a cross-sectional view of an integrated circuit (IC) including an integrated repeater device configured in accordance with an embodiment of the present disclosure.

Figure 1B illustrates a cross-sectional view of an IC including an integrated repeater device configured in accordance with another embodiment of the present disclosure.

Figure 2A illustrates a cross-sectional view of an IC including an integrated repeater device configured in accordance with another embodiment of the present disclosure.

Figure 2B illustrates a cross-sectional view of an IC including an integrated repeater device configured in accordance with another embodiment of the present disclosure.

Figure 3 illustrates a plan view of an example alignment of a repeater device with landing pad portions associated with interconnects of a host IC, in accordance with an embodiment of the present disclosure.

Figures 4A–4F illustrate an IC fabrication process flow for forming an IC, in accordance with an embodiment of the present disclosure.

Figure 5 illustrates a computing system implemented with integrated circuit structures or devices formed using the disclosed techniques in accordance with an example embodiment.

These and other features of the present embodiments will be understood better by reading the following detailed description, taken together with the figures herein described. In the drawings, each identical or nearly identical component that is illustrated in various figures may be represented by a like numeral. For purposes of clarity, not every component may be labeled in every drawing. Furthermore, as will be appreciated, the figures are not necessarily drawn to scale or intended to limit the described embodiments to the specific configurations shown. For instance, while some figures generally indicate straight lines, right angles, and smooth surfaces,

an actual implementation of the disclosed techniques may have less than perfect straight lines and right angles, and some features may have surface topography or otherwise be non-smooth, given real-world limitations of fabrication processes. In short, the figures are provided merely to show example structures.

DETAILED DESCRIPTION

Techniques are disclosed for integrating a back-end repeater device with an integrated circuit (IC) chip or die. One embodiment of the present disclosure includes a separately manufactured repeater that is electrically coupled at a given upper interconnect layer (or layers) to locally boost the back-end signal in those layer(s). Power to the repeater can be provisioned from either of a nearby frontside power source or backside power source, as the case may be, rather than from the semiconductor layer, thereby avoiding use of routing resources through intervening interconnect layers. In accordance with some embodiments, the separately manufactured repeater device may be coupled directly to an upper back-end-of-line (BEOL) interconnect layer of a host IC by a flip-and-bond process, local or otherwise proximate to a frontside power source of the host IC. In still other embodiments, a host IC may undergo a backside reveal process through which backside interconnects are revealed, and the repeater device may be coupled directly therewith, local or otherwise proximate to a backside power source. Numerous configurations and variations will be apparent in light of this disclosure.

General Overview

Typical back-end interconnects are disposed above the transistors of the semiconductor or so-called device layer of a host IC. The interconnects, which can be metal or other electrically conductive lines, for example, may be disposed in one or more so-called interconnect layers, with vias connecting the lines of the device layer and/or different interconnect layers. One or more insulating materials or air gaps may separate the lines and vias. The interconnect layers are normally referred to by number (e.g., metal layer 0, metal layer 1, metal layer 2, and so on), increasing with each consecutive back-end-of-line (BEOL) layer progressing away from the underlying device layer. Electrical signals from the device layer are transported through a given interconnect (or plurality of interconnects) to an intended destination of the host IC (e.g., such as an electrode or device contact at the IC frontside or backside surface). Electrical signals destined for upper interconnect layers, such as BEOL metal layers 8 or 9, for example, may weaken as they travel through various intervening interconnect layers. Thus, such signals can benefit from being strengthened using repeaters. With existing IC architectures, however, back-end repeaters are deployed at the semiconductor layer, which may not be sufficient to boost a signal at upper

interconnect layers. In addition, even if a repeater were to be simply provisioned local to a given upper layer, such a configuration would call for routing not only the signal being boosted, but also power signals (V_{cc} and V_{ss}) to the repeater from all the way down at the device layer of the semiconductor surface. Such a configuration, therefore, would consume routing resources (i.e., space within a given IC) that might be better used for routing other conductors of the IC being fabricated.

Thus, and in accordance with some embodiments of the present disclosure, techniques are disclosed for integrating a back-end repeater device with an integrated circuit (IC) chip or die. One example embodiment includes a separately manufactured repeater that is electrically coupled at a given upper BEOL metal layer (or layers) to locally boost the back-end signal at those upper layer(s). Power to the repeater (e.g., V_{cc} and V_{ss}) can be provisioned from either of a nearby frontside power source or backside power source, as the case may be, rather than from the semiconductor layer, thereby avoiding use of routing resources between the semiconductor layer and the repeater. In accordance with some embodiments, a repeater device configured as described herein may undergo a flip-and-bond process through which the repeater device may be coupled, for example, directly with a BEOL metal layer (e.g., metal layer 8 or 9) of a host IC, local (or otherwise proximate) to a frontside power source. In accordance with some other embodiments, a host IC may undergo a backside reveal process through which backside interconnects are revealed, and the repeater device may be coupled directly therewith, local (or otherwise proximate) to a backside power source.

In accordance with some embodiments, electrical connection of an integrated repeater element directly at an upper metal layer, such as BEOL metal layers 8 and 9 (generally referred to herein as Metal8 and Metal9 layers, respectively), may serve to boost or otherwise enhance back-end signal locally. Given that such end-of-line Metal8/Metal9 layers are relatively close to the power supply source of a given host IC, in some cases, an integrated repeater of this configuration may simplify back-end routing requirements, freeing up considerable routing resources and thus allowing for more functionality to be provided on the host IC chip or die. In some instances, in this type of configuration, back-end lithography constraints that otherwise would result from typical repeater routing requirements may be eased, reducing fabrication cost. In some cases, resistance-capacitance (RC) delay may be reduced, speeding up digital signal propagation and communications in critical circuits using repeaters provided as described herein.

Although reference to Metal8/Metal9 layers is made herein with respect to some example embodiments, note that any interconnect configuration having a plurality of interconnect layers can employ the techniques provided herein, wherein upper or end-of-line interconnect layers are bonded with a repeater layer. Further note that once a repeater layer is installed in a given

location of an interconnect stack, additional interconnect layers then can be further fabricated on that repeater layer, so as to provide one or more intermediate repeater layers, as well as end-of-line repeaters.

In accordance with some embodiments, use of the disclosed techniques may be detected, for example, by transmission electron microscopy (TEM), scanning electron microscopy (SEM), or other visual inspection of a given IC having an integrated repeater layer connected directly with a Metal8/Metal9 layer (or other intermediate or upper interconnect layer of a host IC) or connected directly with a backside interconnect, as described herein.

Structure and Operation

Figure 1A illustrates a cross-sectional view of an integrated circuit (IC) 100a including an integrated repeater device 300 configured in accordance with an embodiment of the present disclosure. Figure 1B illustrates a cross-sectional view of an IC 100a including an integrated repeater device 300 configured in accordance with another embodiment of the present disclosure. Figure 2A illustrates a cross-sectional view of an IC 100b including an integrated repeater device 300 configured in accordance with another embodiment of the present disclosure. Figure 2B illustrates a cross-sectional view of an IC 100b including an integrated repeater device 300 configured in accordance with another embodiment of the present disclosure. For consistency and ease of understanding of the present disclosure, ICs 100a and 100b hereinafter may be collectively referred to generally as an IC 100, except where separately enumerated.

As can be seen from the figures, IC 100 includes a semiconductor substrate 102 and a transistor device layer 104 disposed adjacent (e.g., on or otherwise over) semiconductor substrate 102. Semiconductor substrate 102 may have any of a wide range of configurations. For instance, in some embodiments, semiconductor substrate 102 may be a bulk semiconductor substrate, a semiconductor-on-insulator (XOI, where X represents a semiconductor material) structure, a semiconductor wafer, or a multi-layered structure. The material composition of semiconductor substrate 102 may be customized, as desired for a given target application or end-use. For instance, in some cases, semiconductor substrate 102 may be formed from any one, or combination, of silicon (Si), germanium (Ge), and silicon-germanium (SiGe), among others. Transistor device layer 104 can include any quantity and any type(s) of transistor devices, as desired for a given target application or end-use. Other suitable materials and configurations for semiconductor substrate 102 and transistor device layer 104 will depend on a given application and will be apparent in light of this disclosure.

IC 100 further includes one or more dielectric layers 106 and one or more interconnects 108. In accordance with some embodiments, a given dielectric layer 106 may be disposed

adjacent (e.g., on or otherwise over) transistor device layer 104, and one or more interconnects 108 may be disposed therein, such as is generally shown by IC 100a in Figures 1A–1B. In accordance with some other embodiments, one or more dielectric layers 106 may be disposed adjacent (e.g., on or otherwise over) a backside of semiconductor substrate 102, and one or more interconnects 108 may be disposed therein, such as is generally shown by IC 100b in Figures 2A–2B.

A given dielectric layer 106 can be formed from any suitable dielectric material(s), as will be apparent in light of this disclosure. For instance, in some cases, a given dielectric layer 106 may be formed from an oxide such as silicon dioxide (SiO_2), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), zirconium dioxide (ZrO_2), tantalum pentoxide (Ta_2O_5), titanium dioxide (TiO_2), or lanthanum oxide (La_2O_3). In some cases, a given dielectric layer 106 may be formed from a carbon (C)-doped oxide. In some cases, a given dielectric layer 106 may be formed from a nitride such as silicon nitride (Si_3N_4) or a carbide such as silicon carbide (SiC). In a more general sense, and in accordance with some embodiments, dielectric layer 106 may be formed from any one, or combination, of the aforementioned materials. Also, the dimensions of a given dielectric layer 106 can be customized as desired for a given target application or end-use. In some cases, a given dielectric layer 106 may be an inter-layer dielectric (ILD).

A given interconnect 108 can be formed from any suitable electrically conductive material(s), as will be apparent in light of this disclosure. For instance, in some cases, a given interconnect 108 may be formed from any one, or combination, of metals, such as copper (Cu), aluminum (Al), tungsten (W), nickel (Ni), cobalt (Co), silver (Ag), gold (Au), titanium (Ti), and tantalum (Ta), among others. Also, the dimensions and geometry (e.g., cross-sectional profile) of a given interconnect 108 can be customized as desired for a given target application or end-use. As discussed below, a given interconnect 108 may include or otherwise be configured to serve as a landing pad 314 (Figure 3) for a given bump connection 312. Other suitable materials and configurations for transistor device layer 104, dielectric layer(s) 106, and interconnect(s) 108 will depend on a given application and will be apparent in light of this disclosure.

In accordance with some embodiments, a repeater device 300 may be integrated in (or otherwise connected with) IC 100. As can be seen from the figures, in some embodiments, repeater device 300 may include a semiconductor substrate 302, a transistor device layer 304 disposed adjacent (e.g., on or otherwise over) semiconductor substrate 302, one or more dielectric layers 306 disposed adjacent (e.g., on or otherwise over) transistor device layer 304, and one or more interconnects 308 disposed within dielectric layer(s) 306. In some instances, repeater device 300 generally may be referred to, in part or in whole, as a repeater chiplet.

As will be appreciated in light of this disclosure, semiconductor substrate 302 may be formed with any of the example materials and configurations discussed above, for instance, with respect to semiconductor substrate 102. Also, as with transistor device layer 104 (discussed above), transistor device layer 304 may include any quantity and type(s) of transistor devices, as desired for a given target application or end-use, in accordance with some embodiments. As will be further appreciated in light of this disclosure, dielectric layer(s) 306 and interconnect(s) 308 may be formed with any of the example materials and configurations discussed above, for instance, with respect to dielectric layer(s) 106 and interconnect(s) 108, in accordance with some embodiments. In some cases, repeater device 300 may include interconnects 308 of the same material composition, whereas in some other cases, interconnects 308 of different material composition may be provided. Other suitable materials and configurations for repeater device 300 and its constituent components will depend on a given application and will be apparent in light of this disclosure.

In accordance with some embodiments, repeater device 300 further may include or otherwise be provided with one or more bump connections 312. Bump connection(s) 312 can be formed from any suitable electrically conductive material(s), as will be apparent in light of this disclosure, and in some cases may be formed with any of the example materials discussed above, for instance, with respect to interconnect(s) 108 and interconnect(s) 308. Bump connection(s) 312 may be configured to provide electronic contact between a given interconnect 308 of repeater device 300 and a given interconnect 108 of a host IC 100, as well as physical bonding of repeater device 300 with a given interconnect 108 of the host IC 100. In some instances, bump connection(s) 312 may be pre-fabricated on interconnect(s) 308 of repeater device 300 during processing and then aligned and connected with desired interconnect(s) 108 (or other IC chip or die wiring) during subsequent processing (e.g., such as during a process flow like that described below, for instance, with respect to Figures 4A–4F). In some cases, a plurality of interconnects 308 of repeater device 300 may be connected with a plurality of interconnects 108 of a host IC 100 (e.g., such as is generally shown in each of Figures 1B and 2B). Numerous suitable configurations and variations will be apparent in light of this disclosure.

In accordance with some embodiments, connection of repeater device 300 with IC 100 may be provided by the bonding of one or more bump connections 312 with one or more landing pad portions 112 associated with interconnects 108 of IC 100. For instance, consider Figure 3, which illustrates a plan view of an example alignment of a repeater device 300 with landing pad portions 112 associated with interconnects 108 of a host IC 100, in accordance with an embodiment of the present disclosure. A given bump connection 312 may be configured to land substantially aligned (e.g., coarsely aligned or otherwise aligned within a given tolerance) with a

corresponding landing pad portion 112. Connection of a given bump connection 312 with a given landing pad 314 may be provided by any suitable standard, custom, or proprietary technique(s), as will be apparent in light of this disclosure.

In accordance with some embodiments, a repeater device 300 may be connected with interconnect(s) 108 disposed over a frontside of semiconductor substrate 102, such as is generally shown by IC 100a in Figures 1A–1B. In some cases, a repeater device 300 may be connected with frontside interconnect(s) 108, for example, disposed at a back-end-of-line (BEOL) metal layer 8 (generally referred to as a Metal8 layer). In some other cases, a repeater device 300 may be connected with frontside interconnect(s) 108, for example, disposed at a BEOL metal layer 9 (generally referred to as a Metal9 layer). The present disclosure is not intended to be limited only to connection of a repeater device 300 at Metal8/Metal9 layers of a host IC 100, however, as in a more general sense, and in accordance with some embodiments, a repeater device 300 may be connected at any given metal layer, especially any given upper metal layer (e.g., BEOL metal layers 5, 6, 7, 8, 9, 10, or higher) of a host IC 100, as desired for a given target application or end-use. In some cases, a repeater device 300 may be connected, for example, with frontside interconnect(s) 108 disposed at a topmost BEOL metal layer of a host IC 100. In some other cases, a repeater device 300 may be connected, for example, with frontside interconnect(s) 108 disposed at a BEOL metal layer that is directly subjacent a topmost BEOL metal layer of a host IC 100 (i.e., a penultimate BEOL metal layer). In some other cases, a repeater device 300 may be connected, for example, with frontside interconnect(s) 108 disposed at a BEOL metal layer that is not directly superjacent transistor device layer 104 of a host IC 100 and not the topmost or penultimate BEOL metal layer. In some instances, a combination of any one or more of the aforementioned configurations may be employed. Numerous other such configurations and variations will be apparent in light of this disclosure.

In accordance with some other embodiments, a repeater device 300 may be connected with interconnect(s) 108 disposed over a backside of semiconductor substrate 102, such as is generally shown by IC 100b in Figures 2A–2B. In configurations such as that of IC 100b, a power supply may be disposed over the backside semiconductor substrate 102, and, using a back-side reveal process, a repeater device 300 may be connected with backside interconnect(s) 108 such that V_{cc} and V_{ss} may be delivered from the backside of semiconductor substrate 102 to the local repeater device 300. Numerous suitable configurations and variations for connection of repeater device 300 with a given IC 100 will be apparent in light of this disclosure.

As previously noted, in accordance with some embodiments, repeater device 300 may be manufactured separately from and subsequently connected with an IC 100. In some instances, in the connection process (e.g., which may involve a flip-and-bond process), the physical

orientation of repeater device 300 may be inverted. Thus, as generally shown in Figures 1A–1B, for example, repeater device 300 may be upside-down, such that transistor device layer 304 is located physically above dielectric layer(s) 306 and interconnect(s) 308, and semiconductor substrate 302 is located physically above transistor device layer 304. Contrariwise, consider the repeater device 300 of each of Figures 2A and 2B, which does not have an inverted orientation. Numerous suitable configurations and variations will be apparent in light of this disclosure.

Methodology

Figures 4A–4F illustrate an integrated circuit (IC) fabrication process flow for forming an IC, in accordance with an embodiment of the present disclosure. The process flow of Figures 4A–4F can be used, for example, in integrating a repeater device 300 with an IC 100, in accordance with an embodiment of the present disclosure. In a more general sense, and in accordance with some embodiments, the process flow of Figures 4A–4F can be utilized, in part or in whole, to attach a repeater device 300 (e.g., repeater chiplet) to a semiconductor chip or die.

The process flow may begin as in Figure 4A, which illustrates a cross-sectional view 402 of a repeater device 300 configured in accordance with an embodiment of the present disclosure. In this example case, repeater device 300 includes two neighboring regions of transistor device layer(s) 304, dielectric layer(s) 306, and interconnect(s) 308 disposed over a commonly shared semiconductor substrate 302. The present disclosure is not intended to be so limited, however, as in other embodiments, a lesser quantity (e.g., one) or a greater quantity (e.g., three, four, five, or more) of regions of repeater chiplet elements may be disposed over a commonly shared semiconductor substrate 302, as desired. In some cases in which multiple repeater chiplets are present, neighboring chiplets may be physically separated, in part or in whole, by a scribe trench 314, which may be formed using any suitable standard, custom, or proprietary technique(s), as will be apparent in light of this disclosure.

The process flow may continue as in Figure 4B, which illustrates a cross-sectional view 404 of the repeater device 300 of Figure 4A after flipping and bonding with a temporary carrier substrate 200 via an adhesive layer 202, in accordance with an embodiment of the present disclosure. Adhesive layer 202 can be any suitable temporary adhesive bonding material(s), such as, for example, a solvent-release adhesive, a laser-release adhesive, or a thermal-release adhesive, among others. Bonding of repeater device 300 with carrier substrate 200 may be performed using any suitable standard, custom, or proprietary technique(s), as will be apparent in light of this disclosure. For consistency and ease of understanding of the present disclosure, the combination of a repeater device 300 and a carrier substrate 200 (as bonded by an adhesive layer 202) generally may be referred to hereinafter as Portion A.

The process flow may continue as in Figure 4C, which illustrates a cross-sectional view 406 of the Portion A of Figure 4B after thinning semiconductor substrate 302 of repeater device 300, in accordance with an embodiment of the present disclosure. Thinning may be performed via any suitable standard, custom, or proprietary technique(s), as will be apparent in light of this disclosure. In some cases, any one, or combination, of a chemical-mechanical planarization (CMP) process and an etch-and-clean process may be utilized. In an example case, semiconductor substrate 302 may be thinned down until scribe trench 314 is reached.

The process flow may continue as in Figure 4D, which illustrates a cross-sectional view 408 of the Portion A of Figure 4C after inversion and alignment with an IC 100, in accordance with an embodiment of the present disclosure. As discussed above, bump connection(s) 312 of repeater device 300 may be made to substantially align with landing pad portion(s) 112 of interconnect(s) 108 of IC 100 for bonding therewith, in accordance with some embodiments.

The process flow may continue as in Figure 4E, which illustrates a cross-sectional view 410 of the Portion A of Figure 4D after bonding with IC 100, in accordance with an embodiment of the present disclosure. As discussed above, bump connection(s) 312 of repeater device 300 may be bonded with corresponding landing pad portion(s) 112 of interconnect(s) 108 of IC 100 using any suitable standard, custom, or proprietary technique(s), as will be apparent in light of this disclosure.

The process flow may continue as in Figure 4F, which illustrates a cross-sectional view 412 of the Portion A of Figure 4E after separation of a repeater device 300 therefrom, in accordance with an embodiment of the present disclosure. As can be seen, a repeater device 300 that has been bonded with IC 100 may be released from adhesive layer 202 and dislodged from carrier substrate 200 along one or more scribe trenches 314. Additional repeater devices 300, if any, may remain bonded with carrier substrate 200, and the resultant Portion A′ may be made available for optional reuse in additional processing. For instance, Portion A′ optionally may be used in another round of fabrication according to the process flow of Figures 4A–4F (e.g., in attaching another repeater device 300 or other repeater chiplet to a semiconductor chip or die) or any other suitable fabrication process, as will be apparent in light of this disclosure.

At this point in the process flow, there are a wide range of options for how to optionally proceed with further fabrication. For instance, in accordance with some embodiments, additional layer(s) of metal or dielectric materials (or both) can be formed over the available topography, bringing the constituent metal and/or dielectric layers of IC 100 (e.g., the non-repeater die) up to and, optionally, beyond the top surface of repeater device 300 (e.g., resulting in an IC more or less similar to IC 100 of Figures 1A or 1B). Any desired quantity of adjacent layers of interconnects 108 and further formation of dielectric layer(s) 106 may be provided.

Furthermore, it should be noted that, as generally shown in Figure 4F, repeater device 300 may be coupled with IC 100 in a top-side up (e.g., right-side up) orientation, such that semiconductor substrate 302 is physically positioned beneath transistor device layer 304), but the present disclosure is not intended to be so limited. For instance, as generally shown in Figures 1A and 1B, repeater device 300 may be coupled with IC 100 in a top-side down (e.g., upside down) orientation, such that transistor device layer 304 is physically positioned beneath semiconductor substrate 302. To that end, in the example context of the process flow of Figures 4A–4F, a given repeater device 300 could be transferred to a host IC 100 instead without use of a temporary carrier substrate 200 (or adhesive layer 202), in accordance with another embodiment. This would allow repeater device 300 to be directly coupled with IC 100, such that semiconductor substrate 302 resides over transistor device layer 304. In a more general sense, and in accordance with some embodiments, repeater device 300 can be coupled with a given host IC 100 in any given orientation, as desired for a given target application or end-use. Numerous suitable configurations and variations will be apparent in light of this disclosure.

Example System

Figure 5 illustrates a computing system 1000 implemented with integrated circuit structures or devices formed using the disclosed techniques in accordance with an example embodiment. As can be seen, the computing system 1000 houses a motherboard 1002. The motherboard 1002 may include a number of components, including, but not limited to, a processor 1004 and at least one communication chip 1006, each of which can be physically and electrically coupled to the motherboard 1002, or otherwise integrated therein. As will be appreciated, the motherboard 1002 may be, for example, any printed circuit board, whether a main board, a daughterboard mounted on a main board, or the only board of system 1000, etc. Depending on its applications, computing system 1000 may include one or more other components that may or may not be physically and electrically coupled to the motherboard 1002. These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the components included in computing system 1000 may include one or more integrated circuit structures or devices formed using the disclosed techniques in accordance with an example embodiment. In some embodiments, multiple functions can be integrated into one or

more chips (e.g., for instance, note that the communication chip 1006 can be part of or otherwise integrated into the processor 1004).

The communication chip 1006 enables wireless communications for the transfer of data to and from the computing system 1000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including, but not limited to, Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing system 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1004 of the computing system 1000 includes an integrated circuit die packaged within the processor 1004. In some embodiments, the integrated circuit die of the processor includes onboard circuitry that is implemented with one or more integrated circuit structures or devices formed using the disclosed techniques, as variously described herein. The term "processor" may refer to any device or portion of a device that processes, for instance, electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1006 also may include an integrated circuit die packaged within the communication chip 1006. In accordance with some such example embodiments, the integrated circuit die of the communication chip includes one or more integrated circuit structures or devices formed using the disclosed techniques as described herein. As will be appreciated in light of this disclosure, note that multi-standard wireless capability may be integrated directly into the processor 1004 (e.g., where functionality of any chips 1006 is integrated into processor 1004, rather than having separate communication chips). Further note that processor 1004 may be a chip set having such wireless capability. In short, any number of processor 1004 and/or communication chips 1006 can be used. Likewise, any one chip or chip set can have multiple functions integrated therein.

In various implementations, the computing device 1000 may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, a digital video recorder, or any other electronic device that processes data or employs one or more integrated circuit structures or devices formed using the disclosed techniques, as variously described herein.

Further Example Embodiments

The following examples pertain to further embodiments, from which numerous permutations and configurations will be apparent.

Example 1 is an integrated circuit including: a first semiconductor substrate; a first transistor device layer disposed over the first semiconductor substrate; first and second interconnects disposed over the first semiconductor substrate; and a repeater device including: a second semiconductor substrate; a second transistor device layer disposed on the second semiconductor substrate; a dielectric layer disposed on the second transistor device layer; and a first metal line disposed within the dielectric layer and in direct electronic contact with the first and second interconnects.

Example 2 includes the subject matter of any of Examples 1 and 3–12, wherein the first and second interconnects are disposed over a frontside of the first semiconductor substrate.

Example 3 includes the subject matter of any of Examples 1–2 and 4–12, wherein the first and second interconnects are disposed over a frontside of the first semiconductor substrate, over the first transistor device layer, at a back-end-of-line (BEOL) metal layer 8 of the integrated circuit.

Example 4 includes the subject matter of any of Examples 1–3 and 5–12, wherein the first and second interconnects are disposed over a frontside of the first semiconductor substrate, over the first transistor device layer, at a back-end-of-line (BEOL) metal layer 9 of the integrated circuit.

Example 5 includes the subject matter of any of Examples 1–4 and 6–12, wherein the first and second interconnects are disposed over a frontside of the first semiconductor substrate, over the first transistor device layer, at a topmost back-end-of-line (BEOL) metal layer of the integrated circuit.

Example 6 includes the subject matter of any of Examples 1–5 and 7–12, wherein the first and second interconnects are disposed over a frontside of the first semiconductor substrate, over the first transistor device layer, at a back-end-of-line (BEOL) metal layer that is directly subjacent a topmost BEOL metal layer of the integrated circuit.

Example 7 includes the subject matter of any of Examples 1–6 and 8–12, wherein the first and second interconnects are disposed over a frontside of the first semiconductor substrate, over the first transistor device layer, at a back-end-of-line (BEOL) metal layer that is not directly superjacent the first transistor device layer of the integrated circuit.

Example 8 includes the subject matter of any of Examples 1–7 and 9–12, wherein the first and second interconnects are disposed over a backside of the first semiconductor substrate.

Example 9 includes the subject matter of any of Examples 1–8 and 10–12, wherein the repeater device further includes a second metal line disposed within the dielectric layer.

Example 10 includes the subject matter of Example 9, wherein the first and second metal lines are of different material composition.

Example 11 includes the subject matter of any of Examples 1–10 and 12, wherein direct electronic contact between the first metal line of the repeater device and the first and second interconnects is provided by an electrically conductive bump connection.

Example 12 includes the subject matter of any of Examples 1–11, wherein: the first interconnect includes a first landing pad portion with which the first metal line of the repeater device is in direct electronic contact; and the second interconnect includes a second landing pad portion with which the first metal line of the repeater device is in direct electronic contact.

Example 13 is a method of fabricating an integrated circuit, the method including: providing a repeater device including: a first semiconductor substrate; a first transistor device on the first semiconductor substrate; a dielectric layer on the first transistor device layer; and a first metal line within the dielectric layer; and bonding the repeater device with the integrated circuit, the integrated circuit including: a second semiconductor substrate; a second transistor device layer disposed over the second semiconductor substrate; and first and second interconnects disposed over the second semiconductor substrate and in direct electronic contact with the first metal line of the repeater device.

Example 14 includes the subject matter of any of Examples 13 and 15–24, wherein the first and second interconnects are disposed over a frontside of the first semiconductor substrate.

Example 15 includes the subject matter of any of Examples 13–14 and 16–24, wherein the first and second interconnects are disposed over a frontside of the second semiconductor substrate, over the second transistor device layer, at a back-end-of-line (BEOL) metal layer 8 of the integrated circuit.

Example 16 includes the subject matter of any of Examples 13–15 and 17–24, wherein the first and second interconnects are disposed over a frontside of the second semiconductor substrate, over the second transistor device layer, at a back-end-of-line (BEOL) metal layer 9 of the integrated circuit.

Example 17 includes the subject matter of any of Examples 13–16 and 18–24, wherein the first and second interconnects are disposed over a frontside of the first semiconductor substrate, over the first transistor device layer, at a topmost back-end-of-line (BEOL) metal layer of the integrated circuit.

Example 18 includes the subject matter of any of Examples 13–17 and 19–24, wherein the first and second interconnects are disposed over a frontside of the first semiconductor substrate, over the first transistor device layer, at a back-end-of-line (BEOL) metal layer that is directly subjacent a topmost BEOL metal layer of the integrated circuit.

Example 19 includes the subject matter of any of Examples 13–18 and 20–24, wherein the first and second interconnects are disposed over a frontside of the first semiconductor substrate, over the first transistor device layer, at a back-end-of-line (BEOL) metal layer that is not directly superjacent the first transistor device layer of the integrated circuit.

Example 20 includes the subject matter of any of Examples 13–19 and 21–24, wherein bonding the repeater device with the integrated circuit includes: bonding the repeater device with a temporary carrier substrate; thinning the first semiconductor substrate of the repeater device; bonding the first metal line of the repeater device with the first and second interconnects of the integrated circuit; and separating the temporary carrier substrate from the repeater device.

Example 21 includes the subject matter of Example 20, wherein bonding the repeater device with the temporary carrier substrate is provided via at least one of a solvent-release adhesive layer, a laser-release adhesive layer, and a thermal-release adhesive layer.

Example 22 includes the subject matter of Example 20, wherein in bonding the repeater device with the integrated circuit: a first metal bump of the first metal line of the repeater device is bonded with a first landing pad portion of the first interconnect of the integrated circuit; and a second metal bump of the first metal line of the repeater device is bonded with a second landing pad portion of the second interconnect of the integrated circuit.

Example 23 includes the subject matter of any of Examples 13–22 and 24, wherein the first and second interconnects are disposed over a backside of the second semiconductor substrate.

Example 24 includes the subject matter of Example 23, wherein prior to bonding the repeater device with the integrated circuit, the method further includes: revealing the backside of the second semiconductor substrate so as to expose the first and second interconnects.

Example 25 is an integrated circuit including: a first semiconductor substrate; a first transistor device layer disposed over the first semiconductor substrate; a first dielectric layer disposed over the first transistor device layer; a first plurality of interconnects disposed within the first dielectric layer; and a repeater device bonded with the first plurality of interconnects and

including: a second semiconductor substrate; a second transistor device layer disposed over the second semiconductor substrate; a second dielectric layer disposed over the second transistor device layer; and a second plurality of interconnects disposed within the second dielectric layer and in direct electronic contact with the first plurality of interconnects.

Example 26 includes the subject matter of any of Examples 25 and 27–32, wherein the first plurality of interconnects are disposed over a frontside of the first semiconductor substrate.

Example 27 includes the subject matter of any of Examples 25–26 and 28–32, wherein the first plurality of interconnects are disposed over a frontside of the first semiconductor substrate at a back-end-of-line (BEOL) metal layer 8 of the integrated circuit.

Example 28 includes the subject matter of any of Examples 25–27 and 29–32, wherein the first plurality of interconnects are disposed over a frontside of the first semiconductor substrate at a back-end-of-line (BEOL) metal layer 9 of the integrated circuit.

Example 29 includes the subject matter of any of Examples 25–28 and 30–32, wherein the first plurality of interconnects are disposed over a frontside of the first semiconductor substrate at a topmost back-end-of-line (BEOL) metal layer of the integrated circuit.

Example 30 includes the subject matter of any of Examples 25–29 and 31–32, wherein the first plurality of interconnects are disposed over a frontside of the first semiconductor substrate at a back-end-of-line (BEOL) metal layer that is directly subjacent a topmost BEOL metal layer of the integrated circuit.

Example 31 includes the subject matter of any of Examples 25–30 and 32, wherein the first plurality of interconnects are disposed over a frontside of the first semiconductor substrate at a back-end-of-line (BEOL) metal layer that is not directly superjacent the first transistor device layer of the integrated circuit.

Example 32 includes the subject matter of any of Examples 25–31, wherein the repeater device is bonded with the first plurality of interconnects via at least one electrically conductive bump connection.

Example 33 is an integrated circuit including: a first semiconductor substrate; a first transistor device layer disposed over a frontside of the first semiconductor substrate; a first plurality of interconnects disposed over a backside of the first semiconductor substrate; a repeater device bonded with the first plurality of interconnects and including: a second semiconductor substrate; a second transistor device layer disposed over the second semiconductor substrate; a dielectric layer disposed over the second transistor device layer; and a second plurality of interconnects disposed within the dielectric layer and in direct electronic contact with the first plurality of interconnects.

Example 34 includes the subject matter of Example 33, wherein the repeater device is bonded with the first plurality of interconnects via at least one electrically conductive bump connection.

The foregoing description of example embodiments has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the present disclosure to the precise forms disclosed. Many modifications and variations are possible in light of this disclosure. It is intended that the scope of the present disclosure be limited not by this detailed description, but rather by the claims appended hereto. Future-filed applications claiming priority to this application may claim the disclosed subject matter in a different manner and generally may include any set of one or more limitations as variously disclosed or otherwise demonstrated herein.

CLAIMS

What is claimed is:

1. An integrated circuit comprising:

a first semiconductor substrate;

a first transistor device layer disposed over the first semiconductor substrate;

first and second interconnects disposed over the first semiconductor substrate; and

a repeater device comprising:

a second semiconductor substrate;

a second transistor device layer disposed on the second semiconductor substrate;

a dielectric layer disposed on the second transistor device layer; and

a first metal line disposed within the dielectric layer and in direct electronic contact with the first and second interconnects.

2. The integrated circuit of claim 1, wherein the first and second interconnects are disposed over a frontside of the first semiconductor substrate, over the first transistor device layer, at least one of at a back-end-of-line (BEOL) metal layer 8 and at a BEOL metal layer 9 of the integrated circuit.

3. The integrated circuit of claim 1, wherein the first and second interconnects are disposed over a frontside of the first semiconductor substrate, over the first transistor device layer, at a topmost back-end-of-line (BEOL) metal layer of the integrated circuit.

4. The integrated circuit of claim 1, wherein the first and second interconnects are disposed over a frontside of the first semiconductor substrate, over the first transistor device layer, at a back-end-of-line (BEOL) metal layer that is directly subjacent a topmost BEOL metal layer of the integrated circuit.

5. The integrated circuit of claim 1, wherein the first and second interconnects are disposed over a frontside of the first semiconductor substrate, over the first transistor device layer, at a back-end-of-line (BEOL) metal layer that is not directly superjacent the first transistor device layer of the integrated circuit.

6. The integrated circuit of claim 1, wherein the first and second interconnects are disposed over a backside of the first semiconductor substrate.

7. The integrated circuit of claim 1, wherein the repeater device further comprises a second metal line disposed within the dielectric layer.

8. The integrated circuit of any of claims 1–7, wherein direct electronic contact between the first metal line of the repeater device and the first and second interconnects is provided by an electrically conductive bump connection.

9. The integrated circuit of any of claims 1–7, wherein:

the first interconnect includes a first landing pad portion with which the first metal line of the repeater device is in direct electronic contact; and

the second interconnect includes a second landing pad portion with which the first metal line of the repeater device is in direct electronic contact.

10. A method of fabricating an integrated circuit, the method comprising:

providing a repeater device comprising:

a first semiconductor substrate;

a first transistor device on the first semiconductor substrate;

a dielectric layer on the first transistor device layer; and

a first metal line within the dielectric layer; and

bonding the repeater device with the integrated circuit, the integrated circuit comprising:

a second semiconductor substrate;

a second transistor device layer disposed over the second semiconductor substrate; and

first and second interconnects disposed over the second semiconductor substrate and in direct electronic contact with the first metal line of the repeater device.

11. The method of claim 10, wherein the first and second interconnects are disposed over a frontside of the second semiconductor substrate, over the second transistor device layer, at least one of at a back-end-of-line (BEOL) metal layer 8 and at a BEOL metal layer 9 of the integrated circuit.

12. The method of claim 10, wherein the first and second interconnects are disposed over a frontside of the first semiconductor substrate, over the first transistor device layer, at a topmost back-end-of-line (BEOL) metal layer of the integrated circuit.

13. The method of claim 10, wherein the first and second interconnects are disposed over a frontside of the first semiconductor substrate, over the first transistor device layer, at a back-end-of-line (BEOL) metal layer that is at least one of directly subjacent a topmost BEOL metal layer of the integrated circuit and not directly superjacent the first transistor device layer of the integrated circuit.

14. The method of any of claims 10–13, wherein bonding the repeater device with the integrated circuit comprises:

bonding the repeater device with a temporary carrier substrate;

thinning the first semiconductor substrate of the repeater device;

bonding the first metal line of the repeater device with the first and second interconnects of the integrated circuit; and

separating the temporary carrier substrate from the repeater device.

15. The method of claim 14, wherein bonding the repeater device with the temporary carrier substrate is provided via at least one of a solvent-release adhesive layer, a laser-release adhesive layer, and a thermal-release adhesive layer.

16. The method of claim 14, wherein in bonding the repeater device with the integrated circuit:

a first metal bump of the first metal line of the repeater device is bonded with a first landing pad portion of the first interconnect of the integrated circuit; and

a second metal bump of the first metal line of the repeater device is bonded with a second landing pad portion of the second interconnect of the integrated circuit.

17. The method of claim 10, wherein the first and second interconnects are disposed over a backside of the second semiconductor substrate.

18. The method of claim 17, wherein prior to bonding the repeater device with the integrated circuit, the method further comprises:

revealing the backside of the second semiconductor substrate so as to expose the first and second interconnects.

19. An integrated circuit comprising:

a first semiconductor substrate;

a first transistor device layer disposed over the first semiconductor substrate;

a first dielectric layer disposed over the first transistor device layer;

a first plurality of interconnects disposed within the first dielectric layer; and

a repeater device bonded with the first plurality of interconnects and comprising:

a second semiconductor substrate;

a second transistor device layer disposed over the second semiconductor substrate;

a second dielectric layer disposed over the second transistor device layer; and

a second plurality of interconnects disposed within the second dielectric layer and in direct electronic contact with the first plurality of interconnects.

20. The integrated circuit of claim 19, wherein the first plurality of interconnects are disposed over a frontside of the first semiconductor substrate.

21. The integrated circuit of claim 19, wherein the first plurality of interconnects are disposed over a frontside of the first semiconductor substrate at a back-end-of-line (BEOL) metal layer 8 of the integrated circuit.

22. The integrated circuit of claim 19, wherein the first plurality of interconnects are disposed over a frontside of the first semiconductor substrate at a back-end-of-line (BEOL) metal layer 9 of the integrated circuit.

23. The integrated circuit of any of claims 19–22, wherein the repeater device is bonded with the first plurality of interconnects via at least one electrically conductive bump connection.

24. An integrated circuit comprising:

a first semiconductor substrate;

a first transistor device layer disposed over a frontside of the first semiconductor substrate;

a first plurality of interconnects disposed over a backside of the first semiconductor substrate;

a repeater device bonded with the first plurality of interconnects and comprising:

a second semiconductor substrate;

a second transistor device layer disposed over the second semiconductor substrate;

a dielectric layer disposed over the second transistor device layer; and

a second plurality of interconnects disposed within the dielectric layer and in direct electronic contact with the first plurality of interconnects.

25. The integrated circuit of claim 24, wherein the repeater device is bonded with the first plurality of interconnects via at least one electrically conductive bump connection.

Figure 1A

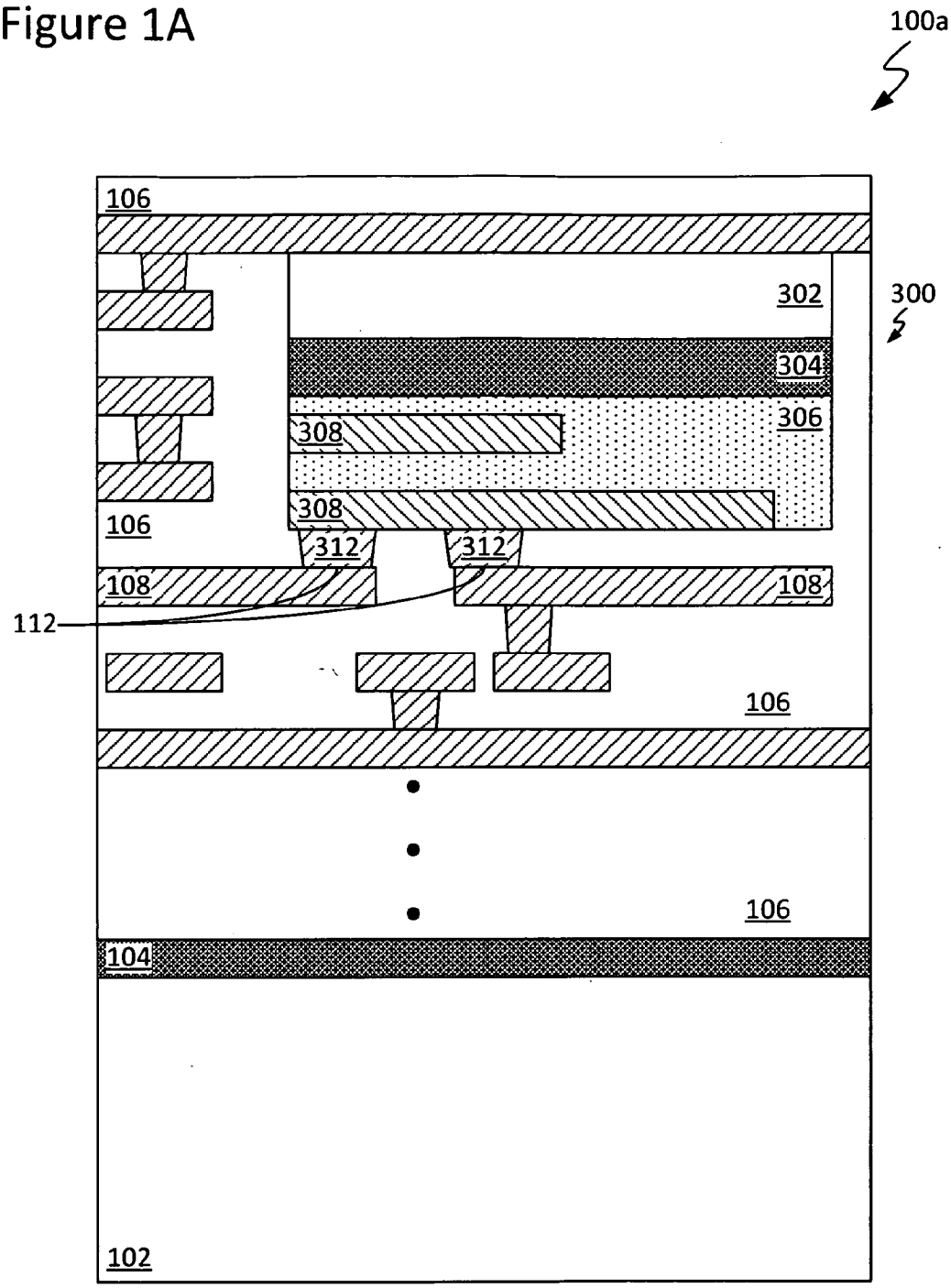

100a
106
302
300
304
306
308
308
106
312
312
108
108
112
106
106
104
102

Figure 1B

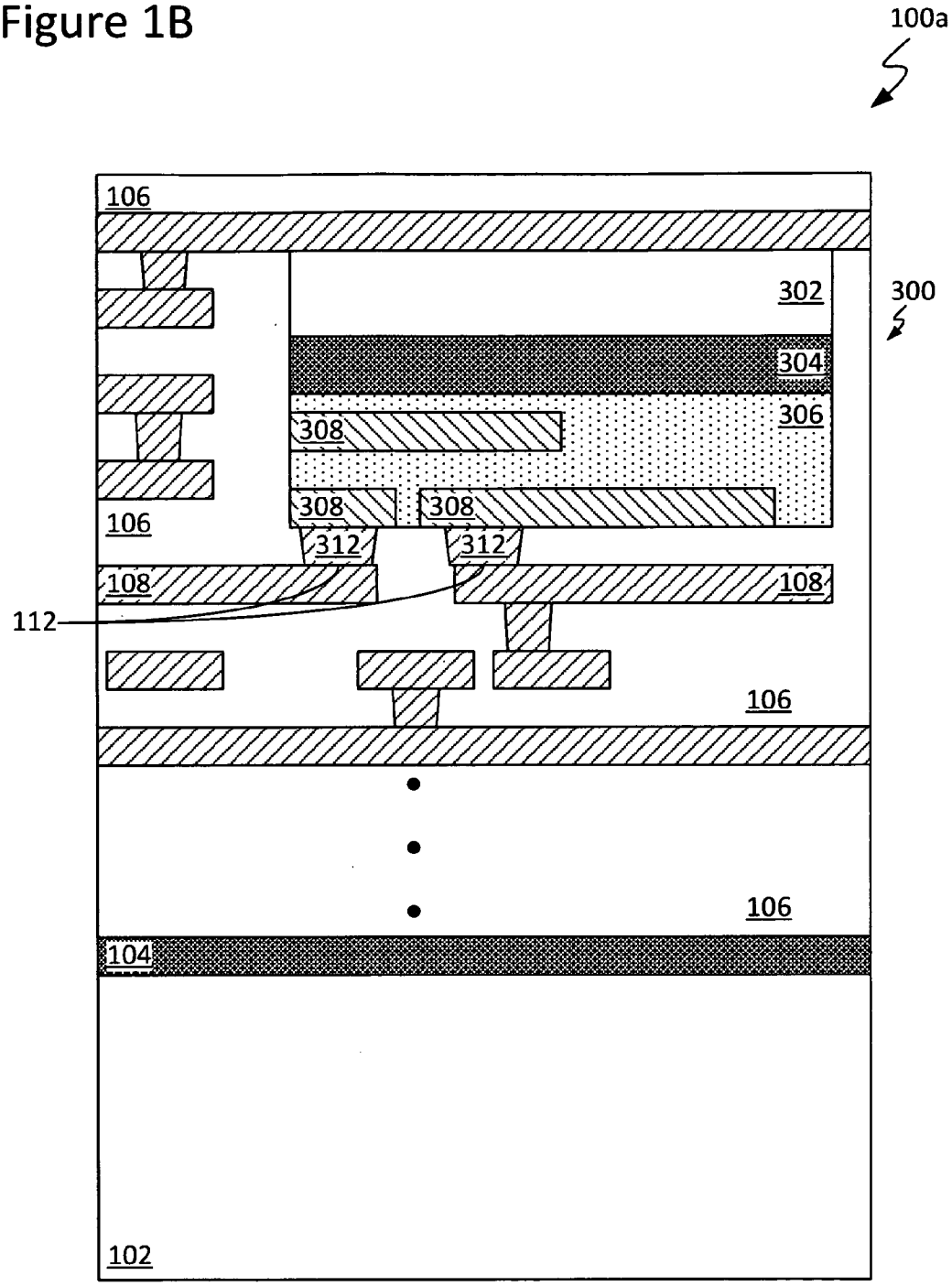

100a
106
302
300
304
306
308
308
308
106
312
312
108
108
112
106
106
104
102

Figure 2A

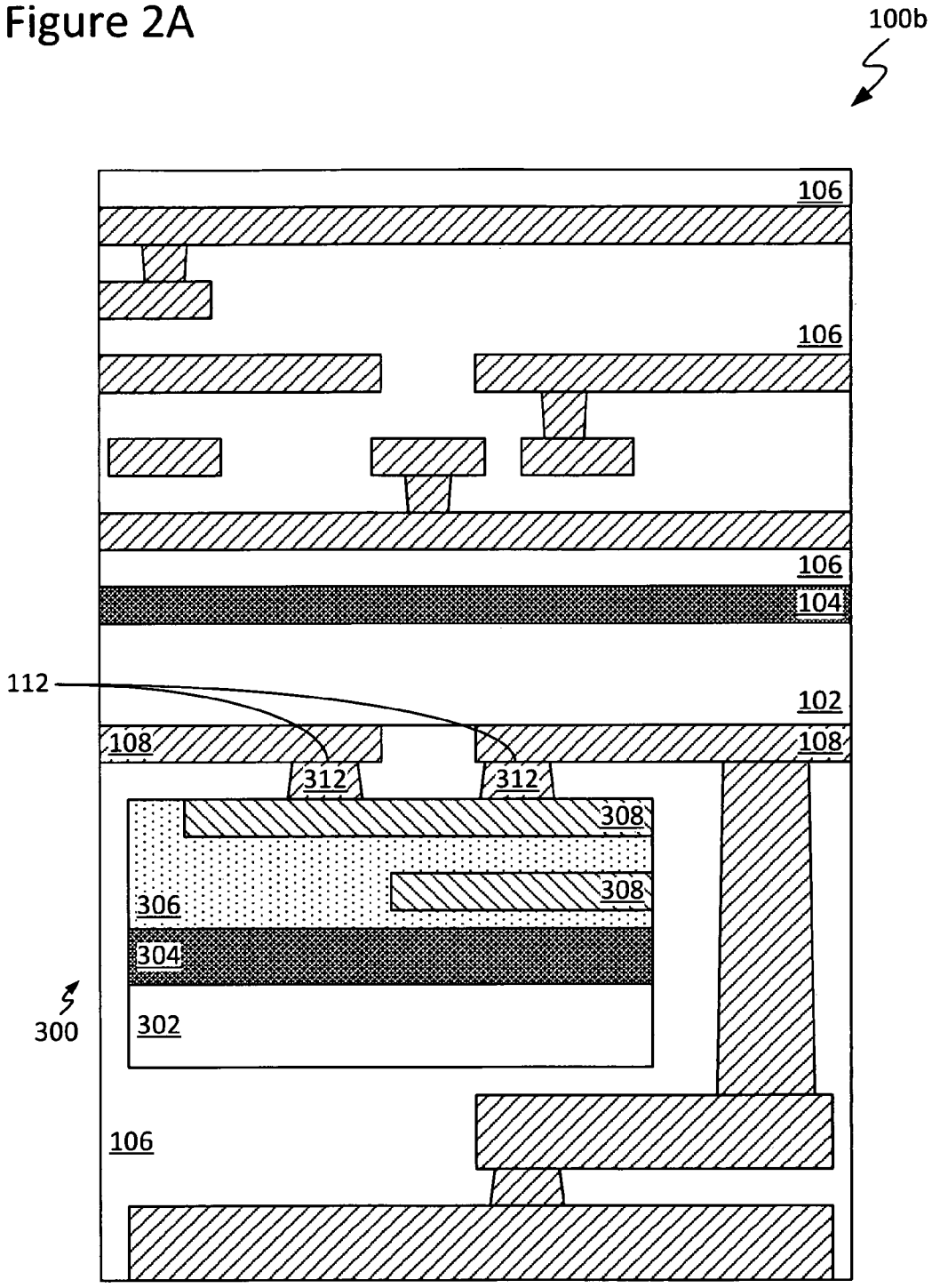

100b
106
106
106
104
112
102
108
108
312
312
308
308
306
304
302
300
106

Figure 2B

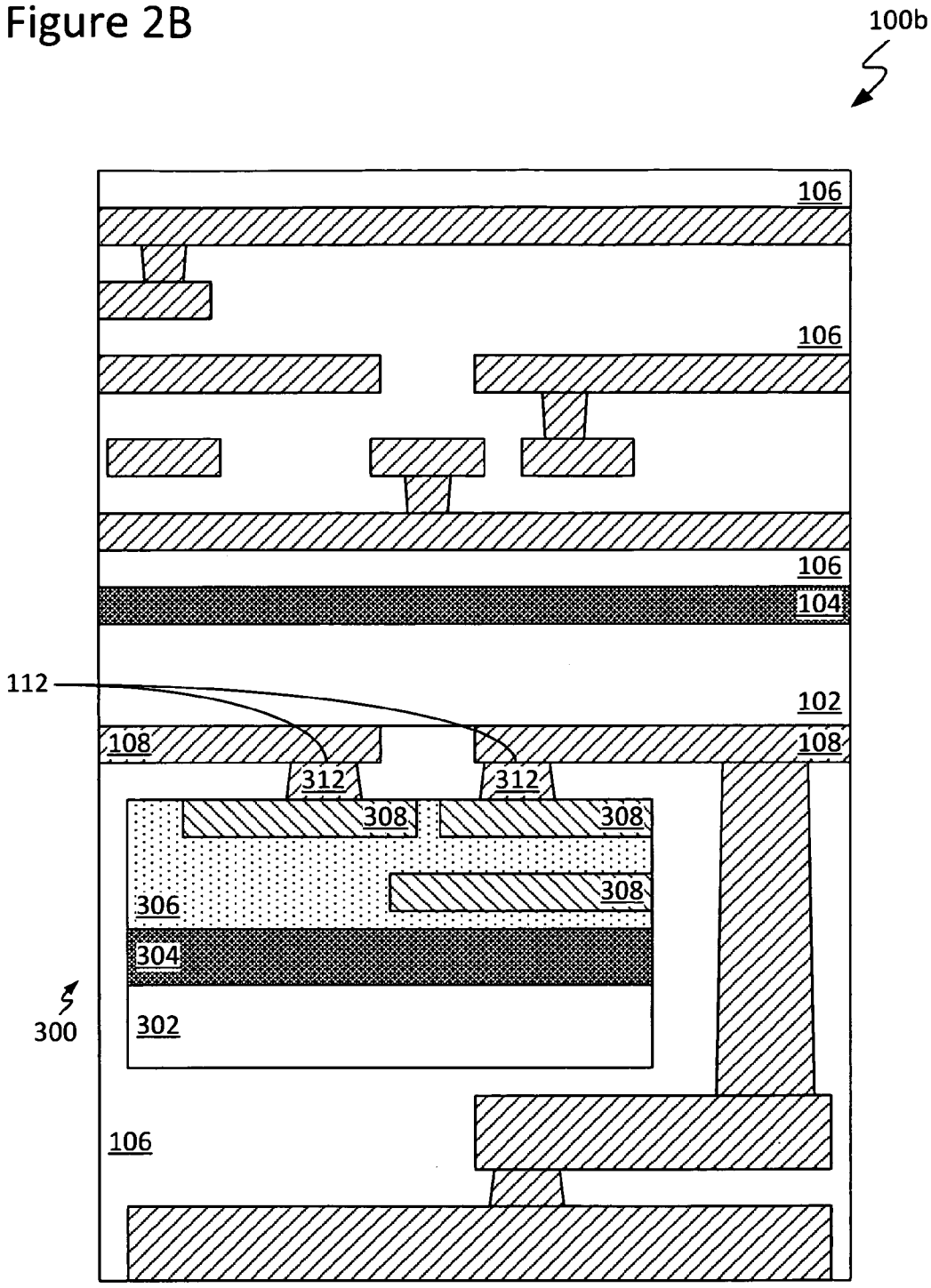

100b
106
106
106
104
112
102
108
108
312
312
308
308
308
306
304
302
300
106

Figure 3

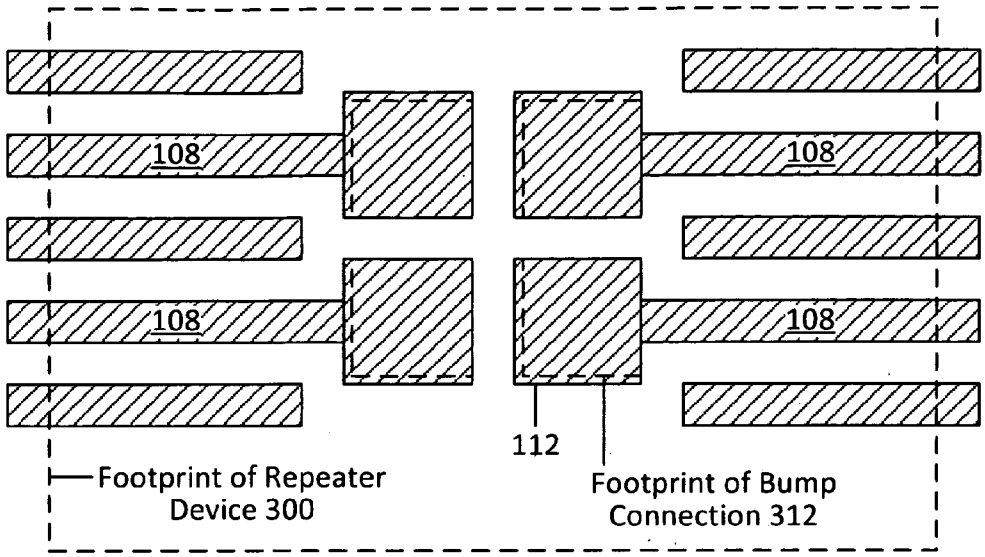


Figure 4A

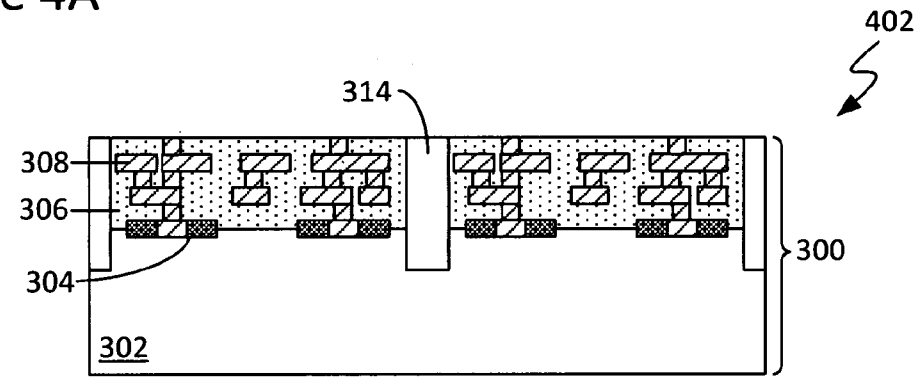


Figure 4B

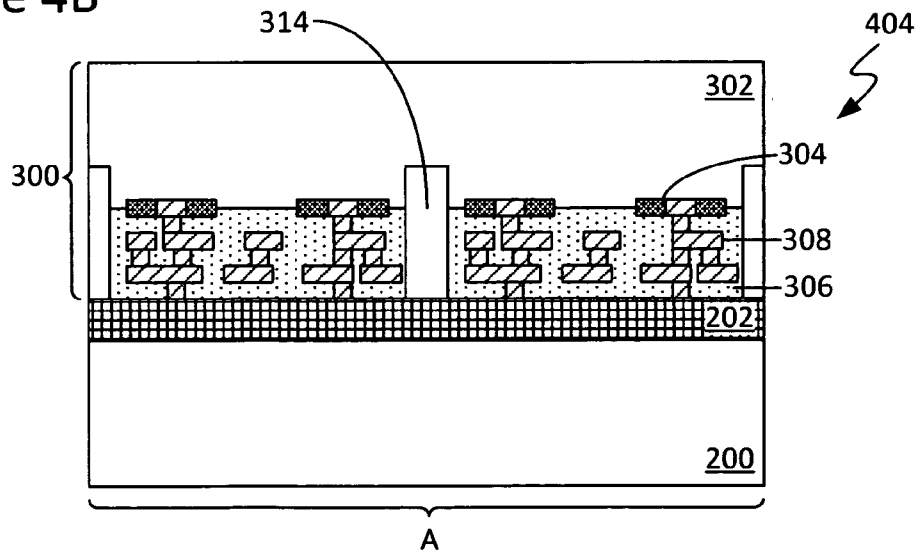


Figure 4C

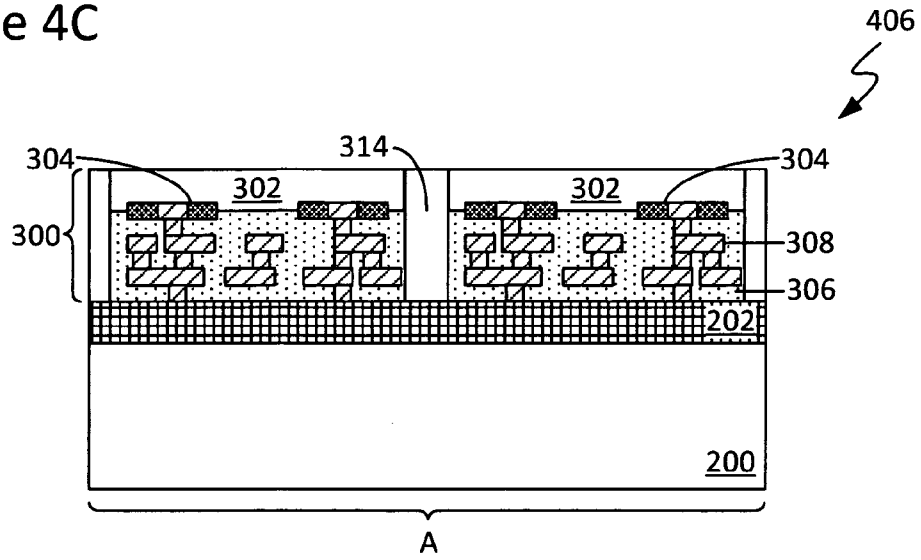


Figure 4D

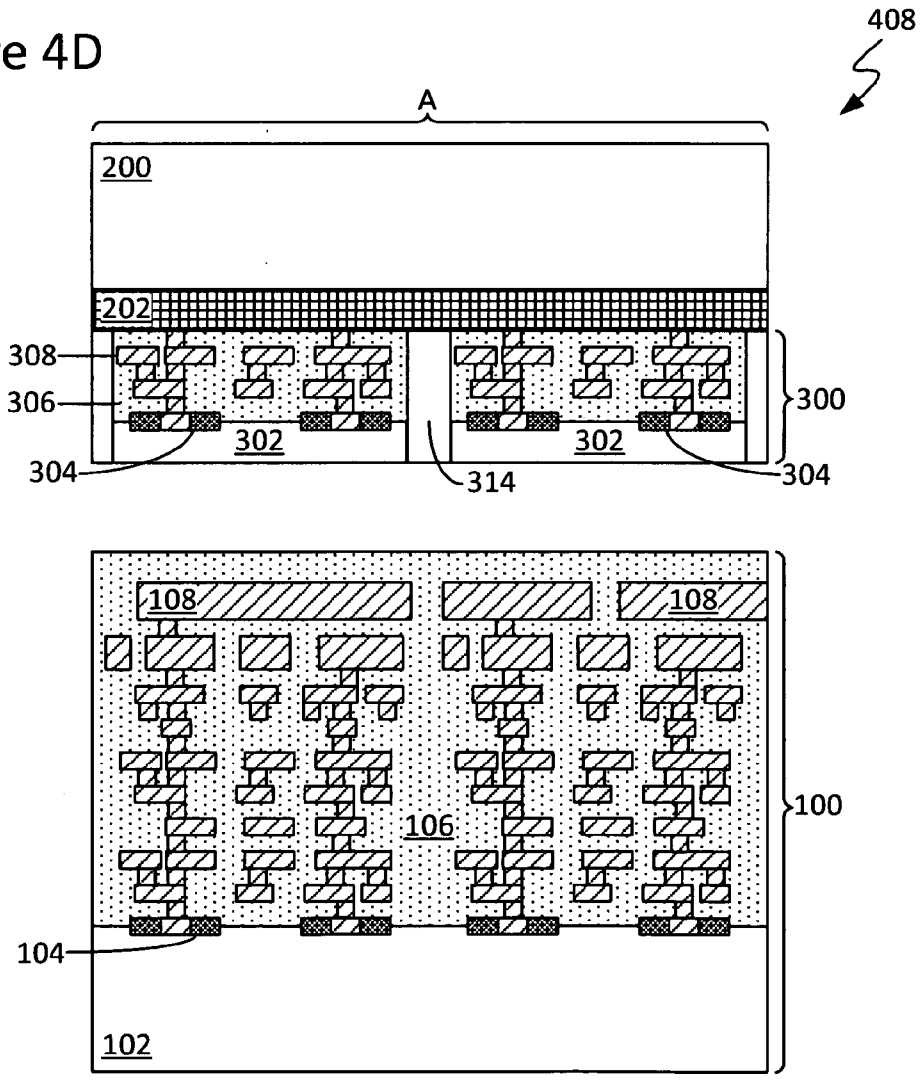


Figure 4E

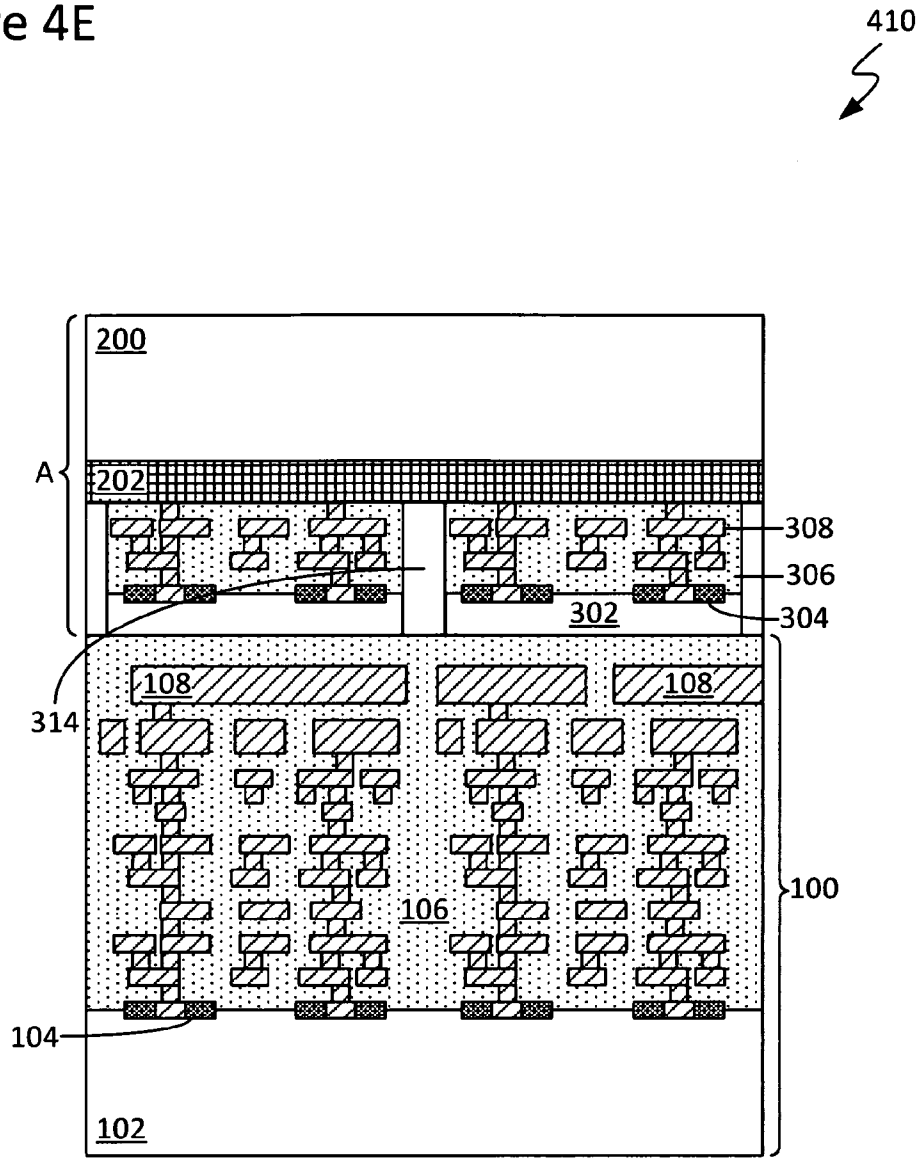


Figure 4F

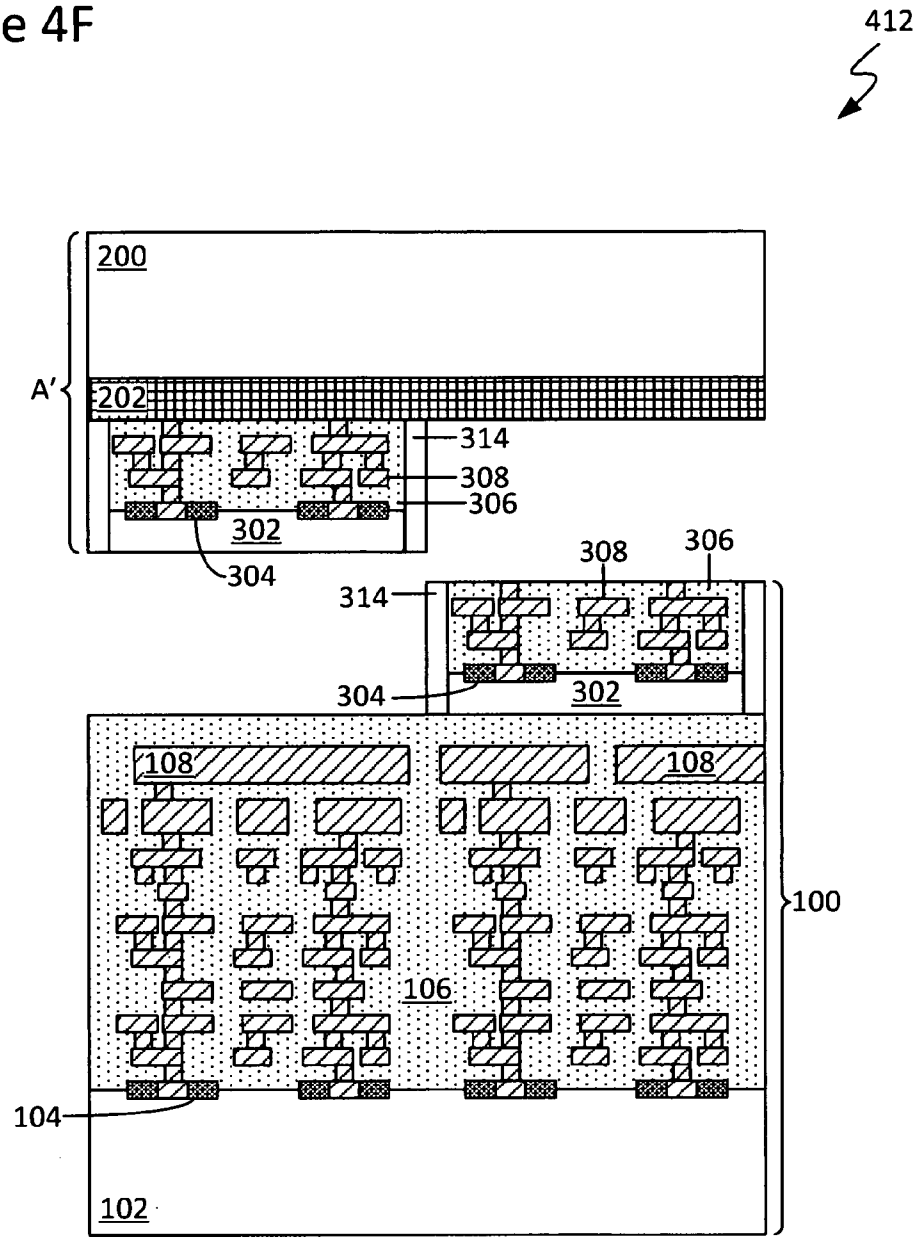
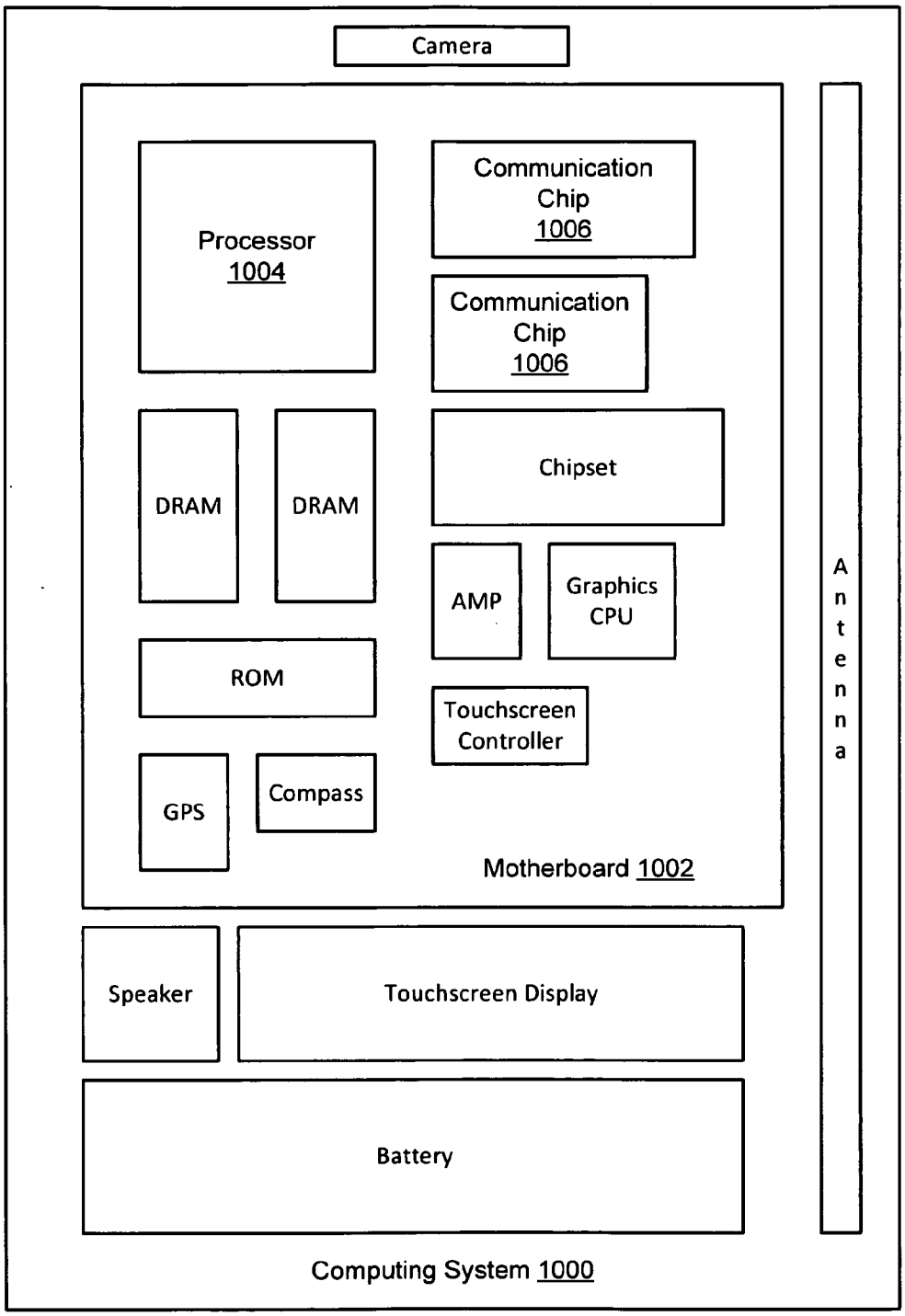

412
200
A'
202
314
308
306
302
304
308
306
314
304
302
108
108
100
106
104
102

Figure 5


Camera
Processor
1004
Communication
Chip
1006
Communication
Chip
1006
DRAM
DRAM
Chipset
AMP
Graphics
CPU
ROM
Touchscreen
Controller
GPS
Compass
Motherboard 1002
Antenna
Speaker
Touchscreen Display
Battery
Computing System 1000

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/000206

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/12(2006.01)i, H01L 25/07(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 23/12; H01L 21/46; H01L 21/336; H01L 23/34; H01L 29/772; G06F 13/36; H01L 27/00; H01L 21/822; H01L 21/82; H01L 25/07

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: integrated circuit, repeater, transistor, power, dielectric layer, interconnect

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008-0277778 A1 (BRUCE K. FURMAN et al.) 13 November 2008 See paragraph [0039], claim 1 and figure 2.	1-25
A	US 2007-0043894 A1 (ARTHUR R. ZINGHER et al.) 22 February 2007 See paragraph [0105], claim 1 and figure 9B.	1-25
A	JP 2001-230326 A (NEC CORP.) 24 August 2001 See paragraph [0028], claims 1-8 and figure 20.	1-25
A	US 2012-0175624 A1 (KARL R. ERICKSON et al.) 12 July 2012 See paragraphs [0019]-[0023], claims 1-3 and figure 7.	1-25
A	JP 2004-079702 A (TOSHIBA CORP.) 11 March 2004 See paragraphs [0025]-[0028], claim 10 and figure 1.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 September 2016 (21.09.2016)	**21 September 2016 (21.09.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/000206

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008-0277778 A1	13/11/2008	US 2010-0081232 A1	01/04/2010
		US 7855101 B2	21/12/2010
US 2007-0043894 A1	22/02/2007	US 2007-0023921 A1	01/02/2007
		US 2010-0129999 A1	27/05/2010
		US 7649245 B2	19/01/2010
		US 7671449 B2	02/03/2010
		US 7838409 B2	23/11/2010
JP 2001-230326 A	24/08/2001	JP 3735855 B2	18/01/2006
		US 2001-0015450 A1	23/08/2001
		US 6515511 B2	04/02/2003
US 2012-0175624 A1	12/07/2012	US 2013-0082268 A1	04/04/2013
		US 8395186 B2	12/03/2013
		US 8575613 B2	05/11/2013
JP 2004-079702 A	11/03/2004	CN 1269213 C	09/08/2006
		CN 1495895 A	12/05/2004
		CN 1495895 C	09/08/2006
		JP 3612313 B2	19/01/2005
		KR 10-2004-0016403 A	21/02/2004
		US 2004-0031995 A1	19/02/2004
		US 6849906 B2	01/02/2005