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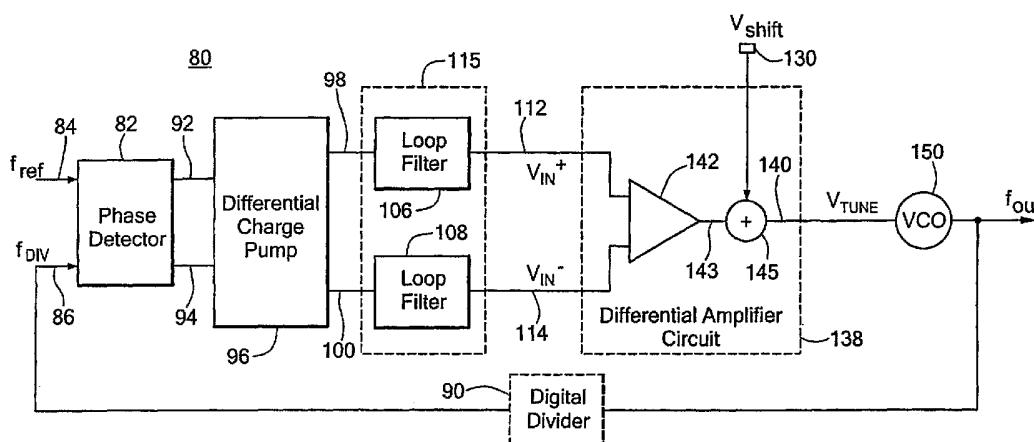
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(54) Title: DIFFERENTIAL CHARGE PUMP PHASE LOCK LOOP (PLL) SYNTHESIZER WITH ADJUSTABLE TUNING VOLTAGE RANGE



(57) Abstract: A differential charge pump PLL synthesizer with adjustable tuning voltage range including a voltage controlled oscillator responsive to a tuning voltage to provide an output frequency. A phase detector circuit is responsive to a reference frequency and the submultiple of the output frequency for generating up and down pulses. A differential charge pump is responsive to the up and down pulses for generating positive and negative differential current pulses. A loop filter is responsive to the positive and negative differential current pulses for providing a differential voltage. A differential amplifier circuit is responsive to the differential voltage and a shift voltage applied at a voltage terminal for shifting the output voltage range of the differential amplifier circuit to provide a predetermined tuning voltage range.

DIFFERENTIAL CHARGE PUMP PHASE LOCK LOOP (PLL) SYNTHESIZER WITH ADJUSTABLE TUNING VOLTAGE RANGE

RELATED APPLICATIONS

This application claims benefit of U.S. Provisional Application No. 60/483,411 filed June 27, 2003, entitled "Fast Locking PLL Based Synthesizer" and U.S. Provisional Application No. 60/544,439 filed February 14, 2004, entitled "Fast Switching PLL Synthesizer for a GSM/EDGE Base Station", both incorporated by reference herein.

FIELD OF THE INVENTION

This invention relates to a differential charge pump phase lock loop (PLL) synthesizer with adjustable tuning voltage range.

BACKGROUND OF THE INVENTION

Conventional PLL synthesizers typically employ a single-ended charge pump to drive a VCO which is typically varactor tuned. The varactor tuned VCO employs a varactor diode which is reversed biased and requires a positive tuning voltage with respect to ground. The single-ended charge pump generates up current and down current pulses which are applied to a loop filter. The loop filter converts the up and down currents to a positive tuning voltage which is applied to the VCO. In a conventional PLL synthesizer employing a single-ended charge pump and passive loop filter, the charge pump output is coupled directly to the VCO's tuning voltage input. Hence, the voltage at the charge pump outputs must span the desired VCO tuning voltage range and may swing close to the rail-to-rail voltage.

It is desirable to keep the VCO gain factor, K_v , as small as possible in a high

performance PLL synthesizer to desensitize the output phase noise from noise at the tuning input. Hence for a given desired output frequency range, the input tuning voltage range is made as large as possible. High performance VCOs typically use an LC tank resonator with frequency tuning achieved by varying the reverse bias voltage across a varactor diode. To minimize noise and for the best gain factor (K_v) linearity, the varactor diode is usually biased at least about 1.5V into reverse bias which results in an allowable tuning voltage range from about 1.5V up to the positive supply.

A high performance PLL also typically requires high output impedance and very good matching of the output up and down currents of the charge pump. The charge pump must also have low leakage currents during the off state in order to minimize static phase error at the PFD input and reference spur sidebands on the VCO output spectrum. It is difficult to design a charge pump that meets these requirements over an output voltage range that must also swing close to the supply rails to meet the desired VCO tuning range.

Ideally, the charge pump output voltage range would be decoupled from the VCO tuning range so that the design of the charge pump could be optimized without the constraint of being compliant over the full VCO tuning range. Such a design would allow the charge pump and the VCO to be optimized independently of each other and allow the VCO to run off a higher supply voltage than the charge pump.

BRIEF SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide a differential charge pump PLL synthesizer with adjustable tuning voltage range.

It is a further object of this invention to provide such a differential charge pump PLL synthesizer which shifts the tuning voltage range by adjusting the output offset of a

differential amplifier circuit connected to a differential charge pump.

It is a further object of this invention to provide such a differential charge pump which de-couples the tuning voltage range from the charge pump outputs.

It is a further object of this invention to provide such a differential charge pump which minimizes the voltage swing needed to be generated by the charge pump and loop filter.

It is a further object of this invention to provide such a differential charge pump which minimizes the differential voltages required at the charge pump outputs.

It is a further object of this invention to provide such a differential charge pump which eases the charge pump design requirements.

It is a further object of this invention to provide such a differential charge pump PLL synthesizer which can select a predetermined tuning voltage range for a particular single-ended VCO.

This invention results from the realization that an innovative differential charge pump PLL synthesizer with adjustable tuning voltage range can be achieved by generating up and down pulses in response to a reference frequency and a sub-multiple of an output frequency; providing positive and negative differential current pulses in response to the up and down pulses with a differential charge pump, generating a differential voltage from the positive and negative differential current pulses with a loop filter and applying a shift voltage at a voltage terminal of a differential amplifier circuit responsive to the differential voltage to shift the output voltage range and provide a predetermined tuning voltage range.

This invention features a differential charge pump PLL synthesizer with adjustable tuning voltage range including a voltage controlled oscillator responsive to a tuning voltage to provide an output frequency, a phase detector circuit responsive to a reference frequency

and a sub-multiple of the output frequency for generating up and down pulses, a differential charge pump responsive to the up and the down pulses for generating positive and negative differential current pulses, a loop filter responsive to the positive and negative differential current pulses for providing a differential voltage, and a differential amplifier circuit responsive to the differential voltage and a shift voltage terminal for shifting the output voltage range of the differential amplifier circuit to provide a predetermined tuning voltage range.

In one embodiment, the shift voltage is greater than about 1V. The differential charge pump PLL may include a summer circuit for adding the shift voltage to the output of the differential amplifier circuit to provide the predetermined tuning voltage range. The PLL may include a frequency divider circuit for generating the sub-multiple of the output frequency. The differential voltage swing may be equal to about one half of the tuning voltage range. The shift voltage may be any voltage in the range equal to about one half of the voltage range above a negative power supply rail of the differential amplifier circuit to a voltage equal to about one half the voltage tuning range below a positive power supply rail of the differential amplifier circuit. The differential amplifier circuit may apply a gain to the differential voltage that may be greater than or equal to 1.

This invention further features a method for providing an adjustable tuning voltage range for a differential charge pump PLL synthesizer including the steps of generating up and down pulses in response to a reference frequency and a sub-multiple of an output frequency, providing positive and negative differential current pulses in response to the up and the down pulses with a differential charge pump, generating a differential voltage from the positive and negative differential current pulses with a loop filter, generating a single ended voltage from the differential voltage with a differential amplifier circuit, and

applying a shift voltage at a voltage terminal to shift the output voltage range of the differential amplifier circuit and provide a predetermined tuning voltage range.

This invention also features a method for providing an adjustable tuning voltage range for a differential charge pump PLL synthesizer including providing a tuning voltage range determined by a voltage swing of the differential outputs of a differential charge pump, and providing a center voltage of the tuning voltage range determined by a shift voltage applied at an input to a differential amplifier circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features and advantages will occur to those skilled in the art from the following description of a preferred embodiment and the accompanying drawings, in which:

Fig. 1 is a schematic block diagram of a prior art PLL synthesizer employing a single-ended charge pump;

Fig. 2 is a schematic block diagram of one embodiment of the differential charge pump PLL synthesizer of this invention;

Fig. 3 is a schematic block diagram showing in further detail the components of the differential charge pump PLL synthesizer shown in Fig. 2; and

Fig. 4 is a block diagram showing the steps for the method for providing an adjustable tuning voltage for a differential charge pump PLL synthesizer of this invention.

PREFERRED EMBODIMENT

Aside from the preferred embodiment or embodiments disclosed below, this invention is capable of other embodiments and of being practiced or being carried out in

various ways. Thus, it is to be understood that the invention is not limited in its application to the details of construction and the arrangements of components set forth in the following description or illustrated in the drawings.

Prior art PLL synthesizer 10, Fig. 1 typically includes phase frequency detector (PFD) 12 responsive to a reference frequency signal, f_{REF} , on line 14 and a sub-multiple of an output frequency signal, n_{DIV} on line 16. Typically, n_{DIV} , is generated with N-divider circuit 18 which divides f_{OUT} on line 31 by N. PFD 12 compares the frequency of f_{REF} and n_{DIV} to determine if the frequency of n_{DIV} needs to be increased or decreased in order to lock f_{REF} to n_{DIV} . PFD 12 generates the appropriate frequency up pulses on line 20 or frequency down pulses on line 22 which is applied to single-ended charge pump 24. Single-ended charge pump 24 is responsive to the frequency up and frequency down pulses and generates current up pulses and current down pulses on line 25 which are applied to loop filter 26. Loop filter 26 is responsive to the current up and current down pulses to generate voltages on line 28 which are applied to single-ended VCO 30 to increase or decrease the frequency of f_{OUT} on line 31 to achieve a lock. As discussed above, for a particular output or tuning voltage range, V_{TUNE} on line 28, the voltages applied to VCO 30 generated by single-ended charge pump 24 and loop filter 26 must equal the voltages for the desired tuning voltage range. Moreover, because the tuning voltages on line 28 are directly coupled to single-ended charge pump 24 and loop filter 26, PLL synthesizer 10 cannot shift or adjust the output voltage range on line 28.

In contrast, differential charge pump phase lock loop (PLL) synthesizer 80, Fig. 2, of this invention can provide a desired tuning range to the VCO with just half of the voltage of the desired tuning range required at outputs 98 and 100 of differential charge pump 98. The tuning voltage can be rail-to-rail and still leave sufficient head-room and foot-room for

differential charge pump 96 to operate within. The tuning range can be shifted up or down to optimise the varactor biasing in VCO 150 without impacting the design of charge pump 96.

Differential charge pump PLL synthesizer 80 includes phase detector circuit 82 responsive to a reference frequency, f_{REF} , on line 84 and a sub-multiple of an output frequency, f_{DIV} , on line 86, (e.g., a sub-multiple of the output frequency f_{OUT} on line 88 which has been divided by N by divider circuit 90). Phase detector circuit 82 generates frequency up pulses on line 92 and frequency down pulses on line 94 which are input to differential charge pump 96. Differential charge pump 96 generates current up and current down pulses on lines 98 and 100 to charge or discharge capacitors in loop filters 106 and 108. Loop filters 106 and 108 are responsive to the current up and current down pulses on line 98 and 100 and convert the current up and current down pulses to positive and negative differential voltages, respectively, between lines 112 and 114. Loop filters 106 and 108, Fig. 3 may include capacitors 102 and 103, and capacitors 104 and 105, respectively. Although in this example two loop filters are employed, this is not a necessary limitation of this invention, as a single loop filter network, as indicated by dashed line 115, Fig. 2 may be employed, or a differential loop filter may be utilized, as known by those skilled in the art.

Differential amplifier circuit 138 is responsive to the difference of the voltages on lines 112 and 114 and to a shift voltage, V_{SHIFT} , e.g., 3.0V or 3.5V, applied at voltage terminal 130 to shift the output voltage range on line 140 and minimize the differential voltage swing required across lines 112 and 114 for a desired VCO tuning voltage range. Differential amplifier 138, Fig. 3, where like parts have been given like numbers, may include a four resistor instrumentation amplifier topology, e.g., resistors 160, 162, 164

and 166, as known to those skilled in the art and may include input buffers (not shown) to avoid excessively loading loop filters 106 and 108. Voltage terminal 130 is used to shift the output voltage range of differential amplifier 142 on line 140 to align the voltage output swing with the desired VCO tuning voltage range. In other designs, summer circuit 145, Fig. 2, adds the shift voltage applied at terminal 130 and the voltage on line 143 output by amplifier 142 to provide the predetermined tuning voltage range V_{TUNE} , on line 140 to activate single-ended VCO 150.

The following example, referring to Fig. 2, illustrates how differential charge pump PLL synthesizer 80 of this invention can tune VCO 150 over the full tuning voltage range while the voltages at outputs 98 and 100 of charge pump 96 need to span only half the tuning voltage range. The tuning voltage (V_{TUNE}) of differential charge pump PLL synthesizer 80 is governed by the equation:

$$V_{TUNE} = V_{SHIFT} + (V_{IN}^{+} - V_{IN}^{-}) \quad (1)$$

where V_{TUNE} is the voltage on line 140, V_{SHIFT} is the shift voltage applied at terminal 130, V_{IN}^{+} is the voltage at line 112 and V_{IN}^{-} is the voltage at line 114. If the desired tuning voltage range is 2.0V to 5.0V and differential charge pump 96 and loop filters 106 and 108 generate voltages around a common mode voltage level that is optimum for differential charge pump 96, e.g., 1.75V, setting V_{SHIFT} to 3.5V will provide the desired tuning voltage range of 2.0V to 5.0V with a differential voltage of only 1.5V between lines 112 and 114 as shown by the example in equations (2) to (9) below:

To generate a tuning voltage of 2V:

$$V_{TUNE} = 3.5V + ((1.75V - 0.75V) - (1.75V + 0.75V)) \quad (2)$$

$$V_{TUNE} = 3.5V + (1.0V - 2.5V) \quad (3)$$

$$V_{TUNE} = 3.5V + (-1.5V) \quad (4)$$

$$V_{\text{TUNE}} = 2.0\text{V}, \quad (5)$$

similarly, to generate a tuning voltage of 5V:

$$V_{\text{TUNE}} = 3.5\text{V} + ((1.75\text{V} + 0.75\text{V}) - (1.75\text{V} - 0.75\text{V})) \quad (6)$$

$$V_{\text{TUNE}} = 3.5\text{V} + (2.5\text{V} - 1.0\text{V}) \quad (7)$$

$$V_{\text{TUNE}} = 3.5\text{V} + (1.5\text{V}) \quad (8)$$

$$V_{\text{TUNE}} = 5.0 \quad (9)$$

Hence a tuning voltage range of 3V can be achieved with just a $\pm 0.75\text{V}$ swing or a 1.5V span on the outputs of charge pump 96, indicated at 98 and 100. If the tuning range needs to be shifted down by half a volt, e.g., a range of 1.5V to 4.5V, this can be achieved by reducing the shift voltage from 3.5V to 3.0V without effecting the $\pm 0.75\text{V}$ swing required at outputs 98 and 100 of differential charge pump 96. Hence the span of the tuning range is determined by the voltage swing at voltage outputs 98 and 100 of charge pump 96 and the center of the range is set by the shift voltage applied at terminal 130. With the differential outputs and the independent level shift capability, the output voltage compliance range of differential charge pump 96 needs to be only one half of the desired tuning range. This is in contrast to conventional PLL synthesizers which require the charge pump outputs to span the full tuning voltage range.

The shift voltage may be 3.0V or 3.5V as discussed above, or any voltage in the range from a voltage corresponding to half the desired tuning range above the negative power supply rail (not shown) of differential amplifier circuit 138 to a voltage corresponding to half the desired tuning range below the positive power supply rail (not shown) of differential amplifier circuit 138. Regardless of the level shifting of the tuning range the peak to peak voltage swing at the outputs of differential charge pump 96 needs to

be only one half of the desired tuning voltage range.

As shown above, applying a shift voltage at voltage terminal 130 shifts the tuning voltage (V_{TUNE}) on line 140 output by differential amplifier circuit 96 such that any desired output voltage range can be achieved while maintaining a minimum differential voltage (ΔV) at the inputs of differential amplifier circuit 96. This greatly simplifies the design of charge pump 96 as it provides sufficient head-room and foot-room for cascaded current sources (not shown) used in differential charge pump 96 for highest output impedance and better up to down matching over the required compliance range. Moreover, differential charge pump 96 can utilize lower voltage supply rails and thus take advantage of more advanced process technologies and consume less power. When the difference between V_{IN}^+ and V_{IN}^- , indicated at 112 and 114, is negative, (e.g., $-1.5V$), applying a shift voltage, V_{SHIFT} , of $3.5V$ shifts V_{TUNE} to be positive, e.g., of sufficient voltage to ensure that the VCO's tuning varactor is sufficiently reverse biased.

The voltage swing required at outputs 98 and 100 of differential charge pump 96 for a given tuning voltage range can be further minimized by increasing the gain of differential amplifier circuit 138, Fig. 3. In this embodiment, differential amplifier circuit 38 includes a four resistor configuration, e.g., resistors 160, 162, 164 and 166. Input resistors 162 and 164 each have value equal to R_1 and feedback resistor 166 and V_{shift} resistor 160 each have value equal to R_2 . The tuning voltage (V_{TUNE}) of differential charge pump PLL synthesizer 80 is governed by the equation:

$$V_{TUNE} = V_{SHIFT} + \frac{R_2}{R_1} (V_{IN}^+ - V_{IN}^-) \quad (10)$$

Setting $R_1 = R_2$ provides a differential gain of 1, as used in the example above with equations (1) to (9). By increasing the ratio of R_2/R_1 the differential gain of differential

amplifier circuit 138 can be increased. Hence, the required voltage swing at outputs 98 and 100 of differential charge pump 96 can be varied in accordance with equation (10) above. How much the gain can be increased may be limited by the output phase noise requirement of PLL synthesizer 80, as the noise contribution from differential charge pump 96 increases with the differential amplifier gain.

Method 398, Fig. 4, of providing an adjustable tuning voltage range for a differential charge pump PLL synthesizer of this invention includes the steps of: generating up and down pulses in response to a reference frequency and a sub-multiple of an output frequency, step 400; providing positive and negative differential current pulses in response to the up and down pulses with a differential charge pump; step 402; generating a differential voltage from the positive and negative current pulses with a loop filter, step 404, generating a single-ended voltage from the differential voltage with a differential amplifier circuit, step 406; and applying a shift voltage at a voltage terminal to shift the output voltage range of the differential amplifier and provide a predetermined tuning voltage range, step 408.

Although specific features of the invention are shown in some drawings and not in others, this is for convenience only as each feature may be combined with any or all of the other features in accordance with the invention. The words “including”, “comprising”, “having”, and “with” as used herein are to be interpreted broadly and comprehensively and are not limited to any physical interconnection. Moreover, any embodiments disclosed in the subject application are not to be taken as the only possible embodiments.

Other embodiments will occur to those skilled in the art and are within the following claims:

What is claimed is:

CLAIMS

1. A differential charge pump phase lock loop (PLL) synthesizer with adjustable tuning voltage range comprising:
 - a voltage controlled oscillator responsive to a tuning voltage to provide an output frequency;
 - a phase detector circuit responsive to a reference frequency and a sub-multiple of said output frequency for generating up and down pulses;
 - a differential charge pump responsive to said up and said down pulses for generating positive and negative differential current pulses;
 - a loop filter responsive to said positive and negative differential current pulses for providing a differential voltage; and
 - a differential amplifier circuit responsive to said differential voltage and a shift voltage applied at a voltage terminal for shifting the output voltage range of said differential amplifier circuit to provide a predetermined tuning voltage range.
2. The differential charge pump PLL synthesizer of claim 1 in which said shift voltage is greater than about +1V.
3. The differential charge pump PLL synthesizer of claim 1 further including a summer circuit for adding said shift voltage to the output of said differential amplifier circuit to provide said predetermined tuning voltage range.
4. The differential charge pump PLL synthesizer of claim 1 further including a frequency divider circuit for generating said sub-multiple of said output frequency.

5. The differential charge pump PLL synthesizer of claim 1 in which said differential voltage is equal to about one half of said tuning voltage range.

6. The differential charge pump PLL synthesizer of claim 1 in which said shift voltage is any voltage in the range equal to about one half of said voltage range above a negative power supply rail of said differential amplifier circuit to a voltage equal to about one half said voltage tuning range below a positive power supply rail of said differential amplifier circuit.

7. The differential charge pump PLL synthesizer of claim 1 in which said differential amplifier circuit applies a gain to said differential voltage that is greater than or equal to 1.

8. A method for providing an adjustable tuning voltage range for a differential charge pump PLL synthesizer comprising:

generating up and down pulses in response to a reference frequency and a sub-multiple of an output frequency;

providing positive and negative differential current pulses in response to said up and said down pulses with a differential charge pump;

generating a differential voltage from said positive and negative differential current pulses with a loop filter;

generating a single ended voltage from the said differential voltage with a differential amplifier circuit; and

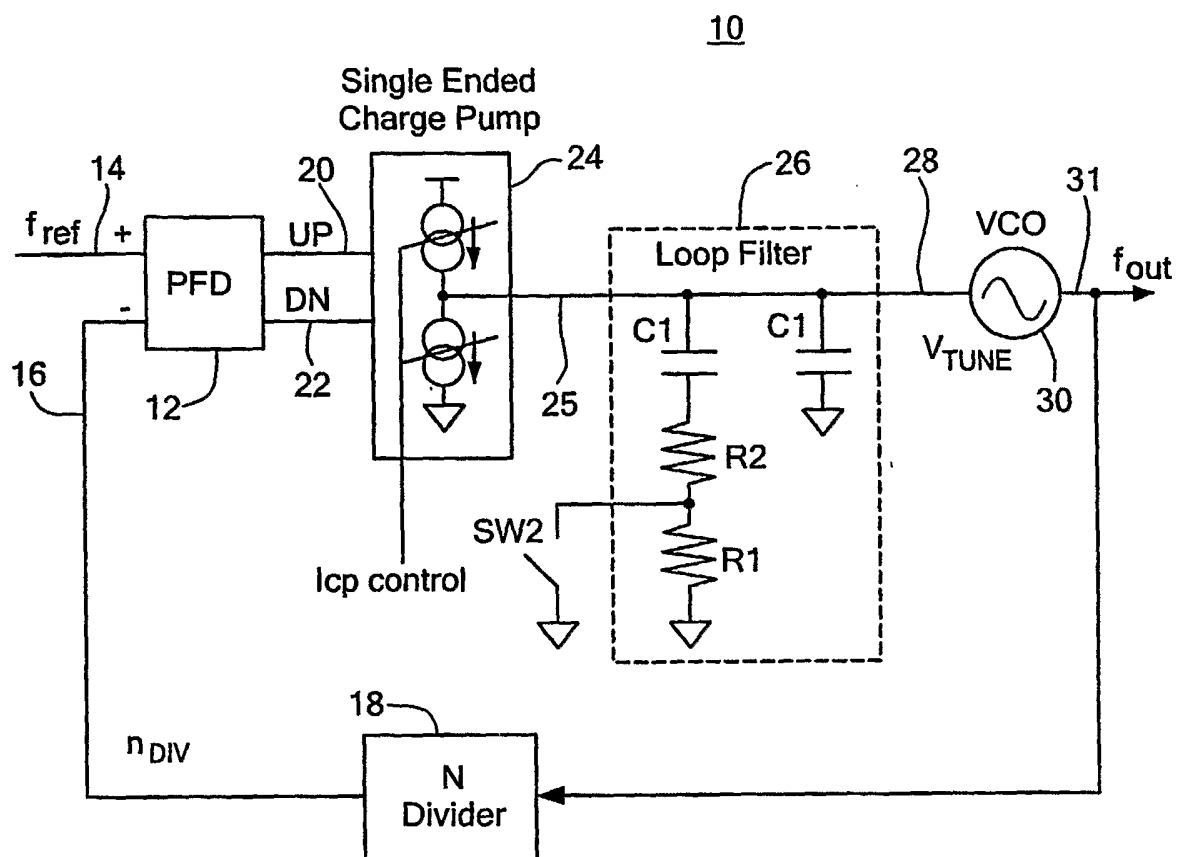
applying a shift voltage at a voltage terminal to shift the output voltage range of said differential amplifier circuit and provide a predetermined tuning voltage range.

9. A method for providing an adjustable tuning voltage range for a differential charge pump PLL synthesizer comprising:

providing a tuning voltage range determined by a voltage swing of the differential outputs of a differential charge pump; and

providing a center voltage of said tuning voltage range determined by a shift voltage applied at an input to a differential amplifier circuit.

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**FIG. 1**

PRIOR ART

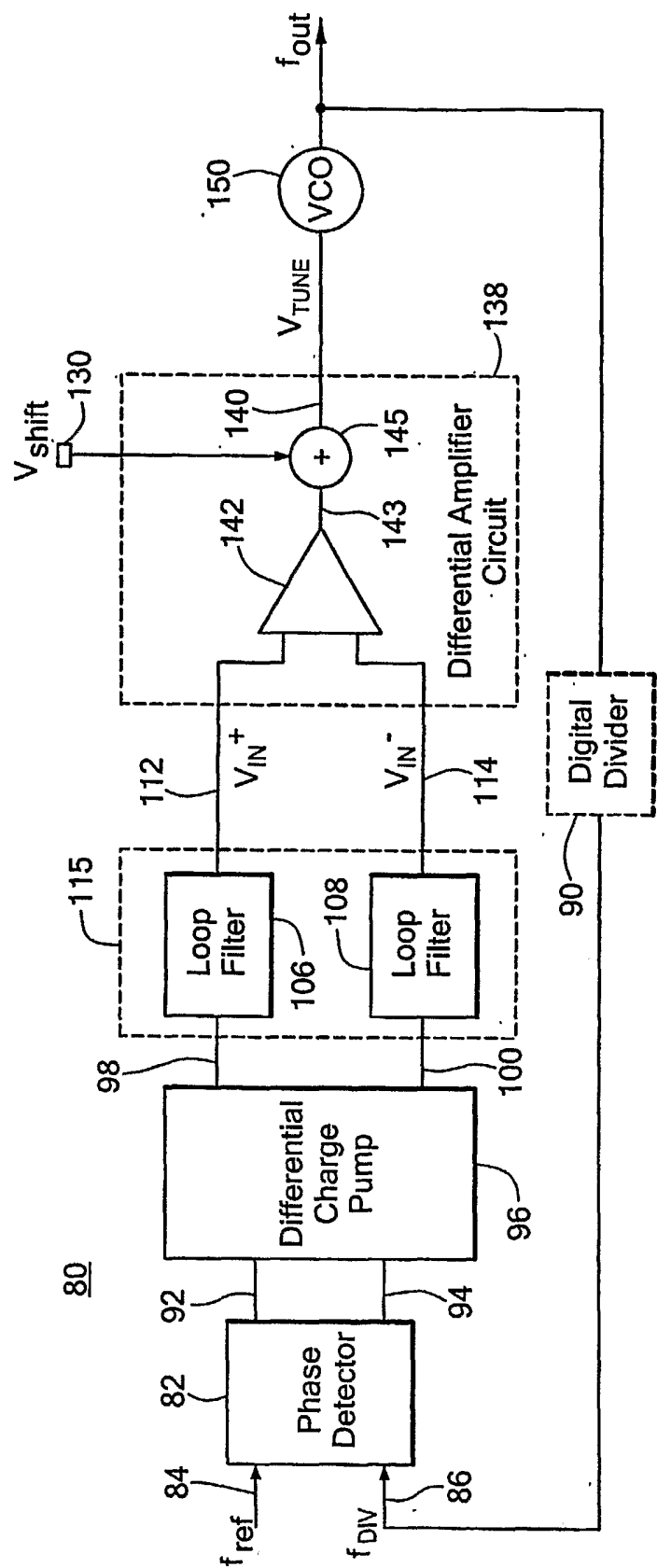


FIG. 2

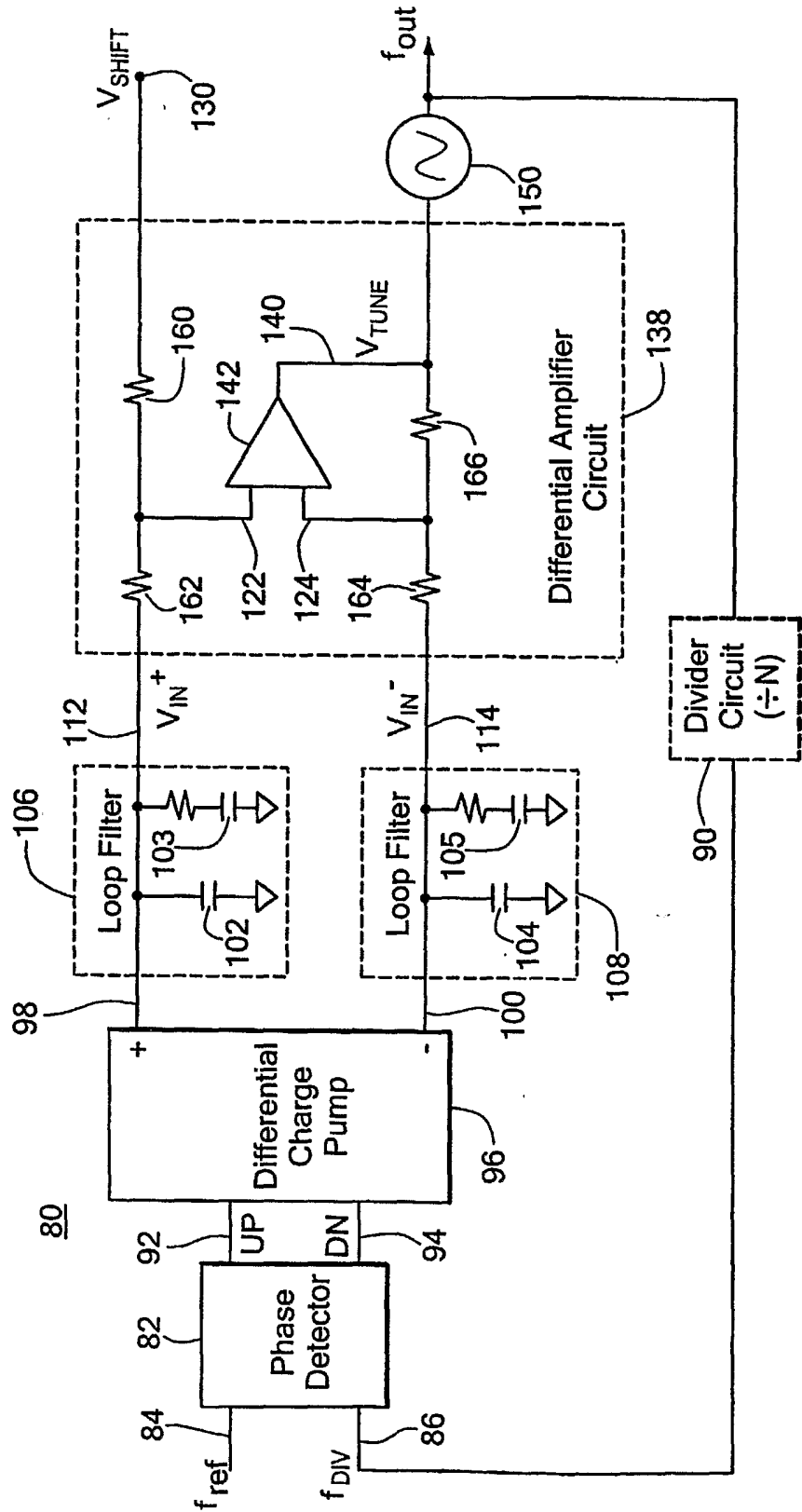
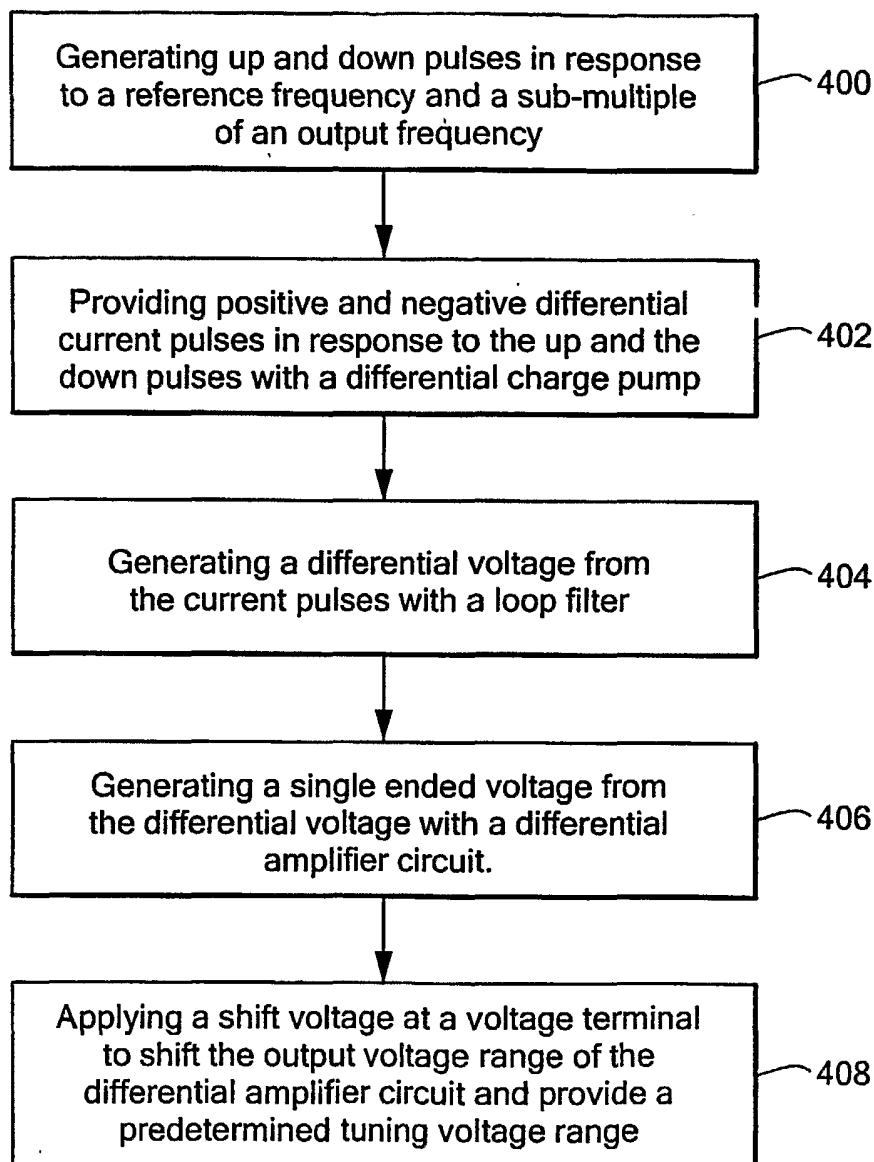


FIG. 3

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398**FIG. 4**