United States Patent

Nakaya

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[45] **May 23, 1972**

[54] TRIGGER CONTROLLING METHOD

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[73] Assignee: **Iwatsu Electric Co., Ltd.,** Tokyo, Japan

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[30] **Foreign Application Priority Data**

July 10, 1969 Japan.....44/54079

[52] **U.S. Cl.**.....**328/63,** 307/269, 328/72, 328/151

[51] **Int. Cl.**.....**H03k 5/00**

[58] **Field of Search**.....307/240, 269; 328/63, 72, 139, 328/141, 151

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Primary Examiner—Donald D. Forrer
Assistant Examiner—R. C. Woodbridge
Attorney—Robert E. Burns and Emmanuel J. Lobato

[57] **ABSTRACT**

An improved trigger controlling method of the present invention uses a memory circuit for storing a signal which is proportional to the differentiated waveform of a sampled observing signal, and the differentiated waveform is controlled by the signal stored in the memory circuit. As a result of this, the improved method of the present invention provides a trigger signal which is obtained automatically and in a stable condition, an output pulse synchronized with an input observing signal for all magnitudes of the input observing signal which is to be applied to a sampling device such as a sampling oscilloscope.

8 Claims, 11 Drawing Figures

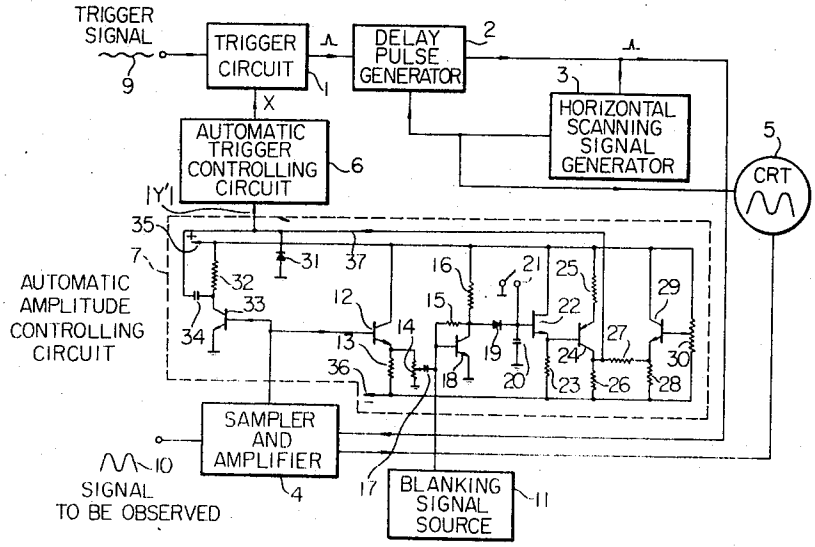
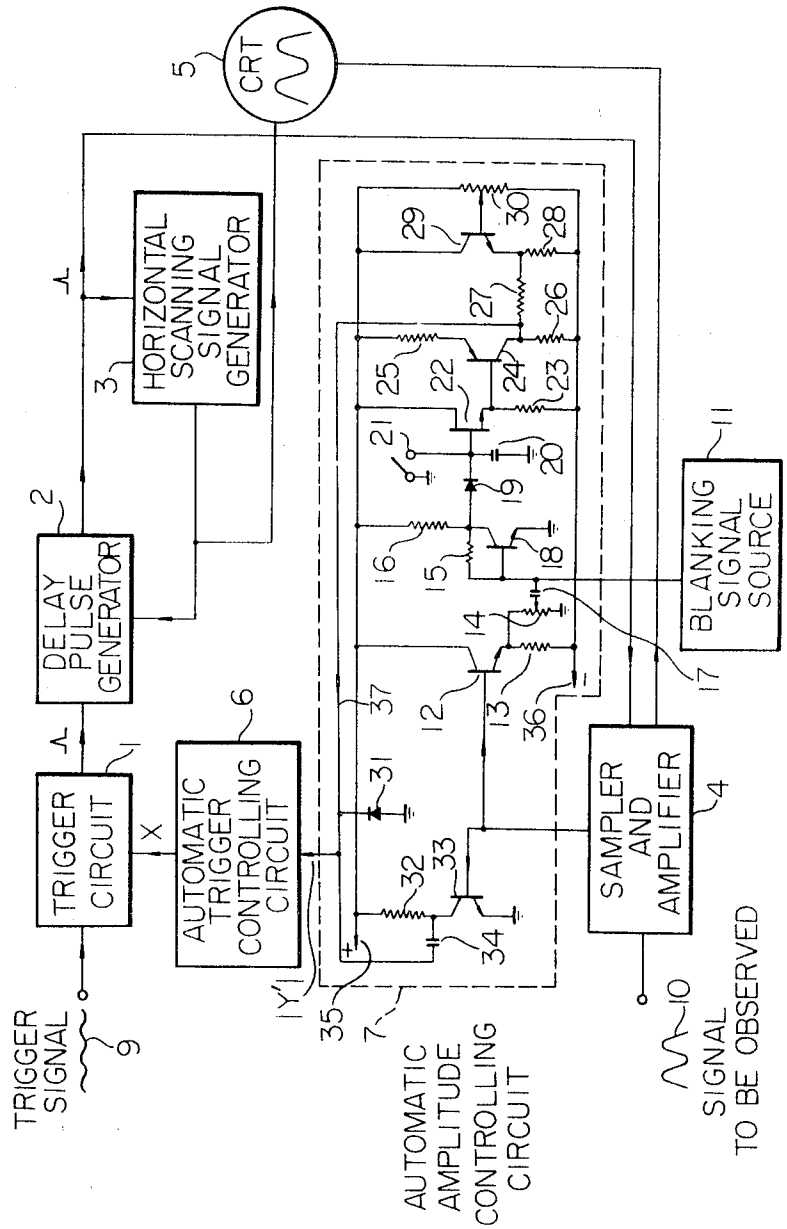


Fig. 1


CRT
5
HORIZONTAL SCANNING SIGNAL GENERATOR
3
DELAY PULSE GENERATOR
2
TRIGGER CIRCUIT
1
AUTOMATIC TRIGGER CONTROLLING CIRCUIT
6
SAMPLER AND AMPLIFIER
4
BLANKING SIGNAL SOURCE
11
TRIGGER SIGNAL
9
SIGNAL TO BE OBSERVED
10
AUTOMATIC AMPLITUDE CONTROLLING CIRCUIT
7
A
X
Y
Y'
12
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14
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Fig. 2A

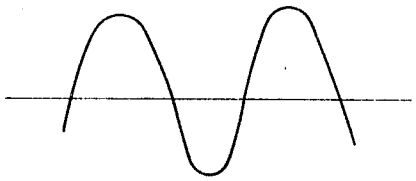

Fig. 2B

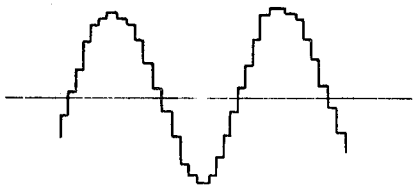

Fig. 2C

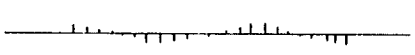

Fig. 2D

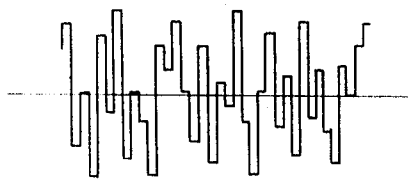

Fig. 2E

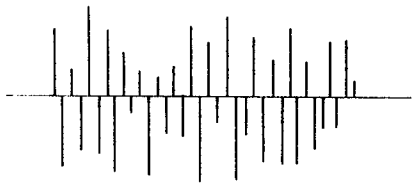

Fig. 3

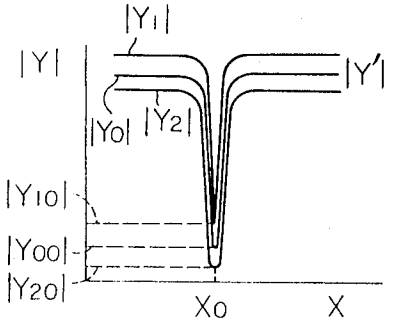

Fig. 4

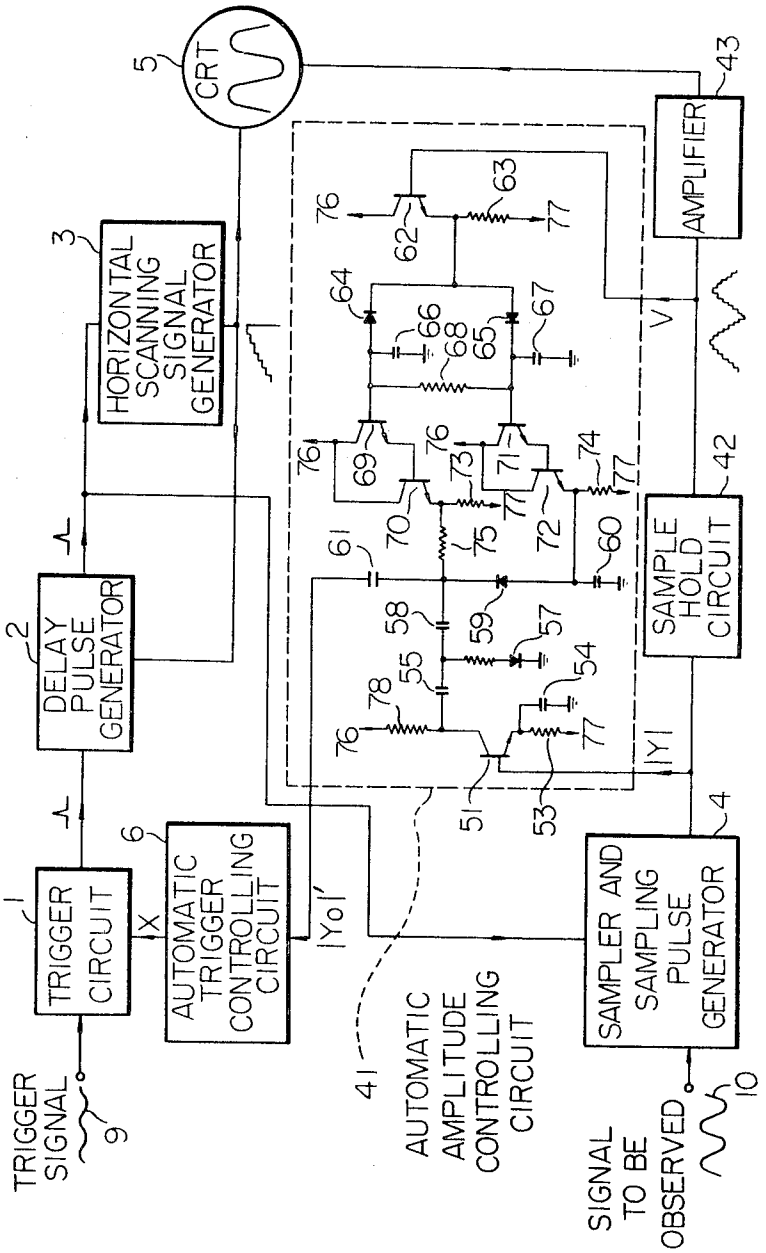
CRT
5
AMPLIFIER
43
HORIZONTAL SCANNING SIGNAL GENERATOR
3
DELAY PULSE GENERATOR
2
TRIGGER CIRCUIT
1
AUTOMATIC TRIGGER CONTROLLING CIRCUIT
6
SAMPLE HOLD CIRCUIT
42
SAMPLER AND SAMPLING PULSE GENERATOR
4
AUTOMATIC AMPLITUDE CONTROLLING CIRCUIT
41
TRIGGER SIGNAL
9
SIGNAL TO BE OBSERVED
10
X
|Yo|'
|Y|
V
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Fig. 5A

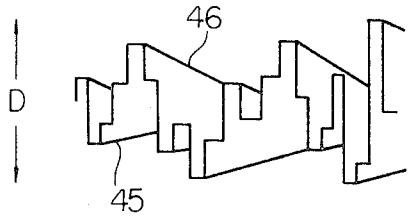


Fig. 5B

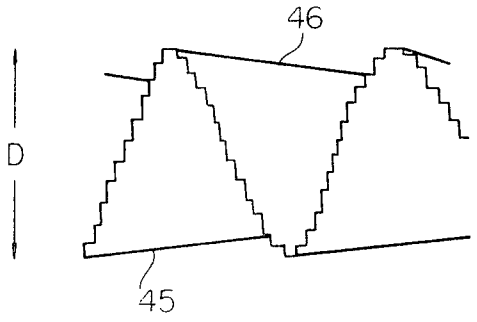
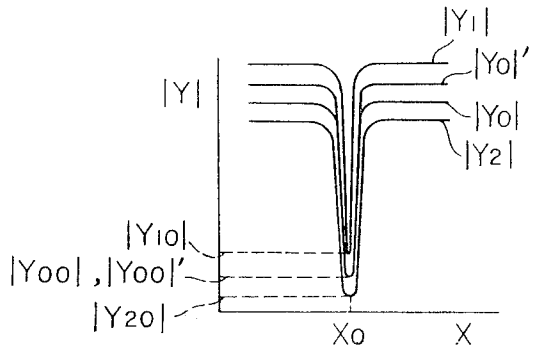


Fig. 6



TRIGGER CONTROLLING METHOD

The present invention relates to an improved trigger controlling method and, more particularly to an improved trigger controlling method for acquiring automatically and in a stable condition an output pulse synchronized with an input observing signal for all magnitudes of the input observing signal on a sampling device such as a sampling oscilloscope.

As is well-known, when an external triggering signal synchronized with an observing input signal applied a sampling device is applied to a triggering circuit, the triggering circuit generates a sequence of pulses synchronized with the above-mentioned input signal. The sequence of pulses thus generated which provides constant amplitude and constant width pulses having a frequency lower than a certain given value or the same frequency as the observing input signal is applied to a delay pulse generator. The delay pulse generator generates, by using the above-mentioned sequence of pulses, a high speed sawtooth wave which determines a time-base axis and generates a sequence of delay pulses by comparing the high speed sawtooth wave with a similar signal as a signal scanning the horizontal axis of the cathode-ray tube. The sequence of delay pulses thus obtained is applied to a sampling apparatus which generates a sampling pulse, samples the input observing signal and holds its sampled values for displaying the input signal on the cathode-ray tube via an amplifier. In order to acquire the above-mentioned sequence of pulses synchronized with the input pulse in the trigger circuit, the voltage applied to the trigger circuit or the current passing through the trigger circuit are manually or automatically controlled. However, as is well experienced by persons skilled in the art, the problem is not completely overcome for carrying out the above-mentioned triggering operation in a stable condition for all magnitudes of the input signal. In order to overcome some of the above mentioned drawbacks, the triggering method disclosed in U.S. Patent Application Serial No. 773,611, filed November 5, 1968, may be used in the sampling device, but that method does not overcome all of such drawbacks.

A principal object of the present invention is to provide an improved trigger controlling method which can overcome troublesome adjustments of the trigger circuit which adjustments are usually necessary with the conventional triggering methods.

Another object of the present invention is to provide an improved trigger controlling method which can carry out the stable triggering operation for a wide range of magnitudes of the input signal.

A further object of the present invention is to provide an improved trigger controlling method which is effectively applicable for various types of sequences of input signals to be converted into output pulses well synchronized with the input signals.

Further features and advantages of the present invention will be apparent from the ensuing description, reference being made to the accompanying drawings to which, however, the scope of the invention is in no way limited.

FIG. 1 is a circuit diagram of an embodiment of a circuit used in the present invention,

FIGS. 2A to 2E is an explanatory diagram for showing a sampled waveform of a sine wave obtained by the sampling device of FIG. 1,

FIG. 3 is an explanatory diagram of the principle adopted in the circuit shown in FIG. 1,

FIG. 4 is another circuit diagram of another embodiment of a circuit used in the present invention,

FIGS. 5A and 5B is an explanatory diagram for showing a sampled waveform of a sine wave obtained by the sampling device of FIG. 4,

FIG. 6 is an explanatory diagram of the principle adopted in the circuit shown in FIG. 4.

Referring to FIG. 1, the trigger controlling method of the present invention comprises a trigger circuit 1, a delay pulse generator 2, a horizontal scanning signal generator 3, a sampler 4, a cathode-ray tube 5, an automatic trigger controlling circuit 6, a blanking signal source 11 and an automatic amplitude controlling circuit 7. An input signal to be observed 10 is applied to the sampler 4, a differentiated output of the sampler 4 is applied to the trigger circuit 1 via the automatic amplitude controlling circuit 7 and the automatic trigger controlling circuit 6. A trigger signal 9 is also applied to the trigger circuit 1. The output of the trigger circuit 1 is applied to the delay pulse generator 2 and the output of the delay pulse generator 2, that is, the delay pulse is applied to the horizontal scanning signal generator 3 and the sampler 4. An output of the horizontal scanning signal generator 3 is applied to the delay pulse generator 2 and to the horizontal axis of the cathode-ray tube 5. An output of the sampler 4 is applied to the vertical axis of the cathode-ray tube 5. The horizontal scanning signal generator 3 and the automatic trigger controlling circuit 6 are, for example, provided for a staircase wave generator.

The automatic amplitude controlling circuit 7, as illustrated in FIG. 1, provides a memory circuit, and has the differentiated output of the sampler 4 applied to a base of a transistor 12 and to a base of a transistor 33. The transistor 12 is provided with an emitter follower connection, and a collector of the transistor 12 is connected to a positive source potential 35, while the emitter of the transistor 12 is connected to a negative source potential 36 via a resistor 13 and to a ground via a variable resistor 14. A sliding contact point of the resistor 14 is connected via a capacitor 17 to a base of a transistor 18 whose emitter is grounded. A collector of the transistor 18 is connected to a positive source potential 35 via a resistor 16 and to the base of the transistor 18 via a resistor 15. The collector of the transistor 18 is also connected via a diode 19 to a capacitor 20 which is provided as a memory capacitor and which has its other terminal grounded. A memory circuit is composed of the diode 19, the capacitor 20, a reset switch 21, a field effect transistor 22 and a resistor 23. A connection point of the diode 19 and the capacitor 20 is connected to a gate of the field effect transistor 22 and to one terminal of the reset switch 21 whose other terminal is grounded. The reset switch can be operated manually, mechanically or electronically. A drain of the field effect transistor 22 is connected to the positive source potential 35, and a source electrode of the field effect transistor 22 is connected to the negative source potential 36 via a resistor 23. The source output of the field effect transistor 22 is connected to a base of a transistor 24 which is provided as a polarity converter. A collector of the transistor 24 is connected to the negative source potential 36 via a resistor 26, and an emitter of the transistor 24 is connected to the positive source potential 35 via a resistor 25. The collector of the transistor 24 is also connected to an emitter of a transistor 29 via a resistor 27, and to a cathode of a diode 31 whose anode is grounded. The transistor 29 is provided for shifting a DC level, and has its collector connected to a positive source potential 35; its emitter connected to the negative source potential 36 via its resistor 28; and a base connected to a slider of a variable resistor 30 whose end terminals are connected, respectively, to the positive source potential 35 and the negative source potential 36. On the other hand, a collector of the transistor 33 is connected to a positive source potential 35 via a resistor 32 and to a connection point of the collector of the transistor 24 and the cathode of the diode 31 via a capacitor 34. An emitter of the transistor 33 is grounded. A blanking signal source 11 which is connected to the base of the transistor 18 is provided for scanning only in a predetermined direction and blanking a signal during a period of scanning in a reversed direction. Usually, a signal of a hold off circuit of a staircase wave generator in the horizontal scanning signal generator 3 is used for a blanking signal of the blanking signal generator 11.

Referring to FIGS. 2A to 2E, the explanation of the principle of the circuit shown in FIG. 1 will be given below. When a sinusoidal signal, as shown in FIG. 2A, is sampled by the sampler in a synchronizing condition, the output of the sampler becomes a sinusoidal waveform having a staircase form as

shown in FIG. 2B. As a result of this, the amplitude of the differential output becomes small as shown in FIG. 2C. However, when a signal is randomly sampled by the sampler in an unsynchronized condition the output of the sampler **4** becomes a waveform as shown in FIG. 2D. Therefore, the differentiated output of the sampler has a large magnitude of an amplitude as shown in FIG. 2E. For convenience, the detailed explanation of the automatic amplitude controlling circuit **7** will be given later. The differentiated output of the sampler causes a variation of an output of the automatic trigger controlling circuit **6**, which latter output controls a variable element such as a tunnel diode included in the trigger circuit. FIG. **3** is an explanatory diagram showing a relation between the differentiated output $|Y|$ of the sampler **4** and the output X of the automatic trigger controlling circuit **6**. In the synchronized condition, the output X of the automatic trigger controlling circuit is displaced to the synchronized point X_0, therefore, the value of the differentiated output $|Y_0|$ of the sampler **4** becomes its minimum value $|Y_{00}|$. The synchronized condition is maintained in the minimum value $|Y_{00}|$ of the differentiated output of the sampler **4**. In the unsynchronized condition, the output X of the automatic trigger controlling circuit **6** is displaced from its minimum value point X_0. Therefore, the value of the differentiated output $|Y_0|$ of the sampler becomes larger than the value of $|Y_{00}|$. For convenience of explanation, a case having only one minimum value is introduced. A discussion applied to the present case in the following description can well and similarly be applied to another case, wherein more than one minimum value is possessed by the curve. When the amplitude of the observing signal changes, its minimum value $|Y_{00}|$ varies as shown in FIG. 2C. As shown in FIG. 3, when the amplitude of the observing signal increases, its minimum value $|Y_{00}|$ becomes $|Y_{10}|$ which is larger than the value $|Y_{00}|$; and when the amplitude of the observing signal decreases, its minimum value $|Y_{00}|$ becomes $|Y_{20}|$ which is smaller than the value $|Y_{00}|$. As a result of this, it is difficult to determine the synchronization point, because for example, when the amplitude of the observing signal decreases, the synchronization point is misunderstood before reaching the value X_0. The automatic amplitude controlling circuit **7** is provided for overcoming the above-mentioned drawback.

In the non-synchronized condition, the differentiated output waveform of the sampler **4** has a large amplitude shown in FIG. 2E. This differentiated waveform of the sampler **4** is applied as a signal $|Y'|$ to the automatic controlling circuit **6** via the transistor **33** and the capacitor **34**, and thereby changes an output X of the automatic trigger controlling circuit **6**. On the other hand, the output of the sampler **4** is applied to the transistor **12** provided for the emitter follower and amplified by the transistor **18**. In this case, a minimum value of $|Y|$ is proportional to an input signal and accordingly the output of the transistor **18** is proportional to an input signal. The output of the transistor **18** is stored into the capacitor **20** via a diode **19**. Field effect transistor **22** is used for maintaining this stored value in the capacitor **20** for a long time. The stored DC signal in the capacitor **20** is applied as an amplitude limiting current **37** to the diode **31** via the transistor **24**, thereby always maintaining a value $|Y'|$ applied to the controlling circuit at a constant value, for example, $|Y_0|$. When a value of X does not reach the value of X_0, the value of $|Y'|$ does not become $|Y_{00}|$, so that the synchronizing condition is not obtained, and the automatic amplitude controlling circuit **7** renders the value of X variable. When the synchronizing condition is obtained in accordance with the variation of X, the output $|Y|$ of the sampler **4** is as shown in FIG. 2C. Therefore, the signal $|Y'|$ applied to the automatic trigger controlling circuit becomes $|Y_{00}|$. As a result of this, the automatic trigger circuit **6** ceases its operation and the value of X becomes X_0. In this condition, if the amplitude of the signal increases without changing the current **37**, $|Y'|$ becomes $|Y_1|$ at the same time $|Y|$ become $|Y_1|$, and then the synchronizing condition cannot be obtained in X_0. Under the present circumstances, the signal $|Y|$ is also applied to the transistor **12** and a larger value of the signal is stored in the capacitor **20**. Accordingly, the signal **37** also becomes a larger current and is applied to the diode **31**, thereby controlling the amplitude of $|Y_1|$. As a result of this, $|Y_0|$ is picked out as $|Y'|$ and becomes $|Y_{00}|$ in X_0. When the observing signal **10** decreases, $|Y|$ becomes $|Y_{20}|$. And if the signal **37** does not change, $|Y'|$ becomes also $|Y_{20}|$ and then the synchronizing condition cannot be obtained, because the automatic trigger controlling circuit **6** ceases operating without reaching the synchronizing point X_0. At this time, the signal stored in the capacitor **20** is discharged by a switch **21**, and newly automatically stores the value proportional to $|Y|$, the signal **37** applied to the diode **31** decreases and $|Y_2|$ is changed to $|Y_0|$ and applied to the automatic trigger controlled circuit **6**. Accordingly, the synchronizing condition is obtained at the synchronizing point X_0. The switching operation of the switch **21** can be carried out manually; or, an electronic or mechanical switch having a predetermined time constant can be used for this purpose.

FIG. **4** shows another embodiment of the present invention. FIG. **4** is similar to FIG. **1** except for the construction of the automatic synchronizing amplitude control circuit **41**. Further in FIG. **1**, for convenience of explanation, a sample hold circuit **42** and an amplifier **43** of FIG. **4** are included in the sampler. Referring to FIG. **4**, the differential output of the sampler **4** is connected to a base of a transistor **51** whose collector is connected through a resistor **78** to a positive source potential **76**. An emitter of the transistor **51** is connected through a resistor **53** to a negative source potential **77** and through a capacitor **54** to ground. The collector of the transistor **51** is connected through a capacitor **55** to a series circuit composed of a resistor **56** and a diode **57** whose cathode is grounded. A connection point of the capacitor **55** and the series circuit is connected through a capacitor **58** to a cathode of a diode **59** that is provided for an amplitude control diode. On the other hand, an output of the sample hold circuit **42** is connected to a base of an NPN transistor **62** whose collector is connected to a positive source potential **76**. An emitter of the transistor **62** is connected through a resistor **63** to a negative potential **77**. An emitter follower output of the transistor **62** is connected to a cathode of a diode **64** and an anode of a diode **65**. An anode of the diode **64** and a cathode of the diode **65** are respectively connected to a capacitor **66** and a capacitor **67**, and to a base of a transistor **69** and a base of a transistor **71**. Other terminals of capacitors **66** and **67** are grounded. A resistor **68** is connected between the bases of transistors **69** and **71**. NPN transistors **69**, **70** and **71**, **72** are provided in a Darlington configuration having a high impedance input circuit, and a field effect transistor can be used instead. Emitters of the transistors **70** and **72** are connected, respectively, through resistors **73** and **74** to a negative source potential **77**. The emitter of the transistor **70** is connected through a resistor **75** to a cathode of the diode **59**, and the emitter of the transistor **72** is connected to an anode of the diode **59**. A connection point of the anode of the diode **59** and the emitter of the transistor **72** is connected alternatingly through a capacitor **60** to ground. An output of the automatic amplitude control circuit **41** is connected to the automatic trigger controlling circuit via a capacitor **61**.

Referring further to FIG. **4**, in the non-synchronized condition, a differential output waveform shown in FIG. 2E of the sampler is applied to the diode **59** via the transistor **51**. On the other hand, an output signal shown in FIG. 2D of the sample hold circuit **42** is applied through the emitter follower transistor **62** to the cathode of the diode **64** and the anode of the diode **65**. The capacitors **66** and **67** are provided as an integrator constituting the storing elements. Output signals stored in the capacitors **66** and **67** are varied respectively with the time constant τ determined by the resistor **68** and the capacitors **66** and **67**. That is, the negative stored level **45** varies toward the positive stored level **46** and the positive stored level **46** varies toward the negative stored level **45** as shown in FIGS. **5A** and **5B**. The difference between the level **45** and **46**

is maintained at the zero level in the condition where no observing signal exists. When the output voltage V is a random staircase wave, the difference between the levels **45** and **46** becomes irregular and the mean difference voltage becomes smaller than the maximum value of the observing signal. This difference voltage is applied to a diode **59** via transistors **69**, **70** and **71**, **72** and a resistor **75**. On the other hand, the amplitude of the differential output applied to the diode **59** is controlled by the above-mentioned difference voltage and is applied to the automatic trigger controlling circuit **6** via a capacitor **61**, as $|Y_0|$ or $|Y_0|'$ larger than $|Y_0|$ as shown in FIG. **6**. The output X of the automatic trigger controlling circuit **6** varies in accordance with the value $|Y_0|'$. When the value X approaches the synchronization point X_0, the value $|Y|$ attains its minimum value in the value X_0. At the same time, the output signal V becomes a regularly sampled staircase waveform larger than the randomly sampled output signal as shown in FIG. **5B**. Accordingly, the minimum value of $|Y_0|'$ becomes $|Y_{00}|$ in the state of $|Y_0|$ or $|Y_{00}|'$ near $|Y_{00}|$, then, the synchronizing condition is obtained. The time constant τ which determines the voltage differences **45** and **46** is selected in such a manner that the value $|Y_0|'$ doesn't exceed the value $|Y_{00}|'$ in the synchronizing condition even in the minimum voltage difference between the voltages **45** and **46**.

When the observing signal increases, the differential output $|Y_0|$ increases and the random observing signal V increases. Consequently, the voltage difference between **45** and **46** shown in FIG. **5** also increases and an input of the automatic trigger controlling circuit becomes $|Y_0|'$. When the synchronized condition is obtained, the output signal V increases and $|Y_0|'$ becomes $|Y_{00}|'$ or a value nearly equal to $|Y_{00}|'$.

When the observing signal decreases, the differential output $|Y_0|$ decreases and the random observing signal V decreases. Consequently, the voltage difference between **45** and **46** shown in FIG. **5** also decreases and the differential output applied to the automatic trigger controlling circuit **6** increases and becomes $|Y_0|'$. When X becomes X_0 and $|Y_0|'$ decreases in the synchronizing condition, the output signal V increases and $|Y_0|'$ becomes its minimum value $|Y_{00}|'$ or a value nearly equal to $|Y_{00}|'$. As a result of this, the response of the automatic trigger controlling circuit **6** ceases and the synchronizing condition is maintained. Referring to FIG. **4**, the resistor **56** and the diode **57** are added in such a manner that the differentiating output applied to the diode **59** is a proportional relation with an amplitude of the observing signal.

When no observing signal exists, the value $|Y_0|'$ has a value $|Y_{00}|'$ or a value nearly equal to $Y_{00}|'$. On the other hand, when one cycle of the observing signal does not appear on the display surface in the synchronizing condition and the voltage difference between **45** and **46** decreases, the differential output $|Y|$ decreases and the value $|Y_0|'$ becomes $|Y_{00}|$ or a value nearly equal to $|Y_{00}|'$. As mentioned above, by using the voltage difference between **45** and **46** as the amplitude controlling signal of the amplitude control circuit, an automatic synchronizing condition can be obtained independent of the amplitude of the observing signal as well as the frequency of the observing signal. For the above-mentioned explanation, NPN transistors are used. However, PNP transistors can be used with some consideration to the polarity of the potential source. If necessary, the amplifiers or emitter follower circuits can be effectively used. Further, negative polarity signals are used as the differential outputs of the automatic triggering circuit. However, positive polarity signals can be used by reversing the polarity of the diodes **57**, **59**, **64** and **65**. The amplifier can be deleted in the case where the differential output $|Y|$ has a sufficiently large value.

As mentioned above, by using the automatic trigger controlling circuit of the present invention, the synchronizing condition can be obtained automatically and over a wide range, independent of the variation of the amplitude of the observing signal.

Modifications of the herein disclosed circuits will occur to those skilled in the art and various combinations of the circuits will be capable of use together for achieving the desired results of the invention. The scope of the invention is to be interpreted accordingly as defined by the appended claims.

What is claimed is:

1. An improved method for controlling a trigger signal for a sampling device including a sampler circuit for sampling and holding an input signal, and a trigger circuit for said sampler circuit, wherein the sampler circuit provides an output signal to be displayed, comprising the steps of differentiating the output signal of the sampler circuit to provide a differentiated output signal, producing a DC signal proportional to the differentiated output signal, storing the DC signal, modifying the amplitude of the differentiated output signal in response to variations in amplitude of the DC signal, applying the modified differentiated output signal to the trigger circuit for producing a trigger signal, and applying the trigger signal to the sampler circuit.

2. An improved trigger controlling method as set forth in claim **1**, further comprising the step of limiting the modification of the differentiated output signal when said differentiated output signal is below a predetermined minimum signal level.

3. An improved trigger controlling method as set forth in claim **1**, further comprising the step of selectively erasing said stored DC signal.

4. An improved method for controlling a trigger signal for a sampling device including a sampler circuit for sampling and holding an input signal, and a trigger circuit for said sampler circuit, wherein the sampler circuit provides an output signal to be displayed, comprising the steps of applying the output signal of the sampler circuit to a capacitive memory circuit, charging the capacitive memory circuit to a voltage level proportional to a maximum amplitude of the sampler circuit output signal, differentiating the output of the sampler circuit to produce a differentiated output signal, modifying the amplitude of the differentiated output signal in response to the voltage level of the memory circuit, discharging the capacitive memory circuit over a predetermined period, applying the modified differentiated output signal to the trigger circuit for producing a trigger signal, and applying the trigger signal to the sampler circuit.

5. An improved trigger controlling method as set forth in claim **4**, further comprising the step of limiting the modification of the differentiated output signal when said differentiated output signal is below a predetermined minimum signal level.

6. An improved trigger controlling method as set forth in claim **3**, wherein said step of storing a DC voltage is performed by charging a capacitor,

and wherein said step of erasing said stored DC voltage is performed by shorting said capacitor.

7. An improved trigger controlling system for a sampling apparatus comprising a sampler circuit for sampling and holding an input signal to be observed and for producing an output signal to be displayed, a differential circuit for differentiating the output of said sampler circuit to produce a differentiated output signal, a trigger circuit having an output connected to the sampler circuit, automatic trigger controlling circuit means having an output connected to said trigger circuit for controlling an output signal of said trigger circuit, automatic amplitude controlling circuit means connected between said differential circuit and said automatic trigger controlling circuit, said automatic amplitude controlling circuit means including a memory circuit means for storing a DC signal proportional to said differentiated output signal of said differential circuit, and an amplitude controlling diode means for modifying said differentiated output signal in response to said DC signal, and means connecting said modified differentiated output signal to said trigger controlling circuit means thereby automatically and in a stable manner obtaining a synchronized condition.

8. An improved trigger controlling system for a sampling apparatus comprising sampler circuit means for sampling and holding an input signal and for producing a sampled output signal; amplitude controlling means including a differentiating circuit having an input connected to said sampler circuit means for producing a differentiated signal at an output thereof, capacitive memory circuit means including capacitor means and having an input connected to said sampler circuit means for charging said capacitor means to a voltage level proportional to a maximum amplitude of the sampler circuit means output signal, means for modifying said differentiated signal in response to said charged voltage level of said capacitor means to produce a modified differentiated signal, and discharging means connected to said capacitor means for discharging said charged voltage level over a predetermined time-constant period; a trigger generating circuit having an output connected to said sampler circuit means; and automatic trigger controlling means having an input connected connected to receive said modified differentiated signal, and an output connected to said trigger generating circuit, whereby said sampler circuit means is automatically and stably synchronized.

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