

[54] ELEVATOR CAR STOPPING STATUS
EVALUATION MEANS
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[58] Field of Search 340/19, 20

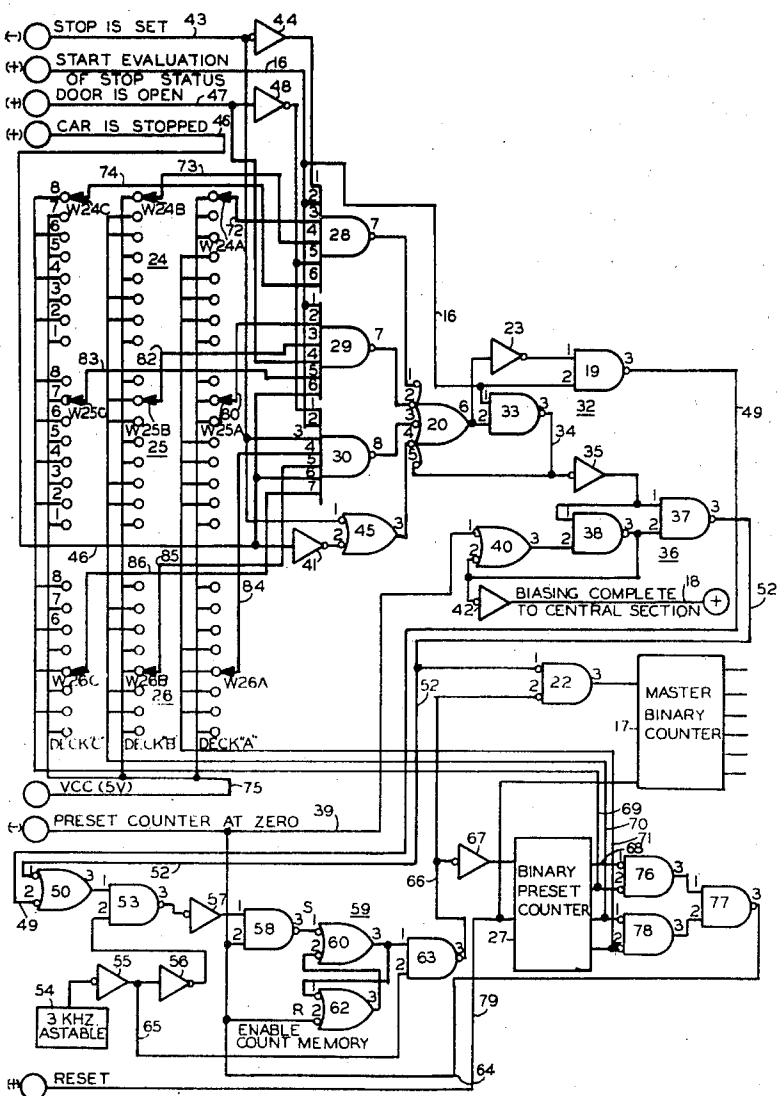
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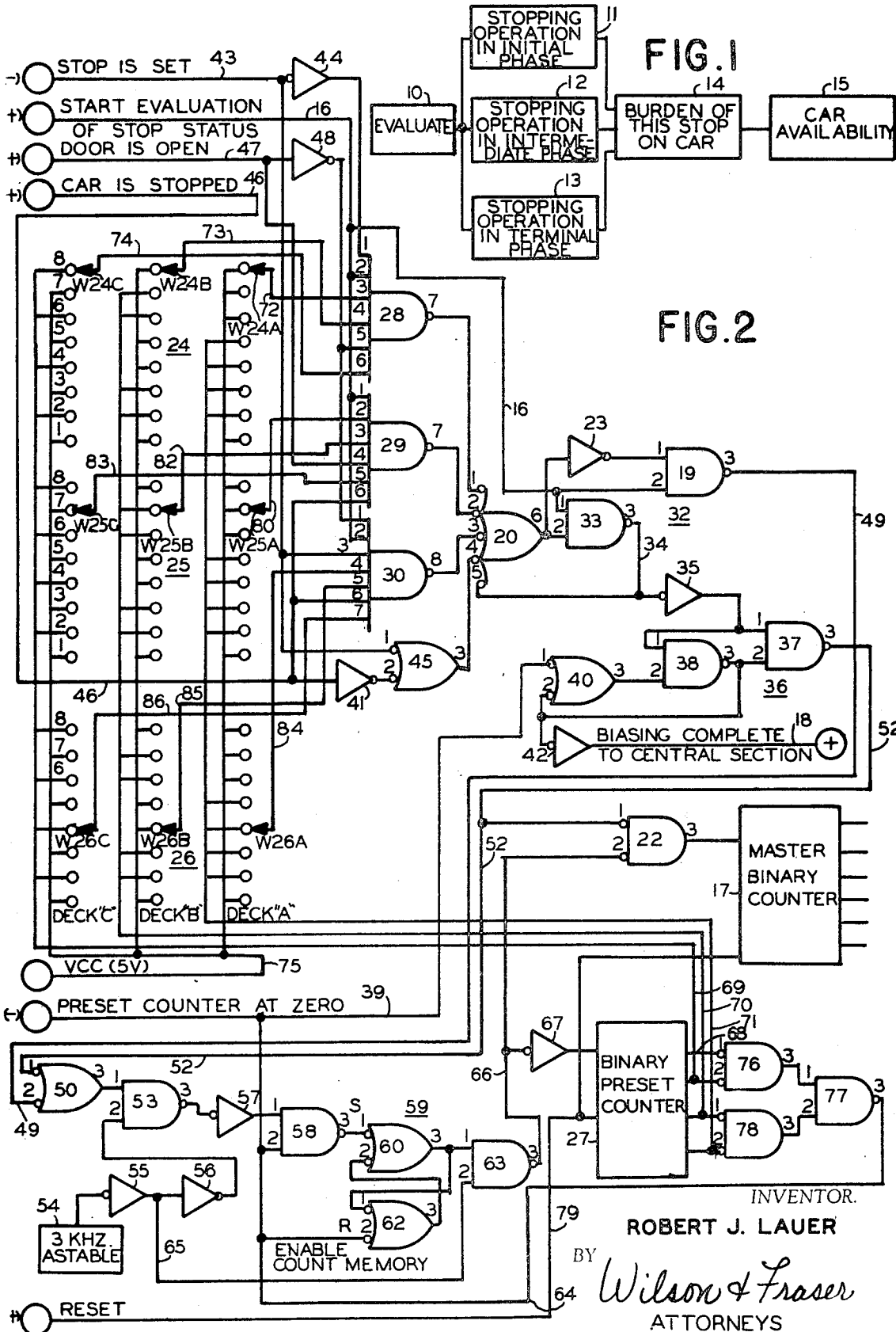
[57] ABSTRACT

A means of defining the anticipated delay until a stopped automatically restarted elevator car at any of a number of landing will again be running. Signals issued in conventional automatic elevator stopping sequences and characteristic of predetermined instances spaced in time during the stopping sequences are employed to gate portions of a pulse train to a pulse counter. The number of pulses gates is scaled to the anticipated delay so that the count in the counter is indicative of that anticipated delay either alone or combined with other factors characteristic of delays to indicate a car's availability for service.

9 Claims, 2 Drawing Figures

[56] References Cited
UNITED STATES PATENTS
3,511,342 5/1970 Hall et al. 187/29 R
3,643,762 2/1972 Schibli 187/29 R





ELEVATOR CAR STOPPING STATUS EVALUATION MEANS

CROSS-REFERENCE TO RELATED APPLICATIONS

This invention relates to the system disclosed in the applications of Gerald D. Robaszkiewicz for "Elevator Control For Optimizing Allotment of Individual Hall Calls to Individual Cars" and "Multiple Digital Comparator" which were filed June 10, 1971, Ser. No. 151,778 and filed June 9, 1971 Ser. No. 151,437, respectively.

FIELD OF THE INVENTION

The present invention relates to elevator controls and more particularly to means for evaluating the service burden imposed upon elevator cars which tends to retard their response.

BACKGROUND OF THE INVENTION

Information concerning the availability of an elevator car for service is significant in directing operation of that car and any cars with which it may be associated. It was recognized early in the development of automatic elevators that car loading was one such factor and many controls have been arranged to take this into consideration. The number of car calls registered in a car is another factor which has been related to the car's availability and utilized in elevator system controls. U.S. Pat. No. 3,511,342 which issued May 12, 1970 for "Elevator Control for Ascertaining The Capability of Cars To Serve Hall Calls" to Donivan L. Hall, William C. Susor and James H. Kuzara is for a system which seeks to assign registered hall calls individually to the car of a group of cars which is best situated from the standpoint of the service burden imposed upon it to serve the hall call. The Hall et al. control optimized allotment of individual hall calls to individual cars considering the assigned hall calls and car calls imposed on individual cars, their loading and their distance from the hall call. Improvements have added the special status of a car which might retard its response such as a parking status at the lobby or a partial shutdown as where the m-g set is off. These controls effectively establish a prediction of the delay to be anticipated in causing the car to travel to the floor of the allotment call, which has been found to be quite accurate.

The present invention enhances the precision of the prediction of delay time by introducing an indication of the stop time to be expected where a car is in a stopping status at the time the service burden on the car is considered. A greater optimization of the allotment process is thereby achieved.

SUMMARY OF THE INVENTION

This invention utilizes the delay to be anticipated for a car committed to stop or stopped as a measure of one service burden imposed on the car. A stopping operation of the car actuates various controls in a predetermined sequence. These sequences normally consume predetermined time intervals in a stop having no extraordinary operations such as the holding of a door or a reopening of a door once it has initiated its closing. Advantage is taken of these sequences to establish a measure of the interval remaining before the car can again be started in motion from the stop to which it is committed.

In the example to be presented, the delay to restarting or the capacity to restart is defined digitally as a series of pulses to a pulse counter. This is done to permit combination with other factors represented as pulse counts particularly where each count is scaled to time, as 0.5 second per pulse, representing the delay in service imposed by the imposed service conditions. It should be appreciated, however, that the measurement can be employed alone to indicate with precision the availability of a car for service. The measure can also be defined as threshold levels as by operating a short delay relay or a long delay relay or by analogue techniques as with an analogue summing circuit. Where the availability of the car or service burden imposed upon it are to be ascertained by this stopping status evaluation means a digital counter can be read by conventional means or as shown in the above noted second patent application and an analogue summer can be read by an analogue signal comparator.

The example illustrates three phases or modes of stopping status as discrete intervals. The greatest delay is imposed if at the time the evaluation is made the car is in the interval from the institution of the stop to the time the car is fully stopped. This is represented by a long train of pulses and is designated as the "car slowdown mode." If the car is stopped with its doors open a delay interval of intermediate length can be anticipated in the door open time and the time to bring the car back into effective travel, hence the "door open mode" produces a pulse train of intermediate length. At the end of the door open interval a further delay in bringing the car up to speed including the door closing time and acceleration time are factors considered as the "car acceleration mode" and represented as a relatively short pulse train. It is to be recognized that these modes develop a cumulative delay in the inverse order recited above. That is, the door open mode includes the acceleration mode and the car slowdown mode includes the door open mode and thus also the acceleration mode. Additional subdivision of a stopping sequence can be undertaken, for example, by distinguishing within the slowdown between slowdown prior to the car's entry into the leveling zone and the final slowdown to a stop in the leveling zone, or during acceleration mode a subdivision could be made between door closing and acceleration up to full speed. With further refinement, the entire stopping mode could be represented as a continuously decreasing delay factor.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a functional block diagram of the invention; and

FIG. 2 is a logic diagram of a digital stopping status evaluation means according to this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The functional block diagram of FIG. 1 represents the invention apart from a control system and elevator car or cars with which it might be combined. The represented functions have been utilized as a portion of a supervisory control as illustrated for allotting individual hall calls to the car of a plurality having the optimum service capability with respect to the call as based upon a prediction of the delay of the car in reaching the floor of the call. A number of factors are considered in addition to each car's stopping status including car loading,

the operative state of the car's motor-generator set, the special service status of the car, hall calls assigned the car, and car calls assigned the car. This system is more fully disclosed in the above-noted G. D. Robaszkiewicz co-pending patent application for "Elevator Control for Optimizing Allotment of Individual Hall Calls to Individual Cars." In that system each of the factors for each car is represented by a pulse count, either as a preset or as a train of pulses, applied to a counter for the car termed a master binary counter. The pulses are scaled to time as time delays anticipated to be imposed on the car for each factor. A generation of pulse counts is instituted when a hall call is registered to cause a call allotment to be initiated and results in an assignment of the call subject to allotment to the optimum service car as ascertained by the car having the lowest count in its master binary counter.

The present invention as represented in FIG. 1 can be considered to be placed in operation when a stopping status evaluation is requested, as during a hall call allotment, indicated by the block 10. The car may be running with no call imposed in which case no stopping status evaluation is undertaken or alternatively it may be in a stopping mode wherein one of its control elements indicates at 11 that the stopping operation is in its initial phase as the signal to stop has been applied to initiate the slowdown to the floor of the call. If the car is in its intermediate stopping phase, another of its controls associated with that portion of its operation is operated as represented at 12 as to indicate the door is fully open. If the stopping operation is in its terminal phase, a third control such as a car start signal or a door close signal as at 13 is operated. Each of 11, 12 or 13 actuate a suitable signal means indicating the burden imposed on the car in terms of the delay until the car will be started as at 14 and this signal is translated to car availability for service at 15. In a multicar system each car is provided with the generally described combination depicted in FIG. 1.

FIG. 2 shows a single car stopping status evaluating means. In the first of the above noted Robaszkiewicz patent applications, this type of means is employed for each of a plurality of elevator cars operating as a system to ascertain which car has the least service burden with respect to a hall call and to assign the hall call to that car. All cars' evaluation means are operated essentially simultaneously after their per floor service burdens have been scanned completely and several static individual car service burden evaluations have been completed as indicated by a (+) signal on lead 16. The stopping status for each car is evaluated and then the summed service burden as represented by the total accumulated count in master binary counter 17 is compared for all cars to ascertain which has the lowest burden and should receive the assignment. The stopping status evaluating means will be described for one car with reference to FIG. 2 and considering no other service burden factors.

If a car is not in a stopping phase when the signal START EVALUATION OF STOP STATUS is imposed on 16 the evaluation sequences are skipped and a signal BIASING COMPLETE TO CENTRAL SECTION is issued at lead 18. A combination of gates issues this signal under these circumstances or upon the conclusion of the signal generation indicating stop status.

In the drawing NAND and NOR gates are depicted by standard symbols as NAND gates 19 and 20 respectively representing a two input and a five input gate employed for a logical "and" and a logical "or" function. NOR 22 is employed as an "and" in the logic. As is conventional the NANDs issue a (+) when any input is (-) and a (-) when all inputs are (+) while the NORs issue a (-) when any input is (+) and a (+) when all inputs are (-). Typically, the gates and the inverters such as 23 are integrated circuits available from Fairchild Semiconductor Division of Fairchild Camera and Instrument Corporation, 313 Fairchild Drive, Mountain View, Calif., such as SN7400N, SN7410N, SN7420N and SN7430N NAND units and SN7402 NOR units. The binary counters are also integrated circuits as one or more 4 bit binary counters SN7493N from the same source.

In the detailed discussion, the logic elements will have their terminals numbered and designated by the element's reference character followed by the terminal number separated by a dash. Where signals are discussed as applied to or issuing from the terminals, their sign will be indicated by a suffix (+) for a positive going signal and (-) for a negative going signal. Thus NAND 19 will be gated when its left-hand input terminals are both positive, designated 19-1+ and 19-2+, to issue a negative signal at its right-hand output terminal, designated 19-3-.

Stop status is represented as a pulse count generated as the capacity complement of a count preset on adjustable, multidecked, selector switches 24, 25 and 26 applied to master binary counter 17 as a readout. This count is controlled by binary preset counter 27 and NAND count gates 28, 29 and 30 which are satisfied to admit the complement of the binary preset counter's capacity, 16 in the example, to the master binary counter 17. When any count gate is satisfied, counting gate NAND 20 is inhibited.

The condition of gate 20 controls the preset counter sequencing means 32 for the stop status evaluator. When 20 is inhibited, an advance signal is passed from NAND 33 via lead 34 and inverter 35 to master counter sequencing means 36. Sequencing means 32 also can gate binary preset counter 27 through gated NAND 19 to cause the counter to accumulate the count satisfying the inhibited gate 28, 29 or 30. Master counter sequencing means 36 admits count to the master binary counter when NAND 37 is gated and issues the signal BIASING COMPLETE TO CENTRAL SECTION on lead 18 by gating NAND 38.

Assume as a first example of operation that at the time evaluation is started, the car is not in a stop mode of operation, but is running so that the stop evaluation is skipped and a BIASING COMPLETE TO CENTRAL SECTION is issued on lead 18. A (+) on start lead 16 to sequence means 32 enables NANDS 19 and 33 with a 19-2+ and a 33-1+. Since no count is to be made, counting NAND 20 is inhibited by 20-4- to issue 20-6+, thereby gating advance NAND 33 with a 33-2+ while inhibiting preset counter NAND 19 with a 19-1- from inverter 23. NAND 33 issues 33-3- to latch 20 with a 20-5- and through inverter 35 enables master binary counter sequencing means 36 with a 37-1+ and a 38-1+.

Sequencing means 36 issues a BIASING COMPLETE TO CENTRAL SECTION as a (+) on lead 18 by gating advance NAND 38. Since the preset counter

27 was not enabled, its count remained at zero to impose a (-) on lead 39 so that NAND 40 received a 40-1- and issued a 40-3+ as a 38-2+. Coincidence of 38-1+ and 38-2+ makes 38-3- to inhibit NAND 37 with 37-2-, to latch NAND 40 with a 40-2-, and to issue through inverter 42 the (+) signal on lead 18.

Where the car is in a stopping mode of operation, NAND 20 is enabled at the time lead 16 receives a (+) signal so that it issues 20-6- to inhibit NAND 33 and gate NAND 19. In the example, three stopping modes are considered. If a stop is set as by the initiation of the slowdown of the car from its running speed to stop it at a floor, a STOP IS SET SIGNAL is present as a (-) on lead 43. This partially enables car slowdown count gate 28 through inverter 44 to impose 28-1+, inhibits car acceleration gate 30 by a 30-3- and inhibits NAND 45 by 45-1-. NAND 45 issues a 45-3+ to satisfy NAND 20 with a 20-4+. Only gate 28 can be enabled if the car is in its slowdown mode since the car is not stopped and, therefore, lead 46 has a (-) signal as 29-6- and 30-6- to inhibit the car door open gate 29 and car acceleration gate 30.

If the car were in the door open mode, as where it is stopped and the door is open to a predetermined degree, a door open limit indicates the door is open to within at least 2 inches of its full open position, a (+) signal is present on lead 47. This signal can be arranged to be cancelled as soon as the car receives a door close signal. With lead 47 (+) 29-4+ enables NAND 29 and inverter 48 by 28-5- and 30-1- inhibits 28 and 30. STOP IS SET signal remains as a (-) on lead 43 to cause NAND 45 to provide a 20-4+ and satisfy NAND 20 so the count sequence can proceed.

The acceleration mode can be measured from the issuance of the car start signal as where door closing is initiated to make lead 47 (-), and can extend until the car starts to move when lead 46 is made (-). At this time the STOP IS SET signal is cancelled, hence lead 43 is (+) and NAND 45 is inhibited by the (+) of the starting signal on lead 46 through inverter 41 to make 45-2- and 45-3+ to gate NAND 20. As the door close signal is imposed, lead 43 goes (+) to inhibit through inverter 44 the car slowdown NAND 28 at 28-1- and directly enable 30 by 30-3+. Lead 47 (-) inhibited the car door open NAND 29 by 29-4- and enabled 30 through inverter 48 by 30-1+. 28-5+ has no effect at this time because of 28-1-. The car has not yet begun to move under these circumstances so lead 46 is (+) to apply an enabling 30-6+.

Assume first that a car has picked up a stopping signal but has not opened its door. NAND 20 is gated since all of its inputs are (+). That is 28, 29 and 30 are all inhibited since they have no count. NAND 45 is inhibited by the STOP IS SET signal on 43 which makes 45-1- and 45-3+, and the latch is released to make lead 34 (+). Counting gate 20 issues a 20-6- which is inverted to a 19-1+ by inverter 23. Since 19-2+ was imposed by the start signal, 19-3- issues on lead 49 to binary preset counter control NAND 50 as 50-2-. At this time the master count gate 37 of sequence means 36 is inhibited to issue a 37-3+ on lead 52 to apply 50-1+ so that the shift of 50-2 from (+) to (-) causes 50-3 to shift from (-) to (+) thereby enabling NAND 53. NAND 53 institutes admission of pulses to the counters.

An astable 54 generates pulses continuously at 3 KHZ so that the first positive going signal twice in-

verted in inverters 55 and 56 gate 53 to issue a pulse 53-3-. This pulse is inverted at 57 to impose 58-1- on NAND 58 to set ENABLE COUNT MEMORY flip flop 59 made up of cross connected NANDs 60 and 62. When memory 59 is set by a negative signal on its set lead as 60-1-, it issues and maintains a 60-3+ enabling signal on pulse admitting NAND 63 until a signal is applied to lead 64 to make reset input 62-2 (-).

With NAND 63 enabled by 63-1+, the negative going pulses from astable 54 inverted to lead 65 by inverter 55 appear as 63-2+ to gate a 63-3- to lead 66 whereby inverter 67 applies advance counts to binary preset counter 27.

Counter 27 has four stages and corresponding outputs at lead 68, 69, 70 and 71 for a count one, two, four and eight respectively. It issues (+) signals at its output to the switches 24, 25 and 26 at their decks A, B and C through the eight, four and two count leads 71, 70 and 69 respectively. Wipers for each deck are designated by the prefix W and the suffix of the deck. Thus, signals are passed by wiper W24A on lead 72 to 28-3, from W24B on lead 73 to 28-4, and from W24C on lead 74 to 28-6. A constant (+) bias can be applied to any of the wipers from a suitable source (not shown) coupled to lead 75 so that, with the ganged wipers of switch 24 at the uppermost position, a (+) signal from lead 75 is coupled to leads 72 and 73 continuously, whereby gate 28 required only a count of two in binary preset counter 27, imposing a (+) on lead 69 through W24C to lead 74 to impose (+) coincidence on the inputs to 28.

When 28 is satisfied, it issues a 28-7- appearing as 20-1- to inhibit NAND 20 which issues 20-6+ to inhibit NAND 19 and gate NAND 33, thereby advancing the sequence to sequence means 36 by a (+) signal from inverter 35. NAND 37 is gated to issue a 37-3- on lead 52 because the partial count in binary preset counter has imposed a (+) on lead 39 to gate NAND 40 and by 40-3- as 38-2- to inhibit NAND 38.

Counter 27 made lead 39 (+) as soon as a count was entered to make lead 68 (+) and thereby cause NOR 76 to inhibit NAND 77 when 76-1 made 76-3- to 77-1- and thus 77-3+. This lead 39 (+) condition is sustained until the capacity count of 16 or zero is achieved and all of leads 68, 69, 70 and 71 are returned to (-) whereby both NORs 76 and 78 are gated to gate NAND 77 and impose a 77-3- on lead 64 to reset the Enable Count Memory 59.

After count NAND 28 is gated to inhibit counting NAND 20, the balance of the pulse count capacity of preset counter 27 is admitted to the master binary counter 17. Thus the capacity complement of the preset value established by the setting of switch 24 is imposed on lead 66 after the count NAND is satisfied until the preset counter is filled and returned to zero. This count is admitted by enabling NOR 22 so that it gates each pulse to counter 17. A 22-1- signal is the COUNT MASTER BINARY COUNTER SIGNAL from gated NAND 37.

When the preset counter returns to zero, it resets the enable count memory 59 and inhibits NAND 40 by a 40-1- causing a 40-3+ to gate NAND 38. NAND 38 by 38-3- inhibits NAND 37 making lead 52 (+) to inhibit NAND 22 and block further pulses to master binary counter 17 and inhibit NAND 50 to block passage of further pulses by NAND 53 from astable 54. 38-3- also latches sequencer 36 by NAND 40 with a 40-2-

and by inverter 42 issues a (+) BIASING COMPLETE TO CENTRAL SECTION at 18.

The count in the master binary counter can be considered indicative of the stopping status of the car and read by conventional means (not shown) coupled to its output leads. Such readout can be enabled by the (+) signal on lead 18. Prior to the next assessment of stopping status, the master binary counter 17 and the binary preset counter are reset by a (+) signal on reset lead 79.

Similar sequences will occur if the car is in its door open phase, however, NAND 29 will provide count control to counting NAND 20 and will receive its controlling signals through decks A, B and C of switch 25. In this instance the wipers of switch 25 are connected W25A to lead 80 and 29-2, W25B to lead 82 and 29-3 and W25C to lead 83 and 29-5.

When the car is in the acceleration phase, count gate 30 controls counting gate 20 and receives its controlling signals from switch 26. Switch wipers apply their counter output or bias counterparts as an eight count level from W26A to lead 84 to 30-4, a four count level from W26B to lead 85 to 20-5, and a two count level from W26C to lead 86 to 30-7.

Selector switches 24, 25 and 26 are shown set respectively at their eighth, seventh and fourth positions to satisfy their respective car slow down count gate 28, car door open count gate 29 and car acceleration count gate 30, with a relatively short preset count of two, an intermediate preset count of four and a relatively long preset count of 10. As a result, the initial portion of the stop interval, that of slowdown, is defined by a long count of 14 into counter 17 (14 being the capacity count complement of two for preset counter 27). In a similar fashion the intermediate portion of the interval, during the door open phase, is defined by a medium length count of 12 (12 being the capacity count complement of four for preset counter 27), and the final portion of the interval, during the acceleration phase, is defined by a short length count of six (the capacity count complement of 10 for preset counter 27). These values can be adjusted by manual repositioning of the wipers of switches 24, 25 and 26. For convenience, all wipers of each switch can be coupled as by a common shaft to afford such adjustment in a single setting for each switch.

It is to be understood that analogue signals or merely on-off signals as relay controls can be substituted for the pulse count and digital read techniques employed in the example set forth above. The concept of segregating the stopping base of a car in an "early to start mode" an "intermediate delay to start mode" and a "long delay to start mode" can be expanded to a greater number of increments or modified to a continuously variable factor of the "anticipated delay to start" as a measure of car availability for additional service. While the anticipated delay to start has been employed in ascertaining one of a number of delay factors on an individual car basis for the purpose of ascertaining the car of a plurality best suited to receive assignment of a registered hall call, it is to be understood that the invention lends itself to many variations including single car control, and for purposes of control other than hall call assignment including car starting and by-passing controls. Accordingly, the above example is to be read as illustrative and not in a limiting sense.

I claim:

1. In an elevator system comprising a car serving a plurality of landings, control means stopping the car at the landings and for starting the car a predetermined interval following the stop of the car, the improvement which comprises means coupled to said control means and responsive to different discrete signals issued by said control means at predetermined times between the stopping setting of said control to stop said car at each of a plurality of said landings and the car stating operation of said control to bring said car to speed; means to initiate an evaluation of the anticipated amount of stopping interval remaining; means responsive to said signal responsive means to generate signals scaled to the anticipated remaining stopping interval and variable indicating means coupled to said signal generating means and said initiating means to indicate the anticipated remaining stopping interval at the time of operation of said evaluation initiating means.

2. A system according to claim 1 wherein said signal generating means is responsive to a first signal characteristic of the early portion of the sequence of said control means bringing said car to a stop and restarting said car at a landing and to a second signal characteristic of the portion of the sequence of said control means bringing said car to a stop and restarting said car at a landing which is later than that characterized by said first signal; and wherein said indicating means when actuated by said initiating means between said first and second signals indicates a relatively long anticipated remaining stopping interval and when actuated by said initiation means subsequent to said second signal indicates a second relatively short anticipated remaining stopping interval.

3. A system according to claim 2 wherein said signal generating means is responsive to a third signal characteristic of a terminal portion of the sequence of said control means bringing said car to a stop and restarting said car at a landing which is subsequent to that portion characterized by said second signal; and wherein said indicating means when actuated by said initiating means subsequent to said third signal indicates a shorter anticipated stopping interval than said second interval.

4. A system according to claim 3 including a car door for the car wherein said early portion occurs during deceleration of the car, said later portion occurs while the car door is open, and said terminal portion occurs upon initiation of door closing.

5. A system according to claim 1 wherein said signal generating means is responsive to a first signal from said control means characteristic of the initiation of slowdown of a car approaching a landing and to a second signal characteristic of the stopping of the car at said landing; and wherein said indicating means when actuated by said initiating means between said first and second signals indicates a relatively long anticipated remaining stopping interval.

6. A system according to claim 1 wherein said signal generating means is responsive to a first signal characteristic of the stopping of the car at said landing and to a second signal characteristic of the initiation of a car start from said landing; and wherein said indicating means when actuated by said initiating means between said first and second signals indicates a relatively short anticipated remaining stopping interval.

7. In an elevator system according to claim 1 including a car door for the car and door control means to

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control said car door position wherein said signal generating means is responsive to a first signal characteristic of said car door being at least partially open; and wherein said indicating means when actuated by said initiating means while said signal generating means is responsive to said first signal indicates a relatively short anticipated remaining stopping interval.

8. A system according to claim 1 wherein said means

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responsive to different discrete signals are controls for trains of signal pulses; and wherein said indicating means is a pulse counter.

9. A system according to claim 1 including means to adjust the magnitude of at least one signal issued by said signal generating means.

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**UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION**

Patent No. 3,742,445 Dated June 26, 1973

Inventor(s) ROBERT J. LAUER

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Abstract, line 10, after "delay" insert - - . Elevator controls
can be actuated according to the anticipated
delay - - .

Column 7, line 30, "for" should be - - four - - .

Column 7, line 51, "base" should be - - phase - - .

Signed and sealed this 14th day of January 1975.

(SEAL)
Attest:

MCCOY M. GIBSON JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents

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