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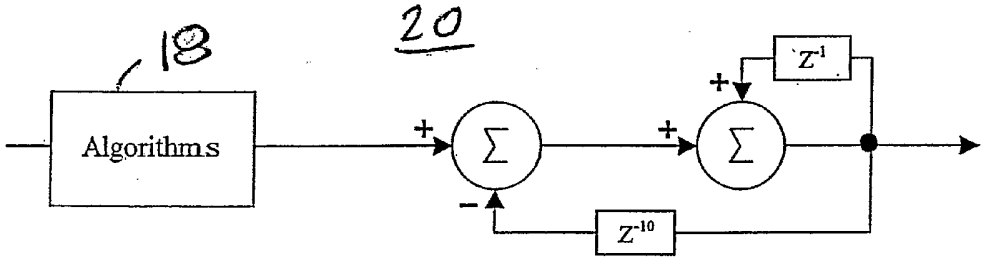
(54) Title: DIGITAL SIGNAL PROCESSOR IMPLEMENTATION OF HIGH IMPEDANCE FAULT ALGORITHMS



(57) Abstract: A digital signal processor implementation of three algorithms used to detect high impedance faults. The algorithms can be wavelet based, higher order statistics based and neural network based. The algorithms are modified to process one second of data instead of ten seconds of data and a double buffered acquisition is connected to the output of the algorithms.

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Digital Signal Processor Implementation Of High Impedance Fault Algorithms

CROSS REFERENCE TO RELATED APPLICATION

This application claims the priority of U.S. provisional patent application Ser. No. 60/553,504 filed on March 16, 2004, entitled " Digital Signal Processor Implementation Of High Impedance Fault Algorithms" the contents of which are relied upon and incorporated herein by reference in their entirety, and the benefit of priority under 35 U.S.C. 119(e) is hereby claimed.

1. Field of the Invention

This invention relates to algorithms for determining the occurrence of a high impedance fault (HIF) condition and more particularly to the implementation of those algorithms using a digital signal processor (DSP) in a relay platform.

2. Description of the Prior Art

Electric utility companies use overhead energized conductors to transport electrical energy to consumers. There are over one million miles of overhead distribution lines in the United States, supplying energy for industrial, commercial, and residential customers. The overhead conductors are exposed to the elements and to abnormal conditions. In some cases, the conductors fall to the ground and, depending on the surface, establish a conducting path. If the surface is grass, soil, or asphalt, a HIF occurs, in which case the fault current is much smaller than that of a typical phase-to-ground fault. This smaller fault current makes detection of such instances difficult with conventional protection devices.

The danger with downed or open conductors is the risk of public contact with the energized lines. Human contact with downed conductors can result in serious injury or even death. The problem is further complicated once a downed conductor is detected. If a relay trips a

circuit breaker at a substation, the loss of power to vital public entities, such as hospitals, airports, and traffic signals, can result in life-threatening situations of equal or greater magnitude. Thus, the problems facing protection engineers are to first detect the disturbances and then to react appropriately.

U.S. Patent Application Serial No. 10/770,270 filed on February 2, 2004 and entitled "High Impedance Fault Detection" ("the '270 application"), the disclosure of which is hereby incorporated herein by reference, and is assigned to the same assignee as the present invention, describes the implementation in a relay platform of three detection algorithms that each use various features of phase and/or ground currents to individually detect a HIF. The HIF detection algorithms described in the '270 application are wavelet based, higher order statistics based and neural network based. It is desirable to implement the three algorithms with a DSP as the DSP is needed for data acquisition and scaling and performs some of the work so that the CPU (central processing unit) in the relay does not have to do everything but:

each of the algorithms in their original formats cover 10 seconds worth of data and thus need a lot of computation power and precision; and

it is impossible to implement the algorithms in their original formats due to hardware limitations and floating-point computations requirements.

The present invention allows the three detection algorithms to be implemented on the relay platform with a DSP. In accordance with the present invention:

the algorithms are modified to process one (1) second of data instead of 10 seconds and circular buffering and accumulation techniques are used to achieve the solution;

double buffering is used for the acquisition; and

there is a fixed-point implementation of each

algorithm.

Summary of the Invention

A method for detecting high impedance faults in electrical power lines. The method comprises:

using a plurality of high impedance fault detection means each having an output for independently detecting the high impedance fault, each of the fault detection means detecting the high impedance faults by analyzing data from the power lines collected for a predetermined period of time and providing at the output a signal based on the analyzed data indicative of the occurrence or non-occurrence of the high impedance faults;

modifying each of the plurality of fault detection means to reduce the predetermined period of time by a factor of 1/n where n is an integer greater than one; and

connecting a buffering system to the output of each of the fault detection means to obtain from the buffering system a signal indicative of the occurrence or non-occurrence of the high impedance fault that is based on the data collected for the predetermined period of time.

A system for detecting high impedance faults in electrical power lines. The system comprises:

a plurality of high impedance fault detection means each having an output for independently detecting the high impedance fault, each of the fault detection means detecting the high impedance faults by analyzing data from the power lines collected for a predetermined period of time and providing at the output a signal based on the analyzed data indicative of the occurrence or non-occurrence of the high impedance faults, each of the plurality of fault detection means modified to reduce the predetermined period of time by a factor of 1/n where n is an integer greater than one; and

a buffering system connected to the output of each of the fault detection means to obtain from the buffering system a signal indicative of the occurrence or non-

occurrence of the high impedance fault that is based on the data collected for the predetermined period of time.

A processing apparatus for determining the occurrence of a high impedance fault in electrical power lines. The processing apparatus comprises:

two buffers each for storing data collected from the power lines for a first predetermined period of time indicative of current flow on the power lines;

a plurality of high impedance fault means each having an output for individually detecting a high impedance fault on the power lines, each of the fault detection means alternately processing for the first predetermined period of time first the data stored in one of the two buffers and then the data stored in the other of the two buffers, each of the high impedance fault detection means providing at the output a signal based on the processed data indicative of the occurrence or non-occurrence of the high impedance faults; and

a buffering system connected to the output of each of the high impedance fault detection means for obtaining a signal indicative of the occurrence or non-occurrence of the high impedance fault that is based on the data collected for a second predetermined period of time that is n times the first predetermined period time where n is an integer that is two or greater.

Description of the Drawing

Fig. 1 shows a block diagram for the double buffered acquisition system used in the system of the present invention.

Fig. 2 shows an embodiment for the circular buffering system used in the system of the present invention.

Description of the Preferred Embodiment(s)

Referring now to Fig. 1, there is shown a block diagram for the double buffered acquisition system 10. System 10 uses a first buffer 12 and a second buffer 14 to store data. While system 10 is storing incoming data

in the first buffer 12, the processing is performed on data already stored in the second buffer 14. When the first buffer 12 is filled, the switch S1 is switched to the second buffer 14 and the switch S2 is switched to the first buffer 12. The switches S1 and S2 switch back and forth every time a buffer is filled. Buffers 12 and 14 are sized to each hold one (1) second worth of data.

A band-pass filter 16 processes the data from buffer 12 or 14 and passes the filtered data to be analyzed by the algorithms 18 as shown in Fig. 1. The algorithms 18 are the three detection algorithms, namely, wavelet based, higher order statistics based and neural network based, described in the '270 application

Even though the processor time-step is equal to 32 cycles/second the results are refreshed every second since it takes one second to process a buffer worth of data.

Each of the algorithms 18 in their format described in the '270 application cover ten seconds worth of data. Since it is not possible in the present invention to implement the algorithms in that format, each of the algorithms 18 are modified to process one second worth of data at a time.

A circular buffering system 20, which is illustrated in Fig. 2, is connected to the output of algorithms 18 to obtain the ten seconds of data that would be obtained from each algorithm 18. While Fig. 2 shows only one system 20 connected to the output of algorithms 18, those of ordinary skill in the art would appreciate that there is a system 20 for each of the algorithms.

System 20, as is shown in Fig. 2, removes the first value for each 10^{th} value added. The algorithm equations were modified to compensate for the errors introduced by the non-linearity due to chopping of the ten-second interval. The data acquired for each second is processed and used as an initial condition to compute the

subsequent one-second data. The results are stored in a ten-second circular buffer used also as accumulator.

The modifications to the algorithms are as follows:

a. the calculation is performed for the 1st one second interval and the output is stored as the accumulator first value;

b. the calculated output is also used as the initial input to calculate the 2nd one second interval and the output is stored as the second accumulator value; and

c. the process continues until ten seconds are reached.

The eleventh one second is considered as the first second and the process is repeated as above. At any given time the total output is the summation of the ten buffer values.

In accordance with the present invention there is a fixed point implementation of each of the three high impedance fault detection algorithms. The algorithms were initially developed using floating-point arithmetic to verify and validate the concept then translated to fixed-point arithmetic for final implementation. Fixed-point digital signal processors are suitable for implementing a large volume of products economically because they are much cheaper, consume less power and execute faster than signal processors containing floating-point arithmetic units.

The code for each algorithm was implemented on a suitable central processing unit such as for example the Motorola ColdFire 5307 CPU with a clock speed of 66 MHz and a unified cache of 64 KB. The data acquisition is performed at a rate of 32 samples per second and the processing of the HIF algorithms is performed once per second in the highest priority task which is interrupted every 4.1ms to perform data transfer from the DSP and protection algorithms.

Results from floating-point and fixed-point simulations were compared and showed no precision lost during the conversion.

It is to be understood that the description of the preferred embodiment(s) is (are) intended to be only illustrative, rather than exhaustive, of the present invention. Those of ordinary skill will be able to make certain additions, deletions, and/or modifications to the embodiment(s) of the disclosed subject matter without departing from the spirit of the invention or its scope, as defined by the appended claims.

What is claimed is:

1. A method for detecting high impedance faults in electrical power lines comprising:

using a plurality of high impedance fault detection means each having an output for independently detecting said high impedance fault, each of said fault detection means detecting said high impedance faults by analyzing data from said power lines collected for a predetermined period of time and providing at said output a signal based on said analyzed data indicative of the occurrence or non-occurrence of said high impedance faults;

modifying each of said plurality of fault detection means to reduce said predetermined period of time by a factor of 1/n where n is an integer greater than one; and

connecting a buffering system to said output of each of said fault detection means to obtain from said buffering system a signal indicative of the occurrence or non-occurrence of said high impedance fault that is based on said data collected for said predetermined period of time.

2. A system for detecting high impedance faults in electrical power lines comprising:

a plurality of high impedance fault detection means each having an output for independently detecting said high impedance fault, each of said fault detection means detecting said high impedance faults by analyzing data from said power lines collected for a predetermined period of time and providing at said output a signal based on said analyzed data indicative of the occurrence or non-occurrence of said high impedance faults, each of said plurality of fault detection means modified to reduce said predetermined period of time by a factor of 1/n where n is an integer greater than one; and

a buffering system connected to said output of each of said fault detection means to obtain from said buffering system a signal indicative of the occurrence or

non-occurrence of said high impedance fault that is based on said data collected for said predetermined period of time.

3. The high impedance fault detection system of claim 2 further comprising two buffers each for alternately storing data collected from said power lines for said reduced predetermined period of time, each of said plurality of high impedance fault detection means alternately processing stored data for said reduced predetermined period of time from said two buffers.

4. The high impedance fault detection system of claim 3 further comprising a filter connected between said two buffers and said high impedance fault detection means.

5. The high impedance fault detection system of claim 2 wherein said buffering system is a circular buffering system.

6. The high impedance fault detection system of claim 2 wherein n is 10 and said predetermined period of time is 10 seconds.

7. A processing apparatus for determining the occurrence of a high impedance fault in electrical power lines comprising:

two buffers each for storing data collected from said power lines for a first predetermined period of time indicative of current flow on said power lines;

a plurality of high impedance fault means each having an output for individually detecting a high impedance fault on said power lines, each of said fault detection means alternately processing for said first predetermined period of time first said data stored in one of said two buffers and then said data stored in the other of said two buffers, each of said high impedance fault detection means providing at said output a signal based on said processed data indicative of the occurrence or non-occurrence of said high impedance faults; and

a buffering system connected to said output of each of said high impedance fault detection means for obtaining a signal indicative of the occurrence or non-occurrence of said high impedance fault that is based on said data collected for a second predetermined period of time that is n times said first predetermined period time where n is an integer that is two or greater.

8. The processing apparatus of claim 7 wherein said buffering system is a circular buffering system.

9. The processing apparatus of claim 7 further comprising a filter connected between said two buffers and said high impedance fault detection means.

10. The processing apparatus of claim 7 wherein said first predetermined period of time is one second and said integer is ten.

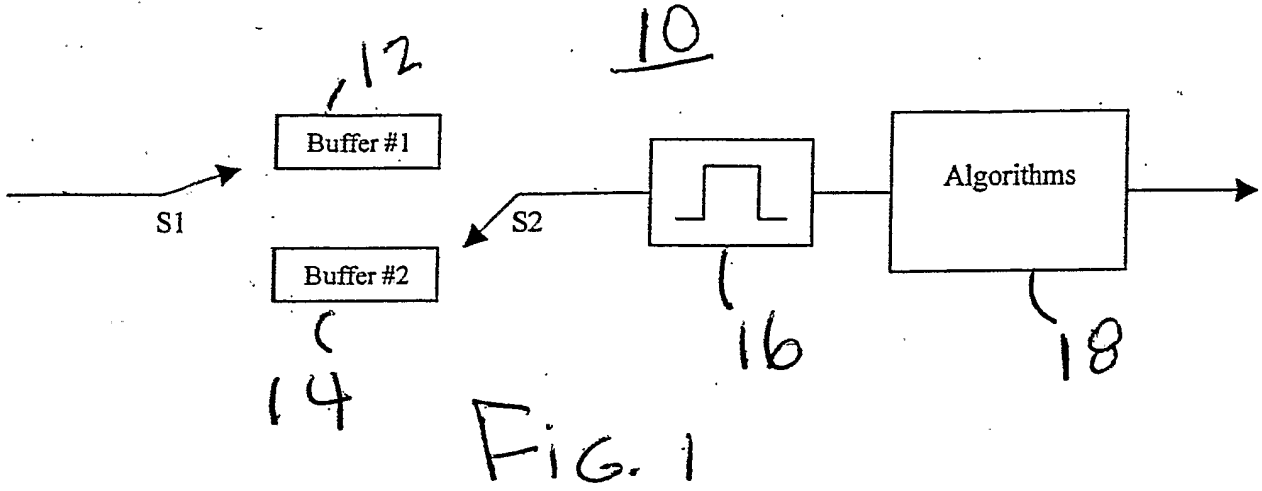
10
12
Buffer #1
S1
S2
Buffer #2
14
16
Algorithms
18

FIG. 1

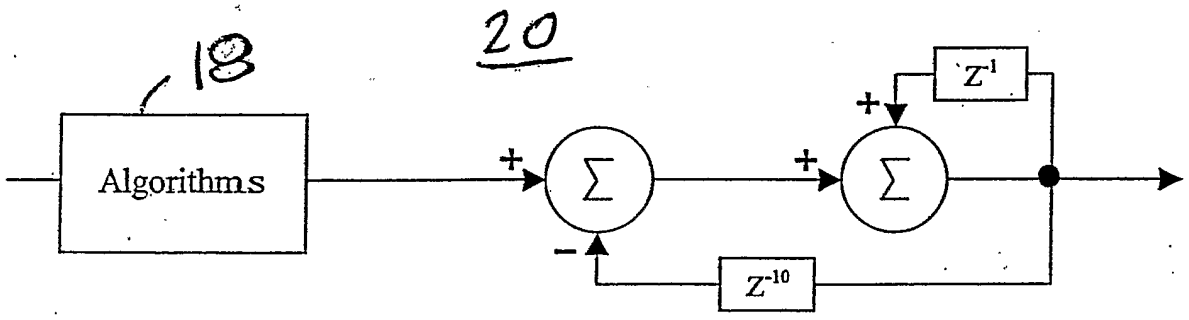
18
20
Algorithms
+
Σ
+
Σ
Z-1
+
−
Z-10

FIG. 2

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/008490

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H02H1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H02H G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 550 751 A (RUSSELL ET AL) 27 August 1996 (1996-08-27) column 7, line 3 - column 8, line 4; figures 1,2	1-10
Y	US 5 602 709 A (AL-DABBAGH ET AL) 11 February 1997 (1997-02-11) column 3, line 31 - line 56 column 10, line 17 - line 40; figure 10 column 13, line 36 - line 54	1-6
Y	PATENT ABSTRACTS OF JAPAN vol. 014, no. 298 (P-1068), 27 June 1990 (1990-06-27) & JP 02 093826 A (NEC CORP), 4 April 1990 (1990-04-04) abstract	7-10

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
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INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 485 093 A (RUSSELL ET AL) 16 January 1996 (1996-01-16) column 6, line 43 - column 8, line 12; figure 1	5,8
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