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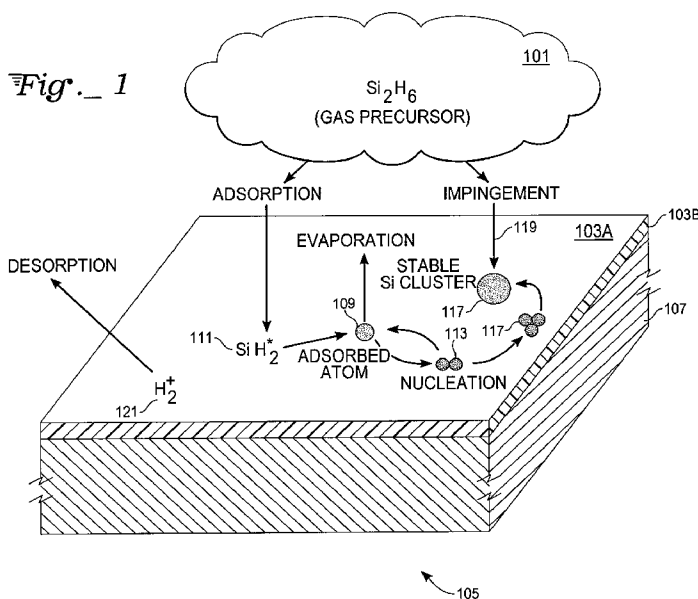
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(54) Title: GROWTH OF METALLIC NANODOTS USING SPECIFIC PRECURSORS



(57) Abstract: A technique to form metallic nanodots in a two-step process involving: (1) reacting a silicon-containing gas precursor (101) (e.g., silane) to form silicon nuclei (117) over a dielectric film layer (103B); and (2) using a metal precursor to form metal nanodots where the metal nanodots use the silicon nuclei (117) from step (1) as nucleation points. Thus, the original silicon nuclei (117) are a core material for a later metallic encapsulation step. Metallic nanodots have applications in devices such as flash memory transistors.

Description

GROWTH OF METALLIC NANODOTS
USING SPECIFIC PRECURSORS

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TECHNICAL FIELD

The invention relates generally to semiconductor devices and more particularly to a fabrication process for generating metallic nanostructures above a dielectric material.

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BACKGROUND ART

Electrically erasable programmable read only memory (EEPROM) structures are commonly used in integrated circuits for non-volatile data storage. As is known, EEPROM device structures commonly include a floating gate that has charge storage capabilities. Charge can be forced into the floating gate structure or removed from the floating gate structure using control voltages. The conductivity of the channel underlying the floating gate is significantly altered by the presence of charges stored in the floating gate. The difference in conductivity due to a charged or uncharged floating gate can be current sensed, thus allowing binary memory states to be determined. The conductivity difference is also represented by shift in the threshold voltage (V_t) associated with the device in the two different states.

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As semiconductor devices continue to evolve, the operating voltages of such semiconductor devices are often reduced in order to suit low power applications. It is desirable for such operating voltage reductions to be accomplished while ensuring that the speed and functionality of the devices is maintained or improved.

A controlling factor in the operating voltages required to program and erase devices that include floating gates is the thickness of the tunnel oxide through which carriers are exchanged between the floating gate and the underlying channel region.

In many prior art device structures, the floating gate is formed from a uniform layer of conducting or semiconducting material such as polysilicon. In such prior art device structures, a thin tunnel dielectric layer beneath the floating gate presents the problem of charge leakage from the floating gate to the underlying channel through defects in the thin tunnel dielectric layer. Such charge leakage can lead to degradation of the memory state stored within the device and is therefore undesirable. In order to avoid such charge leakage, the thickness of tunnel dielectric is often increased. However, thicker tunnel dielectric requires higher (programming and erasing) voltages for storing and removing charge from the floating gate as the charge carriers must pass through the thicker tunnel dielectric. In many cases, higher programming voltages require the implementation of charge pumps on integrated circuits in order to increase the supply voltage to meet programming voltage requirements. Such charge pumps consume a significant amount of die area for the integrated circuit and therefore reduce the memory array area efficiency and increase overall costs.

In order to reduce the required thickness of the tunnel dielectric and improve the area efficiency of the memory structures by reducing the need for charge pumps, the uniform layer of material used for the floating gate may be replaced with a plurality of nanoclusters, which operate as isolated charge storage elements. Such

nanoclusters are also often referred to as nanocrystals, as they may be formed of silicon crystals. In combination, the plurality of nanoclusters provides adequate charge storage capacity while remaining physically isolated from each other such that any leakage occurring with respect to a single nanocluster via a local underlying defect does not cause charge to be drained from other nanoclusters. That is, by controlling average spacing between nanoclusters, it can be ensured that there is no lateral charge flow between nanoclusters in the floating gate. As such, thinner tunnel dielectrics can be used in these device structures. The effect of leakage occurring in such thin tunnel dielectric devices does not cause the loss of state information that occurs in devices that include a uniform-layer floating gate.

A limiting factor in fabrication of devices that include floating gates made up of a plurality of nanoclusters relates to controlling size, density, and uniformity of the nanoclusters within the floating gate structure. The density of the nanoclusters is important in the determination of the change in the threshold voltage for the device between the states where the floating gate is charged or discharged. Higher densities are desirable as they lead to an increased change in threshold voltage when the density of charges per storage element is fixed. Prior art techniques for forming nanoclusters on the oxide tunnel dielectric were limited to a density as low as $5(10^{11})$ nanoclusters per cm^2 . More recently, nanocluster densities of $1(10^{12})$ nanoclusters per cm^2 have been reported. With such a limited density of isolated storage elements, the charge density per nanocluster, or number of carriers that each nanocluster

must retain, is forced to an elevated level. The higher storage density per nanocluster presents difficulties in storing (i.e., programming) a high number of electrons due to quantum confinement. In contrast to this
5 limitation of higher nanocluster densities, lower nanocluster densities yields a smaller programming window at a given programming time. Furthermore, the programming time required for adding subsequent carriers continues to increase as the charge density per
10 nanocluster is elevated. Even increasing the programming time may be insufficient to produce a proper number of carriers.

In one prior art technique for forming silicon nanoclusters, ion implantation is used to implant silicon
15 atoms into a dielectric material. Following implantation, an annealing step causes these implanted silicon atoms to group together through phase separation to form the nanoclusters. Problems arise using such a technique due to the difficulty in controlling the depth
20 at which the silicon nanoclusters are formed due to the phase segregation in the dielectric material. Since the depth at which the isolation storage elements are formed dramatically affects the electrical characteristics of the resulting device, ion implantation does not provide
25 the level of control desired in a manufacturing situation.

In another prior technique for forming the silicon nanoclusters, a thin layer of amorphous silicon is deposited on the tunnel dielectric material. A
30 subsequent annealing step is used to recrystallize the amorphous silicon into the nanoclusters. In order to produce nanoclusters of a desired density and size, the layer of amorphous silicon should be deposited such that

it is on the order of 7-10 angstroms in thickness. Deposition of such thin layers of amorphous silicon is hard to control and therefore impractical in a manufacturing process. In addition to such control
5 issues, additional problems may arise due to preexisting crystalline zones within the amorphous silicon layer. Such preexisting crystallites serve as nucleation sites for crystal growth, which deleteriously interferes with the spontaneous crystal growth desired for formation of
10 the nanoclusters.

In other prior techniques for forming nanoclusters, chemical vapor deposition (CVD) techniques such as low pressure chemical vapor deposition (LPCVD) are used to nucleate and grow the nanoclusters directly on the tunnel
15 oxide. Such prior art LPCVD techniques typically involve a very short deposition time period, on the order of approximately 10 to 30 seconds. Part of this deposition time period includes an incubation period where an adequate number of silicon atoms are generated on the
20 surface of the dielectric prior to the commencement of the clustering activity that forms the crystalline structures of the nanoclusters. The remaining portion of the time is used to nucleate and grow the nanoclusters to the desired size. Due to the fact that the time period
25 associated with nucleation and growth is so short, slight deviations in the processing parameters have profound effects on the resulting density and size uniformity of the resulting nanoclusters. Moreover, systematic effects can be significant. For example, portions of a silicon
30 wafer being processed that are near the source of the reactant gas may realize a much higher density and size of nanoclusters, whereas portions of the wafers that are more distant from the reactant gas source would see lower

densities and smaller sizes of nanoclusters. Such process non-uniformities are undesirable in manufacturing processes.

Prior art techniques exist only to grow
5 semiconductor nanoclusters or nanocrystals. There is no known method to grow metallic nanodots around semiconductor nucleation points (i.e., the nuclei). Existing methods known to exist are merely based on metallic physical vapor deposition (PVD) coatings such as
10 a de-wetting phenomena which occurs during an anneal step or, alternatively, a single-step metallic CVD deposition. However, neither of these techniques allow control of nanocluster density nor nanocluster size.

Advantages of metallic nanodots, as compared with
15 semiconductor nanocrystals, include an ability to store more electrons (e.g., in a flash memory application) since little or no quantum confinement will occur. Therefore, a need exists for a method for including metallic nanoclusters within semiconductor devices in a
20 manner that provides a high density of storage elements while maintaining control over the size dispersion of the storage elements.

SUMMARY

25 Generally, the present invention pertains to a semiconductor memory device with a floating gate that includes a plurality of metallic nanodots and techniques useful in the manufacturing of such a device. In order to prevent oxidation of the formed nanodots, the
30 nanoclusters may be encapsulated or passivated prior to formation of a control dielectric layer. Such encapsulation may include forming a thin dielectric film layer, such as, for example, silicon nitride, on the

nanodots. A gate electrode is then formed over the control dielectric and portions of the encapsulation dielectric. Portions of the plurality of nanodots and the encapsulation dielectric that do not underlie the gate electrode are selectively removed. Source and drain regions are formed by implantation or diffusing of dopants in the semiconductor layer such that a channel region is formed between the source and drain regions underlying the gate electrode.

10 In an exemplary embodiment, the present invention is a method of forming metallic nanodots. The method includes placing a substrate in a reactor chamber, elevating a temperature of the substrate, and reducing a pressure within the chamber. A dielectric film layer is formed on a surface of the substrate, and a plurality of silicon nucleation sites is formed on an exposed surface of the dielectric film layer. The silicon nucleation sites are formed by steps including (1) introducing a silicon-containing precursor gas into the reactor chamber, and (2) disassociating at least a portion of the silicon-containing precursor gas. Substantially each of the plurality of silicon nucleation sites is encapsulated with a metal coating where the metal coating is formed substantially around only the silicon nucleation sites. Metal encapsulation is performed by (1) introducing a metal-containing precursor gas into the reactor chamber, and (2) dissociating at least a portion of the metal-containing precursor gas.

25 In another exemplary embodiment, the present invention is a method of forming a flash memory transistor that includes placing a substrate in a reactor chamber, elevating a temperature of the substrate, and reducing a pressure within the chamber. A silicon

dioxide film layer is formed on a surface of the substrate to a thickness selected to act as a tunneling layer. A plurality of silicon nucleation sites are formed on an exposed surface of the silicon dioxide film layer by (1) introducing a silicon-containing precursor gas into the reactor chamber, and (2) disassociating at least a portion of the silicon-containing precursor gas. Substantially each of the plurality of silicon nucleation sites is encapsulated with a metal coating, thus forming a plurality of metallic nanodots. The metal coating is selectively formed substantially around only the silicon nucleation sites by (1) introducing a metal-containing precursor gas into the reactor chamber, and (2) dissociating at least a portion of the metal-containing precursor gas. A dielectric layer is formed over the plurality of metallic nanodots and a gate electrode is formed over the dielectric layer.

In another exemplary embodiment, the present invention is a flash memory device. The flash memory device includes a substrate, a tunneling dielectric film layer formed over the substrate, and a plurality of metallic nanodots formed over the tunneling dielectric layer. The plurality of metallic nanodots is comprised of a metallic coating formed over a silicon nucleation site. A control dielectric film layer is formed over the plurality of metallic nanodots and a gate electrode is formed over the control dielectric film layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a graphical depiction of formation of core stable silicon clusters.

Fig. 2 is a graphical depiction of growth of core silicon clusters within a chemical deposition tool.

Figs. 3A - 3C indicate a metallic growth deposited on the stable silicon clusters produced in Fig. 2 producing metallic nanodots.

Fig. 4 is a cross-sectional diagram of an exemplary application of metallic nanodots of Fig. 3C used in forming a flash memory device.

DETAILED DESCRIPTION

A basic thin-film deposition process such as one occurring, for example, in a CVD tool, typically involves a number of sequential steps. Atoms and/or molecules produced within a CVD chamber adsorb onto a surface of a substrate. After adsorption, the atoms and/or molecules will frequently diffuse for some distance prior to becoming incorporated into any dielectric film layer present on the surface of a substrate. Incorporation involves a reaction or aggregation of the adsorbed species with each other and with the surface to form bonds between the adsorbed species and the dielectric film layer material. Aggregation of the adsorbed species is referred to as nucleation.

With reference to Fig. 1, an exemplary embodiment of atomic processes illustrates initial formation stages of nanodot formation. A precursor molecule, such as, for example, silane (SiH_4) or disilane (Si_2H_6), form a precursor 101 on a surface 103A of a dielectric film layer 103B of a semiconductor device 105. The dielectric film layer 103B may be, for example, a silicon dioxide film either thermally grown or deposited over a substrate 107. If the dielectric film layer 103B is a thermally grown silicon dioxide layer, the substrate 107 may be a silicon wafer. Moreover, using silicon dioxide for the dielectric film layer 103B may be useful in constructing

a flash memory device. The flash memory device will be described in detail with reference to Figs. 3A - 3D *infra*.

The precursor molecule, in this case disilane, can directly adsorb on the surface of silicon dioxide and form a silicon adsorbed atom 109 on the dielectric film layer surface 103A. This entire process may take place in a typical semiconductor fabrication tool, such as, for example, either a low-pressure CVD (LPCVD) or ultra-high vacuum CVD (UHCVD) deposition tool having a cold wall reactor chamber. Specifics of the chamber are described in detail *infra*.

A reactivity factor, referred to as a sticking coefficient, is a probability of molecules arriving at the surface of a dielectric film layer becoming incorporated into the film. Sticking coefficients can vary from unity to less than $1(10^{-3})$. The sticking coefficient of disilane, as used in this exemplary embodiment, is very small (much less than one) and consequently most of the disilane precursor leaves the reactor in an unreacted state. In the process illustrated in the exemplary embodiment of Fig. 1, the precursor 101 is heated locally near the dielectric film layer 103B thus forming an active radical silylene. The active silylene radical has a sticking coefficient close to unity and is adsorbed on the surface 103A of the dielectric film layer 103B. The active radical silylene readily decomposes to form a silicon adsorbed atom 109. A plurality of silicon adsorbed atoms 109 on the surface 103A of the dielectric film layer 103B diffuse on the surface 103A. Clusters of silicon adsorbed atoms 113 of varying sizes form due to random encounters of the plurality of silicon atoms 109. The clusters of silicon

adsorbed atoms may also dissociate (not shown).

Clustering continues until a larger cluster 115 of a size greater than a critical size is formed. The critical size is on the order of a few atoms. A stable cluster 117 can grow by diffusion of the surface adsorbed atoms 109 or other clusters 113, 115 adhering to each other. The stable cluster 117 may also grow by direct impingement of the active radical or precursor. The stable cluster 117 will act as a nucleation site for later deposition steps which will form a metallic layer around the stable cluster 117.

Desorption of a reaction byproduct, diatomic hydrogen (H_2), is a necessary and regular occurrence that exposes areas of the dielectric film layer surface 103A for adsorbed atom 109 formation. As indicated, adsorbed atom 109 can undergo a process of evaporation 123. Evaporation 123 is undesirable as it depletes the surface of adsorbed atoms 109 available for nucleation. As can be inferred from the foregoing description, formation of nanodot nucleation sites by atomistic nucleation is a complex process but can be controlled with careful attention to process conditions. An exemplary implementation of the process just described is presented in Fig. 2.

A cross-section of a cold wall LPCVD chamber 201 of Fig. 2 includes a substrate heating element 203, an inlet, and an outlet. A substrate 205 mounted within the chamber 201 has a dielectric film layer 207 formed on an uppermost surface of the substrate 205. The substrate heating element 203 rotates the substrate 205 and dielectric film layer 207 within the chamber 201 about a central vertical axis. As discussed with reference to Fig. 1, a formation rate of adsorbed atoms as well as the

surface diffusion and atomic evaporation may be manipulated in various ways within the chamber 201 in order to increase a surface density of resulting nanodots.

5 When a precursor gas containing precursor molecules 211 is flowing within the chamber 201, a hydrodynamic and thermal boundary layer 209 is established over the dielectric film layer 207 and substrate 205. An interior temperature of the chamber 201 is generally at a
10 temperature T_i . The substrate heating element 203 may be adjusted to maintain a temperature of the substrate, T_s , such that $T_s > T_i$. The boundary layer 209 assists in achieving a desired formation rate of adsorbed atoms.

 In a specific exemplary embodiment, a total pressure
15 within the chamber 201 is approximately in the range of 10 to 70 Torr, although ranges of pressure from 1 to 300 Torr or more may be used. Walls of the chamber 201 are cooled to a temperature much lower than a temperature of the substrate 205. The substrate 205 is heated and
20 maintained at a relatively-fixed temperature by the substrate heating element 203. In this embodiment, the surface temperature of the substrate 205 is in a range of approximately 400 °C to 1000 °C. The substrate heating element 203 may be implemented as a light heat source, a
25 radiant heat source, or by other heating elements such as resistive heating elements.

 The boundary layer 209 is in a gaseous state. An upper 209A and lower boundary 209B of the boundary layer 209 have temperatures nearly equal to the temperature, T_s ,
30 of substrate 205 at the lower boundary 209B and close to the inlet temperature, T_i , at the upper boundary 209A. A precursor, such as disilane gas, along with a large excess of an inert carrier gas, such as hydrogen (H_2)

enter the chamber 201 at the inlet and are the precursor and carrier gases are mixed.

In a specific exemplary embodiment, a partial pressure of the precursor gas is chosen to be in a range of approximately 10 mTorr to 1000 mTorr for silicon nucleation site formation from either silane or disilane. The inlet temperature of the gases typically approximates ambient temperature. The boundary layer 209 forms in the presence of any flowing gas within the chamber 201 under conditions where the Knudsen number is less than 0.1. The Knudsen number (Kn) is a dimensionless number defined as the ratio of a molecular mean free path length to a representative physical length scale. The Knudsen number is defined mathematically as:

$$\text{Kn} = \frac{\lambda}{L} = \frac{k_B T}{\sqrt{2} \pi \sigma^2 P L}$$

where λ is the mean free path (nm), L is a physical length scale (nm), k_B is Boltzmann's constant ($1.38(10^{-23})$ Joules/°K), T is the temperature of the gas (°K), σ is a diameter of the gas molecule under consideration (nm), and P is the total pressure (Pa).

Precursor molecules 211, for example, are heated as they transport across the boundary layer 209 to the upper surface of the dielectric film layer 207. Heating the precursor molecules 211 causes a partial or complete dissociation of the precursor gas. For example, a gas phase decomposition reaction as will be described *infra* is known to occur.

Consequently, the surface of the dielectric film layer 207 is exposed to a mixture of disilane 213, silane 215, and silylene 217. The silylene 217 is a very active species and readily adsorbs on the surface of the

dielectric film layer 207 while disilane and silane have substantially lower sticking coefficients and reaction rates on the surface. The adsorbed surface molecules (disilane, silane, and silylene) then decompose at the substrate temperature to form a silicon adsorbed atom 219. Diatomic hydrogen, H_2 , is desorbed as a byproduct and removed from the boundary layer 209. Silicon atoms 219 nucleate forming stable silicon clusters 221.

Fig. 2 further shows a gas flow velocity profile formed within the boundary layer 209. At the lower boundary 209B (coincident with the top surface of the dielectric film layer 207), a hydrodynamic no-slip condition of gas flow velocity implies a zero-velocity condition while a gas flow velocity at the upper boundary 209A is approximately equal to a mean velocity in the chamber 201.

With reference to Fig. 3A, the deposition process described in Figs. 1 and 2 is completed. A plurality of stable silicon clusters 221 are formed on the dielectric film layer 207. In a specific exemplary embodiment, the substrate 205 is a silicon wafer substrate 205. The dielectric film layer 207 is a silicon dioxide layer which acts as a tunnel oxide for a flash memory device, described *infra*.

In Fig. 3B, similar deposition techniques described with reference to Figs. 1 and 2 are applied to a metal precursor. Metal precursor molecules 301 interact exclusively with the plurality of stable silicon clusters 221 (Fig. 3A) to form a plurality of small metallic nanodots 303. A core of each of the plurality of nanodots 221 is thus the stable silicon clusters 221 (not shown in Fig. 3B). The metal precursor molecules only deposit around the core material of the stable silicon

clusters 221. Thus, due to the nature of chemical interactions between the metal precursor molecules 301, the stable silicon clusters 221, and the dielectric film layer 207, deposition does not occur on the dielectric film layer 207. Specific metal-containing gas precursors that may be used include titanium tetrachloride (TiCl_4) or tungsten hexafluoride (WF_6), each delivered as a mixture with a hydrogen carrier gas (e.g., $\text{TiCl}_4\text{-H}_2$ or $\text{WF}_6\text{-H}_2$). Using one of these precursor gases results in a metallic coating over the stable silicon clusters 221. The metallic coating is, for example, titanium silicide (TiSi_2) or tungsten (W). Other metallic precursors and resulting metals are known to one of skill in the art.

In another exemplary embodiment, TiCl_4 is mixed with H_2 and dichlorosilane (SiH_2Cl_2 or DCS). DCS is used to balance the selectivity of deposition on the nucleation site versus self-nucleation or forming a metallic layer on the blanket oxide. In a specific exemplary embodiment, the process is carried out in a reactor at a pressure of 1 to 100 Torr at a temperature of 650 °C to 1000 °C, with a DCS and TiCl_4 partial pressure of 0.1 to 5 Torr each with an H_2 carrier gas. Additionally, germane (GeH_4) or hydrogen chloride (HCl) may be added to further enhance selectivity control.

In another exemplary embodiment employing selective tungsten growth, WF_6 is mixed with H_2 and SiH_4 . Here, SiH_4 is used to balance the selectivity of deposition on the nucleation site versus self-nucleation or forming a metallic layer on the blanket oxide. In a specific exemplary embodiment, the process is carried out in a reactor at a pressure of 1 to 100 mTorr at a temperature of 300 °C to 700 °C, with flow rates of 5 to 50 sccm for WF_6 and 2 to 10 sccm for SiH_4 , with an argon (Ar) carrier

gas. Additionally, a small H₂ flow may be added to further enhance selectivity control.

Overall, selectivity of processes described is enhanced if formation of Si core nanoclusters and metallic growth around the core nanoclusters occurs within the same reactor (e.g., within the same LPCVD reactor or within a common cluster tool such that all processes are performed without breaking vacuum or under an N₂ ambient), thus preventing any native oxide growth on the core nanoclusters.

Deposition of metal precursor molecules 301 continues until larger sizes of metallic nanodots 305 are formed (Fig. 3C). Gas flow rates, deposition times, and substrate temperatures are parameters which may be varied to achieve a particular target size range of the metallic nanodots 305.

In Fig. 4, the metallic nanodots 305 are used to form an exemplary flash memory device 400. The substrate 205 may be of various materials. For semiconductor applications, the substrate 205 may be silicon, germanium or silicon-on-insulator (SOI). However, other substrate materials may be used. For example, compound semiconductors (e.g., compounds of elements, especially elements from periodic table groups III-V and II-VI) may be readily employed as the substrate 205. The dielectric film layer 207 may be of various materials, such as silicon dioxide, silicon nitride, or silicon oxynitride. Further, the dielectric film layer 207 may be comprised of a multilayer dielectric or a high dielectric constant (high-k) material (high-k dielectric materials are known in the art and include films such as tantalum pentoxide (Ta₂O₅), zirconium oxide (ZrO₂), hafnium oxide (HfO₂), and lead-zirconate-titanate (PZT). However, other

dielectric materials may be employed as well.

In a specific exemplary embodiment, the dielectric film layer 207 is silicon dioxide formed on an uppermost surface of a silicon substrate by thermal oxidation of silicon. The metallic nanodots are formed over the
5 dielectric film layer 207 by methods described herein.

An additional dielectric film layer 401, for example, a deposited silicon nitride layer, is formed over the metallic nanodots 305. A control gate 403 is then deposited over the additional dielectric film layer
10 401. The control gate layer 403 may be a deposited polysilicon layer. Conventional photolithographic techniques are used to etch a remaining portion of the dielectric film layer 207, the additional dielectric film layer 401, and the control gate layer 403 to a final form
15 as shown in Fig. 4. The deposition of the film layers (other than growth and deposition of the metallic nanodots 305) and the photolithographic techniques are known in the art.

Dielectric spacers 405 are formed by depositing a blanket dielectric film layer (not shown), patterning, and etching. The etching is typically performed using an reactive-ion etch (RIE) process, thus removing primarily those portions of the blanket dielectric film layer that
20 are substantially parallel (i.e., horizontal portions) to an uppermost surface of the substrate 205. The RIE process thus leaves substantially intact vertical portions of the blanket dielectric film layer. Consequently, the resulting dielectric spacers 405 are
25 self-aligned with a given feature. Further, the dielectric spacers 405 allow an etch or alignment step surrounding the given feature to be below a photolithographic limit of resolution since the etch or
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alignment is now based merely on a thickness of the blanket dielectric film layer and a step-height of a proximate structure. Since a size of the dielectric spacers 405 are dependent on the thickness of chosen film layers, spacers may be created as thin as approximately 30 Å or less.

A final dopant step provides source and drain dopant areas 407 for the exemplary flash memory device 400. As is known to a skilled artisan, the dopant areas 407 may be either implanted or diffused.

In the foregoing specification, the present invention has been described with reference to specific embodiments thereof. It will, however, be evident to a skilled artisan that various modifications and changes can be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. For example, skilled artisans will appreciate that various types of dielectric layers or stacks of dielectric layers may be employed as a base for forming nanodots. Further, various types of metallic precursor gases exist which may be implemented to form nanodots by employing techniques described herein. Such techniques may be implemented in a variety of process tools such as, for example, those tools used in atomic layer deposition (ALD), chemical vapor deposition (CVD), low-pressure CVD (LPCVD), plasma-enhanced CVD (PECVD), or plasma-assisted CVD (PACVD). The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

Claims

1. A method of forming metallic nanodots, the method comprising:

5 forming a dielectric film layer on a surface of a substrate;

 forming a plurality of silicon nucleation sites on an exposed surface of the dielectric film layer, the plurality of silicon nucleation sites being formed by
10 steps including:

 (i) introducing a silicon-containing precursor gas into the reactor chamber, and

 (ii) disassociating at least a portion of the silicon-containing precursor gas; and

15 encapsulating the plurality of silicon nucleation sites with a metal coating, the metal coating being selectively formed substantially around only the silicon nucleation sites by steps including:

 (i) introducing a metal-containing precursor
20 gas into the reactor chamber, and

 (ii) dissociating at least a portion of the metal-containing precursor gas.

2. The method of claim 1 wherein the silicon-containing
25 precursor gas is selected to be silane.

3. The method of claim 1 wherein the silicon-containing precursor gas is selected to be disilane.

30 4. The method of claim 1 wherein the metal-containing precursor gas is selected to be titanium tetrachloride.

5. The method of claim 1 wherein the metal-containing precursor gas is selected to be tungsten hexafluoride.

5 6. The method of claim 1 wherein a temperature of the substrate is elevated to a range of about 400 °C to 1000 °C.

7. The method of claim 1 wherein a pressure within the
10 chamber is reduced to a range of about 1 Torr to 300 Torr.

8. The method of claim 1, further comprising selecting the dielectric film layer to be silicon dioxide.

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9. A method of forming a flash memory transistor, the method comprising:

forming a silicon dioxide film layer on a surface of a substrate to a thickness selected to act as a tunneling
20 layer;

forming a plurality of silicon nucleation sites on an exposed surface of the silicon dioxide film layer, the silicon nucleation sites being formed by steps including:

- 25 (i) introducing a silicon-containing precursor gas into the reactor chamber, and
(ii) disassociating at least a portion of the silicon-containing precursor gas;

encapsulating the plurality of silicon nucleation sites with a metal coating thus forming a plurality of
30 metallic nanodots, the metal coating being selectively formed substantially around only the silicon nucleation sites by steps including:

(i) introducing a metal-containing precursor gas into the reactor chamber, and

(ii) dissociating at least a portion of the metal-containing precursor gas;

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forming a dielectric layer over the plurality of metallic nanodots; and

forming a gate electrode over the dielectric layer.

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10. The method of claim 9 wherein the silicon-containing precursor gas is selected to be silane.

11. The method of claim 9 wherein the silicon-containing precursor gas is selected to be disilane.

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12. The method of claim 9 wherein the metal-containing precursor gas is selected to be titanium tetrachloride.

13. The method of claim 9 wherein the metal-containing precursor gas is selected to be tungsten hexafluoride.

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14. The method of claim 9 wherein material selected for the gate electrode is polysilicon.

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15. A flash memory device comprising:

a substrate;

a tunneling dielectric film layer formed over the substrate;

a plurality of metallic nanodots formed over the

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tunneling dielectric layer, each one of the plurality of metallic nanodots comprised of a metallic coating formed over a silicon nucleation site;

a control dielectric film layer formed over the plurality of metallic nanodots; and

a gate electrode formed over the control dielectric film layer.

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16. The flash memory device of claim 15 wherein the tunneling dielectric film layer is comprised of silicon dioxide.

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17. The flash memory device of claim 15 wherein the tunneling dielectric film layer is comprised of nitrided silicon dioxide.

15

18. The flash memory device of claim 15 wherein the tunneling dielectric film layer is comprised of silicon oxynitride.

20

19. The flash memory device of claim 15 wherein the tunneling dielectric film layer is comprised of a high-k dielectric material.

20. The flash memory device of claim 15 wherein the substrate is comprised of silicon.

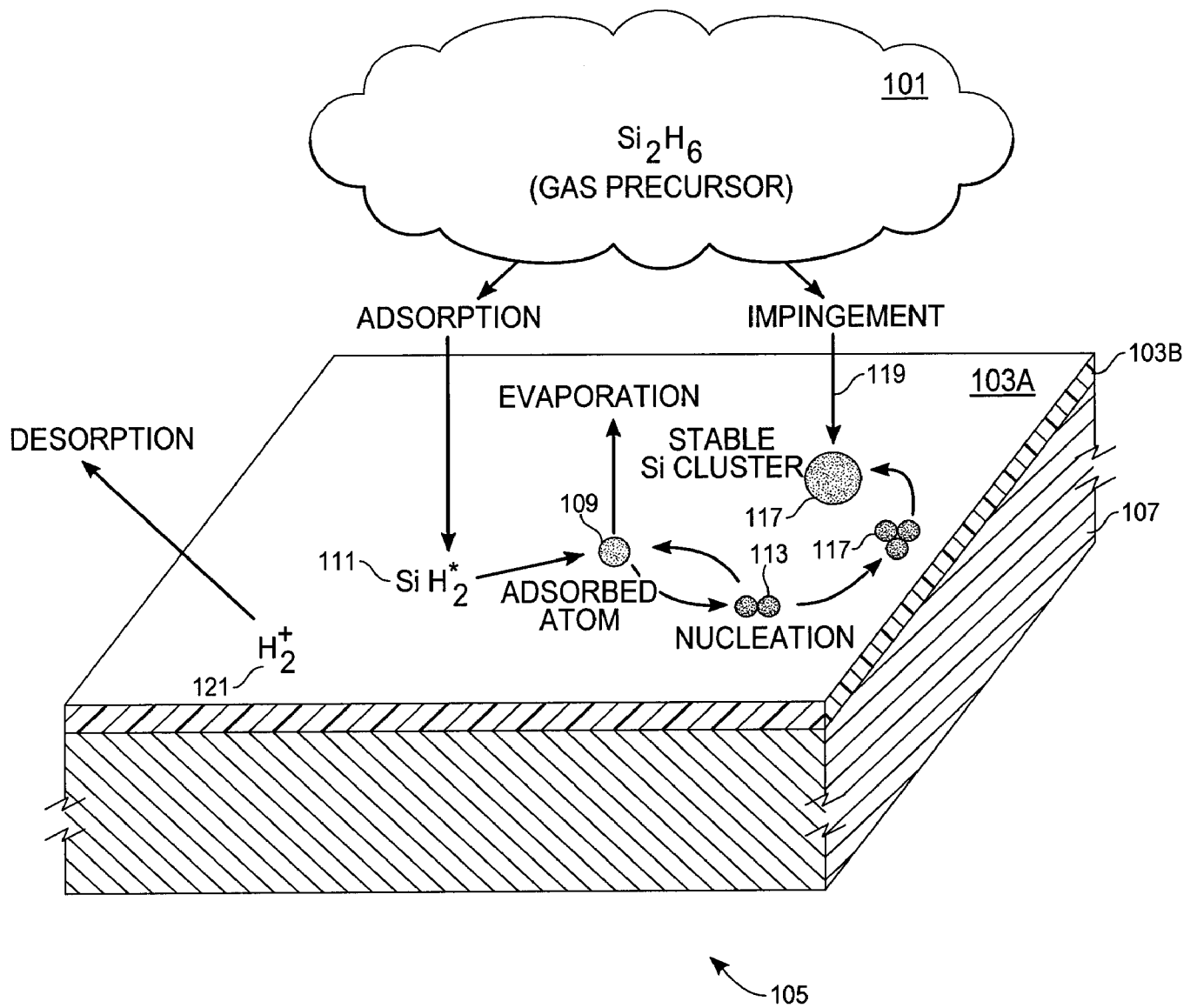
25

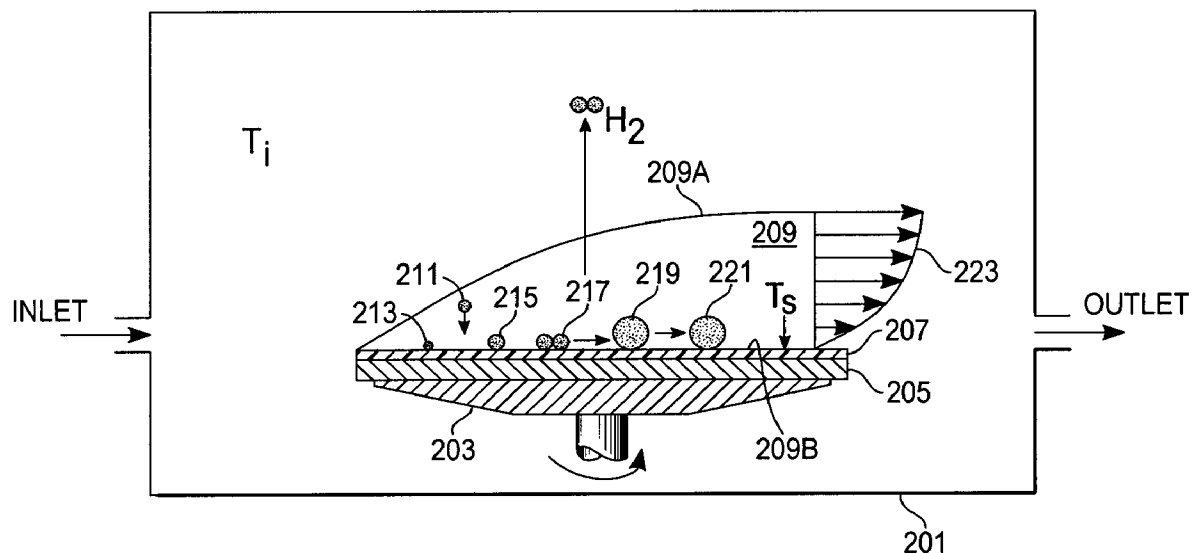
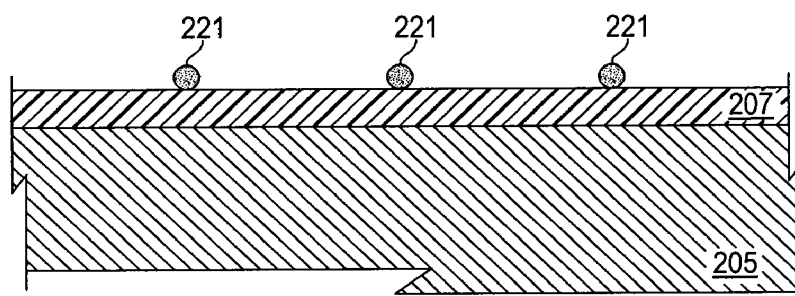
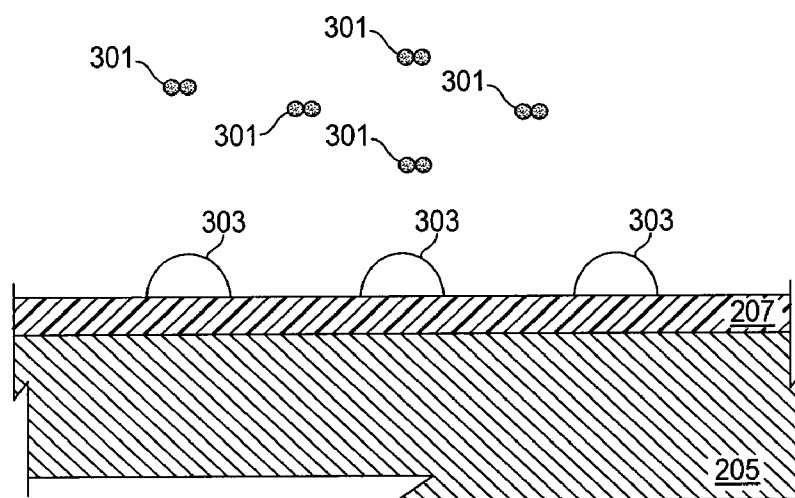
21. The flash memory device of claim 20 wherein the tunneling dielectric film layer is comprised of thermally-grown silicon dioxide.

22. The flash memory device of claim 15 further comprising:

5 a source dopant area formed on a first edge of the plurality of metallic nanodots and near a surface of the substrate and in electrical communication with the plurality of metallic nanodots; and

10 a drain dopant area formed on a second edge of the plurality of metallic nanodots and near a surface of the substrate and in electrical communication with the plurality of metallic nanodots, the second edge being distal to the first edge.

*Fig. 1*

*Fig. 2**Fig. 3A**Fig. 3B*

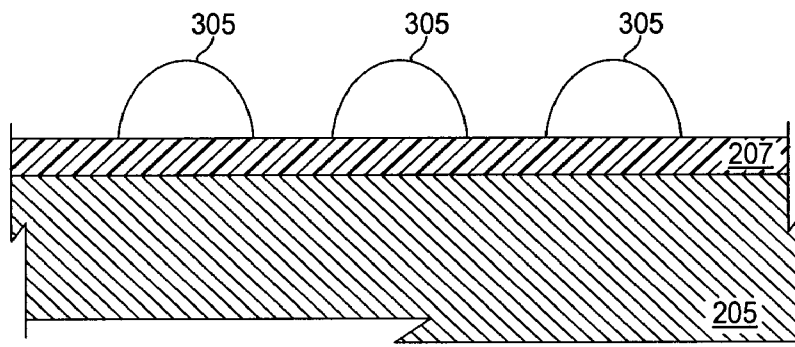


Fig. 3C

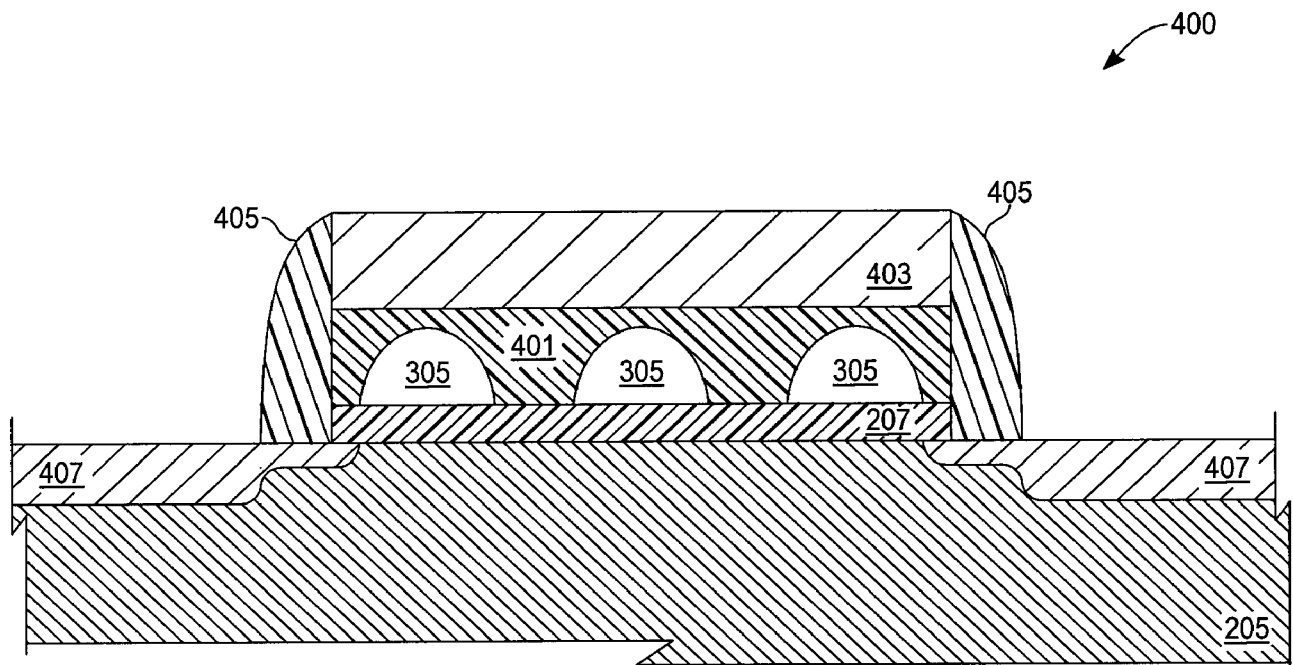


Fig. 4