



- (51) **International Patent Classification:**
G06F 13/42 (2006.01) *G06F 12/02* (2006.01)
- (21) **International Application Number:**
PCT/JP2012/006759
- (22) **International Filing Date:**
23 October 2012 (23.10.2012)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (71) **Applicant:** HITACHI, LTD. [JP/JP]; 6-6, Marunouchi 1-chome, Chiyoda-ku, Tokyo, 1008280 (JP).
- (72) **Inventors:** IKEDA, Yasuhiro; c/o HITACHI, LTD., Yokohama Research Laboratory, 292, Yoshida-cho, Totsuka-ku, Yokohama-shi, Kanagawa, 2440817 (JP). UEMATSU, Yutaka; c/o HITACHI, LTD., Yokohama Research Laboratory, 292, Yoshida-cho, Totsuka-ku, Yokohama-shi, Kanagawa, 2440817 (JP). MURAOKA, Satoshi; c/o HITACHI, LTD., Yokohama Research Laboratory, 292, Yoshida-cho, Totsuka-ku, Yokohama-shi, Kanagawa, 2440817 (JP).
- (74) **Agents:** HIRAKI, Yusuke et al.; Atago Green Hills MORI Tower 32F, 5-1, Atago 2-chome, Minato-ku, Tokyo, 1056232 (JP).

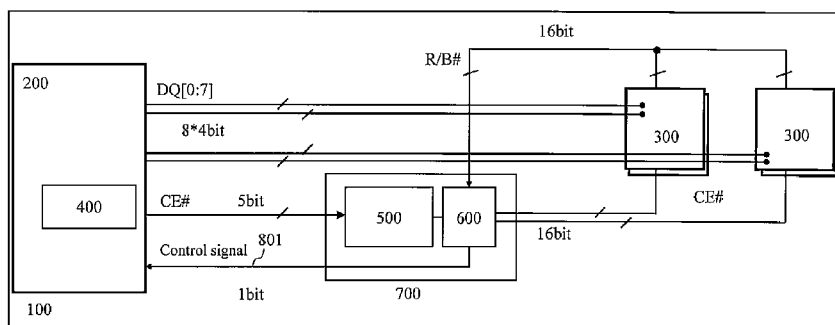
- (81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) **Title:** SIGNAL TRANSMISSION SYSTEM AND STORAGE SYSTEM

Fig. 1



(57) **Abstract:** A signal transmission system is provided which connects a memory controller and a plurality of semiconductor memories. The signal transmission system comprises a semiconductor device arranged between the memory controller and the plurality of memories, in which: the semiconductor device comprises a control circuit; and the control circuit receives a signal from the semiconductor memory and outputs a control signal to the memory controller in response to the signal from the semiconductor memory.

Description

Title of Invention: SIGNAL TRANSMISSION SYSTEM AND STORAGE SYSTEM

Technical Field

[0001] The present invention relates to a signal transmission system and a storage system including the signal transmission system.

Background Art

[0002] In recent years, there is a growing need for a large-capacity storage system using a low-cost and high-density flash memory. To realize the large-capacity storage system, it is considered that more flash memories are connected. However, if more flash memories are connected, a signal (CE#) to select a chip and a signal (R/B#) to notify an operation state of the chip increase. When the numbers of these signals increase, signal lines of these signals increase and the number of pins in a memory controller increases. As a result, the package size becomes large and the cost becomes high.

[0003] Therefore, a configuration to reduce signal lines in a semiconductor device is required. The related art of the present technical field includes Patent Literature 1. Patent Literature 1 describes that "A semiconductor device comprises both a mode signal generating circuit 11 to generate a plurality of mode signals M0 to M2 corresponding to the operation modes of the semiconductor device, and a test signal generating circuit 12 to generate a plurality of test signals T0 to T2 for testing the semiconductor device in the operation modes corresponding to the generated mode signals M0 to M2. The semiconductor device transmits each of the mode signals M0 to M2 and the test signals T0 to T2 to predetermined regions via a plurality of signal conductors. In this case, an encoder circuit 16 to encode the mode signals M0 to M2 and the test signals T0 to T2, and to supply them to the signal conductors as encode signals S0 to S3 with the number of bits fewer than the sum of the number of bits of both the mode signals M0 to M2 and the test signals T0 to T2, is arranged" (see Abstract).

Citation List

Patent Literature

[0004] PTL 1: JP Patent Publication (Kokai) No. 2000-46921

Summary of Invention

Technical Problem

[0005] In above Patent Literature 1, although the mode signals and the test signals are encoded to reduce signal lines for these signals, in this configuration, a reduction effect

of signal lines, that is, the number of pins in a memory controller is small. Also, in Patent Literature 1, the mode signals and the test signals are targeted, but a signal (CE#) to select a chip and a signal (R/B#) to notify an operation state of the chip are not considered.

[0006] The present invention provides a signal transmission system that can reduce the number of pins in a memory controller, and a storage system including the signal transmission system.

Solution to Problem

[0007] To solve the above problem, for example, a configuration recited in the claims is adopted. Although the present application includes a plurality of means to solve the above problem, as an example, a signal transmission system connecting a memory controller and a plurality of semiconductor memories includes a semiconductor device arranged between the memory controller and the plurality of semiconductor memories, in which the semiconductor device includes a control circuit; and the control circuit receives a signal from the semiconductor memory and outputs a control signal to the memory controller in response to the signal from the semiconductor memory.

[0008] Also, according to another example, a storage system is provided which includes a storage controller and a storage device group including a plurality of semiconductor memory packages. In this storage system, the semiconductor memory package includes a semiconductor memory control unit, a plurality of semiconductor memories and a semiconductor device arranged between the semiconductor memory control unit and the plurality of semiconductor memories. Also, the semiconductor device includes a control circuit, and the control circuit receives a signal from the semiconductor memory and outputs a control signal to the semiconductor memory control unit in response to the signal from the semiconductor memory.

Advantageous Effects of Invention

[0009] According to the present invention, it is possible to reduce the number of pins in a memory controller. By this means, the occupation area of signal lines in a board becomes small and it is possible to realize high-density mounting.

[0010] Further features related to the present invention are clarified from description of the present specification and the accompanying drawings. Also, other problems, configurations and advantages than the above will be clarified in the following explanation of examples.

Brief Description of Drawings

[0011] [fig.1]Fig. 1 is an example of a configuration of a signal transmission system according to Example 1 of the present invention.

[fig.2]Fig. 2 is an example of a configuration of a control circuit according to Example

1 of the present invention.

[fig.3]Fig. 3 is a view for explaining signal lines of a signal transmission system in the related art.

[fig.4]Fig. 4 is a view for explaining signal lines of a signal transmission system in a case in which Example 1 of the present invention is applied.

[fig.5]Fig. 5 is a view for explaining a board line layer in a signal transmission system in the related art.

[fig.6]Fig. 6 is a view for explaining a board line layer in a case in which Example 1 of the present invention is applied.

[fig.7]Fig. 7 is an example of a configuration of a signal transmission system according to Example 2 of the present invention.

[fig.8]Fig. 8 is an example of a configuration of a signal transmission system according to Example 3 of the present invention.

[fig.9]Fig. 9 is an example of a configuration of a signal transmission system according to Example 4 of the present invention.

[fig.10]Fig. 10 is an overall view of a storage system according to Example 5 of the present invention.

[fig.11]Fig. 11 is an example of a configuration of a flash package according to Example 5 of the present invention.

Description of Embodiments

[0012] In the following, examples of the present invention will be explained with reference to the accompanying drawings. Also, although the accompanying drawings illustrate specific examples based on the principle of the present invention, these are used to understand the present invention and are never used to interpret the present invention in a limited manner.

[0013] Also, in the following examples, "CE#" denotes a chip enable signal to select a chip. Also, "R/B#" denotes a ready busy signal to notify a chip operation state. Also, "DQ" denotes a data signal.

[0014] <Example 1>

Fig. 1 illustrates an example of a configuration of a signal transmission system according to the present example mounted on a board. On a board 100, a memory controller 200 and a plurality of flash memories (i.e. semiconductor memories) 300 are provided. In the present example, four flash memories 300 are arranged on the board 100. Also, in the present example, although four flash memories are connected to one memory controller, it is not limited to this configuration, and a configuration is possible in which the memory controller 200 and the flash memory 300 are connected at a ratio of 1 to n (arbitrary number). Also, the flash memory 300 includes a plurality

of chips. In the present example, for example, each flash memory 300 includes eight chips.

[0015] The present example provides a signal transmission system connecting between the memory controller 200 and the flash memory 300. A CE# signal denotes a signal for selecting a chip of the flash memory 300 and an R/B# signal denotes a signal for notifying an operation state (i.e. busy state) of the chip of the flash memory 300. Also, in the present example, a case is assumed where 16-bit CE# signals and 16-bit R/B# signals are required.

[0016] Also, in Fig. 1, DQ[0:7] indicates 0th to 7th data signals, that is, it means that there are eight signal lines of DQ signals. In the present example, there are four sets of eight signal lines of DQ signals in association with each flash memory 300, and therefore there are 32-bit (8 x 4) signal lines of DQ signals.

[0017] In the following, an example will be explained with respect to a signal transmission system to reduce the number of pins for a CE# signal to select a chip and the number of pins for an R/B# signal to notify an operation state of the chip in the memory controller 200.

[0018] The memory controller 200 includes an encode circuit 400 that encodes the CE# signal. The encode circuit 400 encodes the CE# signal and outputs the encoded CE# signal (5 bits). The breakdown of this 5-bit signal is explained, and 4 bits are used as a signal to select a chip of 16 bits and 1 bit is used as a signal not to select a chip (i.e. all off).

[0019] The board 100 includes a semiconductor device 700 provided between the memory controller 200 and the flash memory 300. The semiconductor device 700 includes a decode circuit 500 that decodes the CE# signal encoded by the encode circuit 400, and a control circuit 600 that receives the R/B# signal from the flash memory 300 and outputs a control signal 801 to the memory controller 200. The control signal 801 denotes a 1-bit signal indicating whether a chip selected by the CE# signal is in a busy state. That is, the control circuit 600 detects whether the chip selected by the CE# signal is in a busy state. The memory controller 200 can know by the control signal 801 whether the chip selected by the CE# signal is in a busy state, and can control re-transmission of the CE# signal.

[0020] Fig. 2 is a view illustrating an example of a control circuit. Although there are various possible realization configurations of the control circuit 600 in Fig. 1, as an example, a circuit 1100 that masks the CE# signal by the R/B# signal is possible.

[0021] The circuit 1100 includes a plurality of first OR circuits 1101 and a second OR circuit 1102. The decode circuit 500 decodes the 5-bit signal encoded by the encode circuit 400 and acquires 16-bit CE# signals. Each of 16-bit CE# signals is input to the first OR circuit 1101. Also, although it is omitted in Fig. 2, actually, signal lines of

16-bit CE# signals extend from the decode circuit 500 and the first OR circuit 1101 is arranged every signal line of the CE# signal. Also, the R/B# signal corresponding to a chip selected by the CE# signal is input to the first OR circuit 1101 as a NOT input. By this means, in a case in which the chip is in a busy state, the CE# signal is not transmitted to the flash memory 300 and it is possible to control the CE# signal using the R/B# signal.

[0022] Also, outputs of the first OR circuits 1101 are each input to the second OR circuit 1102. Subsequently, an output of the second OR circuit 1102 is output to the memory controller 200 as the control signal 801. Thus, an OR computation of the CE# signal and the R/B# signal corresponding to a chip selected by the CE# signal is performed in the first OR circuits 1101 and the outputs of the first OR circuits 1101 are subjected to OR computation in the second OR circuit 1102 to output the control signal 801. By this means, the circuit 1100 can output, as the control signal 801, a decision as to whether the chip selected by the CE# signal is in a busy state. By this means, the memory controller 200 can know by the control signal 801 whether the chip selected by the CE# signal is in a busy state.

[0023] Also, a configuration of the control circuit 600 is not limited to the above circuit 1100 and may be realized by a different configuration as long as it is possible to detect by the configuration whether a selected chip is in a busy state. Also, a configuration of controlling the CE# signal using the R/B# signal may be realized by other configurations.

[0024] Fig. 3 illustrates signal lines in a memory controller in the related art and Fig. 4 illustrates signal lines in a case in which the present example is applied. As illustrated in Fig. 3, in the related art, signal lines of both CE# signals and R/B# signals are connected from the memory controller 200 to the flash memories 300. According to the present example, as illustrated in Fig. 4, only signal lines of CE# signals are connected from the memory controller 200 to the semiconductor device 700. Also, since signal lines of R/B# signals from the flash memories 300 are connected to the semiconductor device 700, it is possible to reduce the signal lines of R/B# signals input in the memory controller 200, and, as a result, it is possible to reduce pins for the R/B# signals in the memory controller 200. Therefore, by applying the present example, since it is possible to reduce the number of signal lines, the occupation area of signal lines in the board 100 becomes small and it is possible to realize high-density mounting. Also, it is possible to use an available pin in the memory controller 200 as a pin for a connector power source or a grand pin, and it is possible to improve signal quality.

[0025] Fig. 5 illustrates a board configuration in the related art and Fig. 6 illustrates a board configuration in a case in which the present example is applied. In a case in which

signal lines 1200 of various signals extend from the memory controller 200, the memory controller 200 and the signal lines (i.e. wires) 1200 are connected by soldering balls 1300 and the signal lines 1200 are formed in a layered manner as wire layers. As illustrated in Fig. 3, in the related art, signal lines of both CE# signals and R/B# signals are connected from the memory controller 200 to the flash memories 300. Therefore, as illustrated in Fig. 5, the layer number of wire layers in the board 100 increases. Meanwhile, according to the present example, as illustrated in Fig. 4, it is possible to reduce signal lines of R/B# signals input in the memory controller 200. Therefore, as illustrated in Fig. 6, it is possible to reduce the layer number of wire layers of the board 100 and realize a lower cost of the board 100.

- [0026] As described above, according to the present example, by encoding CE# signals, it is possible to reduce the number of CE# signals output from the memory controller 200, and, furthermore, it is possible to receive R/B# signals output from the flash memories 300 by the semiconductor device 700 and realize control of the CE# signals. For example, the circuit 1100 in Fig. 2 masks a CE# signal using an R/B# signal. In the circuit 1100, in a case in which a chip of the flash memory 300 is in a busy state, a CE# signal is not transmitted to the flash memory 300. Also, by the control signal 801, the circuit 1100 reports to the memory controller 200 that a selected chip is in a busy state, and thereby it is possible to control CE# signals.
- [0027] In the present example, signal lines of R/B# signals from the flash memories 300 are connected to the semiconductor device 700. As illustrated in Fig. 4, since the signal lines of R/B# signals need not be connected to the memory controller 200, it is possible to drastically reduce the number of pins required in the memory controller 200. Alternatively, by reducing the number of pins required in the memory controller 200 with respect to memory buses, it is possible to control more memory buses in the memory controller 200. As a result, it is possible to realize high performance (i.e. throughput improvement) in a signal transmission system.
- [0028] Also, in a signal transmission system connecting the memory controller 200 and the flash memories 300, by reducing the number of pins for a CE# signal to select a chip and the number of pins for an R/B# signal to notify an operation state of the chip, it is possible to realize a low cost of the memory controller 200 and high-density mounting. In the following, a specific reduction number of pins will be illustrated.
- [0029] In the present example, a case is assumed where four flash memories 300 are mounted on the board 100 and 16-bit CE# signals and 16-bit R/B# signals are required. In this case, the number of pins for the CE# signals and R/B# signals in the memory controller 200 is 32 pins. In the present example, to encode the CE# signals in the memory controller 200, it is possible to reduce 16 pins for the CE# signals to 5 pins (4 pins (16-bit selection) + 1 pin (for all-pins off)). Furthermore, the R/B# signals output

from the flash memories 300 are input to the semiconductor device 700 and the CE# signals are subjected to mask processing by the R/B# signals. Also, in the memory controller 200, a 1-bit signal line (i.e. signal line of the control signal 801) for reporting a result of the mask processing is connected. That is, it is possible to reduce 16 pins for the R/B# signals to 1 pin. As described above, the number of pins required for the CE# signals and R/B# signals is reduced from 32 pins to 6 pins, that is, it is possible to reduce the number of required pins by about 80%.

[0030] Also, the present example is a more preferable embodiment, and, as a variation example, it is possible to form the present invention by removing part of the configuration explained above. In the present example, to reduce the number of pins required for CE# signals, the memory controller 200 includes the encode circuit 400 that encodes the CE# signals, and the semiconductor device 700 includes the decode circuit 500. For example, it is possible to form the present invention by removing these encode circuit 400 and decode circuit 500. To reduce the number of pins required in the memory controller 200, the signal transmission system may include at least the control circuit 600 that detects whether a chip selected by a CE# signal is in a busy state.

[0031] <Example 2>

Fig. 7 illustrates an example of a configuration diagram of a signal transmission system according to the present example mounted on a board. Here, in Example 2, the same reference numerals are assigned to the same components as in the above example and their explanation will be omitted. In the following, only different parts from the configuration in Example 1 will be explained.

[0032] In the present example, a switch circuit 800 is arranged between the memory controller 200 and the flash memories 300. The switch circuit 800 is a circuit that switches DQ signals. In the present example, 8-bit signal lines of DQ signals are connected from the memory controller 200 to the switch circuit 800. Also, 32-bits (8 x 4) signal lines of DQ signals are connected from the switch circuit 800 to the flash memories 300.

[0033] The memory controller 200 includes a circuit 201 that outputs a control signal 802 to control a switch in the switch circuit 800. Also, 2-bit signal lines of the control signal 802 are connected from the memory controller 200 to the switch circuit 800. Therefore, by the control signal 802, it is possible to control which signal line of DQ signal is selected in the switch circuit 800.

[0034] According to the present example, by providing the switch circuit 800 between the memory controller 200 and the flash memories 300, it is possible to reduce the number of pins for DQ signals in the memory controller 200. To be more specific, it is possible to reduce 32 pins for DQ signals to 10 pins (8 bits (for DQ signals) + 2 bits (for the

control signal 802)). Thus, by reducing the number of pins for DQ signals in the memory controller 200, it is possible to further enhance the advantage of Example 1.

[0035] <Example 3>

Fig. 8 illustrates an example of a configuration of a signal transmission system according to the present example mounted on a board. Here, in Example 3, the same reference numerals are assigned to the same components as in the above example and their explanation will be omitted. In the following, only different parts from the configuration in Example 2 will be explained.

[0036] In the present example, the switch circuit 800 is mounted inside the semiconductor device 700. A feature of Example 3 lies in generating the control signal 802 for controlling the switch circuit 800, in the semiconductor device 700 instead of the memory controller 200.

[0037] Although there are various methods of implementing a circuit that generates a control signal for controlling the switch circuit 800 in the semiconductor device 700, as an example, there is a possible circuit that generates the control signal 802 using a CE# signal. Since the CE# signal indicates which chip of the flash memory 300 is selected, it is possible to use the CE# signal.

[0038] For example, the semiconductor device 700 includes four OR circuits between the decode circuit 500 and the switch circuit 800. Regarding 16-bit CE# signals output from the decode circuit 500, 4-bit CE# signals to select the identical flash memory 300 are input to the identical OR circuit and the output of each OR circuit is input to the switch circuit 800. According to this configuration, using CE# signals, it is possible to report which flash memory 300 is selected, to the switch circuit 800. That is, it is possible to use outputs of the OR circuits as the control signal 802 to control the switch circuit 800. Also, a configuration of generating a control signal in the semiconductor device 700 is not limited to the above configuration and may be realized by other configurations.

[0039] According to the present example, it is possible to reduce the number of pins for control signals for the switch circuit 800 in the memory controller 200. Also, since it is possible to implement the decode circuit 500, the control circuit 600 and the switch circuit 800 on one semiconductor device 700, compared to a case in which these are separately mounted, it is possible to reduce a mounting space on the board 100.

[0040] <Example 4>

Fig. 9 illustrates an example of a configuration in which a flash memory and a semiconductor device are mounted on a DIMM board and a memory controller is mounted on a board. Here, in Example 4, the same reference numerals are assigned to the same components as in the above examples and their explanation will be omitted.

[0041] On the board 100, a DIMM board 900 is connected via a DIMM connector 1000.

Also, the flash memory 300 and the semiconductor device 700 are mounted on the DIMM board 900. Also, the memory controller 200 is mounted on the board 100. A feature of Example 4 lies in supporting variation in the memory capacity by changing the DIMM board 900. Furthermore, by mounting the semiconductor device 700 on the DIMM board 900, it is possible to reduce the number of pins required for signals of the DIMM connector 1000. Also, it is also possible to use an available pin as a pin for the power source of the DIMM connector 1000 or a ground pin, and it is possible to improve signal quality.

[0042] <Example 5>

The signal transmission system of the present invention is applicable to the following calculator system. Fig. 10 is an example of a configuration of a calculator system including a storage system, and Fig. 11 is an example of a flash package which is a storage device of the storage system in Fig. 10.

[0043] The calculator system includes a plurality of computers 10 and a storage system 1. The computers 10 and the storage system 1 are connected via a communication network such as an SAN (Storage Area Network) 12.

[0044] The storage system 1 includes a storage controller 2 and a storage device group 14 connected to the storage controller 2. The storage device group 14 may be formed including various storage media or may be formed with storage media of the same type. In the present example, the storage device group 14 includes a plurality of flash packages 15.

[0045] The storage controller 2 includes a communication interface device, a storage device and a control device connected to the communication device and the storage device. The storage controller 2 includes, for example, an SAN interface (I/F) 6 and disk interface (I/F) 7 as a communication interface device. The SAN interface 6 is connected to an SAN 12 and the disk interface 7 is connected to the storage device group 14.

[0046] The storage controller 2 includes, for example, a memory 4 and a cache memory 5 as a storage device. Also, the storage controller 2 includes, for example, a CPU 3 as a control device. The control device may include a dedicated hardware circuit to perform predetermined processing (such as compression, decompression, encryption and decryption), in addition to a processor like the CPU 3.

[0047] The memory 4 stores various programs to manage the storage system 1 by the storage controller 2, and information. The CPU 3 can perform predetermined processing by executing the programs based on the information stored in the memory 4.

[0048] The cache memory 5 is normally a volatile memory such as a DRAM (Dynamic Random Access Memory). The cache memory 5 temporarily stores data written into

part of the storage device group 14 and data read from the storage device group 14. For example, the storage controller 2 accepts a writing request from the computer 10, writes data corresponding to the write request into the cache memory 5 and completes the write request (e.g. transmits a completion report for the writing request to the computer 10).

- [0049] The storage device group 14 includes a RAID (Redundant Array of Independent (or Inexpensive) Disks) group. The RAID group stores data according to a predetermined RAID level. Based on the storage space of the RAID group, a logical volume (hereinafter referred to as "VOL") is created. Regarding the VOL, there is a VOL type provided to the computer 10 and other VOL types. The former VOL is designated by an I/O request from the computer 10. The latter VOL is, for example, a component of a pool including a storage area assigned to a virtual VOL (i.e. VOL according to thin provisioning) provided to the computer 10.
- [0050] For example, as a RAID group, the storage device group 14 is formed with the plurality of flash packages 15. A configuration of the flash packages 15 will be explained using Fig. 11.
- [0051] The flash package 15 includes a plurality of FM (Flash Memory) chips 32 and an FM controller 20 connected thereto. The FM chip 32 is formed with, for example, a plurality of physical blocks. Each physical block is formed with a plurality of physical pages. The FM chip 32 is, for example, an NAND-type flash memory. Each cell of the FM chip 32 may be an SLC (Single Level Cell) or an MLC (Multi Level Cell).
- [0052] The FM controller 20 includes a communication interface device, a storage device and a control device connected to the communication interface device and the storage device. The FM controller 20 includes, for example, a higher interface (I/F) 23 and a plurality of FM interface (I/F) control units 24 as a communication interface device. Also, the FM controller 20 includes, for example, a DRAM 11 as a storage device. Also, the FM controller 20 includes, for example, a CPU 21 as a control device.
- [0053] The FM controller 20 is connected to the DRAM 11 via an internal bus 22. The DRAM 11 stores various programs to manage the flash package 15, and information. The CPU 21 can realize various functions by executing the programs based on the information stored in the DRAM 11.
- [0054] The FM interface control unit 24 is connected to an SW (Switch) 31 and the SW 31 is connected to a plurality of FM chips 32 mounted on the DIMM board 30. The FM interface control unit 24 independently controls the plurality of FM chips using a CE# signal. The FM interface control unit 24 operates in response to the reading/writing request from the CPU 21. In the reading/writing request, a physical address (PBA (Physical Block Address)) of the reading source or writing destination area is designated.

- [0055] The FM interface control unit 24 calculates a physical block and physical page of the reading source or writing destination from this PBA, and performs reading/writing processing with respect to the calculated physical block and physical page. Also, the FM interface control unit 24 includes an ECC (Error Correction Code) generation circuit and an ECC correction circuit. At the time of the writing of data, in a buffer, the ECC generation circuit generates an ECC with respect to compression data, and the compression data and the ECC are written in the FM chip 32. Also, at the time of the reading of data, compression data (e.g. reading data) from the FM chip 32 is checked in the ECC correction circuit and, in a case in which a data loss is detected, the compression data is corrected in the ECC correction circuit.
- [0056] The above examples are applicable to the signal transmission system between the FM interface control unit 24 and the FM chip 32 in Fig. 11. The FM interface control unit 24 includes an encode circuit that encodes a CE# signal. Also, the semiconductor device 700 is arranged between the FM interface control unit 24 and the FM chip 32. The semiconductor device 700 is mounted together with the FM chip 32 on the DIMM board 30.
- [0057] The semiconductor device 700 has the same function as in the above examples. That is, the semiconductor device 700 includes (1) a decode circuit that decodes a CE# signal encoded in the FM interface control unit 24, and (2) a control circuit that controls the CE# signal by an R/B# signal output from the FM chip 32 and, in a case in which a chip selected by the CE# signal is in a busy state, reports the busy state to the FM interface control unit 24 by a control signal.
- [0058] Also, the SW 31 corresponds to the switch circuit 800 in Fig. 7. The FM interface control unit 24 includes a circuit that outputs a control signal to control a switch in the SW 31. By this control signal, it is possible to control which signal line of DQ signal is selected in the SW 31. Naturally, as illustrated in Fig. 10, the SW 31 may be provided in the semiconductor device 700 such that a control signal for controlling the switch of the SW 31 is generated in the semiconductor device 700.
- [0059] According to the present example, it is effective to realize a low cost of the signal transmission system and further a large capacity and high-density mounting by connection of a flash memory device in a calculator system such as a storage system.
- [0060] Also, the above examples can be applied to a case in which a flash memory (FM) is used in the memory 4 or the cache memory 5 in the storage controller 2. For example, the above examples can be applied to the signal transmission system between the CPU 3, which controls these memories 4 and 5, and the memories 4 and 5.
- [0061] Also, the present invention is not limited to the above examples and includes various variation examples. For example, the above examples give a specific explanation to describe the present invention in an easily understood manner, and are not necessarily

limited to what includes all explained components. Also, it is possible to replace part of the configuration of a certain example with the configuration of another example, and it is possible to add the configuration of a certain example to the configuration of another example. Also, regarding part of the configuration of each example, it is possible to add, delete or replace a certain configuration.

[0062] Also, signal wires and the element of each configuration required for explanation are illustrated, and it is not always true that all signal wires and the element of each configuration are provided on products. Actually, a case is possible where there are a plurality of types of signal wire topologies connecting configurations and a plurality of elements of configurations.

Reference Signs List

- [0063]
- 1 Storage system
 - 2 Storage controller
 - 3 CPU
 - 4 Memory
 - 5 Cache memory
 - 6 SAN interface
 - 7 Disk interface
 - 10 Computer
 - 11 DRAM
 - 14 Storage device group
 - 15 Flash package
 - 20 FM controller
 - 21 CPU
 - 22 Internal bus
 - 23 Higher interface
 - 24 FM interface control unit (semiconductor memory control unit)
 - 30 DIMM board
 - 32 FM chip (semiconductor memory)
 - 100 Board
 - 200 Memory controller
 - 201 Circuit
 - 300 Flash memory (semiconductor memory)
 - 400 Encode circuit
 - 500 Decode circuit
 - 600 Control circuit
 - 700 Semiconductor device

800 Switch circuit

900 DIMM board

1000 DIMM connector

1100 Circuit

1101 First OR circuit

1102 Second OR circuit

Claims

- [Claim 1] A signal transmission system connecting a memory controller and a plurality of semiconductor memories, comprising:
a semiconductor device arranged between the memory controller and the plurality of semiconductor memories,
wherein the semiconductor device comprises a control circuit, and
wherein the control circuit receives a signal from the semiconductor memory and outputs a control signal to the memory controller in response to the signal from the semiconductor memory.
- [Claim 2] The signal transmission system according to claim 1, wherein the control circuit receives a first signal from the memory controller and transmits the first signal to the semiconductor memory, and
wherein the control circuit receives a second signal from the semiconductor memory that receives the first signal, and outputs the control signal to the memory controller in response to the second signal.
- [Claim 3] The signal transmission system according to claim 2, wherein the memory controller comprises an encode circuit that encodes the first signal, and the semiconductor device comprises a decode circuit that decodes the first signal encoded in the encode circuit, and
wherein in response to the second signal, the control circuit controls the operation for transmitting the first signal decoded in the decode circuit to the semiconductor memory.
- [Claim 4] The signal transmission system according to claim 3, further comprising a switch circuit that is arranged between the memory controller and the plurality of semiconductor memories, and switches a data signal.
- [Claim 5] The signal transmission system according to claim 4, wherein the memory controller comprises a circuit that transmits a control signal for controlling the switch of the data signal to the switch circuit.
- [Claim 6] The signal transmission system according to claim 4, wherein the switch circuit is mounted in the semiconductor device, and the switch circuit controls the switch of the data signal by a control signal generated based on the first signal.
- [Claim 7] The signal transmission system according to claim 4, wherein the plurality of semiconductor memories and the switch circuit are mounted on a DIMM board.
- [Claim 8] The signal transmission system according to claim 7, wherein the semi-

conductor device is mounted on the DIMM board.

[Claim 9] The signal transmission system according to any one of claims 2 to 8, wherein the semiconductor memory is an NAND-type flash memory, the first signal is a signal for selecting a chip for the NAND-type flash memory, and the second signal is a ready busy signal for notifying a chip operation state.

[Claim 10] A storage system comprising a storage controller and a storage device group comprising a plurality of semiconductor memory packages, wherein the semiconductor memory package comprises a semiconductor memory control unit, a plurality of semiconductor memories and a semiconductor device arranged between the semiconductor memory control unit and the plurality of semiconductor memories, wherein the semiconductor device comprises a control circuit, and wherein the control circuit receives a signal from the semiconductor memory and outputs a control signal to the semiconductor memory control unit in response to the signal from the semiconductor memory.

[Claim 11] The storage system according to claim 10, wherein the control circuit receives a first signal from the semiconductor memory control unit and transmits the first signal to the semiconductor memory, and wherein the control circuit receives a second signal from the semiconductor memory that receives the first signal, and outputs the control signal to the semiconductor memory control unit in response to the second signal.

[Claim 12] The storage system according to claim 11, wherein the semiconductor memory control unit comprises an encode circuit that encodes the first signal, and the semiconductor device comprises a decode circuit that decodes the first signal encoded in the encode circuit, and wherein in response to the second signal, the control circuit controls the operation for transmitting the first signal decoded in the decode circuit to the semiconductor memory.

[Claim 13] The storage system according to claim 12, further comprising a switch circuit that is arranged between the semiconductor memory control unit and the plurality of semiconductor memories, and switches a data signal.

[Claim 14] The storage system according to claim 13, wherein the semiconductor memory control unit comprises a circuit that transmits a control signal for controlling the switch of the data signal to the switch circuit.

[Claim 15] The storage system according to claim 13, wherein the switch circuit is

mounted in the semiconductor device, and the switch circuit controls the switch of the data signal by a control signal generated based on the first signal.

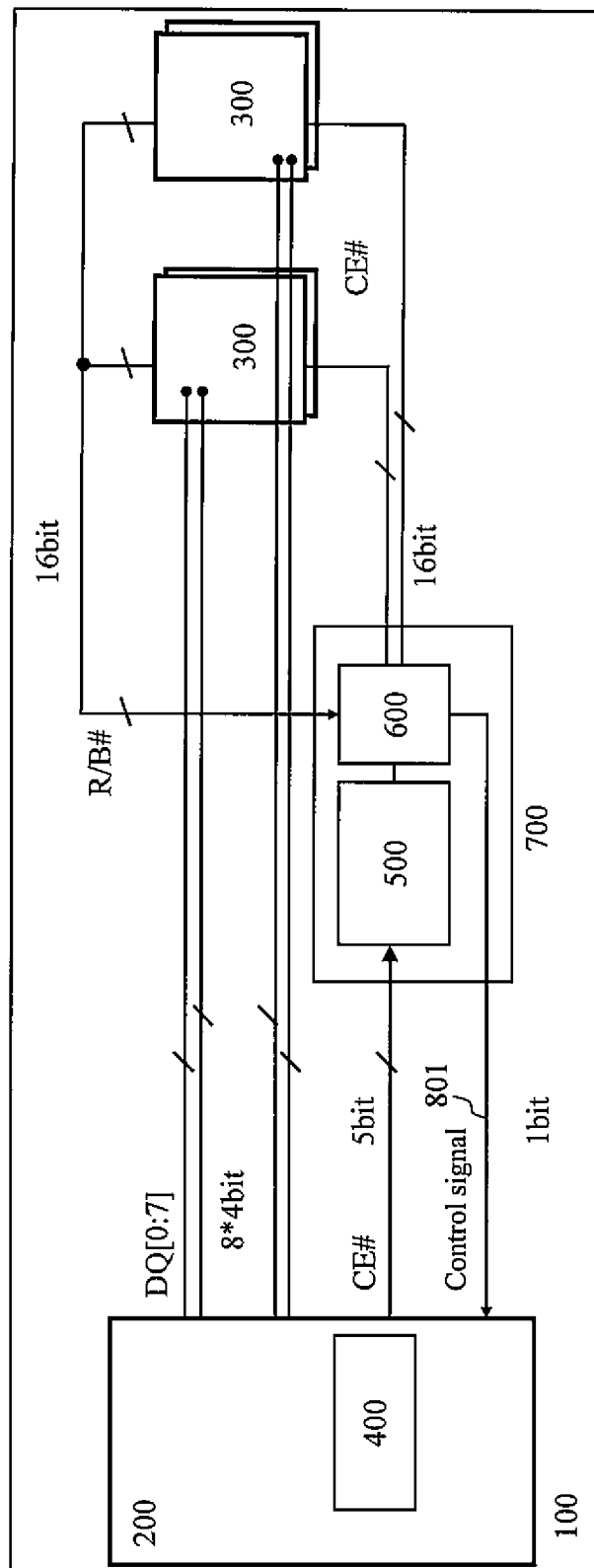
[Claim 16] The storage system according to claim 13, wherein the plurality of semiconductor memories and the switch circuit are mounted on a DIMM board.

[Claim 17] The storage system according to claim 16, wherein the semiconductor device is mounted on the DIMM board.

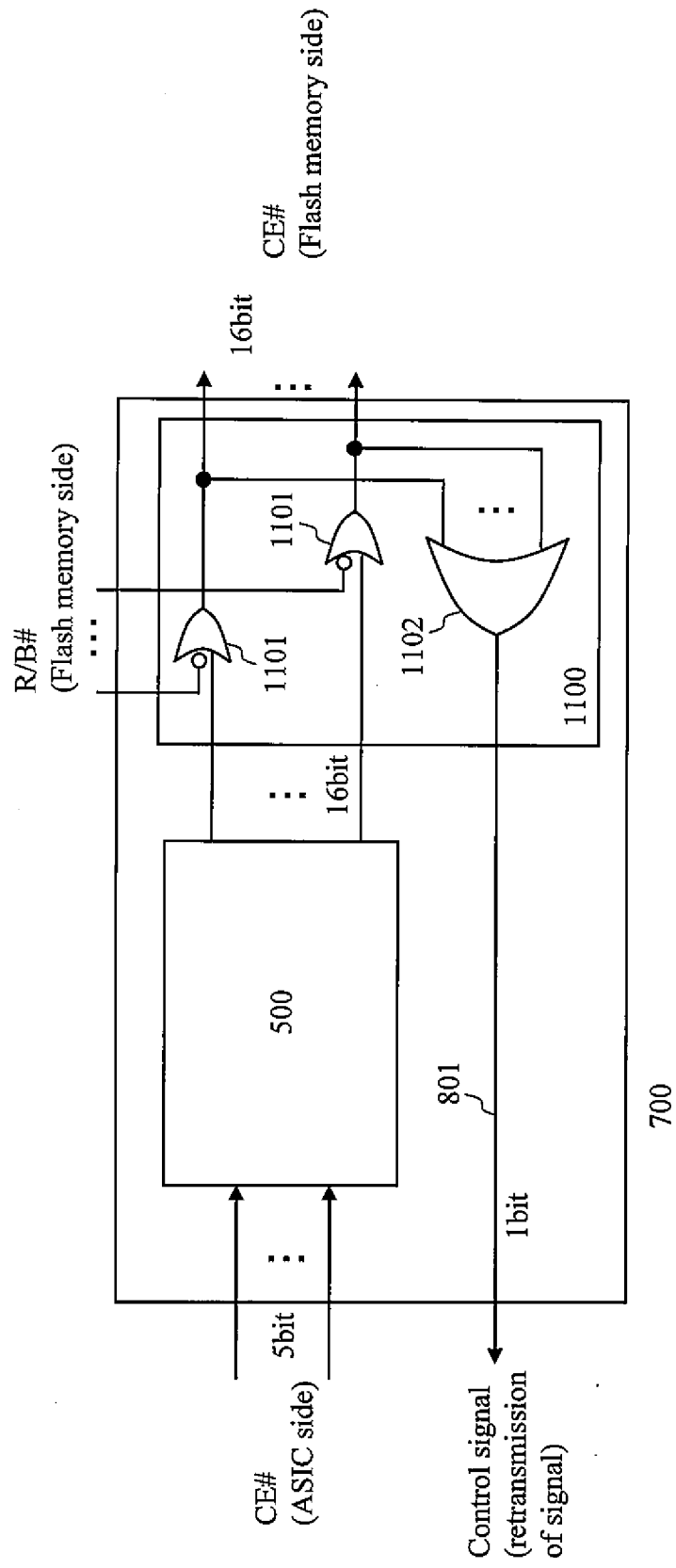
[Claim 18] The storage system according to any one of claims 11 to 17, wherein the semiconductor memory is an NAND-type flash memory, the first signal is a signal for selecting a chip for the NAND-type flash memory, and the second signal is a ready busy signal for notifying a chip operation state.

[Fig. 1]

Fig. 1

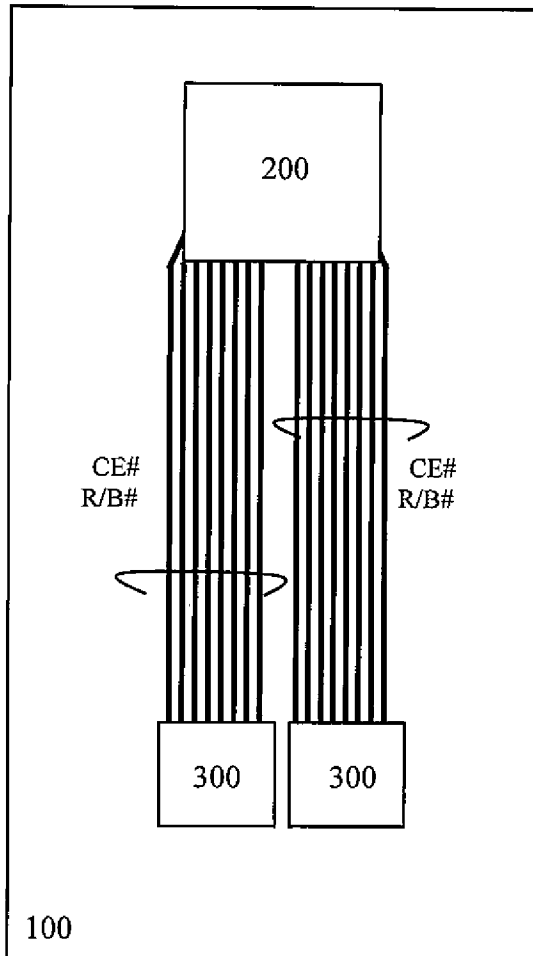


[Fig. 2]



[Fig. 3]

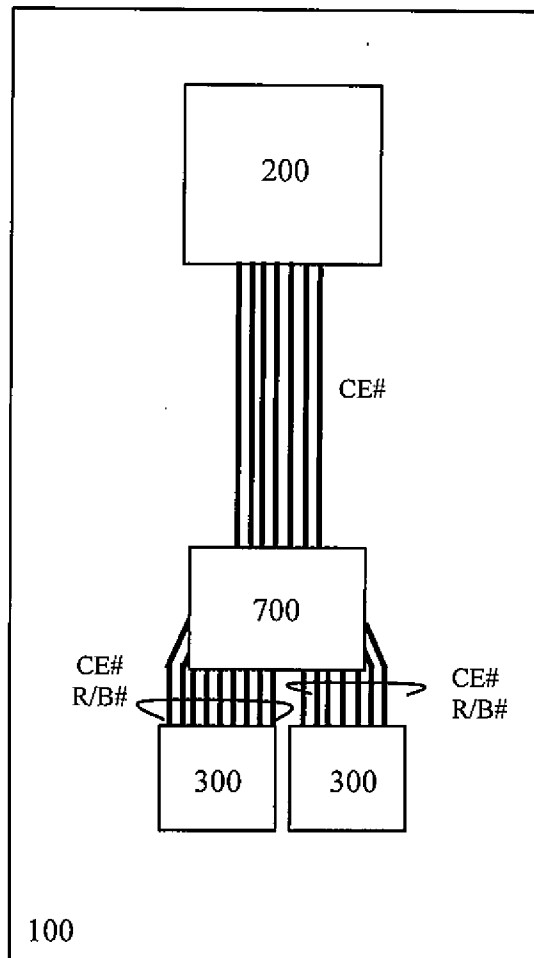
Fig. 3



(Related art)

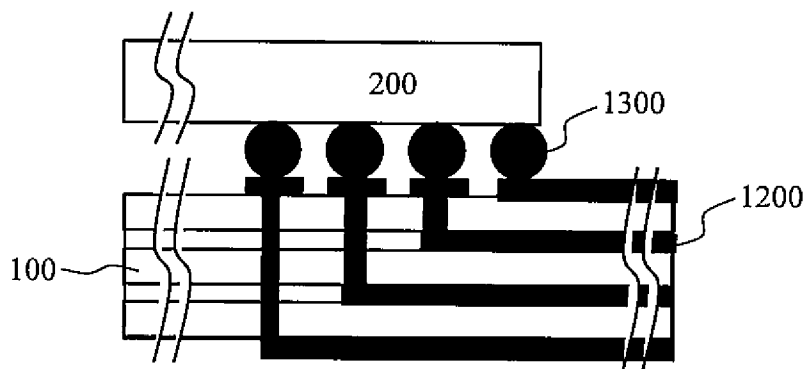
[Fig. 4]

Fig. 4



[Fig. 5]

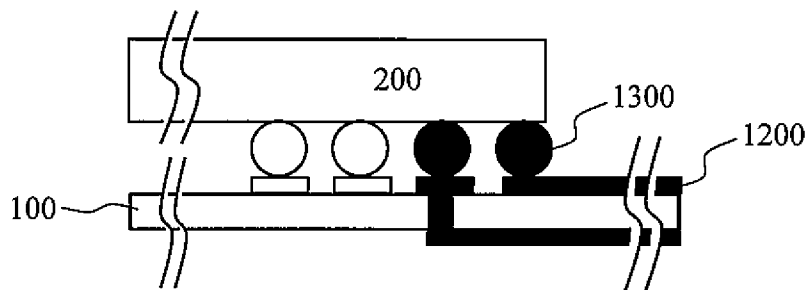
Fig. 5



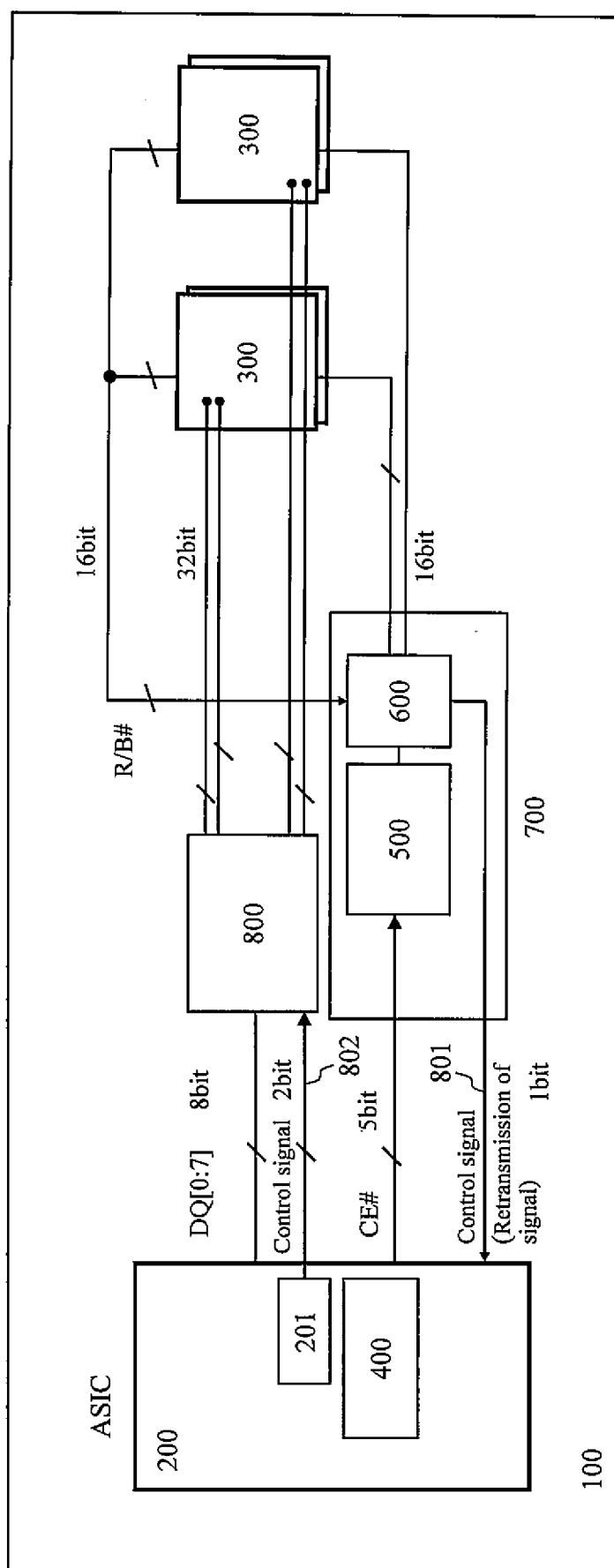
(Related art)

[Fig. 6]

Fig. 6

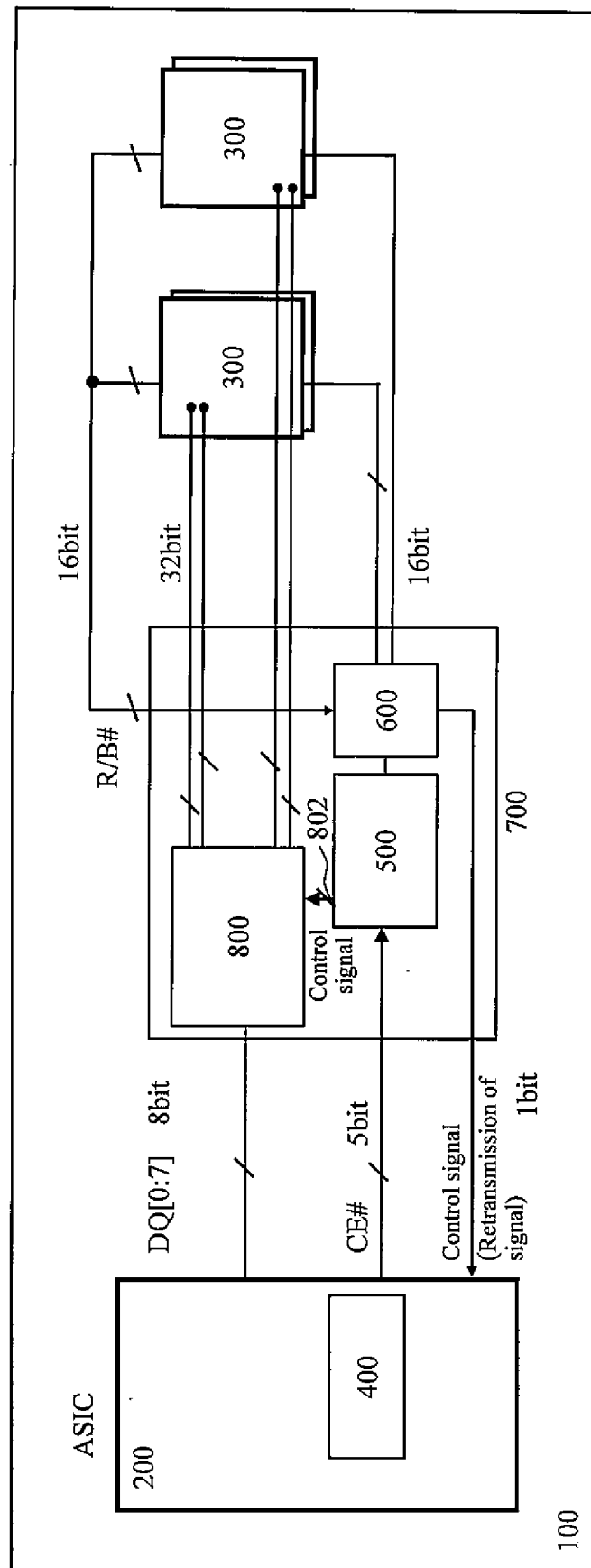


[Fig. 7]



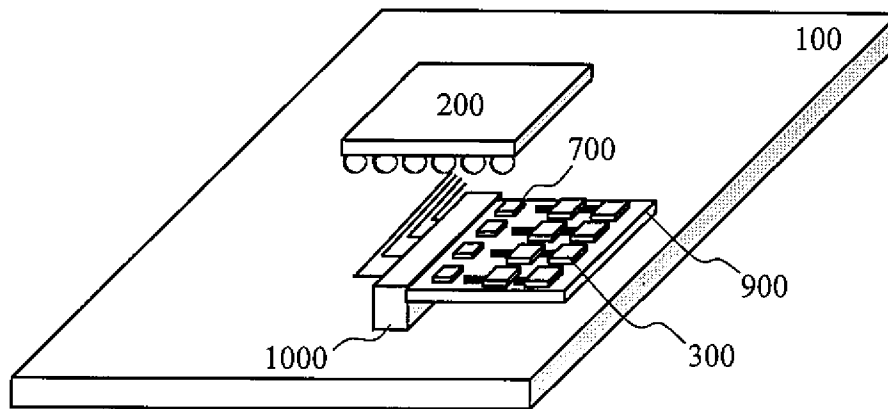
[Fig. 8]

Fig. 8



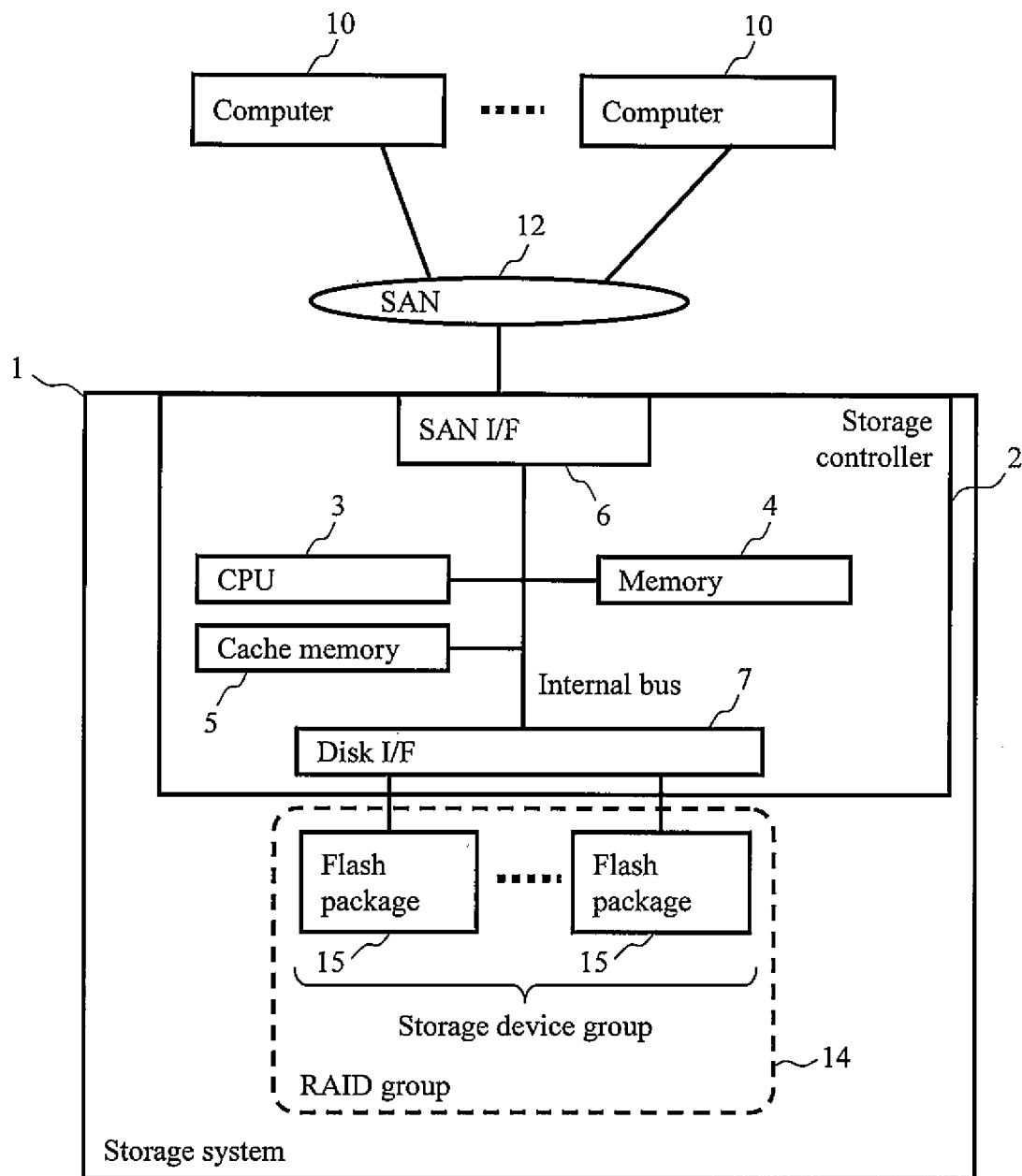
[Fig. 9]

Fig. 9



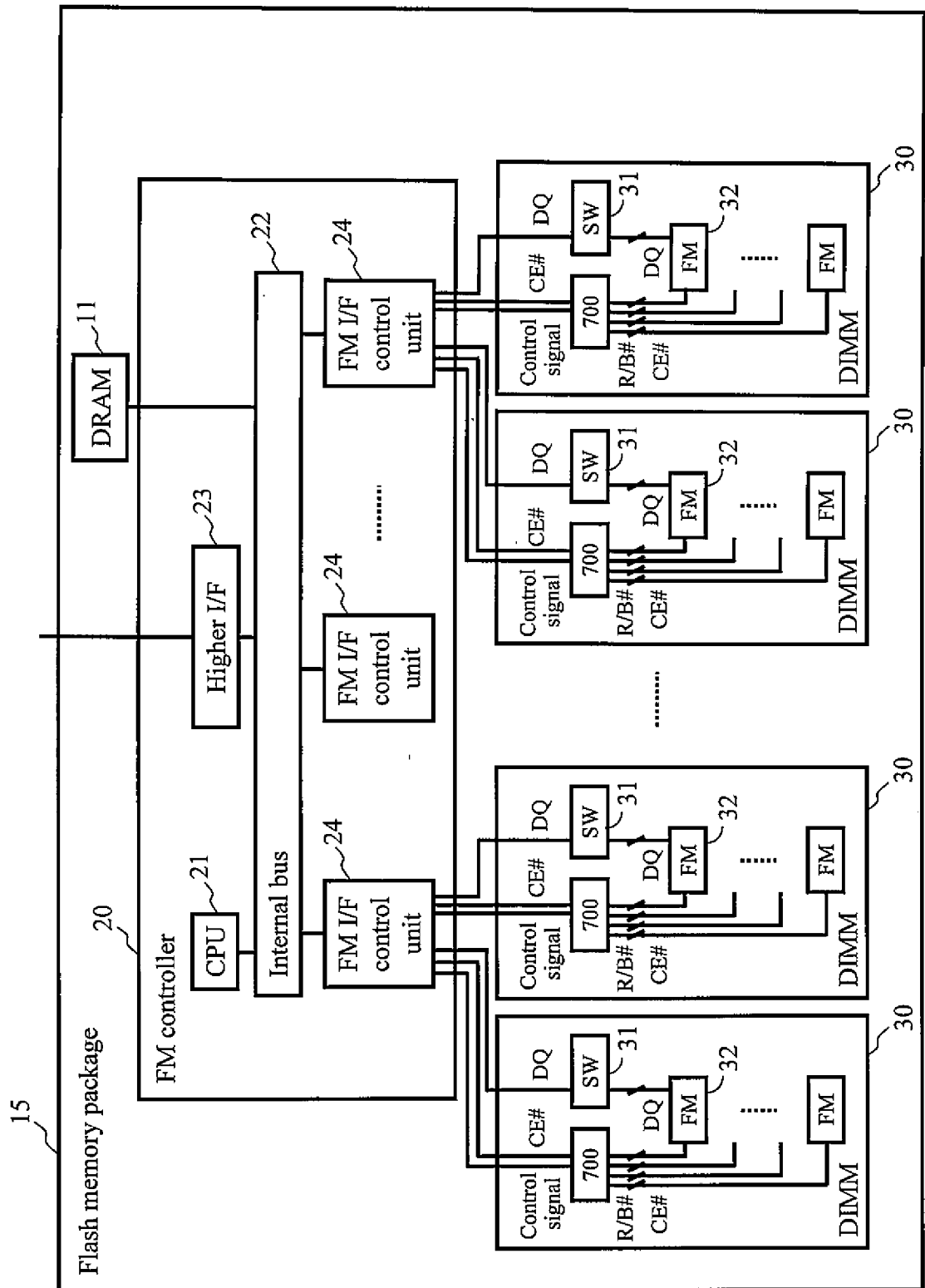
[Fig. 10]

Fig. 10



[Fig. 11]

Fig. 11



INTERNATIONAL SEARCH REPORT

International application No
PCT/JP2012/006759

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F13/42 G06F12/02
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 822 251 A (BRUCE RICARDO H [US] ET AL) 13 October 1998 (1998-10-13) abstract; figures 2,4	1-18
X	US 2005/286284 A1 (SEE SUN-TECK [US] ET AL) 29 December 2005 (2005-12-29) abstract; figure 4A paragraphs [0010], [0011], [0013], [0033] - [0037]	1-18
A	US 2004/006664 A1 (HELZER AMIR [IL] ET AL) 8 January 2004 (2004-01-08) abstract	1-18



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

2 May 2013

Date of mailing of the international search report

14/05/2013

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Jünger, Bernhard

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/JP2012/006759

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5822251	A	13-10-1998	NONE
US 2005286284	A1	29-12-2005	NONE
US 2004006664	A1	08-01-2004	AU 2003253775 A1 23-01-2004
			US 2004006664 A1 08-01-2004
			WO 2004006263 A1 15-01-2004