

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
1 June 2006 (01.06.2006)

PCT

(10) International Publication Number
WO 2006/057793 A3

(51) International Patent Classification:
G06F 11/10 (2006.01) **GI1C 29/00** (2006.01)

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(21) International Application Number:
PCT/US2005/040086

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(22) International Filing Date:
3 November 2005 (03.11.2005)

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/997,604 23 November 2004 (23.11.2004) US

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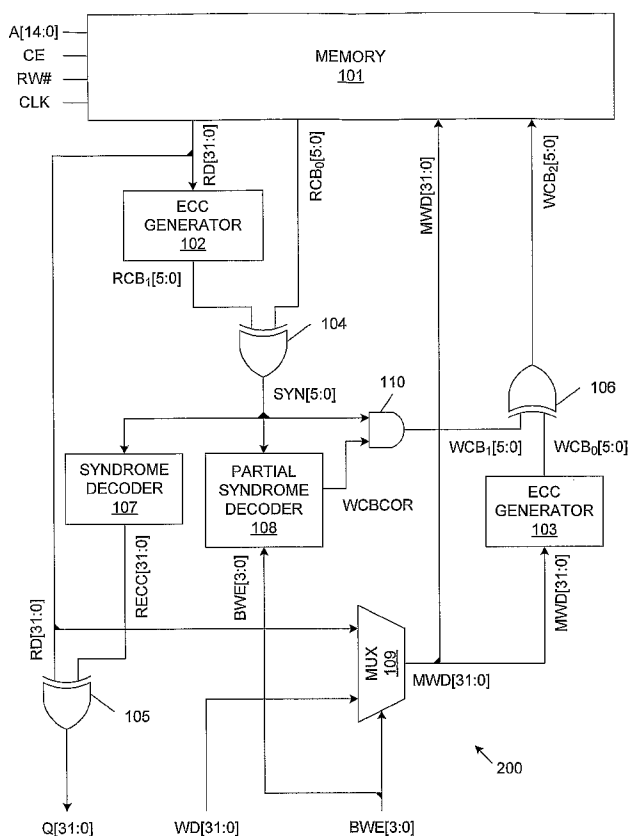
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,

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[Continued on next page]

(54) Title: PREDICTIVE ERROR CORRECTION CODE GENERATION FACILITATING HIGH-SPEED BYTE-WRITE IN A SEMICONDUCTOR MEMORY



(57) Abstract: Write check bits are generated in a predictive manner for partial-word write transactions in a memory system implementing error correction coding. A read data word (RD) and associated read check bits (RCB) are read from a memory (101) address. If an error exists in a byte of the read data word, this byte is identified. At the same time, one or more bytes of the uncorrected read data word are merged with one or more bytes of a write data word (WD), thereby creating a merged data word (MWD). Write check bits (WCB) are generated in response to the merged data word. If the merged data word includes a byte of the read data word which contains an error, the write check bits are modified to reflect this error. The merged data word and the modified (or unmodified) write check bits are then written to the address.



FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT,
RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA,
GN, GQ, GW, ML, MR, NE, SN, TD, TG).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

- *with international search report*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report:

31 May 2007

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US05/40086

A. CLASSIFICATION OF SUBJECT MATTER

IPC: **G06F 11/10**(2006.01);**G11C 29/00**(2006.01)

USPC: 711/155;714/773

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 711/155; 714/773

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 3,814,921 A (NIBBY et al) 04 June 1974 (04.06.1974), see the abstract and figure 2.	1-8

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

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Date of the actual completion of the international search

12 February 2007 (12.02.2007)

Date of mailing of the international search report

04 APR 2007

Name and mailing address of the ISA/US

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