Abstract: A memory array includes a plurality of memory cells (20) formed on a semiconductor substrate (22). Individual of the memory cells include first (24) and second (26) field effect transistors respectively comprising a gate (28/30), a channel region, and a pair of source/drain regions. The gates of the first and second field effect transistors are formed in openings in the substrate and are hard wired together. A conductive data is formed in openings in the substrate and line is hard wired to two of the source/drain regions. A charge storage device is hard wired to at least one of the source/drain regions other than the two.
GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, 
ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), 
European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, 
FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, 
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