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(54) **Title**: EXTENDED USE OF LOGARITHM AND EXPONENT INSTRUCTIONS

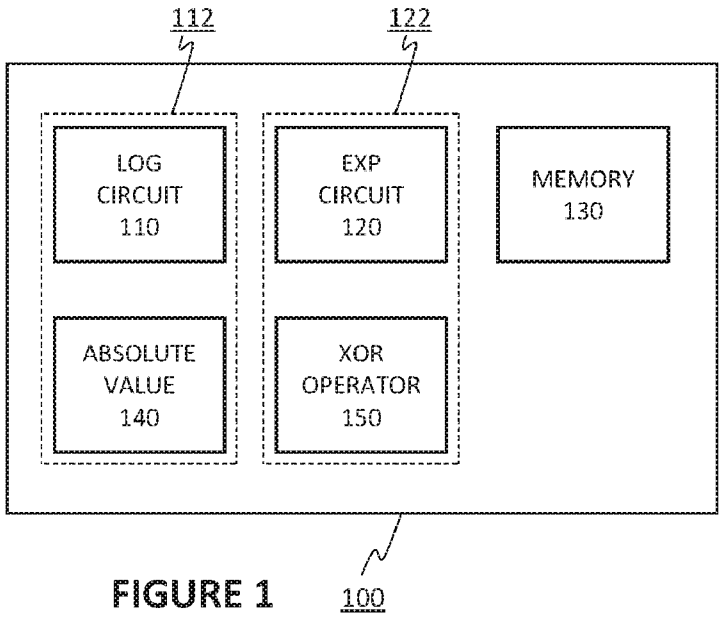


FIGURE 1

(57) **Abstract**: Embodiments of the present disclosure are based on a recognition that some processors are configured with instructions to compute logarithms and exponents (i.e. some processors include log and exp circuits). Embodiments of the present disclosure are further based on an insight that the use of the existing log and exp circuits could be extended to compute certain other functions by using the existing log and exp circuits to transform from a Cartesian to a logarithmic domain and vice versa and performing the actual computations of the functions in the logarithmic domain, which may be computationally easier than performing the computations in the Cartesian domain.

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EXTENDED USE OF LOGARITHM AND EXPONENT INSTRUCTIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of and priority from U.S. Patent Application Serial No. 14/685,978 filed 14 April 2015 entitled "EXTENDED USE OF LOGARITHM AND EXPONENT INSTRUCTIONS," which is incorporated herein by reference in its entirety.

TECHNICAL FIELD OF THE DISCLOSURE

[0002] The present invention relates to computer processing techniques, in particular to systems and methods for computing various functions of one or more input variables.

BACKGROUND

[0003] Configuring processors with instructions to compute various functions, from multiplication and division to nonlinear functions such as e.g. square roots, reciprocals, and reciprocal square roots, is not a trivial task. What is needed in the art are systems and methods that improve on this task.

OVERVIEW

[0004] One aspect of the present invention provides an apparatus for computing a nonlinear function of an input variable (X). The apparatus includes a logarithmic (log) circuit configured to compute a logarithm of a first input value and a reciprocal circuit configured to obtain (e.g. access in a shared memory that may be accessible by both the log circuit and the reciprocal circuit, or receive from the log circuit) the computed logarithm of the first input value. The reciprocal circuit is configured to, when enabled, negate the logarithm of the first input value and provide the negated logarithm of the first input value as an output of the reciprocal circuit, and, when disabled, provide the logarithm of the first input value as the output of the reciprocal circuit. The apparatus further includes a root circuit configured to obtain (e.g. access in a shared memory that

may be accessible by both the reciprocal circuit and the root circuit, or receive from the root circuit) the output of the reciprocal circuit and configured to, when enabled, divide the received output of the reciprocal circuit by N and provide the divided output of the reciprocal circuit as an output of the root circuit, and, when disabled, provide the received output of the reciprocal circuit as the output of the root circuit. The apparatus further includes a control logic configured to enable the reciprocal circuit and disable the root circuit when the nonlinear function is a reciprocal, disable the reciprocal circuit and enable the root circuit when the nonlinear function is a Nth root (e.g. when N=2, the function is a square root; when N=3, the function is a cubed root, etc.), and enable the reciprocal circuit and enable the root circuit when the nonlinear function is a reciprocal Nth root.

[0005] As is clear from present disclosure, circuits referred to herein as "reciprocal circuit" and "root circuit" or "square root circuit" do not actually perform the reciprocal and root or square root computations as understood in a Cartesian domain, but are configured to modify values in the logarithmic domain in a way that correspond to the desired function in the Cartesian domain.

[0006] A corresponding method for computing a nonlinear function of an input variable is also disclosed. The method includes instructing a logarithmic circuit to compute a logarithm of a first input value, and instructing a reciprocal circuit to obtain the logarithm of the first input value and to perform, when enabled, negate the logarithm of the first input value and provide the negated logarithm of the first input value as an output of the reciprocal circuit, and, when disabled, provide the logarithm of the first input value as the output of the reciprocal circuit. The method further includes instructing a root circuit to obtain the output of the reciprocal circuit and to perform, when enabled, divide the received output of the reciprocal circuit by 2 and provide the divided output of the reciprocal circuit as an output of the root circuit, and, when disabled, provide the received output of the reciprocal circuit as the output of the root circuit. The method also includes enabling the reciprocal circuit and disabling the root circuit when the nonlinear function is a reciprocal, disabling the reciprocal circuit and enabling the root circuit when the nonlinear function is an Nth root, and enabling the

reciprocal circuit and enabling the root circuit when the nonlinear function is a reciprocal Nth root.

[0007] According to another aspect of the present disclosure, an apparatus for computing an Nth root of an input variable is provided. The apparatus includes a logarithmic circuit configured to compute a logarithm of a first input value, a root circuit configured to divide the logarithm of the first input value by N and provide the divided logarithm as an output of the root circuit, and an exponential circuit configured to compute an exponent of the output of the root circuit.

[0008] According to still another aspect of the present disclosure, an apparatus for computing a reciprocal of an input variable is provided. The apparatus includes a logarithmic circuit configured to compute a logarithm of a first input value; a reciprocal circuit configured to negate the logarithm of the first input value and provide the negated logarithm of the first input value as an output of the reciprocal circuit; and an exponential circuit configured to compute an exponent of the output of the reciprocal circuit.

[0009] In some embodiments of the various aspects described above, the apparatus may further include an absolute value circuit configured to compute an absolute value of the input variable, store a sign of the input variable, and provide the computed absolute value to the logarithmic circuit as the first input value. In such embodiments, the exponential circuit may further be configured to combine the computed exponent with the stored sign of the input variable.

[0010] According to yet another aspect of the present disclosure, an apparatus for performing a multiplication of two input variables is provided. The apparatus includes an absolute value circuit configured to compute an absolute value of a first input variable and determine (and possibly store) a sign of the first input variable, and compute an absolute value of a second input variable and determine (and possibly store) a sign of the second input variable, a logarithmic circuit configured to compute a logarithm of the absolute value of the first input variable and to compute a logarithm of the absolute value of the second input variable, a multiplication circuit configured to compute a sum by adding the logarithm of the absolute value of the first input variable to the logarithm

of the absolute value of the second input variable and provide the sum as an output of the multiplication circuit, an XOR circuit configured to perform an XOR operation on Boolean values representing the sign of the first input variable and the sign of the second input variable, and an exponential circuit configured to compute an exponent of the output of the multiplication circuit and to combine the exponent with an outcome of the XOR operation on the Boolean values representing the sign of the first input variable and the sign of the second input variable.

[0011] According to yet another aspect of the present disclosure, an apparatus for performing a division of two input variables is provided. The apparatus includes an absolute value circuit configured to compute an absolute value of a first input variable and determine (and possibly store) a sign of the first input variable, and compute an absolute value of a second input variable and determine (and possibly store) a sign of the second input variable, a logarithmic circuit configured to compute a logarithm of the absolute value of the first input variable and to compute a logarithm of the absolute value of the second input variable, a division circuit configured to compute a difference by subtracting the logarithm of the absolute value of the second input variable from the logarithm of the absolute value of the first input variable and provide the difference as an output of the division circuit, an XOR circuit configured to perform an XOR operation on Boolean values representing the sign of the first input variable and the sign of the second input variable, and an exponential circuit configured to compute an exponent of the output of the division circuit and to combine the exponent with an outcome of the XOR operation on the Boolean values representing the sign of the first input variable and the sign of the second input variable.

[0012] Other aspects of the present disclosure relate to methods performed by an apparatus or enabling an apparatus according to any one of the aspects described herein to carry out its' functionality, as well as to computer programs and computer-readable storage medium, preferably non-transitory, comprising instructions for carrying out such methods.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] To provide a more complete understanding of the present disclosure and features and advantages thereof, reference is made to the following description, taken in conjunction with the accompanying figures, wherein like reference numerals represent like parts, in which:

[0014] FIGURE 1 is a diagram illustrating a system configured to perform multiplication and division, according to some embodiments of the present invention;

[0015] FIGURE 2A is a diagram illustrating an extended log circuit configured to be used in performing multiplication and division, according to some embodiments of the present invention;

[0016] FIGURE 2B is a diagram illustrating an extended exp circuit configured to be used in performing multiplication and division, according to some embodiments of the present invention;

[0017] FIGURE 3 is a flow diagram of method steps illustrating use of the system of FIGURE 1 and/or extended circuits of FIGUREs 2A and/or 2B to perform multiplication and division, according to some embodiments of the present invention;

[0018] FIGURE 4 is a diagram illustrating a system configured to perform reciprocal, square root, and/or reciprocal square root calculations, according to some embodiments of the present invention;

[0019] FIGURE 5 is a diagram illustrating an extended log circuit configured to be used in performing reciprocal, square root, and/or reciprocal square root calculations, according to some embodiments of the present invention; and

[0020] FIGURE 6 is a flow diagram of method steps illustrating use of the system of FIGURE 4 and/or the extended log circuit of FIGURE 5 to perform reciprocal, square root, and/or reciprocal square root calculations, according to some embodiments of the present invention.

DESCRIPTION OF EXAMPLE EMBODIMENTS OF THE DISCLOSURE

[0021] Embodiments of the present disclosure are based on a recognition that some processors are configured with instructions to compute logarithms and exponents,

for example with log2 and exp2 instructions which could be used e.g. for the purpose of greater dynamic range when representing numbers between 0 and 1. Processor instructions to compute logarithms and exponents are referred to in the following as "log circuits" and "exp circuits," respectively. Embodiments of the present disclosure are further based on an insight that the use of the existing log and exp circuits could be extended to compute certain other functions by using the existing log and exp circuits to transform from a Cartesian to a logarithmic domain and vice versa and performing the actual computations of the functions in the logarithmic domain because doing so may be computationally easier than performing the computations in the Cartesian domain.

[0022] Such an approach may be useful for functions such as division and multiplication, in case the processor does not have multiplication or division instructions, because multiplication and division in a Cartesian domain translates to simple addition and subtraction in a logarithmic domain, as illustrated by the following equations:

$$(xy) = exp_b(log_b(x) + log_b(y)) \qquad (1)$$

$$(x/y) = exp_b(log_b(x) - log_b(y)) \qquad (2)$$

[0023] However, logarithmic computations can only work on positive inputs, which prevents the straightforward use of this approach for many applications where computations need to be performed with negative inputs or where it is not known ahead of time whether the input will be positive or negative.

[0024] Such an approach may also be useful for computing nonlinear functions such as square root, reciprocal, and reciprocal square root, because computation of such functions may also be made easier and more efficient in the logarithmic domain, as illustrated by the following equations:

$$\sqrt{x} = exp_b\left(\frac{1}{2} * log_b(x)\right) \qquad (3)$$

$$\frac{1}{x} = exp_b(-(log_b(x)) \qquad (4)$$

$$\frac{1}{\sqrt{x}} = exp_b((-(log_2(x)) \gg 1) \qquad (5)$$

[0025] Therefore, it would be desirable to extend the functionality of the existing log and exp circuits to calculate other nonlinear functions, in particular reciprocals (e.g. inverse), square root, and inverse square root.

Performing computations in the logarithmic domain on any non-zero number

[0026] FIGURE 1 is a diagram illustrating a system 100 configured to perform multiplication and division, according to some embodiments of the present invention. As shown, the system 100 includes a log circuit 110 for performing computation of a logarithm to a certain base on an input value received by the circuit, an exp circuit 120 for performing computation of an exponent to a certain base on an input value received by the circuit, and a memory 130 for e.g. storing input values, results of intermediate computations, and/or final results. The memory 130 could comprise any memory such as, but not limited to, hardware registers, cache memory, system memory, processors state condition codes, external storage, or any other types of available destinations for processor instructions.

[0027] In addition, the system 100 further includes an absolute value circuit 140, i.e. instructions for computing an absolute value of an input value received by this circuit and storing the sign of the original input value, e.g. in the memory 130. Further, the system 100 also includes an XOR operator circuit 150, i.e. instructions for performing an XOR operation on two or more Boolean inputs received by this circuit.

[0028] In an embodiment, the absolute value 140 could be implemented by extending the functionality of existing log circuit 110 (shown in FIGURE 1 with a dashed box 112 surrounding the log circuit 110 and the absolute value 140) by adding the ability to perform the absolute value function on a number prior to putting that value through the existing log circuit. The log circuit 110 could then be configured to write the original sign and the computed log of the absolute value to processor registers. Additionally or alternatively, in an embodiment, the XOR operator 150 could be implemented by extending the functionality of existing exp circuit 120 (shown in FIGURE 1 with a dashed box 122 surrounding the exp circuit 120 and the XOR operator 150) by adding the ability to perform the XOR operation and applying the correct sign to the final output of multiplication or division. Such extended log and exp circuits 112 and 122 are shown in FIGUREs 2A and 2B, respectively.

[0029] Operation of the system 100 is further illustrated in FIGURE 3.

[0030] FIGURE 3 is a flow diagram 300 of method steps illustrating use of the system of FIGURE 1 to perform multiplication and division, according to some embodiments of the present invention. While FIGURE 3 is described with reference to the system of FIGURE 1, any system configured to perform steps illustrated in FIGURE 3, in any order, is within a scope of the present disclosure.

[0031] The method 300 may begin in step 302, where the system 100 receives input values X and Y to compute either multiplication or a division operation on them. To that end, in an embodiment, the extended log circuit 112 may be called with each input value (shown as "input 202" in FIGURE 2A) taken from the memory 130, e.g. from a respective processor register (or, if performed sequentially for two input values, from the same input value processor register).

[0032] In step 304, the sign of the input value X is extracted (shown as "original sign 204" in FIGURE 2A) and is written to the memory 130 (shown as "result sign 208" in FIGURE 2A), e.g. to a processor register designated for that purpose, and, in step 306, the absolute value operation is performed on the input value (shown as "absolute value 206" in FIGURE 2A). Steps 304 and 306 may be performed either by the extended log circuit 112, as indicated above with references to FIGURE 2A, or by the absolute value circuit 140. Preferably, the signs of X and Y are stored as Boolean values – e.g. "0" indicating a positive value and "1" indicating a negative value.

[0033] In step 308, the original log circuit is called with the absolute value computed in step 306 (shown as "log 210" in FIGURE 2A). The output of the log circuit is written to the memory 130, e.g. to a processor register designated for that purpose (shown as "result log 212" in FIGURE 2A).

[0034] Steps 304-308 are performed for the input value Y as well.

[0035] When the method 300 proceeds to step 310, logarithmic values for X and Y have been computed. In step 310, the system 100 performs computation of an intermediary result in the logarithmic domain using the logarithmic values for X and Y obtained in step 308. If the desired operation is multiplication X*Y, then in step 310 the system 100 adds the logarithmic values for X and Y in accordance with equation (1). If

the desired operation is division X/Y, then in step 310 the system 100 subtracts the logarithmic value of Y from that of X in accordance with equation (2).

[0036] In step 312, the exp circuit 120 computes the exponent of the intermediary result computed in step 310.

[0037] In step 314, the XOR operator 150 performs XOR operation on the stored signs of X and Y. If e.g. "0" was stored to indicate a positive value and "1" was stored to indicate a negative value, then the outcome of XOR operator 150 would be "0" if either both X and Y were positive or both X and Y were negative, and would be "1" if one of X and Y was positive and the other one was negative.

[0038] In step 316, the result in the Cartesian domain is obtained by combining the result of using the exp circuit in step 312 with the result of the XOR operation in step 314.

[0039] In one embodiment, steps 312-316 could be performed by the system 100.

[0040] In an embodiment where steps 312-316 are performed by the extended exp circuit 122, these steps may include calling the extended instruction 122 with the value taken from the memory (e.g. processor register) containing the output of the add/subtract of step 310 (shown as "input 214" in FIGURE 2B). The original exp circuit may then be used to calculate the output in Cartesian format, as shown with "exp 216" in FIGURE 2B. XOR is performed (shown as "XOR 222" in FIGURE 2B) on the values in the two registers (shown as "sign X 218" and "sign Y 220" in FIGURE 2B) that contain the original sign values that were stored in step 304. The result of 222 is then used to select (shown as "sign decision 224" in FIGURE 2B) whether the result of 216, or a negated version of that result, is provided as a result of the multiplication/division (shown as "final result 226" in FIGURE 2B), e.g. written as the output to a processor register.

[0041] In FIGUREs 2A and 2B, grey shading and thicker lining is used to illustrate functionality that is added to the conventional log and exp circuits, respectively, to arrive at the extended log and exp circuits illustrated in these FIGUREs. Thus, in FIGURE 2A, elements 204, 206, and 208 are added, while in FIGURE 2B, elements 218, 220, 222, and 224 are added.

[0042] While functionality of the extended log and exp circuits illustrated in FIGUREs 2A and 2B was described with reference to multiplication and division (i.e. two input values), these circuits, with modifications as would be apparent to a person skilled in the art, could also be used to perform operations in the logarithmic domain on any negative input value.

Extending functionality of existing log and exp circuits to compute other nonlinear functions

[0043] FIGURE 4 is a diagram illustrating a system 400 configured to perform reciprocal, square root, and/or reciprocal square root calculations, according to some embodiments of the present invention. As shown, the system 400 includes a log circuit 410 for performing computation of a logarithm to a certain base on an input value received by the circuit, an exp circuit 420 for performing computation of an exponent to a certain base on an input value received by the circuit, and a memory 430 for e.g. storing input values, results of intermediate computations, and/or final results. Discussions provided for the memory 130 are applicable to the memory 430 and, in the interests of brevity, are not repeated.

[0044] In addition, the system 400 further includes an absolute value circuit 440, i.e. instructions for computing an absolute value of an input value received by this circuit and storing the sign of the original input value, e.g. in the memory 430. Further, the system 400 may also include a reciprocal circuit 460, i.e. instructions for performing a reciprocal operation on an input received by this circuit and/or a square root circuit 470, i.e. instructions for performing a square root operation on an input received by this circuit. In the following, unless specified otherwise, the system 400 is described to have the functionality to both compute reciprocals and square roots (by including, respectively, circuits 460 and 470). However, in various embodiments, the system 400 may include only one of these circuits, e.g. only the reciprocal circuit 460 or only the square root circuit 470.

[0045] In an embodiment, the absolute value 440 and one or both of the reciprocal circuit 460 and the square root circuit 470 could be implemented by extending

the functionality of existing log circuit 410 (shown in FIGURE 4 with a dashed box 412 surrounding the log circuit 410, the absolute value 440, the reciprocal circuit 460, and the square root circuit 470) by adding the ability to perform the absolute value function on an input value prior to putting that value through the reciprocal and/or square root circuits. Such extended log circuits 412 is shown in FIGURE 5.

[0046] As shown in FIGURE 5, extra functionality to be added to the existing log instruction could be to modify the output the existing log circuit, divide the log result by 2 for square root and/or negate the result for reciprocal selected by the operation code ("opcode"). After that, once the extended log instruction is complete, the exp instruction can be executed to bring the result back to the Cartesian domain. The output of the exp instruction will be the result of the function specified by the log instruction's opcode. The sign for the output could be decided by the stored sign of the original input value, similar to the manner described above.

[0047] Turning to FIGURE 5 in greater detail, as shown, input value X (shown as "input 502" in FIGURE 5) is used to extract and store the original sign of the input value (shown, respectively, as "original sign 504" and "result sign 506" in FIGURE 5). The absolute value of the input value X is then computed (shown as "absolute value 508" in FIGURE 5). The absolute value of X is passed to the existing log circuit, such as e.g. log circuit 410 (shown as "log 510" in FIGURE 5), which converts the absolute value of the input value X to the logarithmic domain.

[0048] In case both the reciprocal circuit 460 and the square root circuit 470 are implemented, a SELECT functionality may be implemented by a control logic (not shown in FIGUREs) configured to provide a select signal indicating which calculation is to be performed on the input value in the logarithmic domain (i.e. on the output of the log 510). A RECIPROCAL SELECT signal could be used to indicate that reciprocal of X is to be computed (shown as "reciprocal select 512" in FIGURE 5), while a SQUARE ROOT SELECT signal could be used to indicate that square root of X is to be computed (shown as "square root select 514" in FIGURE 5). Both RECIPROCAL SELECT and SQUARE ROOT SELECT signals could be used to indicate that reciprocal square root of X is to be computed. A person skilled in the art can envision other implementations of a control

logic configured to enable and disable respective circuits, all of which are within the scope of the present disclosure.

[0049] The output of the log 510 is passed to the reciprocal circuit 460, where, in presence of reciprocal select signal 512 a reciprocal of X is calculated (shown as "reciprocal 516" in FIGURE 5), which, in the logarithmic domain, reduces to negating the value received from the log 510, in accordance with equation (4). The output of the reciprocal circuit 460 is then passed to the square root circuit 470, where, in presence of square root select signal 514 a square root of the value passed to the circuit 470 is calculated (shown as "square root 518" in FIGURE 5), which, in the logarithmic domain, reduces to dividing the received value by 2, in accordance with equation (5). The result of the computation of a desired nonlinear function in the logarithmic domain may then be written to the memory 430, e.g. to a processor register calculated (shown as "result 520" in FIGURE 5).

[0050] In FIGURE 5, grey shading and thicker lining is used to illustrate functionality that is added to the conventional log circuit to arrive at the extended log circuit illustrated in this FIGURE. Thus, in FIGURE 5, elements 504, 506, 508, 512, 514, 516, and 518 are added.

[0051] Operation of the system 400, possibly implemented with the extended circuit of Figure 5, is further illustrated in FIGURE 6.

[0052] FIGURE 6 is a flow diagram 600 of method steps illustrating use of the system of FIGURE 4 to perform reciprocal, square root, and/or reciprocal square root calculations, according to some embodiments of the present invention. While FIGURE 6 is described with reference to the system of FIGURE 4, any system configured to perform steps illustrated in FIGURE 6, in any order, is within a scope of the present disclosure.

[0053] The method 600 may begin in step 602, where the system 600 receives a request to calculate reciprocal, square root, or a reciprocal square root on an input value X. To that end, in an embodiment, the extended log circuit 412 may be called with the input 502 taken from the memory 430, e.g. from a processor register.

[0054] Steps 604, 606, and 608, performed on the input value X are analogous to steps 304, 306, and 308 described above (but now only for one input value) and, therefore, in the interests of brevity, the description of these steps is not repeated here.

[0055] When the method 600 proceeds to step 610, logarithmic value for X has been computed. In step 610, if the nonlinear function to be computed on the input value X is reciprocal (i.e. reciprocal select signal is present, square root select signal is absent) or reciprocal square root (i.e. both reciprocal select signal and square root select signal are present), the system 400 performs computation of an intermediary reciprocal result in the logarithmic domain using the logarithmic value for X obtained in step 608 by negating the value obtained in step 608.

[0056] If the nonlinear function to be computed on the input value X is only the square root of X (i.e. reciprocal select signal is absent, square root select signal is present), then step 610 is skipped and the output of step 608 is provided to the square root circuit, step 612.

[0057] In step 612, if the nonlinear function to be computed on the input value X is square root, the system 400 performs computation of an intermediary square root result in the logarithmic domain by right-shifting the logarithmic value for X obtained in step 608 (i.e. reciprocal select signal is absent, square root select signal is present). Alternatively, if, in step 612, the nonlinear function to be computed on the input value X is reciprocal square root, the system 400 performs computation of an intermediary reciprocal square root result in the logarithmic domain by right-shifting the logarithmic value obtained in step 610 (i.e. both reciprocal select signal and square root select signal are present).

[0058] In step 614, the exp circuit 420 computes the exponent of the intermediary result computed either in step 610 or 612, depending on which nonlinear function is to be computed.

[0059] In step 614, the final result for performing the desired nonlinear function may be combined with the stored sign of X and the output of the exp step 614. In one embodiment, if the original request (step 602) indicated that a square root of a negative

value was to be computed, then step 614 could include outputting an indication, e.g. as a flag, that the result is an imaginary number.

Variations and implementations

[0060] While embodiments of the present invention were described above with references to exemplary implementations as shown in FIGURES 1-6, a person skilled in the art will realize that the various teachings described above are applicable to a large variety of other implementations. For example, the general teachings described herein are applicable to both floating point and fixed point instructions, with the differences in each particular implementation being apparent to a person skilled in the art. In another example, while the teachings provided herein referred specifically to a square root computation, the element referred to as the square root circuit could be configured to compute any Nth root of an input value by dividing the logarithm of the received input value by N (e.g. by dividing by 3 instead of two when the root is a cubed root, etc.)

[0061] In certain contexts, the features discussed herein can be applicable to automotive systems, medical systems, scientific instrumentation, wireless and wired communications, radar, industrial process control, audio and video equipment, current sensing, instrumentation (which can be highly precise), and other digital-processing-based systems.

[0062] Moreover, certain embodiments discussed above can be provisioned in digital signal processing technologies for medical imaging, patient monitoring, medical instrumentation, and home healthcare. This could include pulmonary monitors, accelerometers, heart rate monitors, pacemakers, etc. Other applications can involve automotive technologies for safety systems (e.g., stability control systems, driver assistance systems, braking systems, infotainment and interior applications of any kind).

[0063] In yet other example scenarios, the teachings of the present disclosure can be applicable in the industrial markets that include process control systems that help drive productivity, energy efficiency, and reliability. In consumer applications, the teachings of the signal processing circuits discussed above can be used for image processing, auto focus, and image stabilization (e.g., for digital still cameras, camcorders,

etc.). Other consumer applications can include audio and video processors for home theater systems, DVD recorders, and high-definition televisions.

[0064] In the discussions of the embodiments above, components of a system, such as e.g. clocks, multiplexers, buffers, and/or other components can readily be replaced, substituted, or otherwise modified in order to accommodate particular circuitry needs. Moreover, it should be noted that the use of complementary electronic devices, hardware, software, etc. offer an equally viable option for implementing the teachings of the present disclosure.

[0065] Parts of various systems for extending functionality of existing log and exp circuits can include electronic circuitry to perform the functions described herein. In some cases, one or more parts of the system can be provided by a processor specially configured for carrying out the functions described herein. For instance, the processor may include one or more application specific components, or may include programmable logic gates which are configured to carry out the functions describe herein. The circuitry can operate in analog domain, digital domain, or in a mixed signal domain. In some instances, the processor may be configured to carrying out the functions described herein by executing one or more instructions stored on a non-transitory computer readable storage medium.

[0066] In one example embodiment, any number of electrical circuits of FIGURES 1-6 may be implemented on a board of an associated electronic device. The board can be a general circuit board that can hold various components of the internal electronic system of the electronic device and, further, provide connectors for other peripherals. More specifically, the board can provide the electrical connections by which the other components of the system can communicate electrically. Any suitable processors (inclusive of digital signal processors, microprocessors, supporting chipsets, etc.), computer-readable non-transitory memory elements, etc. can be suitably coupled to the board based on particular configuration needs, processing demands, computer designs, etc. Other components such as external storage, additional sensors, controllers for audio/video display, and peripheral devices may be attached to the board as plug-in cards, via cables, or integrated into the board itself. In various embodiments, the

functionalities described herein may be implemented in emulation form as software or firmware running within one or more configurable (e.g., programmable) elements arranged in a structure that supports these functions. The software or firmware providing the emulation may be provided on non-transitory computer-readable storage medium comprising instructions to allow a processor to carry out those functionalities.

[0067] In another example embodiment, the electrical circuits of FIGURES 1-6 may be implemented as stand-alone modules (e.g., a device with associated components and circuitry configured to perform a specific application or function) or implemented as plug-in modules into application specific hardware of electronic devices. Note that particular embodiments of the present disclosure may be readily included in a system on chip (SOC) package, either in part, or in whole. An SOC represents an IC that integrates components of a computer or other electronic system into a single chip. It may contain digital, analog, mixed-signal, and often radio frequency functions: all of which may be provided on a single chip substrate. Other embodiments may include a multi-chip-module (MCM), with a plurality of separate ICs located within a single electronic package and configured to interact closely with each other through the electronic package. In various other embodiments, the functionalities of extended log and exp circuits may be implemented in one or more silicon cores in Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs), and other semiconductor chips.

[0068] It is also imperative to note that all of the specifications, dimensions, and relationships outlined herein (e.g., the number of processors, logic operations, etc.) have only been offered for purposes of example and teaching only. Such information may be varied considerably without departing from the spirit of the present disclosure, or the scope of the appended claims. The specifications apply only to one non-limiting example and, accordingly, they should be construed as such. In the foregoing description, example embodiments have been described with reference to particular processor and/or component arrangements. Various modifications and changes may be made to such embodiments without departing from the scope of the appended claims. The description and drawings are, accordingly, to be regarded in an illustrative rather than in a restrictive sense.

[0069] Note that with the numerous examples provided herein, interaction may be described in terms of two, three, four, or more electrical components. However, this has been done for purposes of clarity and example only. It should be appreciated that the system can be consolidated in any suitable manner. Along similar design alternatives, any of the illustrated components, modules, and elements of FIGURES 1-6 may be combined in various possible configurations, all of which are clearly within the broad scope of this Specification. In certain cases, it may be easier to describe one or more of the functionalities of a given set of flows by only referencing a limited number of electrical elements. It should be appreciated that the electrical circuits of FIGURES 1-6 and its teachings are readily scalable and can accommodate a large number of components, as well as more complicated/sophisticated arrangements and configurations. Accordingly, the examples provided should not limit the scope or inhibit the broad teachings of the electrical circuits as potentially applied to a myriad of other architectures.

[0070] Note that in this Specification, references to various features (e.g., elements, structures, modules, components, steps, operations, characteristics, etc.) included in “one embodiment”, “example embodiment”, “an embodiment”, “another embodiment”, “some embodiments”, “various embodiments”, “other embodiments”, “alternative embodiment”, and the like are intended to mean that any such features are included in one or more embodiments of the present disclosure, but may or may not necessarily be combined in the same embodiments.

[0071] It is also important to note that the functions related to extending functionality of existing log and exp circuits illustrate only some of the possible functions that may be executed by, or within, system illustrated in FIGURES 1-6. Some of these operations may be deleted or removed where appropriate, or these operations may be modified or changed considerably without departing from the scope of the present disclosure. In addition, the timing of these operations may be altered considerably. The preceding operational flows have been offered for purposes of example and discussion. Substantial flexibility is provided by embodiments described herein in that any suitable

arrangements, chronologies, configurations, and timing mechanisms may be provided without departing from the teachings of the present disclosure.

[0072] Numerous other changes, substitutions, variations, alterations, and modifications may be ascertained to one skilled in the art and it is intended that the present disclosure encompass all such changes, substitutions, variations, alterations, and modifications as falling within the scope of the appended claims. In order to assist the United States Patent and Trademark Office (USPTO) and, additionally, any readers of any patent issued on this application in interpreting the claims appended hereto, Applicant wishes to note that the Applicant: (a) does not intend any of the appended claims to invoke paragraph six (6) of 35 U.S.C. section 112 as it exists on the date of the filing hereof unless the words “means for” or “step for” are specifically used in the particular claims; and (b) does not intend, by any statement in the specification, to limit this disclosure in any way that is not otherwise reflected in the appended claims.

[0073] Note that all optional features of the apparatus described above may also be implemented with respect to the method or process described herein and specifics in the examples may be used anywhere in one or more embodiments.

[0074] Although the claims are presented in single dependency format in the style used before the USPTO, it should be understood that any claim can depend on and be combined with any preceding claim of the same type unless that is clearly technically infeasible.

WHAT IS CLAIMED IS:

1. An apparatus for computing a nonlinear function of an input variable, the apparatus comprising:

a logarithmic circuit configured to compute a logarithm of a first input value;

a reciprocal circuit configured to obtain the logarithm of the first input value and configured to:

when enabled, negate the logarithm of the first input value and provide the negated logarithm of the first input value as an output of the reciprocal circuit, and

when disabled, provide the logarithm of the first input value as the output of the reciprocal circuit;

a root circuit configured to obtain the output of the reciprocal circuit and configured to:

when enabled, divide the received output of the reciprocal circuit by N and provide the divided output of the reciprocal circuit as an output of the root circuit, and

when disabled, provide the received output of the reciprocal circuit as the output of the root circuit;

a control logic configured to:

enable the reciprocal circuit and disable the root circuit when the nonlinear function is a reciprocal,

disable the reciprocal circuit and enable the root circuit when the nonlinear function is an Nth root, and

enable the reciprocal circuit and enable the root circuit when the nonlinear function is a reciprocal Nth root.

2. The apparatus according to claim 1, further comprising:

an exponential circuit configured to compute an exponent of the output of the root circuit.

3. The apparatus according to claim 1, further comprising:

an absolute value circuit configured to compute an absolute value of the input variable, store a sign of the input variable, and provide the computed absolute value to the logarithmic circuit as the first input value.

4. The apparatus according to claim 3, further comprising:

an exponential circuit configured to compute an exponent of the output of the root circuit and to combine the computed exponent with the stored sign of the input variable.

5. The apparatus according to claim 1, wherein the first input value is a floating point value.

6. The apparatus according to claim 1, wherein the first input value is a fixed point value.

7. The apparatus according to claim 1, wherein the apparatus is implemented in an application specific integrated circuit (ASIC), a programmable gate array (PGA), or a digital signal processor (DSP).

8. A non-transitory computer readable storage medium storing one or more computer readable instructions which, when executed on a processor, configure the processor to carry out a method for computing a nonlinear function of an input variable, the method comprising:

instructing a logarithmic circuit to compute a logarithm of a first input value;

instructing a reciprocal circuit to obtain the logarithm of the first input value and to perform:

when enabled, negate the logarithm of the first input value and provide the negated logarithm of the first input value as an output of the reciprocal circuit, and

when disabled, provide the logarithm of the first input value as the output of the reciprocal circuit;

instructing a root circuit to obtain the output of the reciprocal circuit and to perform:

when enabled, divide the received output of the reciprocal circuit by 2 and provide the divided output of the reciprocal circuit as an output of the root circuit, and

when disabled, provide the received output of the reciprocal circuit as the output of the root circuit;

enabling the reciprocal circuit and disabling the root circuit when the nonlinear function is a reciprocal;

disabling the reciprocal circuit and enabling the root circuit when the nonlinear function is a Nth root; and

enabling the reciprocal circuit and enabling the root circuit when the nonlinear function is a reciprocal Nth root.

9. An apparatus for computing a reciprocal of an input variable, the apparatus comprising:

a logarithmic circuit configured to compute a logarithm of a first input value;

a reciprocal circuit configured to negate the logarithm of the first input value and provide the negated logarithm of the first input value as an output of the reciprocal circuit; and

an exponential circuit configured to compute an exponent of the output of the reciprocal circuit.

10. The apparatus according to claim 9, further comprising:

an absolute value circuit configured to compute an absolute value of the input variable, store a sign of the input variable, and provide the computed absolute value to the logarithmic circuit as the first input value.

11. The apparatus according to claim 10, wherein the exponential circuit is further configured to combine the computed exponent with the stored sign of the input variable.

12. The apparatus according to claim 9, wherein the first input value is a floating point value.

13. The apparatus according to claim 9, wherein the first input value is a fixed point value.

14. The apparatus according to claim 9, wherein the apparatus is implemented in an application specific integrated circuit (ASIC), a programmable gate array (PGA), or a digital signal processor (DSP).

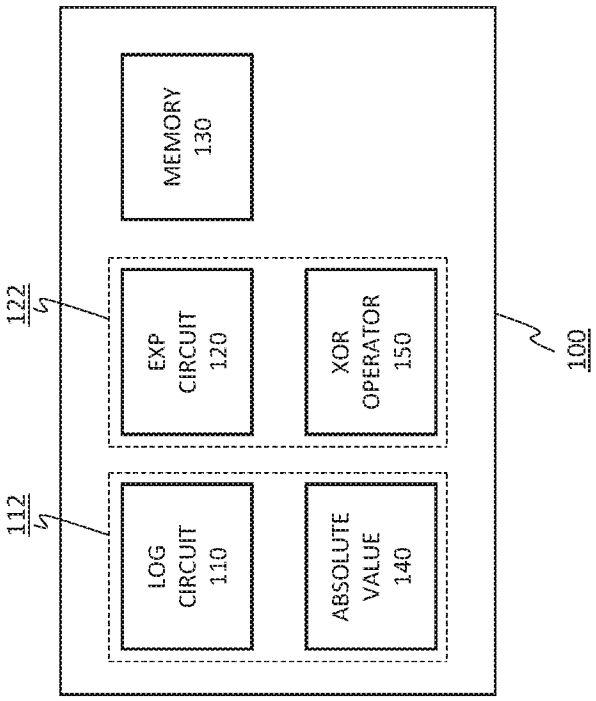

MEMORY
130
122
EXP
CIRCUIT
120
XOR
OPERATOR
150
100
112
LOG
CIRCUIT
110
ABSOLUTE
VALUE
140

FIGURE 1

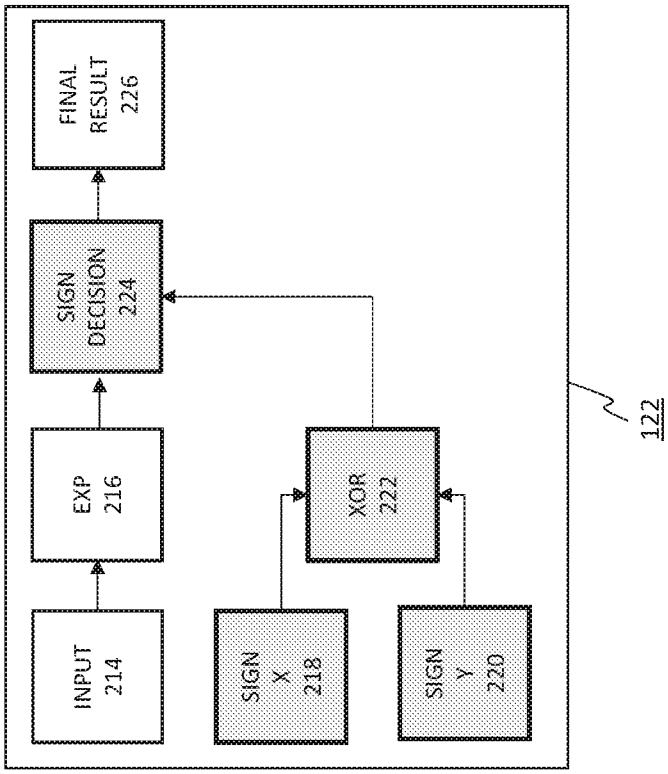


FIGURE 2B

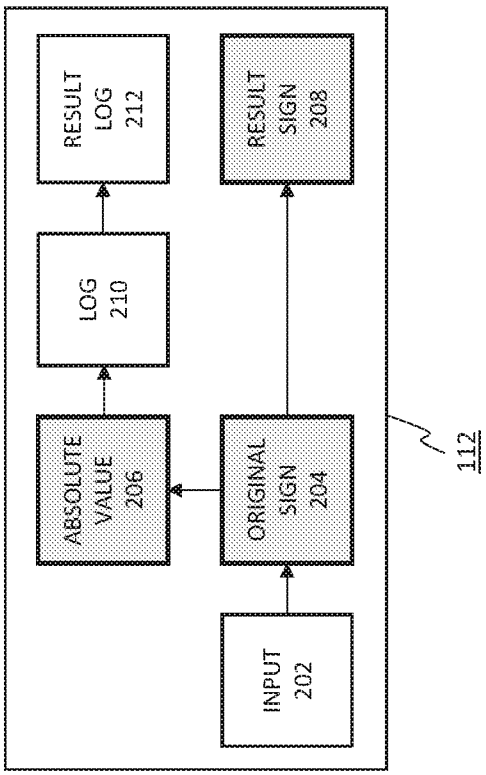


FIGURE 2A

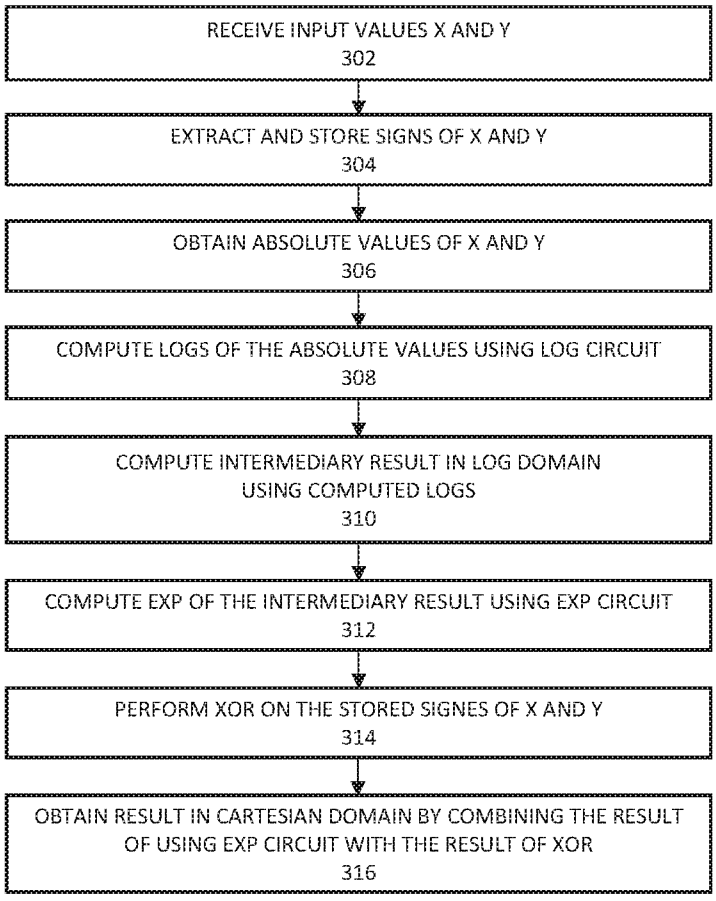

RECEIVE INPUT VALUES X AND Y
302
EXTRACT AND STORE SIGNS OF X AND Y
304
OBTAIN ABSOLUTE VALUES OF X AND Y
306
COMPUTE LOGS OF THE ABSOLUTE VALUES USING LOG CIRCUIT
308
COMPUTE INTERMEDIARY RESULT IN LOG DOMAIN USING COMPUTED LOGS
310
COMPUTE EXP OF THE INTERMEDIARY RESULT USING EXP CIRCUIT
312
PERFORM XOR ON THE STORED SIGNES OF X AND Y
314
OBTAIN RESULT IN CARTESIAN DOMAIN BY COMBINING THE RESULT OF USING EXP CIRCUIT WITH THE RESULT OF XOR
316
300

FIGURE 3

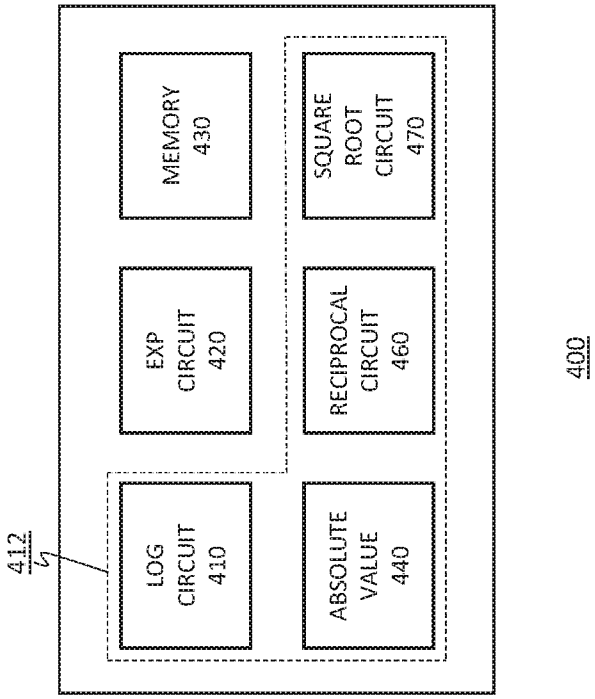

412
LOG CIRCUIT 410
EXP CIRCUIT 420
MEMORY 430
ABSOLUTE VALUE 440
RECIPROCAL CIRCUIT 460
SQUARE ROOT CIRCUIT 470
400

FIGURE 4

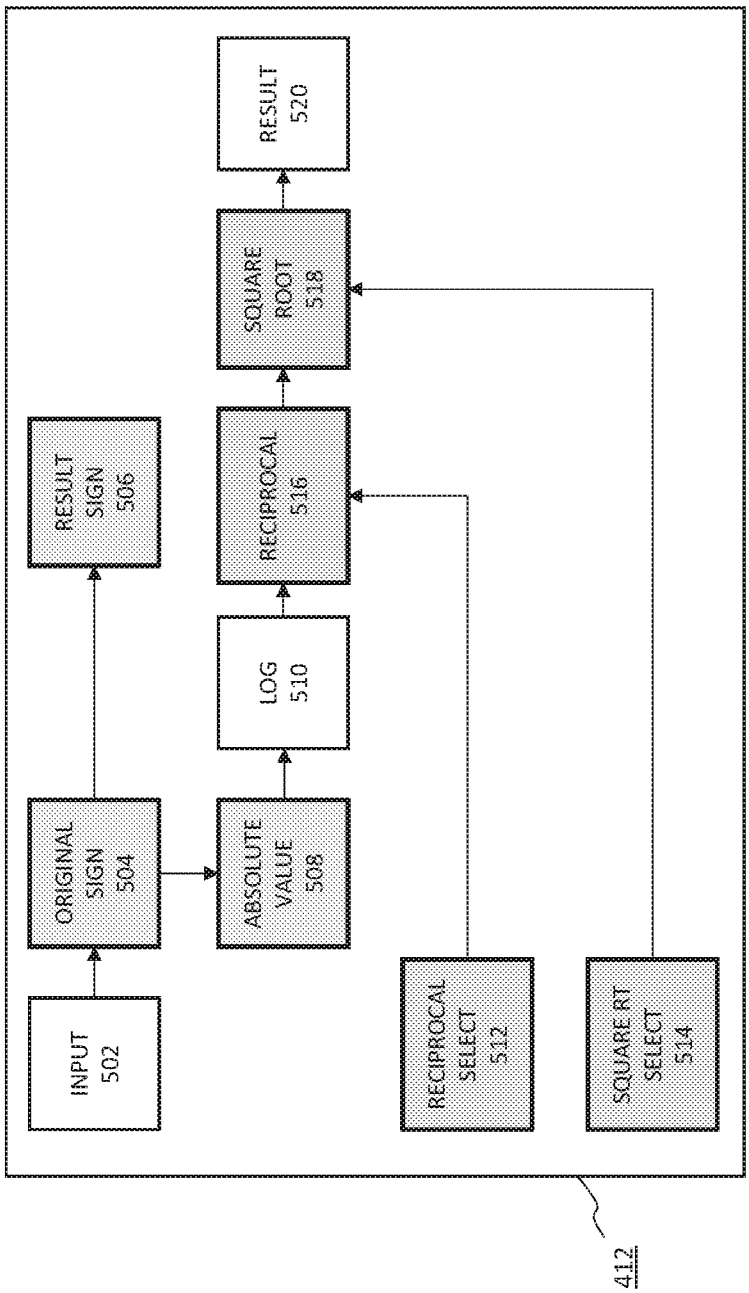

INPUT 502
ORIGINAL SIGN 504
RESULT SIGN 506
ABSOLUTE VALUE 508
LOG 510
RECIPROCAL 516
SQUARE ROOT 518
RESULT 520
RECIPROCAL SELECT 512
SQUARE RT SELECT 514
412

FIGURE 5

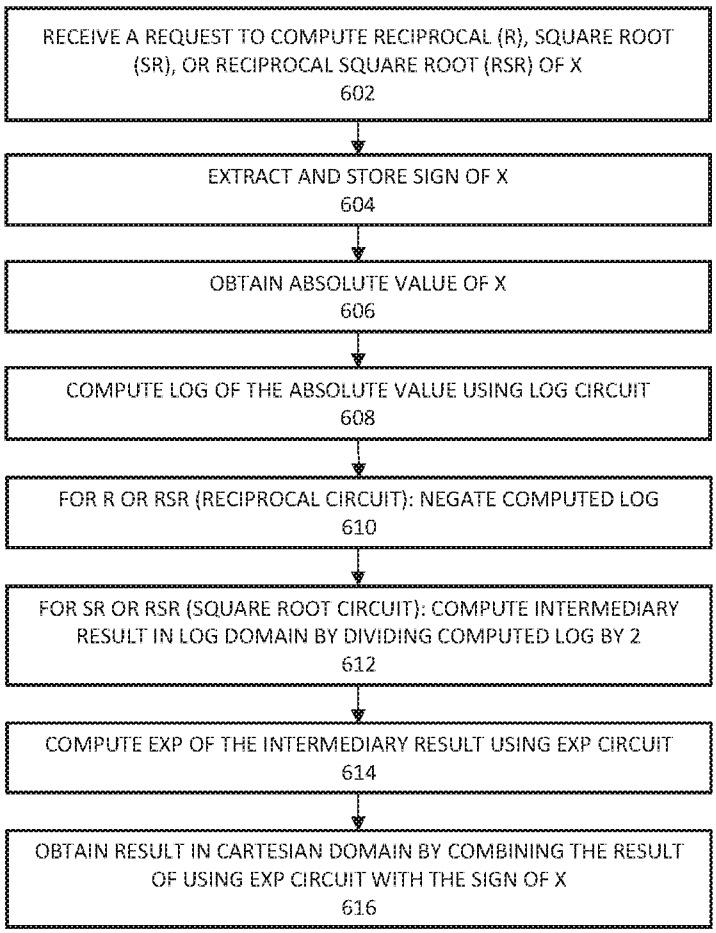

RECEIVE A REQUEST TO COMPUTE RECIPROCAL (R), SQUARE ROOT (SR), OR RECIPROCAL SQUARE ROOT (RSR) OF X
602
EXTRACT AND STORE SIGN OF X
604
OBTAIN ABSOLUTE VALUE OF X
606
COMPUTE LOG OF THE ABSOLUTE VALUE USING LOG CIRCUIT
608
FOR R OR RSR (RECIPROCAL CIRCUIT): NEGATE COMPUTED LOG
610
FOR SR OR RSR (SQUARE ROOT CIRCUIT): COMPUTE INTERMEDIARY RESULT IN LOG DOMAIN BY DIVIDING COMPUTED LOG BY 2
612
COMPUTE EXP OF THE INTERMEDIARY RESULT USING EXP CIRCUIT
614
OBTAIN RESULT IN CARTESIAN DOMAIN BY COMBINING THE RESULT OF USING EXP CIRCUIT WITH THE SIGN OF X
616
600

FIGURE 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/026093

A. CLASSIFICATION OF SUBJECT MATTER
IPC (2016.01) G06F 7/544

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC (2016.01) G06F 7/544

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Databases consulted: Esp@cenet, Google Patents
Search terms used: nonlinear, logarithmic circuit, negated, devide, root

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012203814 A1 Jennings et al. 09 Aug 2012 (2012/08/09) The whole document	1-14
A	US 2008243985 A1 Tang et al. 02 Oct 2008 (2008/10/02) The whole document	1-14

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 Jul 2016	01 Aug 2016

Name and mailing address of the ISA:	Authorized officer
Israel Patent Office Technology Park, Bldg.5, Malcha, Jerusalem, 9695101, Israel Facsimile No. 972-2-5651616	PLACHINTA Ekaterina Telephone No. 972-2-5651740

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2016/026093

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